7-17-00

Trip Report on the Visit to Innotech July 17, 2000

Joseph Greenberg

Ray Escoffier, John Webber, and Ray Escoffier attended the design review meeting on the 17th. Joe Greenberg stayed an additional day.

Technical details were discussed in comparing Innotech's version of the 256 lag block of the correlator, versus that in the spec. All issues were resolved.

4K vs 8K

It was decided that there will be 4K Lags per chip, not 8K Lags.
A 4K chip will be 11 mm square, cost $45, and dissipate 1.5 Watts.
An 8K chip would have been 14 mm square, cost $98, and dissipate 3.0 Watts.

Schedule

September 1, 2000 Innotech completes logical design.
Design review with NRAO.
Innotech starts design simulation, with Joe Greenberg assisting.
October 2000 Innotech Design Complete. Final Design Review with NRAO.
January 2001 Order 400 Prototypes
April 2001 Receive Prototypes
October 2001 Get funding for production quantities
1Q 2002 Order production quantities (10,000 or 40,000 TBD)

Miscellaneous Points

First the prototypes will be used to populate a single first round Correlator board (64 chips). Next a complete 4 board plane will be built (256 chips).

The current package choice is a 240 pin PQFP, cavity down, with a copper slug. These will sell for about five dollars apiece.

The piece cost for 10,000 pieces would be $70/chip. 40,000 pieces would be $45/chip.

Lou's father said DC to DC converters on the board is the way to go.

If an error requires a complete new set of masks, the cost would be about $140,000. If the fault could be fixed in a layer of metal, the cost would be about $30,000.

Power Simulation Results

Lou's current simulations yielded 2 Watts at 167 MHz. This scales to 1.5 Watts at 125 MHz.

A simulation, with the adder output being all 9's (worst case) yielded 1.6 Watts. Changing the output to all 5's only reduced the power 2%, showing there isn't much power dissipated in the ripple output chain.

Innotech Action Items

1. Send us the package specifications.
2. Send us the I/O library components book via email.
3. Continue with the chip design and layout.
4. Upon receiving the updated Specification, assure that it agrees with their current design.

NRAO Action Items

1. Incorporate discussed changes in the Chip Specification.
   These changes include:

A) Adding a ring oscillator to allow determination of the process speed. Target nominal speed will be 125 MHz. Controlled by a pin that tri-states all outputs except the ring oscillator output which is turned on.

B) Add Program word bits to set outputs high and low for test purposes.

C) Include a section outlining a methodology for doing the production test. This should test all elements of the logic.

Actions for NRAO to Consider (Comments invited)

1. When we get the large order of chips, a Nitrogen Storage box would be a good investment, unless the chips were in hermetically sealed packages.
2. Some sort of accelerated life test of the finished chips would be desirable.
3. Going to a Ball Grid Array would allow putting the 64 antenna array on a 12U card, instead of the four 9U cards in the current design. This entails eliminating the Aux bus and putting the chip in a 208 pin BGA. This package is 23 mm square, as opposed to 32 mm square, plus leads for a PQFP. The main disadvantage would be the high power density on the one card (256 ASICS times 1.4 Watts equals 358 Watts).
4. Lowering the supply voltage from 1.8 to 1.6 Volts, would give a power reduction from 1.6 to 1.25 Watts.

5. If we gate off the Aux bus's upward propagation, it would save 3% of the power on the affected chips. We had the gating originally and eliminated it to allow signals for test purposes. We could always have a separate program word for the test purposes.

6. It might be necessary to pay attention to the coefficient of expansion of the chips, versus that of the board, to guard against lead flexing.