6-29-00

Brief reports for JRDG of 6-29-00:

(1) Report on 1/f noise

Calculations have been made and compared to results reported by Kooi et al. for a particular SIS receiver. Based on work by Wollack & Pospieszalski, assuming a 6-stage amplifier with 16 GHz bandwidth. Results to be reviewed by Marian and written up. Briefly: for integration times greater than about 1 msec, noise is about 3e-4 essentially regardless of integration time. Kooi results for comparison for his 345 GHz receiver with 100 MHz bandwidth (properly scaled—info not in paper) are about 1e-4 for time scales 0.5-15 sec. Since a perfect receiver with 16 GHz BW would give 6e-6 in one sec, either receiver is far worse than a perfect one.

Plan to do some lab measurements on 230 GHz SIS mixer receiver with 8 GHz BW beginning in August, analogous to Kooi measurements.

Don't know level of atmospheric fluctuations—need science group help. There was an incomplete Holdaway memo on this subject.

If instrument rather than atmosphere is limiting:
Load-switched radiometer? Still a stability challenge.
Correlation receiver? More complex.

(2) LO development status

Series of measurements for 80 GHz LO driver: short-term phase noise, temperature dependence of phase (long-term drift), amplitude noise all characterized. Amplitude noise needs more work. Memo nearly written.

Chain using 110-220 GHz fixed-tuned doubler, but without the intended 110 GHz power amplifier (final doubler grossly underdriven—also non-optimum diodes), gave 2 mW from 220 to 228 GHz, and >200 μW from 204 to 232 GHz. Not enough yet to drive the next stage, but plenty to drive an SIS mixer. Intend to use this for further noise tests.

For frequencies above about 300 GHz, the JPL approach with membrane or suspended structure looks like the way to go; above 600 GHz, varistor rather than varactor mode looks increasingly attractive. JPL cycle time for design/fab/test is much too long—on the order of one year. JPL and NRAO are trying to set up a deal with Jack East at U Michigan to produce smaller wafers with same features on much faster time scale for rapid prototyping. Designs for 80-240 and 220-660 triplers are targeted at this path.