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Report on Trip to JPL, HRL, and TRW

December 5-8, 1999

Eric Bryerton and John Webber

Introduction

On December 5-8, Eric Bryerton and John Webber traveled to the Los Angeles area to meet with representatives of JPL (Jet Propulsion Laboratory) who are working on power amplifier design for the FIRST (Far-Infrared and Sub-millimeter Telescope) LO system. Their requirements are similar enough to those of ALMA (see Appendix) that a collaboration is being considered. The terms of the collaboration as well as the possible benefits to both parties was discussed. An overview of their progress was also heard. Bryerton and Webber also met with S. Weinreb's graduate student at Caltech, Matthew Morgan, who would be working on MMIC designs for the ALMA power amplifiers. Bryerton and Webber also visited the labs of HRL and TRW to explore the possibility of a development contract directly with these companies. This report summarizes these discussions.

Dec. 5 Caltech

Sander Weinreb and Matthew Morgan

First, Morgan showed us the design he is presently working on, a 3-stage, microstrip, 87-108 GHz design on TRW's 0.15 um GaAs process with 100 mW predicted output power. The design of the on-chip power combining network was discussed. He showed us small-signal simulations indicating 10-11dB gain over the entire band. Using a curtice cubic model supplied by TRW, he will soon do large-signal simulations for output power.

Since the HRL wafer run is coming up first, in February, Morgan will begin to work on that design instead. There was some discussion on CPW versus microstrip. Weinreb felt that for a 2-mil substrate at W-band, microstrip is okay. For the HRL process, however, the vias are larger, necessitating the use of CPW. Samoska has a 2-stage, CPW design on HRL's process with 50 mW predicted output power from 85-140 GHz. (Measurements are described later.)

Noise performance of these amplifiers was also discussed. Weinreb was particularly concerned about the amplitude noise at the IF, 4-12 GHz away from the carrier. Weinreb felt that a YIG filter might be necessary after the final power amplifier to meet the 3K/uW spec. Weinreb also felt that a wideband Schottky mixer plus LNA is good enough to make amplitude noise measurements; there is no need to use a SIS mixer. Weinreb is also concerned about parametric effects on noise, but this is not well understood. Weinreb mentioned that an upcoming course on power amplifier design given by Dr. Komiak might address this topic.

Dec. 6 JPL

Sander Weinreb, Todd Gaier, Lorene Samoska, John Pearson, and Imran Mehdi

Samoska showed us the most recent results from the FIRST power amplifiers (TRW process): >200 mW from 71-82 GHz, >100 mW from 88-106 GHz, and >100 mW from 99-114 GHz. She also showed measurements of two chips combined using a magic-T with >300 mW from

89-104 GHz. The next TRW wafer run was discussed. She has several open slots for new designs on which we could place some designs for our needs. These designs would need to be completed by April. Samoska also showed us power measurements of a wideband CPW driver (HRL process): 25-40 mW from 65-105 GHz.

We met with T. Gaier to discuss packaging issues. The FIRST MMICs are larger than a cutoff wavelength meaning the cavity they are placed in is resonant over frequencies where the device has gain causing stability problems. On an individual basis, each amplifier takes two additional days of an engineer's time to debug after assembly. He is therefore reluctant to give us chips without our knowledge of their packaging procedure. The suggestion was made that Bryerton visit for a week or two to learn their packaging procedure with blocks fabricated by NRAO using JPL's designs. In exchange, we would fabricate additional blocks for JPL's use. They are also willing to lend us a 80-GHz packaged amplifier for our testing. We just need to let them know 7-10 days before we need it.

We later all met with J. Pearson and I. Mehdi to discuss the terms of a collaboration. We explained why we wanted to borrow the 80-GHz amplifier, for phase and amplitude noise measurements. There was some discussion on whether this was necessary since a similar experiment performed recently by Kooi showed no additional noise introduced by a millimeter-wave power amplifier when placed before a multiplier. It was agreed that a confirmation of these results would be a useful exercise. Webber stated that our needs call for the 72-95 GHz and 100-120 GHz amplifiers to be completed first since they will supply the LO for the first receivers placed on the antennas. To get up to 120 GHz, the consensus was that we need to use InP. Therefore, it was agreed that M. Morgan should design a 100-120 GHz InP power amplifier for the HRL wafer run coming in February, then work on designs for the 72-95 GHz band for the TRW wafer run in April.

Dec. 7 HRL

Loi Nguyen and Mehran Matloubian

Nguyen and Matloubian began by describing HRL's recent results in the MMIC power amplifier area. They have a 2-stage CPW design with 20-30% bandwidth at 94 GHz, 60 mW output power, and 10.6 dB gain. They showed us measurements of a 3-stage CPW design with 30 dB gain at 140 GHz and greater than 10 dB gain from 130-160 GHz and 10 mW power using their 0.1 um InP process. They showed us power measurements of L. Samoska's design from 105-140 GHz with 16 dBm output power dropping to 14dBm at the upper end and 13 dB gain. We mentioned our plan of Weinreb placing a 100-120 GHz design on the upcoming wafer run; they were in full support of this. If we used their design team, they could not guarantee anything at this time. But once there was a demonstration of a successful chip design, they could enter into a fixed-price contract with guaranteed deliverables. Nguyen later gave us a tour of their facilities.

Dec. 8 TRW

Richard Lai, Y. C. Chen, Peter McAdam (Manager–Advanced Technology Directorate), and Marshall Huang

We began by giving an overview of the ALMA project to McAdam, leading to our power amplifier requirements. McAdam basically gave his blessing to a TRW-NRAO collaboration

provided TRW does not lose money. It was again the consensus that for the highest band, we need InP, and that it is probably preferable for the other bands as well. It was agreed that a good place to start is joining with JPL for half of the upcoming wafer run. Later, when we know our construction budget, we can discuss a more complete development. The possibility of TRW delivering packaged amplifiers was also discussed. They, in fact, prefer this. Lai then gave us a quick tour of their facilities.

Recommendations

Based on the discussions with HRL and TRW and the availability of development money, it would be premature to enter into a development contract with either of these companies until designs meeting our requirements have been demonstrated. In each case, we asked them directly whether they would accept a firm, fixed-price development contract to meet our amplifier requirements. In each case, they responded reluctantly: "Yes, but you couldn't afford it because we're not sure how much engineering would be required." They agreed that a guess of several hundred thousand dollars is about right.

Therefore, we believe (and TRW and HRL concur) that the best approach at this point is to combine our development work with FIRST since our requirements are similar. MMIC design for these processes is sufficiently well understood that a graduate student, M. Morgan, with S. Weinreb's mentorship should be able to produce designs approaching our requirements. Here is what we would expect to get:

1. Many power amplifier chips of proven design which overlap at least part of our bands. These will be very useful for performing noise evaluation and overall LO performance over portions of the ALMA bands. In S. Weinreb's opinion, at least a dozen of these should be sacrificed in accelerated lifetime testing, something which has not yet been done on these devices.

2. Some power amplifier chips designed for the two amplifier bands with highest priority: the 72-95 GHz amplifier which drives the LO for the 211-275 and 275-370 GHz receivers, and the 100-120 GHz amplifier which drives the LO for the 602-720 GHz receiver. It is likely that these chips will not quite be precisely centered where we want them, and that they will not quite meet the power requirements without power combining; however, they should be close enough to be useful and one more round of iteration in the design could achieve our objectives.

The difficult job, we learned on this trip, is packaging. This is something we should therefore work closely with the FIRST group on. To begin this collaboration, Bryerton and a technician should spend some time with the FIRST group learning their packaging procedure. Then, with the chips NRAO receives from upcoming wafer runs, we should continue to work with JPL to improve the packaging techniques. We should also keep the possibility open, if the construction budget allows, of contracting directly with TRW for delivery of packaged amplifier modules.

Appendix

Power Amplifier Frequency Bands

FIRST	***ALMA***
71-79 GHz	65-85 GHz
80-92	72-95
88-99	87-108
92-106	100-120
106-112.5	