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Design and Fabrication of THz Sources

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Introduction

This proposal discusses the design and fabrication of GaAs MMIC multiplier circuits for use as local oscillators for THz receivers. The goal is to develop a prototype fabrication process that will allow complete realization of these circuits using the facilities of the Solid State Electronics Laboratory at the University of Michigan. These initial designs will be used as proof of concept studies for a variety of applications. The research will transfer existing MMIC fabrication methods from the Microelectronics Laboratory at JPL, combine this technology with fabrication methods already in use or under development at Michigan and finally produce small quantities of circuits designed to meet NRAO receiver local oscillator applications. The main effort on this project will be the development of the prototype fabrication process. However, we will also need information for THz frequency circuit design and varactor physics. We plan to develop improved device and circuit models on a companion project. The proposal for this project is being submitted to JPL.

Circuit Fabrication

Not clear exactly what Michigan should do - wait to see one results?

We would like to fabricate the circuits designed here and also develop a process to fabricate circuits designed elsewhere. A major part of the effort will be to transfer the technology presently being used at JPL to the Solid State Laboratory. Some of the process steps, optical lithography, ohmic contacts and etching are already being used here. We have an excellent electron beam lithography tool, but we will have to develop a process to match the JPL anode definition process. Wafer thinning is an open issue. Our present MMIC circuit design uses full thickness GaAs wafers without thinning. The JPL etch stop substrate removal process technology will be needed to produce circuits with the same thickness as existing JPL designs.

typically ~600μm

to 50μm even at 200 GHz

The major advantage of this approach will hopefully be a shorter design/fabricate/test time. This should also allow more design iteration and optimization. It is reasonable to fabricate several wafers in parallel, so different doping structures can be tested. The laboratory also has a pattern generator mask maker, so the time needed to make optical mask sets is reduced. We usually do initial mask layouts using AutoCad, and then transfer the design to the mask maker. This approach should also allow designs to be optimized for NRAO specific applications. The tradeoffs between power and efficiency and between low temperature vs. room temperature may be different for the NRAO receivers. Also, the NRAO array requires many more multipliers than a single space mission. Issues with assembly and cost are much more important here. We need to think ahead to the requirements for large numbers of these circuits and plan for low cost assembly and testing.

There are some limitations to this approach too. We can produce prototype circuits, but they will not be fabricated under the same conditions or requirements as space qualified samples. We need to define the NRAO requirements on this issue. A second issue is

18 mos. to delivery of useful chips?

cost? $1500 - $2000 each, usually order 5 at once

material. Delivery times for commercial MBE wafers can be 3 to 4 months. The advantages of a quick fabrication cycle go away if we need this much time to obtain material. In the past we have used a single layer design, with a variety of different mask sets. However, we use small cm size die, so there were several iterations per each 3 inch wafer. I expect that we will want to have several different designs on each mask set and several copies of each circuit. It would be reasonable to fabricate ¼ or ½ wafers, with the remaining portion available for additional fabrication if necessary. It would also be reasonable to pick some initial wafer designs and then design the circuits using these wafers. The doping and epitaxial layer thickness scale with the frequency with an unknown effect due to the temperature, but it would be important order some wafers in advance and to try to find a commercial source with reasonable delivery times. We would also have to work out the details of getting circuit designs from NRAO.Hopefully we could have process run starts often enough to set up a regular schedule for the circuits and the wafer doping type.

Statement of Work

The goal of this project is to design and fabricate MMICs for THz sources. The tasks include

1. Transfer wafer fabrication process from JPL to UM Solid State Electronics Laboratory,
2. Modify the process to optimize for NRAO requirements, in particular ease of fabrication and assembly into blocks,
3. Using input from the simulations developed for the JPL project optimize the designs for THz applications, with a goal of developing a quick turn around process,
4. Use this process to fabricate circuits for submillimeter wave and THz sources.

Schedule?

Budget

A budget for 2 years is shown on the next page. The major item is support for ½ a graduate student (25% corresponds to the appointment, full time graduate students have a 50% appointment) along with tution. I am planning to support the other ½ with a similar contract with JPL. I also expect to visit NRAO several times, so the travel funds are a bit higher than normal. The use of the Solid State Laboratory is covered by the lab fee. This will cover all lab use. I haven't included the cost of MBE wafers. Since there is overhead on supplies, it cost less to order them outside the contract. We can combine several wafers on a single order to lower the unit cost.

masks? included in cost - Michigan makes them

East: Michigan comes up with a process - then NRAO design conforms to rules
go from AutoCAD to e-beam at Michigan

If we target 650 GHz, process may not work well for Band 7

7/18/00

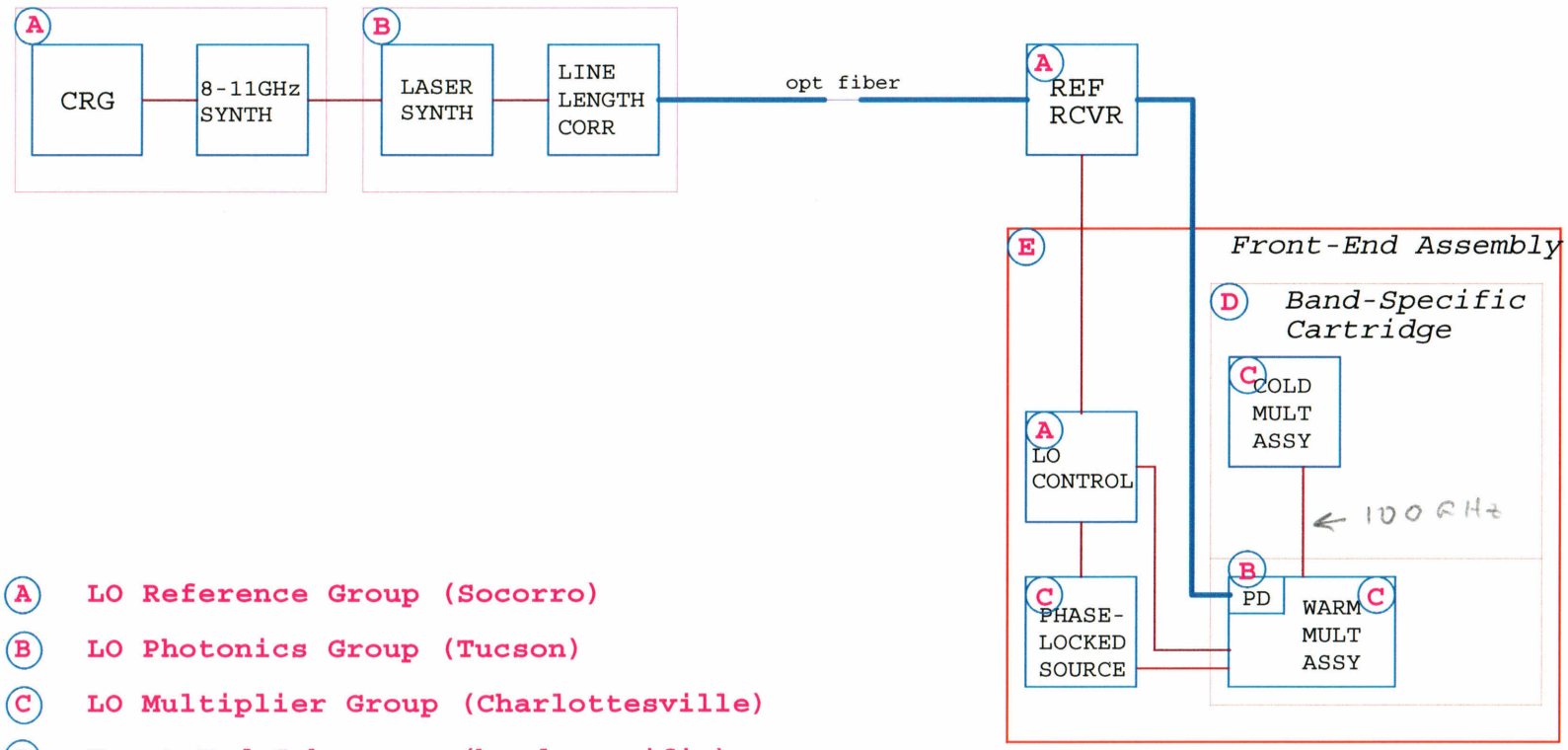
BUDGET

		Year 1	Year 2	Total	
J. East					
Project Director					
cal year	10%	10,209	10,515	20,724	99118 102092
Grad Stu Res Asst	1				12356
Terms 3	25%	9,545	9,831	19,376	12727
Subtotal		19,754	20,346	40,100	
Fringe Benefits at	22%	4,346	4,476	8,822	
Tuition		5,748	6,035	11,783	5474 5748
Materials and Supplies (Incl. postage, copies, toll)		100	100	200	
Travel		2,400	2,400	4,800	
Publications		1,000	1,000	2,000	
Laboratory Fees		5,400	5,400	10,800	$900/month for Si bay.
Subtotal		38,748	39,757	78,505	
Indirect Cost	51.5%	16,995	17,367	34,362	
Total		55,743	57,124	112,867	

Is 10% of PI + 25% of a grad student (x2?) sufficient?

Central Building

Antenna



- (A) LO Reference Group (Socorro)
- (B) LO Photonics Group (Tucson)
- (C) LO Multiplier Group (Charlottesville)
- (D) Front End Sub-group (band specific)
- (E) Receiver Integregration Group (TBD)

Title: ALMA FIRST LO SUBSYSTEM ORGANIZATION		
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