ALMA Memo No. 510

The ALMA Digitizer (DG) Demultiplexer : Design, Performances in DG Assembly and Production Acceptance Tests

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Abstract: A high frequency, low power 1:16 deserializer has been developed using the 0.25µm BiCMOS SiGe technology from *ST* Microelectronics to meet the ALMA project requirements. The input shift register is clocked at 4 GHz and the output data are transferred at 250 MHz. Nominal operation has been observed up to 8 GHz. With 2.5 V supply, the circuit dissipates around 650 mW an especially low value compared to existing similar circuits. The chip is available in an industrial package and exhibits low thermal resistance (about 25 °C/W) thus implying long lifetime as required for the ALMA project. Functional tests including those performed with a self-test block embedded in the deserializer are briefly described. Our deserializer is integrated in a prototype ALMA Digitizer assembly which includes a 3-bit (8-level), 4 GS/s sampler developed with the same SiGe process. Based on Digitizer state counts measurements, Allan variance tests and long term operation in the laboratory environment, we conclude that the prototype Digitizer assembly is operational. The deserializer chip has reached the final production stage after static and dynamic qualification tests have been performed on a first restricted number of production chips.

1. Introduction

The main goal of this paper is twofold: *(i)* describe the architecture of the high speed demultiplexer chip associated with the 3-bit, 8-level analog-to-digital converter (ADC) of the ALMA project; *(ii)* discuss some technical details and performance tests of this new chip integrated in the full ALMA Digitizer assembly. Our design is optimized for low voltage and power dissipation using the BiCMOS7 SiGe technology from ST Microelectronics (*ST*) and the *ST* design tools and rules. The most important characteristics of this technology are 0.25µm width for the MOS transistors and about 80 GHz transition frequency for the bipolar transistors. Our new demultiplexer is integrated in the ALMA Digitizer assembly which will also be briefly described. It is ready for full ALMA production after we have successfully completed static and dynamic acceptance tests.

Fig. 1 shows the location of the demultiplexer in the ALMA data transmission chain. It is located immediately after the 3-bit, 8-level ADC (to be described in a separate memo) and ahead of the Data transmitter which includes a data formatter and an optical conversion stage before transmitting the data through the fiber. A digital rack aboard each antenna houses the Digitizer (ADC and DEMUX), Digitizer clock (PLL module) and Data transmitter shown in Fig. 1.

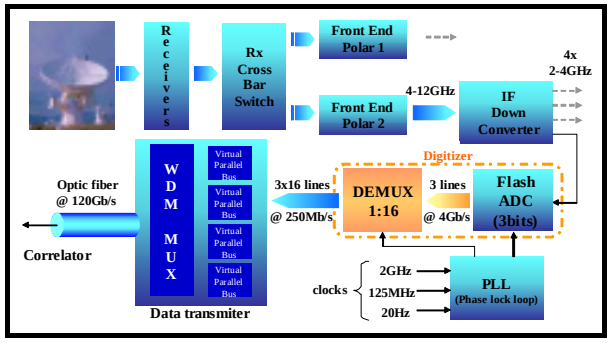

Fig. 1. Schematic of the ALMA data processing chain up to the Data transmitter showing the location of the 1:16 demultiplexer (DEMUX)

The ADC sampling frequency is 4 GHz and a demultiplexing stage is mandatory in order to slow down the data flow before correlation. There is one demultiplexer per bit and there are three chips for each ADC. We have adopted a demultiplexing factor of 1:16 as a good compromise between the chip design complexity and system constraints.

The main specifications of the ALMA demultiplexer chip are driven by the chip functionality specifications and its location in the data processing chain (see e.g. [1] and Fig. 1). The demultiplexer input bit rate is 4 Gb/s and the chip delivers 250 Mb/s for each of its 16 outputs.

Because of the remoteness of the ALMA operations site (5000-m elevation), special care must be taken in designing a chip with low power dissipation in order to maximize the lifetime.
The demultiplexer is driven by two clock signals (4 GHz and 250 MHz) which are generated by the Digitizer clock module (PLL block in Fig. 1). The 4 GHz clock phase is adjustable (see details in [2]) and implements the interferometric fine delay tracking which is required to minimize the signal to noise ratio loss in the ALMA array. The 250 MHz demultiplexer clock phase may thus vary and the Digitizer assembly output data are recaptured with a fixed 250 MHz clock sent to the formatter in the Digital transmitter.
Finally, we have implemented in our design an internal built-in-self-test in order to check that the chip is operational and that all system clocks are nominally delivered to the Digitizer assembly.

2. Demultiplexer Structure Choice

Adjustment of the phase of the 4 GHz sampling clock is used to implement the fine delay tracking. Therefore, there is no 4 GHz reset signal available from the ALMA system and we cannot rely on the classical demultiplexer structure with a DFF tree [3]-[4]; it would need a reset signal in order to synchronize all demultiplexing chips in parallel [5]. For this reason, we have used another structure shown in Fig. 2. It combines a shift register and a parallel register (synchronizer) to build-in the deserializer function.

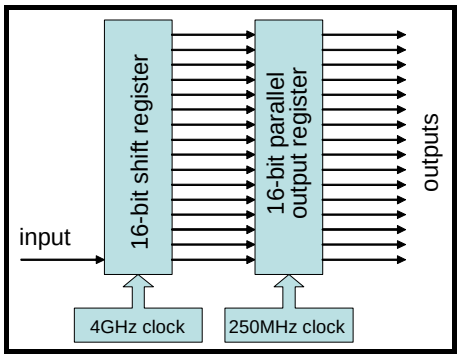

Fig. 2. Synoptic view of the ALMA demultiplexer

In the example below (Fig. 3), we detail the functionality of a 1:2 demultiplexer.

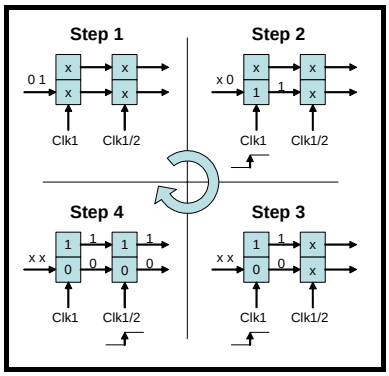

Fig. 3. Visualization of a 1:2 demultiplexing process

On the rising edge of the clock, the shift registers are sampled, so that the first bit of the input data flows into the shift register and is forwarded to the input of the synchronizer. On the following rising transition of the clock the bit into the shift register is shifted and the second bit of the input data goes into the shift register. This process will occur until the last bit of the input data is sent to the register. Then, for the next sample step, the bits located at the synchronizer input are memorized and transferred to the output.
With such a process the ALMA 3-bit data flow (one bit per demultiplexer input) is deserialized for each demultiplexer at the same time on identical output buffers without any reset signal. In fact, synchronization is achieved thanks to the architecture of the Digitizer assembly sub-system in which the same 4 GHz clock is distributed to all demultiplexing chips.

3. Demultiplexer Sub-systems Description

The demultiplexing function is implemented in five main sub-systems of the integrated circuit:

- The data input amplifiers provide impedance matching for the LVDS standard and decrease the commutation time in order to reduce the indecision zone before the shift register.
- The clock amplifiers transform the 4 GHz and the 250 MHz sinusoidal signals delivered from the external sources into square wave signals usable by the D-Latches.
- The shift-register is driven by the 4 GHz clock and shifts the input data.
- The synchronizer is driven by the 250 MHz clock and captures the shift register outputs.

- The output buffers transform the data from the synchronizer into standard LVDS signals.

Electrical details and simulations results for the various DEMUX blocks are given in [6] and in the following we describe some of the most important sub-systems of our integrated circuit.

a. The D-Latches

The D-Latches are the core of the demultiplexer; they act as memory cells based on a DFF structure. A topology with three stacked transistors [3] can be used because the power supply is 2.5 V.

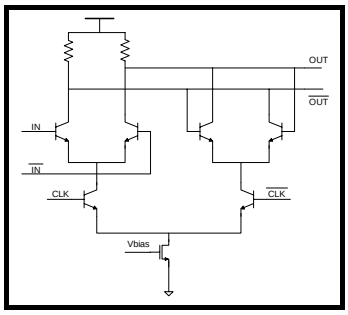

Fig. 4. Schematic of a D-Latch

This D-Latch cell is a fully differential architecture [4] with the clock and data being driven by differential pairs (Fig. 4). This structure reduces the transparency probability because the clock signals are fully differential. For this reason, the first differential pair and the latch cannot be open at the same time. Bipolar transistors are used for the commutation functions because they have higher transition frequency than the MOS transistors. The latter ones are used as the current generators.
With the goal of reducing the power consumption in mind, we have designed a D-Latch with the minimum size allowed by the technology and we have then optimized the current and resistors. All signals have rise and fall times lower than 60 ps.

b. Output buffers

The output buffers convert the synchronizer signals into LVDS signals as required by the ALMA data formatter. The standard LVDS main characteristics are given in Table 1.

Table 1. LVDS main characteristics

	Min	Typ	Max	Unit
Differential impedance	80	100	120	Ω
High voltage			1.475	V
Low voltage	0.925			V
Differential voltage	250		400	mV

The current consumption in the buffers is relatively high because the demultiplexer has 16 outputs which drive large input capacitors and the interconnection interfaces. We have adopted the structure shown in Fig. 5 in order to optimize the power consumption of this stage [7]-[8].

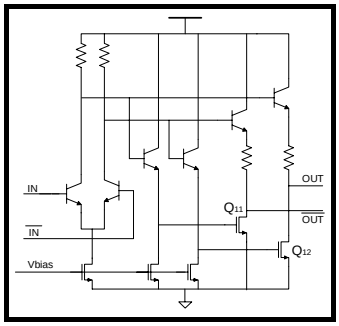

Fig. 5. Schematic of the demultiplexer LVDS output

The resistors located in the output stage generate a small voltage shift in order to adjust the common mode voltage to about 1.2 V.

c. Built-in-self-test design

An internal self-test sub-system is implemented in each demultiplexer in order to check in situ that each demultiplexer chip is functional. This implementation requires to define an easily predictable self-test output signal with very low degradation of system performances during the normal operational mode (no self-test). To solve this difficulty, the structure described in Fig. 6 has been implemented.

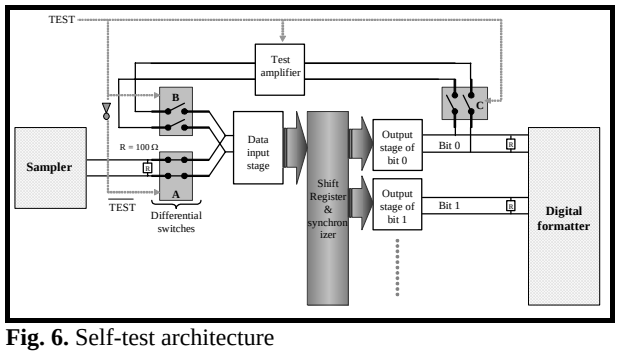

Fig. 6. Self-test architecture

The self-test stage includes an amplifier and three differential switches driven by an ‘enable’ pin. The switch sizes have been optimized in order to

minimize potential harmful consequences on the demultiplexer performances. The 'enable' signal allows us to easily switch from the nominal mode to the test mode:

- In the nominal mode, switch A is closed and switches B and C are open. In this configuration, the signal coming from the sampler goes through the switch to be deserialized.
- In the test mode, switch A is open and switches B and C are closed. The signal coming from the sampler is then disabled and a loop is created between one output and the input. Subsequently, the demultiplexer acts as a frequency divider and the output signals are in agreement with the test mode requirement (see Section 4, b. below).

4. Demultiplexer Characteristics and Test results

Our demultiplexer design is called PHOBOS 1 for the final prototype chip while PHOBOS 2 is used for the same design but with minor differences for the ALMA production chips (see Section 7).

a. Test PCB description

A specific Printed Circuit Board (PCB) has been developed to easily check the demultiplexer chip performances. This PCB (Fig. 7) integrates all of the blocks required for nominal ALMA operation: the 4 GHz and 250 MHz clock amplifiers, connectors and power supply module.

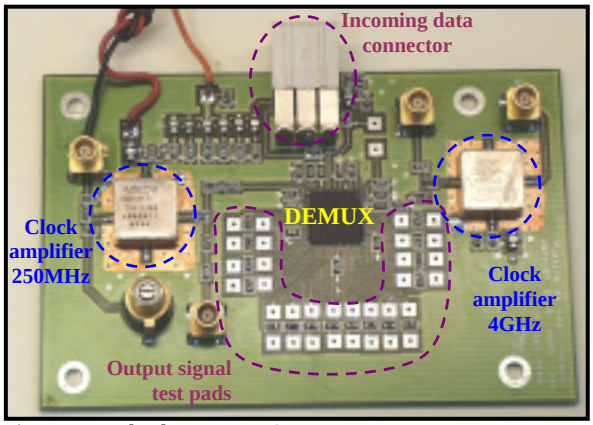

Fig. 7. Demultiplexer test PCB

b. Main characteristics and Functional tests

The nominal operating frequency of the ALMA demultiplexer chip is 4 GHz but we have verified that our design is functional up to 8 GHz. The main characteristics of this chip are gathered in Table 2 and we briefly comment a few of them.

The current consumption corresponds to normal operation without the built-in-self-test amplifier. The consumption measured on several chips with 10 mA resolution is 260 mA. The 60 dB rejection corresponds to the rejection of the 4 GHz clock measured on the test PCB at the 250 MHz clock input. The internal rise and fall times are deduced from simulations while the rise and fall times at the demultiplexer outputs are measured with the test and application PCBs; the output rise/fall times are in agreement with our simulations.

Table 2. Demultiplexer main characteristics (PHOBOS 1)

Technology	0.25 µm BiCMOS SiGe
Power supply	2.5 V
Current consumption	260 mA
Nominal register clock frequency	4 GHz
Max register clock frequency	8 GHz
4 GHz clock power	0 dBm
250 MHz clock power	0 dBm
4 GHz rejection on 250 MHz clock input	60 dB
I/O standard	LVDS
Input rise/fall time (typical)	70 ps
Outputs rise/fall time (typical)	200 ps
Approximate number of transistors	1300

A typical eye diagram for one test PCB demultiplexer output is shown in Fig. 8. It shows that the output signal is in agreement with the LVDS standard. The output voltage swing is 350 mV (±20mV) with a common mode voltage around 1.2 V. The small common mode oscillations observed in Fig. 8 are due to the 4 GHz clock transparency.
If we apply to the demultiplexer input a signal which is a multiple integer of the synchronization clock all outputs are static with a predictable state. For example, if the input data frequency is equal to 1.6 GHz, the demultiplexer outputs [S0 … S15] must be as shown in Fig. 9. Similar tests have been performed at 500 MHz, 1 GHz and 2 GHz; results are as expected.

It is worth mentioning that, thanks to the rise and fall sharp edges and low jitter of the internal and output signals, our demultiplexer design is characterized by a rather long time during which the internal and output circuit states are stable.

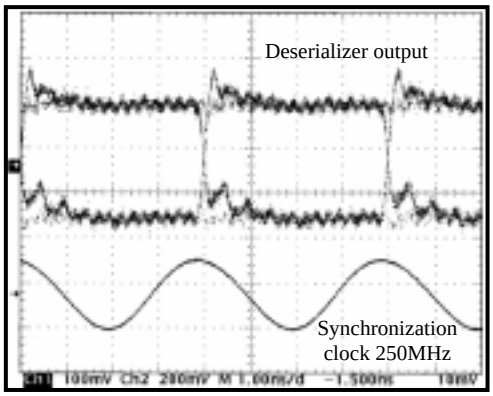

Fig. 8. Eye diagram of one test PCB deserializer output

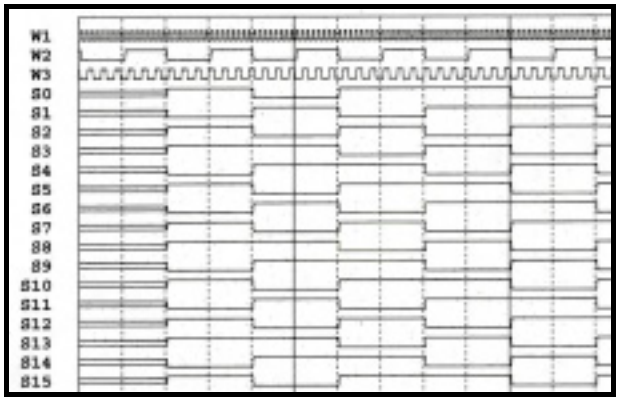

Fig. 9. Demultiplexer simulation results for a 1.6 GHz input signal (W1: 4GHz Clock; W2 : 250 MHz Clock; W3 : 1.6 GHz input signal)

c. Self-test check

The self test mode is activated when the 'enable' pin is connected to 2.5 V. We then know that the demultiplexer chip is nominally working by verifying that all outputs toggle at the same frequency. Because of non negligible propagation time in the self-test loop the output signal is 1/4th of the transfer clock frequency (Fig. 10).

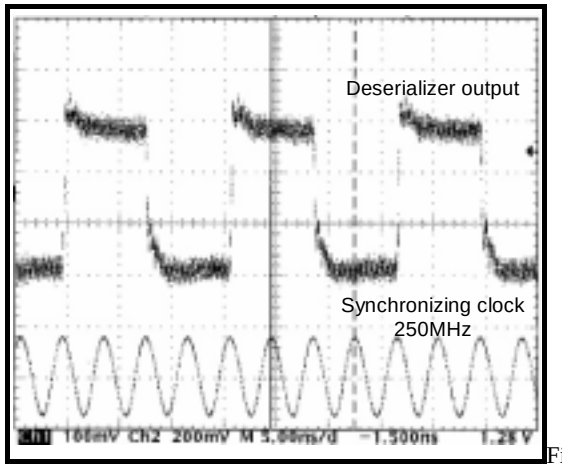

Fig. **Fig. 10.** One deserializer output of demultiplexer self-test loop

In addition, the self-test mode allows us to check that if the demultiplexer outputs behave as expected, then the 4 GHz and 250 MHz clocks are nominally distributed throughout the complete Digitizer assembly (sampler and demultiplexer boards). (This nominal clock distribution check results from the clock distribution design that we have adopted for the Digitizer assembly.)

5. Sub-milliWatt Consumption and Implication on Lifetime

The power consumption of the ALMA demultiplexer is around 650 mW. Most of the consumption is driven by the output buffers (about 40%), the shift register made of 16 serial DFF latches (about 25%) and the synchronizer block which synchronizes the shift register output bits with the 250 MHz clock (about 18%). The consumption is increased by about 50 mW when the built-in-self-test amplifier is active.

A comparison of our design with existing high frequency 1:16 deserializers shows that our deserializer exhibits higher performances (see red dots in Fig. 11). Our product exhibits low power consumption from 4 to 8 GHz and, in addition, its outputs can be synchronized with an outside high frequency signal as required for ALMA.

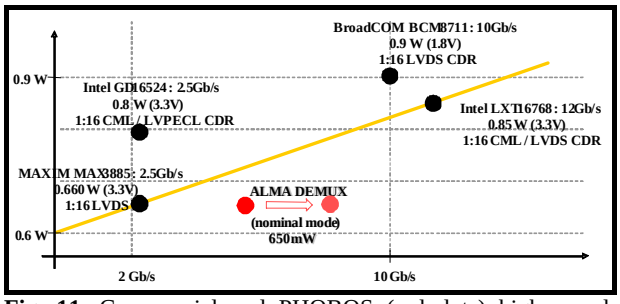

Fig. 11. Commercial and PHOBOS (red dots) high speed demultiplexers

Estimating the lifetime of our integrated circuit is beyond the scope of this paper. However, we stress here the importance of two aspects: the chip package quality and ageing effects due to heat dissipation.

The PHOBOS design benefits from the standard VQFN68 package (10x10x1.0 68 Pitch 0.5) which is qualified for large telecom and consumer volume productions. It is expected that such a package will protect the die from any corrosion for many years. The thermal resistance of the VQFN68 package is about 25 °C/W. Adding the thermal resistance of the demultiplexer PCB and mechanical support we derive a total of 40 °C/W. In a thermally controlled 20 °C environment the silicon junction temperature is less than 50 °C, thus greatly reducing ageing effects. In addition, we note that the fully qualified BiCMOS7 process used here, combined with low junction temperature, clearly tend to minimize long term time variations of some electrical parameters inside our circuit.

6. Integration in the ALMA Digitizer Assembly

The individual chips are available in a fully industrial package (see previous Section) and, for the ALMA project, there are three demultiplexer chips assembled on a same demultiplexer board (Fig. 12). The input connector (white Coaxipack connector in the upper part of Fig. 12) receives a 12 Gbit/s data flow from the sampler sub-assembly after digitization of one 2 to 4 GHz polarization channel.

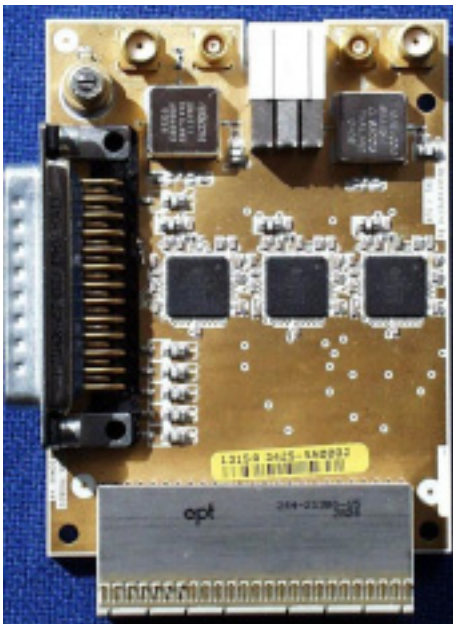

Fig. 12. Demultiplexer chip sub-assembly for the ALMA 3-bit, 8-level ADC

There are two different polarization channels per intermediate frequency band (2-4 GHz) and these two channels are assembled together with a clock distribution board in a single Digitizer assembly (Fig. 13). A few number of industrial prototype Digitizer assemblies have been fabricated according to our design by Solectron-France, accepted and qualified by us for delivery to the ALMA prototype integration center.

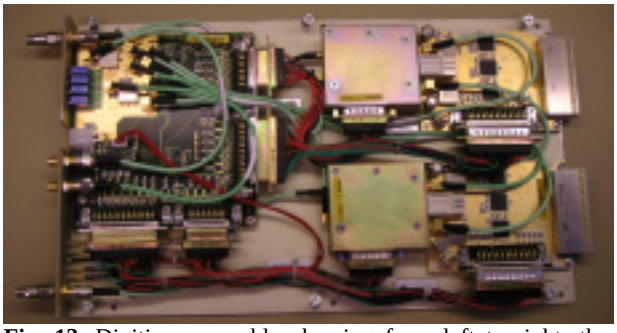

Fig. 13. Digitizer assembly showing from left to right: the clock and power distribution board and connectors; the sampler and demultiplexer sub-assemblies for each of the 2 polarization channels

The Digitizer assembly and associated sampler (VEGA design) will be described elsewhere. We simply mention here that in order to qualify and adjust the complete Digitizer assembly one must use the ALMA digitizer clock module described in [2] and perform an internal phase adjustment by adjusting the 4 GHz clock phase relative to the 250 MHz clock. To check the Digitizer assembly performances we have used two different but

similar tools: a specific Digitizer Test Equipment (see [1] and [9]) and a digital Test Fixture [10].
The Test Fixture is primarily used to test the digital filter cards of the ALMA Correlator but can also be interfaced to the demultiplexed digitizer output to provide sample statistics and spectrum plots [10]. An example of reconstructed broad band spectrum with added spectral line, obtained with a broad band noise source and a weak monochromatic signal at the Digitizer assembly input, is shown in Fig. 14. Such a plot, no DC offset at the demultiplexed digitizer output of 16 LVDS signals, and sampler state counts behaving as expected for broad band Gaussian noise demonstrate that the Digitizer assembly is performing well.

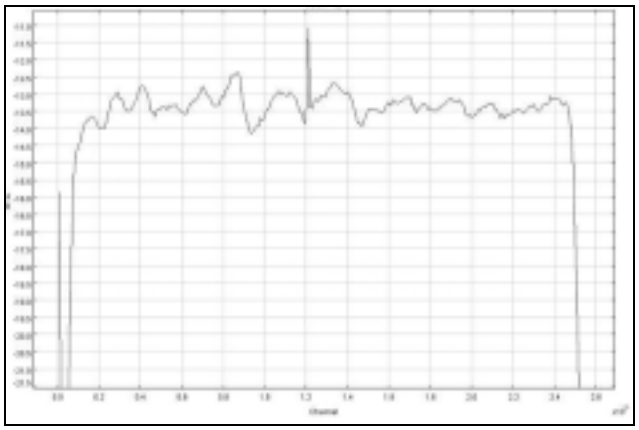

Fig. 14. Reconstructed spectrum from broad band noise source (0.5 dBm at Digitizer input in 2-4 GHz) with added weak line (-22dBm) at 3.0625GHz. The inband ripple is less than +/- 0.7 dB across the effective bandwidth (2.1 to 3.9 GHz due to an antialiasing filter)

The Digitizer Test Equipment [9] allows us to visualize the frequency response, sample statistics and Allan variance plots of the Digitizer assembly in a single screen (using the LabView graphical programming language) so that we can perform quick dynamic adjustments and characterization of the assembly. We have verified that in the full Digitizer assembly the VEGA samplers exhibit a good Allan variance profile. Typically, with 50 msec integration time step (12.5 Msamples) the variance decreases with the square root of time, as expected, and reaches a minimum of 2.5 10^{-8} around 100 sec.

7. Demultiplexer Production Acceptance Tests

The ALMA production chip design is identical to the final prototype chip described in Section 4. It is called PHOBOS 2 instead of PHOBOS 1 because of minor changes in the production layout.

Production acceptance tests include both static and dynamic tests. In order to perform qualifying static tests of our demultiplexer, we have first derived (using Monte Carlo simulations) the expected supply currents and output voltages for the PHOBOS circuit in a special test configuration allowing us to verify that the circuit outputs toggle. Later, *ST* has performed the recommended static tests on a first PHOBOS 2 production lot. These tests have been made with a special *ST* industrial tester [11] to allow the selection of the best 100 PHOBOS packaged chips.
At a later stage we have performed two categories of dynamic acceptance tests: one with the PCB described in Section 4 in the nominal and built-in-self-test mode, and the other one with a socket set-up on a special PCB in order to quickly test several chips without directly assembling the chips on a PCB. All tests have shown fully functional outputs and a total current consumption of about 280 mA in good agreement with results in Table 2.

The ALMA production will provide the number of chips required for the first eight ALMA antennas and for the rest of the array. The actual *ST* wafer production covers much more than what is needed for the ALMA project so that delivering the quantities needed for other known interferometric projects in Europe, North America and Japan should be possible.

8. Conclusion

We have described the main features of a new high speed, low dissipation, demultiplexer meeting the ALMA project requirements. We have relied on the BiCMOS SiGe technology used for the ALMA prototype sampler to diminish the demultiplexer development time. The design structure of this new demultiplexer is specific to ALMA and enables synchronization with the slightly phase shifting 4 GHz sampler clock.
The demultiplexer described in this work has reached the final industrial production stage after we have successfully performed several static and dynamic qualification tests. We have also demonstrated that the ALMA Digitizer assembly which incorporates our demultiplexer design is functional. The latter demonstration is made by reconstructing the power spectrum over the ALMA 2-4 GHz Intermediate Frequency bandwidth (using

a broad band noise source and a specific auto-correlator equipment) and by checking the state counts and Allan variance of the sampler.

Acknowledgements
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