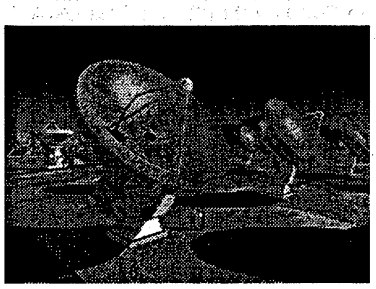
Draft only



Atacama Large Millimeter Array

Interface Control Document

Between:

Front End Band 4 Cartridge

And:

Front End Cartridge Bias Module

FEND-40.02.04.00-40.02.04.06-A-ICD

Version: A Status: Draft

2004-09-24

Prepared By:		
Name(s) and Signature(s)	**Organization**	**Date**
S. Asayama T. Takakiyo	NAOJ NAOJ	2004-09-24
Approved By:		
Name and Signature	**Organization**	**Date**
Released By:		
Name and Signature	**Organization**	**Date**

Change Record

Version	Date	Affected Section(s)	Change Request #	Reason/Initiation/Remarks
A	2004-09-17	N/A	N/A still draft document	

Table of Contents

1 TBD/TBC ITEMS 5
2 DESCRIPTION 5
2.1 Purpose 5
2.2 Scope 5
3 RELATED DOCUMENTS AND DRAWINGS 5
3.1 References 5
3.2 Abbreviations and Acronyms 6
3.3 Glossary 6
3.4 Related Interface Control Drawings 6
4 PHYSICAL SYSTEM INTERFACES 6
4.1 Mechanical Interface 6
4.2 Electrical Power Interface 7
4.3 Electronic Interface 7
5 SAFETY INTERFACE 14

List of Tables

TABLE 1 : MIXER BIAS LINES 9
TABLE 3 : PREAMPLIFIER BIAS LINES 11
TABLE 5 : MIXER MAGNET BIAS LINES 12
TABLE 7 : MIXER HEATER BIAS LINES, ESN PINS 13
TABLE 9 : CARTRIDGE TEMPERATURE SENSOR LINES 13
TABLE 11 : OTHER MONITOR POINTS (BAND 6 LIMITS SHOWN) 13

List of Figures

FIGURE 1 : HERMETIC FEED-THROUGH INTERFACE 15

1 TBD/TBC Items

The following items are to be determined (TBD):

Reference [1] author, doc. numbers
Maximum heater bias current.
Amplifier bias circuit voltage limit provided in the cartridge.

The following items are to be confirmed (TBC):

Different source impedance for mixer bias voltage and current monitors.
Amplifier bias requirements.
Required minimum voltage compliance range for the magnet bias.
Mixer bias circuit bandwidth.

2 Description

2.1 Purpose

The purpose of this document is to provide a detailed description of the interface between the Front End Band 4 Cartridge and Bias Module, both electrical and mechanical. Functionally, this specifies interfaces for the following components:

1. SIS mixer bias circuits.
2. SIS mixer de-flux heaters.
3. Cooled IF amplifiers.
4. Temperature sensors.

2.2 Scope

The scope of this document is limited to only what is necessary to clearly specify the interface between these subsystems. For detailed descriptions, specifications, circuit and wiring diagrams, etc. of the Band 4 cartridge or Bias module, please refer to the appropriate documents [1-2], listed below. This document was drafted with reference to [RD5]

3 Related Documents and Drawings

3.1 References

[1] FEND-40.02.04.00-001, "Front End Band 4 Cartridge Technical Specifications".

[2] FEND-40.04.02.00-002-A-MAN, "Front End Cartridge Bias Module Technical Description", W. Grammer.

[3] FEND-40.02.00.00-002, "Bias Feedthrough Plate Assembly", W. Grammer.

[4] ?, "Cartridge Base Plate band 4", K. Kimura

[5] FEND-40.02.09.00-40.04.02.00-A-ICD, "ICD between Band 9 Cartridge and Front End Cartridge Bias Module

3.2 Abbreviations and Acronyms

Signal – provides the name of the signal,
Pol – is one of the two orthogonal polarizations
Conn – connector

3.3 Glossary

None.

3.4 Related Interface Control Drawings

None.

4 Physical System Interfaces

4.1 Mechanical Interface

All interconnects between the cartridge and bias module are via two mating pairs of 51-pin metal-shell connectors, of the series MIL-PRF-83513 (original U.S. military designation; also referred to as "MDM" or "Micro-D" style connectors).

The cartridge-side connectors are hermetic with socket contacts, welded or epoxied onto a common flange with an O-ring groove, and bolted as an assembly into the cartridge base plate (the vacuum side of the assembly is also connectorized, but with pin contacts). Specifications and a detailed drawing of this feed-through assembly are given in [3]; refer to the drawing [4] for details regarding placement and orientation of the bias feed-through assembly on the cartridge base plate.

On the bias module side, mating connectors are right-angle, PCB-mount types with pin contacts and no jackposts (e.g., Glenair p/n M83513/11-G01NN). The bias

module blind-mates to the cartridge base plate connector, and is attached with four 10mm-long M5 socket head screws.

Figure 1 shows a diagram of the hermetic feed-through assembly installed in the base plate, from the ambient side. The precise location of Pin1 on each connector is given, relative to one of the four flange screws (M3 socket head, 8mm long). Also shown is the required nominal height of the mating connectors on the bias module side.

4.2 Electrical Power Interface

None.

4.3 Electronic Interface

In general, the maximum voltage range allowed on any pin shall not exceed ±5V, a limit imposed by the bias electronics. The only exception to this is the mixer heaters, which are specifically designed for 24VDC operation.

The baseline Band 4 configuration used a DSB mixer scheme that includes only one mixer, amplifier and magnet per polarization. Bias lines for a second mixer, amplifier and magnet per polarization are retained to allow a potential future upgrade to a side-band separating mixer scheme.

The Band 4 SIS mixers use a 6-wire DC bias scheme consisting of excitation lines, denoted as S+ and S-, and junction voltage and current sense lines Vj+, Vj-, Ij+, Ij-. Table 1 shows the connector and pin assignment, input/output range and required resolution (junction voltage set, voltage and current monitors) for each of the mixers.

The 3-stage IF preamplifiers for Band 4 each use a pair of gate and drain wires for biasing each stage, with a 7^{th} wire as the ground (device's source) return. Table 2 shows the connector and pin assignment, input range and required resolution (drain voltage and current set) for each of the preamps. Also shown in the table is the bias interface for the LEDs built into the preamps.

Each component mixer incorporates a superconducting electromagnet. In Band 4, each mixer uses one magnet bias channel. Table 3 shows the connector and pin assignment, input range and required resolution (magnet current set) for each magnet.

The mixer heaters on each polarization channel are wired together, and take 24VDC (switched), from the bias module. Table 4 shows the connector and pin assignment for each set of heaters.

There are a total of five 2-wire temperature sensors in the Band 4 cartridge, and one unused sensor channel. Table 5 gives the connector and pin assignment for each sensor, as well as the output range and required resolution (given in Kelvin rather than volts, due to the nonlinear sensor I-V characteristic).

In addition, there are a number of current and voltage monitor points not physically located at the hermetic feed-through connector, but whose resolution needs to be specified as part of this interface document. These items are listed in Table 6.

Lastly, two connector pins on Polarization '0' are dedicated to an electronic serial number (ESN). The device type is a Maxim DS2401; Table 4 shows the pin assignments.

A final note: All maximum values shown in the tables are absolute limits, and apply to *all* Front End bands. Maximum ranges specific to Band 4 are shown as footnotes, in cases where they are less than the absolute limits.

Table 1 : Mixer Bias Lines

Conn	Pin	Signal	Pol	Comp. Mixer	Description	Maximum Range	Source
J12-C9	13	S+M1P0	0	1	+ Source	-4V to +4V @ 1 mA[1,2,3]	Bias Mod.
J12-C9	31	S-M1P0	0	1	- Source	0V	Bias Mod.
J12-C9	30	VJ+M1P0	0	1	+ Junc. voltage	-20mV to +20mV[4]	Mixer
J12-C9	47	VJ-M11P0	0	1	- Junc. voltage		Mixer
J12-C9	12	IJ+M1P0	0	1	+ Junc. current	-10mV to +10mV[5]	Mixer
J12-C9	46	IJ-M1P0	0	1	- Junc. current		Mixer
J12-C9	5	S+M2P0	0	2	+ Source	-4V to +4V @ 1 mA[1,2,3]	Bias Mod.
J12-C9	23	S-M2P0	0	2	- Source	0V	Bias Mod.
J12-C9	22	VJ+M2P0	0	2	+ Junc. voltage	-20mV to +20mV[4]	Mixer
J12-C9	39	VJ-M2P0	0	2	- Junc. voltage		Mixer
J12-C9	4	IJ+M2P0	0	2	+ Junc. current	-10mV to +10mV[5]	Mixer
J12-C9	38	IJ-M2P0	0	2	- Junc. current		Mixer
J12-C9	14	MXRFRM1P0	0	1	Mixer frame ground [6]		Mixer
J12-C9	6	MXRFRM2P0	0	2	Mixer frame ground [6]		Mixer
J14-C9	13	S+M1P1	1	1	+ Source	-4V to +4V @ 1 mA[1,2,3]	Bias Mod.
J14-C9	31	S-M1P1	1	1	- Source	0V	Bias Mod.
J14-C9	30	VJ+M1P1	1	1	+ Junc. voltage	-20mV to +20mV[4]	Mixer
J14-C9	47	VJ-M1P1	1	1	- Junc. voltage		Mixer
J14-C9	12	IJ+M1P1	1	1	+ Junc. current	-10mV to +10mV[5]	Mixer
J14-C9	46	IJ-M1P1	1	1	- Junc. current		Mixer
J14-C9	5	S+M2P1	1	2	+ Source	-4V to +4V @ 1 mA[1,2,3]	Bias Mod.
J14-C9	23	S-M2P1	1	2	- Source	0V	Bias Mod.
J14-C9	22	VJ+M2P1	1	2	+ Junc. voltage	-20mV to +20mV[4]	Mixer
J14-C9	39	VJ-M2P1	1	2	- Junc. voltage		Mixer
J14-C9	4	IJ+M2P1	1	2	+ Junc. current	-10mV to +10mV[5]	Mixer
J14-C9	38	IJ-M2P1	1	2	- Junc. current		Mixer
J14-C9	14	MXRFRM1P1	1	1	Mixer frame ground [6]		Mixer

[1] Nominal Band 4 range is **±3V**. This assumes a 1-junction mixer with a bias tee [5], additional 3KΩ internal source resistor and minimum normal junction resistance of 10Ω. This yields ±10 mV at the mixer. Assuming that the Band 6 protection circuit is used, circuitry within the cartridge clamps the applied voltage at ±3V on S+, and ±0.7V on S-, VJ+, VJ-, IJ+ and IJ-, relative to earth ground.

[2] For Band 4, minimum mixer voltage set resolution is **0.005mV** (referred to mixer junction).

[3] For Band 4, an (Allen variance) bias stability of 0.2 μV over a time scale of 0.1-1 sec is needed to keep the bias' contribution to the cartridge gain stability below the 1.6×10^{-4} level budgeted for the bias stability (out of 6×10^{-4} specified in the cartridge technical specifications).

[4] For Band 4, minimum mixer voltage monitor resolution is **0.005mV**. VJ source impedance = 10 KΩ.

[5] For Band 4, nominal range for mixer current monitor is **±10mV**; minimum mixer current monitor resolution is **1μV**. IJ source impedance = 20 KΩ **(TBC)**; Current sense resistor = 10-20Ω.

[6] Added in case required for shields, *etc.*, but Band 4 does not intend to use the mixer frame ground.

Table 1 : Mixer Bias Lines

Conn	Pin	Signal	Pol	Comp. Mixer	Description	Maximum Range	Source
J14-C9	6	MXRFRM2P1	0	2	Mixer frame ground [6]		Mixer

Table 2 : Preamplifier Bias Lines

Conn	Pin	Signal	Pol	Port	Description	Maximum Range	Source
J12-C9	29	VD1_A1P0	0	1	Drain voltage, HFET stage 1	0 to +3V @ 20mA[7,8,9]	Bias Mod.
J12-C9	11	VD2_A1P0	0	1	Drain voltage, HFET stage 2	----"----	Bias Mod.
J12-C9	45	VD3_A1P0	0	1	Drain voltage, HFET stage 3	----"----	Bias Mod.
J12-C9	27	VD4_A1P0	0	1	Drain voltage, HFET stage 4[10]	----"----	Bias Mod.
J12-C9	44	VG1_A1P0	0	1	Gate voltage, HFET stage 1	±5.0V @ 1mA[11]	Bias Mod.
J12-C9	10	VG2_A1P0	0	1	Gate voltage, HFET stage 2	----"----	Bias Mod.
J12-C9	28	VG3_A1P0	0	1	Gate voltage, HFET stage 3	----"----	Bias Mod.
J12-C9	9	VG4_A1P0	0	1	Gate voltage, HFET stage 4[10]	----"----	Bias Mod.
J12-C9	48	GNDAMP1P0	0	1	Common, HFET bias		Bias Mod.
J12-C9	43	VLED+P0	0	1	LED supply current[12]	0 to 6mA	Bias Mod.
J12-C9	26	VLED-P0	0	1	LED return current[12]	----"----	Bias Mod.
J12-C9	21	VD1_A2P0	0	2	Drain voltage, HFET stage 1	0 to +3V @ 20mA[7,8,9]	Bias Mod.
J12-C9	3	VD2_A2P0	0	2	Drain voltage, HFET stage 2	----"----	Bias Mod.
J12-C9	37	VD3_A2P0	0	2	Drain voltage, HFET stage 3	----"----	Bias Mod.
J12-C9	19	VD4_A2P0	0	2	Drain voltage, HFET stage 4[10]	----"----	Bias Mod.
J12-C9	36	VG1_A2P0	0	2	Gate voltage, HFET stage 1	±5.0V @ 1mA[11]	Bias Mod.
J12-C9	2	VG2_A2P0	0	2	Gate voltage, HFET stage 2	----"----	Bias Mod.
J12-C9	20	VG3_A2P0	0	2	Gate voltage, HFET stage 3	----"----	Bias Mod.
J12-C9	1	VG4_A2P0	0	2	Gate voltage, HFET stage 4[10]	----"----	Bias Mod.
J12-C9	40	GNDAMP2P0	0	2	Common, HFET bias		Bias Mod.
J12-C9	33	AUXGND1P0	0	1	Auxiliary Preamp Ground[10]		Bias Mod.
J12-C9	15	AUXGND2P0	0	2	Auxiliary Preamp Ground[10]		Bias Mod.
J14-C9	29	VD1_A1P1	1	1	Drain voltage, HFET stage 1	0 to +3V @ 20mA[7,8,9]	Bias Mod.
J14-C9	11	VD2_A1P1	1	1	Drain voltage, HFET stage 2	----"----	Bias Mod.
J14-C9	45	VD3_A1P1	1	1	Drain voltage, HFET stage 3	----"----	Bias Mod.
J14-C9	27	VD4_A1P1	1	1	Drain voltage, HFET stage 4[10]	----"----	Bias Mod.
J14-C9	44	VG1_A1P1	1	1	Gate voltage, HFET stage 1	±5.0V @ 1mA[11]	Bias Mod.
J14-C9	10	VG2_A1P1	1	1	Gate voltage, HFET stage 2	----"----	Bias Mod.
J14-C9	28	VG3_A1P1	1	1	Gate voltage, HFET stage 3	----"----	Bias Mod.
J14-C9	9	VG4_A1P1	1	1	Gate voltage, HFET stage 4[10]	----"----	Bias Mod.
J14-C9	48	GNDAMP1P1	1	1	Common, HFET bias	----"----	Bias Mod.
J14-C9	43	VLED+P1	1	1	LED supply current[12]	0 to 6mA	Bias Mod.

[7] For Band 4, the nominal voltage range is **0.3 to 1.5V**. The drain current shall be in the range 2-7 mA. Protection circuitry within the cartridge limits the applied drain voltage on all HFETs to the range TBD.

[8] Band 4 min. drain voltage set resolution is **10 mV**, with an absolute accuracy of **20 mV**; min. drain current set resolution is **20 μA**, with an absolute accuracy of **0.1 mA**.

[9] For Band 4, a drain bias stability **800 nV/Hz$^{0.5}$ at 1 sec.** is needed to meet the 10^{-4} gain stability requirement in the amplifier specification. A total bias noise of less than **20 μV_{rms}** over 0.1-800 Hz is also needed. The bias circuit regulation bandwidth should cover DC to 20 Hz.

[10] Not used for Band 4.

[11] For Band 4, protection circuitry within the cartridge limits the applied gate voltage to a range of **±TBDV**.

[12] The use of LEDs is not foreseen in the Band 4 amplifiers.

Table 2 : Preamplifier Bias Lines

Conn	Pin	Signal	Pol	Port	Description	Maximum Range	Source
J14-C9	26	VLED-P1	1	1	LED return current[12]	----"----	Bias Mod.
J14-C9	21	VD1_A2P1	1	2	Drain voltage, HFET stage 1	0 to +3V @ 20mA[7,8,9]	Bias Mod.
J14-C9	3	VD2_A2P1	1	2	Drain voltage, HFET stage 2	----"----	Bias Mod.
J14-C9	37	VD3_A2P1	1	2	Drain voltage, HFET stage 3	----"----	Bias Mod.
J14-C9	19	VD4_A2P1	1	2	Drain voltage, HFET stage 4[10]	----"----	Bias Mod.
J14-C9	36	VG1_A2P1	1	2	Gate voltage, HFET stage 1	±5.0V @ 1mA[11]	Bias Mod.
J14-C9	2	VG2_A2P1	1	2	Gate voltage, HFET stage 2	----"----	Bias Mod.
J14-C9	20	VG3_A2P1	1	2	Gate voltage, HFET stage 3	----"----	Bias Mod.
J14-C9	1	VG4_A2P1	1	2	Gate voltage, HFET stage 4[10]	----"----	Bias Mod.
J14-C9	40	GNDAMP2P1	1	2	Common, HFET bias		Bias Mod.
J14-C9	33	AUXGND1P1	1	1	Auxiliary Preamp Ground[10]		Bias Mod.
J14-C9	15	AUXGND2P1	1	2	Auxiliary Preamp Ground[10]		Bias Mod.

Table 3 : Mixer Magnet Bias Lines

Conn	Pin	Signal	Pol	Description	Maximum Range	Source
J12-C9	41	IMAG+M1P0	0	+ Magnet current	0 to ±100mA[13]	Bias Mod.
J12-C9	24	IMAG-M1P0	0	- Magnet current		Bias Mod.
J12-C9	49	IMAG+M2P0	0	+ Magnet current[14]	----"----	Bias Mod.
J12-C9	32	IMAG-M2P0	0	- Magnet current[14]		Bias Mod.
J14-C9	41	IMAG+M1P0	1	+ Magnetic field current	----"----	Bias Mod.
J14-C9	24	IMAG-M1P0	1	- Magnetic field current		Bias Mod.
J14-C9	49	IMAG+M2P0	1	+ Magnet current[14]	----"----	Bias Mod.
J14-C9	32	IMAG-M2P0	1	- Magnet current[14]		Bias Mod.

[13] For Band 9, the nominal range is **±50mA;** min. current set resolution = **0.005 mA**. Magnet biasing is constant-current and programmable. Required min. compliance range = **±1V (TBC)**.

[14] Not used in DSB mixer configuration.

Table 4 : Mixer Heater Bias Lines, ESN Pins

Conn	Pin	Signal	Pol	Description	Maximum Range	Source
J12-C9	25	VHTR+P0	0	+ Mixer heater voltage	24VDC @ 200 mA[15]	Bias Mod.
J12-C9	7	VHTR-P0	0	- Mixer heater voltage	----"----	Bias Mod.
J14-C9	25	VHTR+P1	1	+ Mixer heater voltage	----"----	Bias Mod.
J14-C9	7	VHTR-P1	1	- Mixer heater voltage	----"----	Bias Mod.
J12-C9	17	ESN_DATA	0	ESN chip data line	TTL, 0-5V	Cartridge
J12-C9	35	ESN_GND	0	ESN chip ground line	0V	Cartridge

Table 5 : Cartridge Temperature Sensor Lines

Conn	Pin	Signal	Pol	Description[16]	Maximum Range	Source
J12-C9	16	90KTMP+	-	+Temp. sensor, 90K plate	0.5V to 1.61V[17]	Sensor
J12-C9	50	90KTMP-	-	-Temp. sensor, 90K plate	----"----	----"----
J14-C9	16	20KTMP+	-	+Temp. sensor, 20K plate	----"----	----"----
J14-C9	50	20KTMP-	-	-Temp. sensor, 20K plate	----"----	----"----
J12-C9	51	4KTMP+	-	+Temp. sensor, 4K plate	----"----	----"----
J12-C9	34	4KTMP-	-	- Temp. sensor, 4K plate	----"----	----"----
J12-C9	8	MXRTMP+P0	0	+ Temp. sensor, Mixer	----"----	----"----
J12-C9	42	MXRTMP-P0	0	- Temp. sensor, Mixer	----"----	----"----
J14-C9	8	MXRTMP+P1	1	+ Temp. sensor, Mixer	----"----	----"----
J14-C9	42	MXRTMP-P1	1	- Temp. sensor, Mixer	----"----	----"----
J14-C9	51	SPARETMP+	-	+ Temp. sensor, spare	----"----	----"----
J14-C9	34	SPARETMP-	-	- Temp. sensor, spare	----"----	----"----

Table 6 : Other Monitor Points [18]

Parameter[19]	Description	Maximum Range	Resolution
IMAG	Magnet current	-50mA to +50mA	0.3mA[20]
VMAG	Magnet voltage	± 3V	2mV[20]
IHTR	Mixer heater current	0 to 83mA	0.1mA
VD	HFET Drain voltage	0 to +2.5V	10mV
ID	HFET Drain current	0 to 20mA	0.1mA
VG	HFET Gate voltage	-0.7 V to +0.7 V	50mV

[15] Heater biasing is fixed constant-voltage, with ON/OFF control. For Band 9, the maximum current = **TBD mA**. Minimum ON/OFF rise/fall time for heater current = **100 ms**.

[16] All temperature sensors are silicon diode type, Lakeshore DT-670A (or equivalent).

[17] Corresponds to a temperature range from 325K to 3K, with 10μA ± 0.05% sensor current. Required minimum resolution = **0.1K**.

[18] The Band 6 limits are shown here, and are acceptable for Band 9.

[19] Common to both polarizations and all channels.

[20] Required current and voltage monitor resolution, for measurement of normal (i.e., warm) coil resistance.

5 Cartridge Grounding Scheme

The mixer bias will be grounded inside the mixer block (on the return side of the SIS device).

The amplifier bias will be grounded inside the amplifier housing (on the 4K level of the cryostat).

The heater will be grounded inside the mixer housing.

The magnet will be isolated from ground.

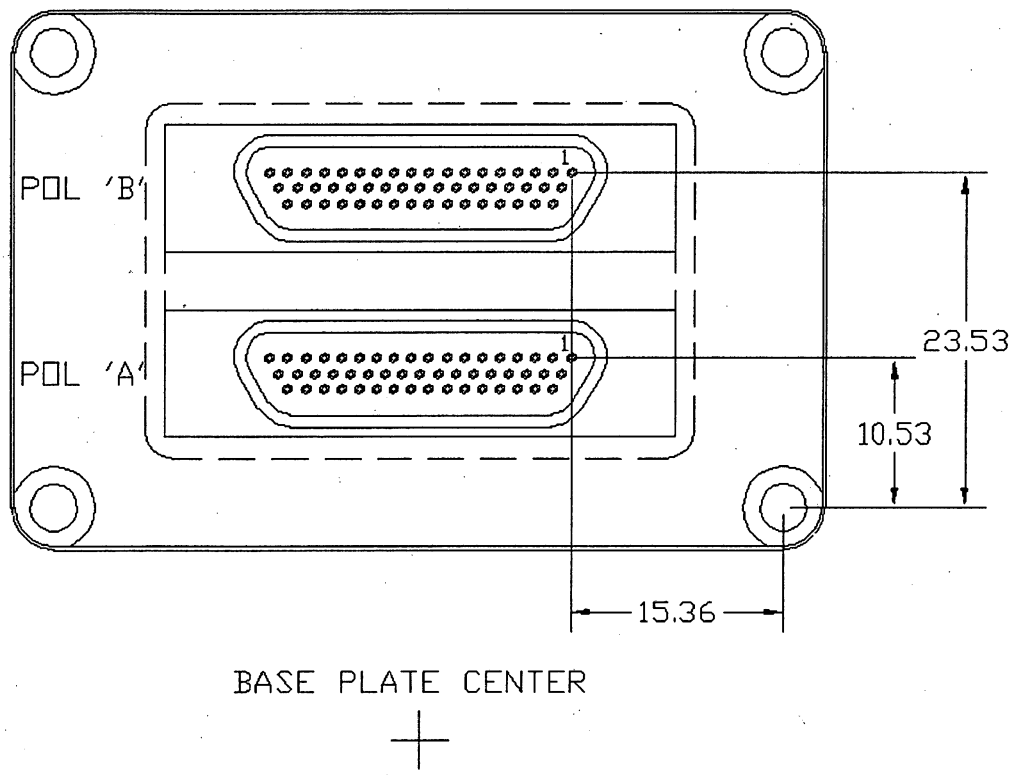
The temperature sensors will be isolated from ground.

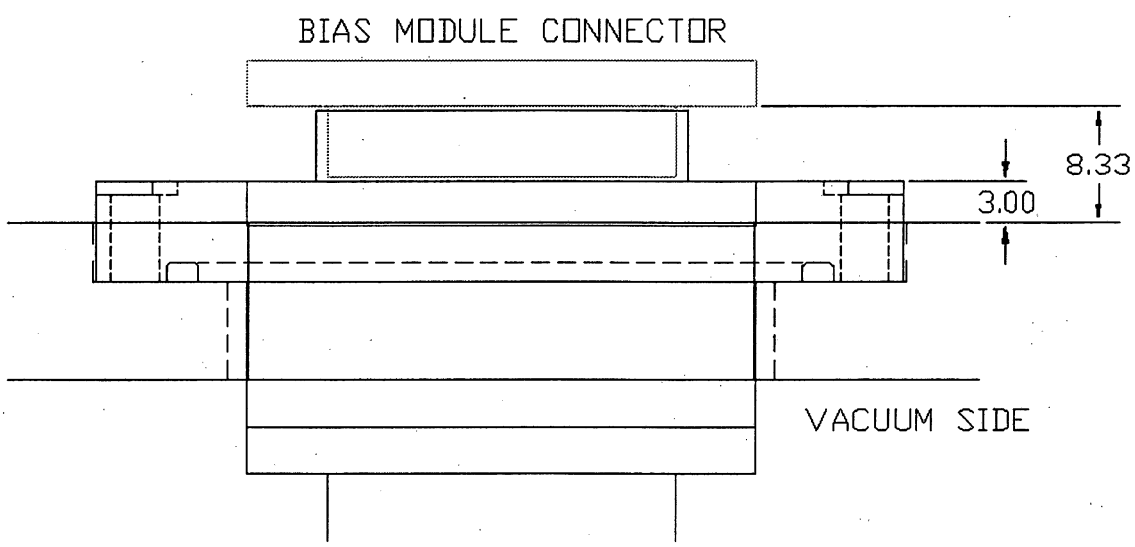
6 Mixer Bias Circuit Bandwidth

Due to the high bandwidth of the bias electronics' mixer bias circuit, the cartridge's mixer bias circuit (including ESD protection) should have an input bandwidth of at least 50 kHz (TBC).

7 Safety Interface

The specified heater voltage (+24V) is not considered a potential shock hazard. The bias module side (the source end) has recessed and shrouded pin contacts on the mating connectors, which should reduce the risk of shorting.





Note that Polarizations 'A' and 'B' correspond to '0' and '1', respectively.

Figure 1 : Hermetic Feed-Through Interface