NATIONAL RADIO ASTRONOMY OBSERVATORY
Green Bank, West Virginia

Electronics Division Internal Report No. 104

A DIGITAL FREQUENCY SYNTHESIZER

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SEPTEMBER 1971

NUMBER OF COPIES: 150

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A DIGITAL FREQUENCY SYNTHESIZER

M. Balister

I. Introduction

The availability of fast digital integrated circuits has made possible the construction of digital frequency synthesizers with output frequencies of up to several hundred megahertz. The block diagram of the basic digital synthesizer is shown in Figure 1. The critical block is the programmable frequency divider which has to operate at F_0; the current practical upper frequency limit is about 50 MHz.

There are two ways to extend the output frequency range beyond this 50 MHz limit. The first is to use a frequency multiplier to give MF_0; the second is to use a prescaler between F_0 and the input to the divider. Figure 2 shows a digital frequency synthesizer using both these techniques.

There was an NRAO requirement for a stable signal source covering the frequency range 350-450 MHz in 1 MHz steps. A digital frequency synthesizer of the type outlined in Figure 2 meeting this specification is described in this report.

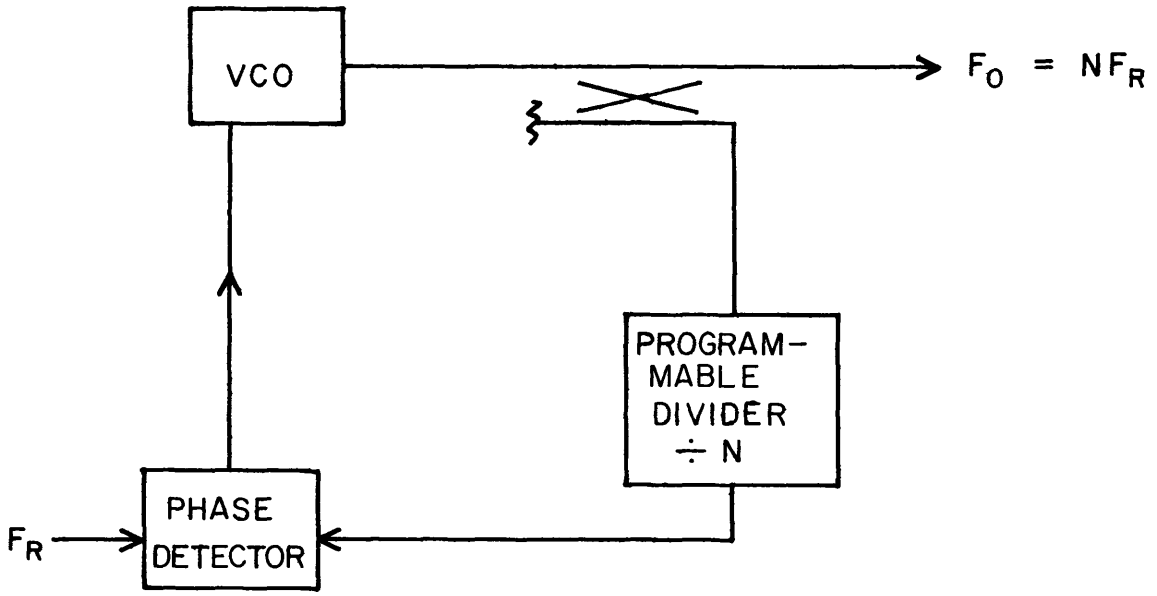
II. Description

1) RF Circuits

Figure 3 shows the detailed block diagram of the synthesizer; the output frequency can be set in MHz steps from 300-550 MHz by a front panel Digitran switch. A panel light indicates when the PLL is locked; a front panel voltage adjustment must be made if the loop does not lock.

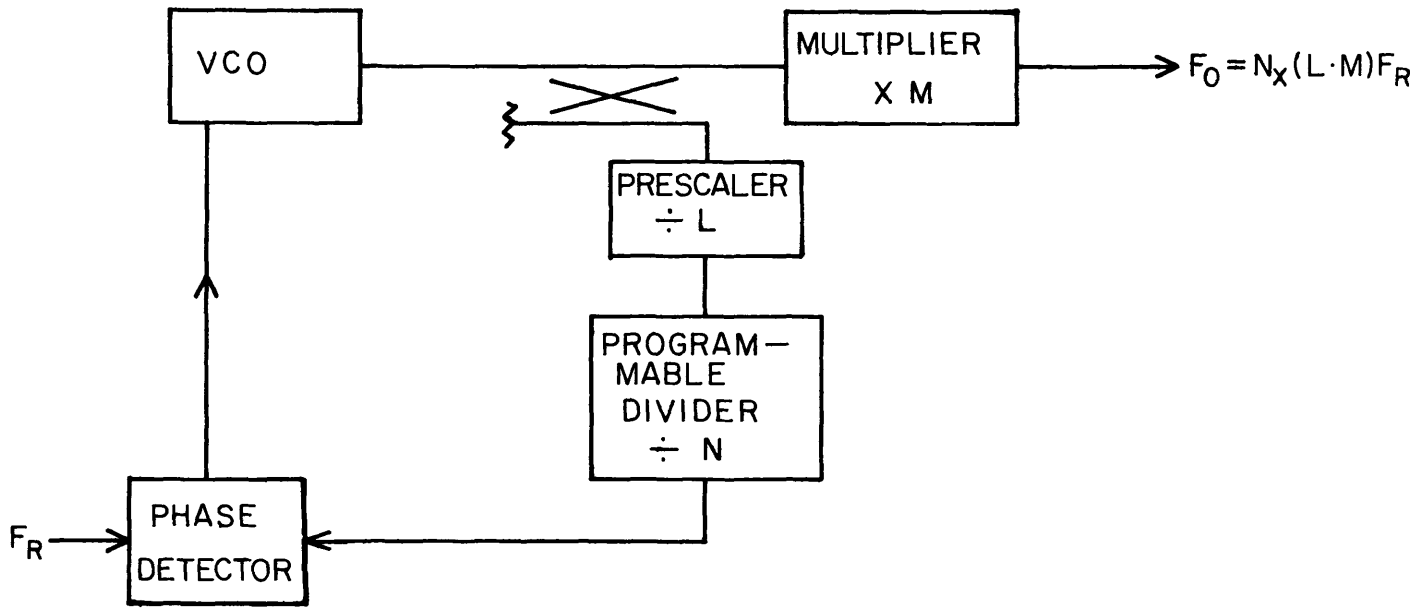
The VCO is a varactor tuned transistor oscillator covering the frequency range 150-300 MHz; the output power is $\geq$ 100 mW. The output drives a X2 frequency multiplier; a 16 dB directional coupler couples off some of the input signal to drive the prescaler. Both these circuits are shown in Figures 4 and 5. The prescaler consists of a MECL III 1670 followed by a MECL II 1034; both are D-style flip-flops. The divider will operate to 300 MHz; however, correct operation above 275 MHz is critically dependent on the input level. This limits the operation of the synthesizer to about 550 MHz.

The fundamental and third harmonic outputs of the doubler are filtered by a 300-600 MHz bandpass filter. An Avantek VA 103 unit amplifier boosts the output to about 6 mW.



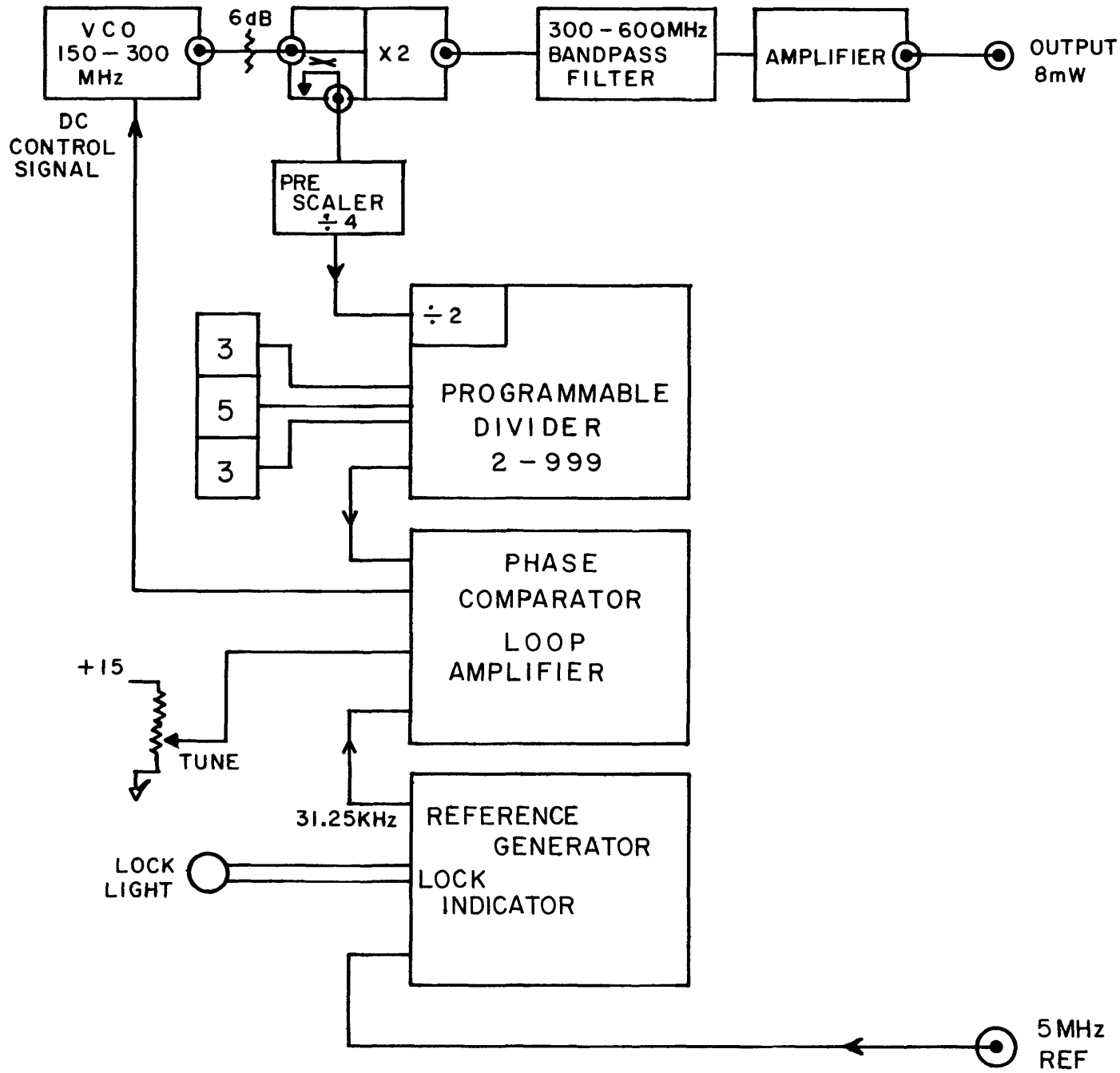
BASIC BLOCK DIAGRAM OF DIGITAL SYTHESIZER

FIG. 1



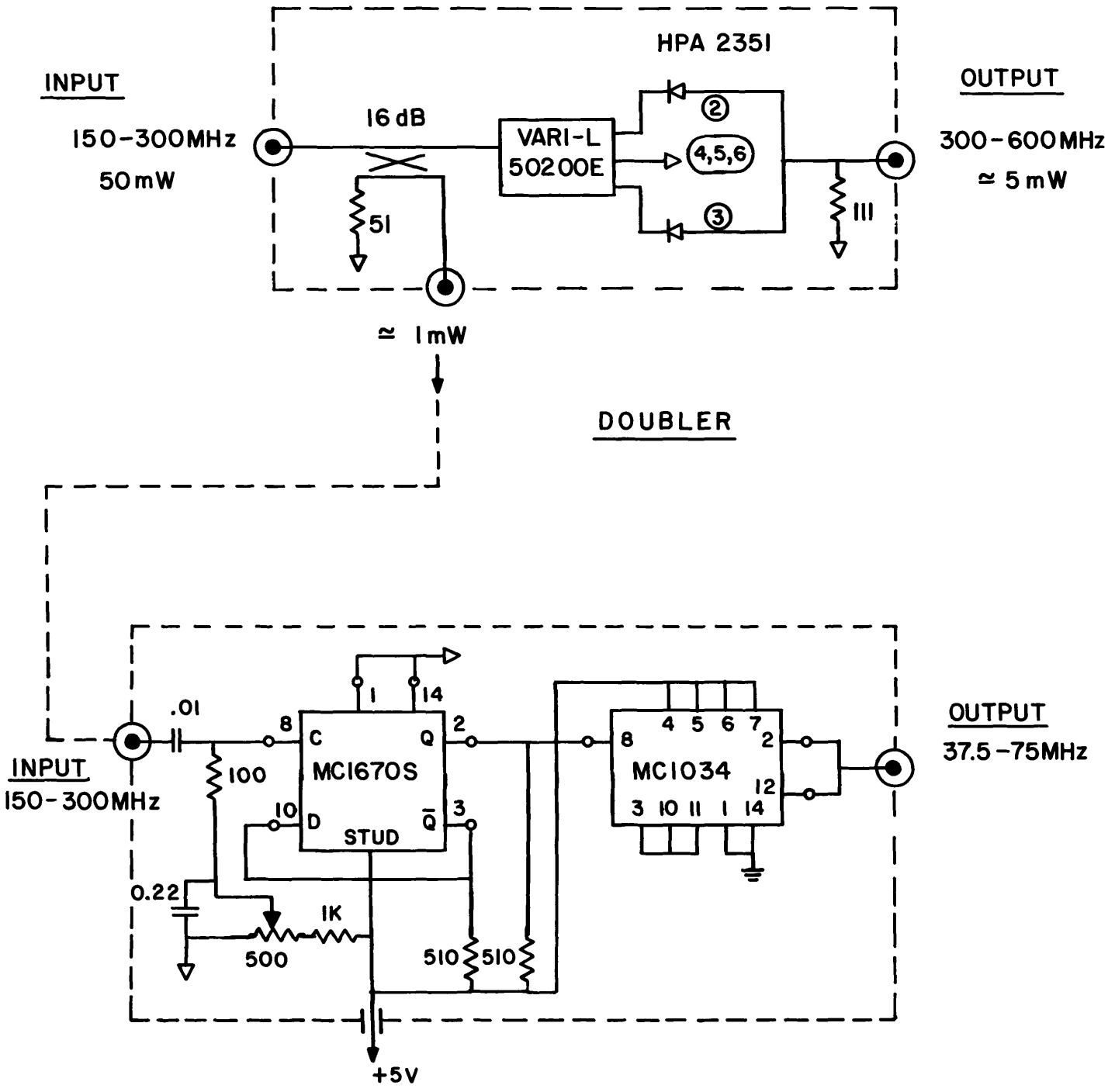
HIGHER FREQUENCY VERSION OF BASIC SYNTHESIZER

FIG. 2



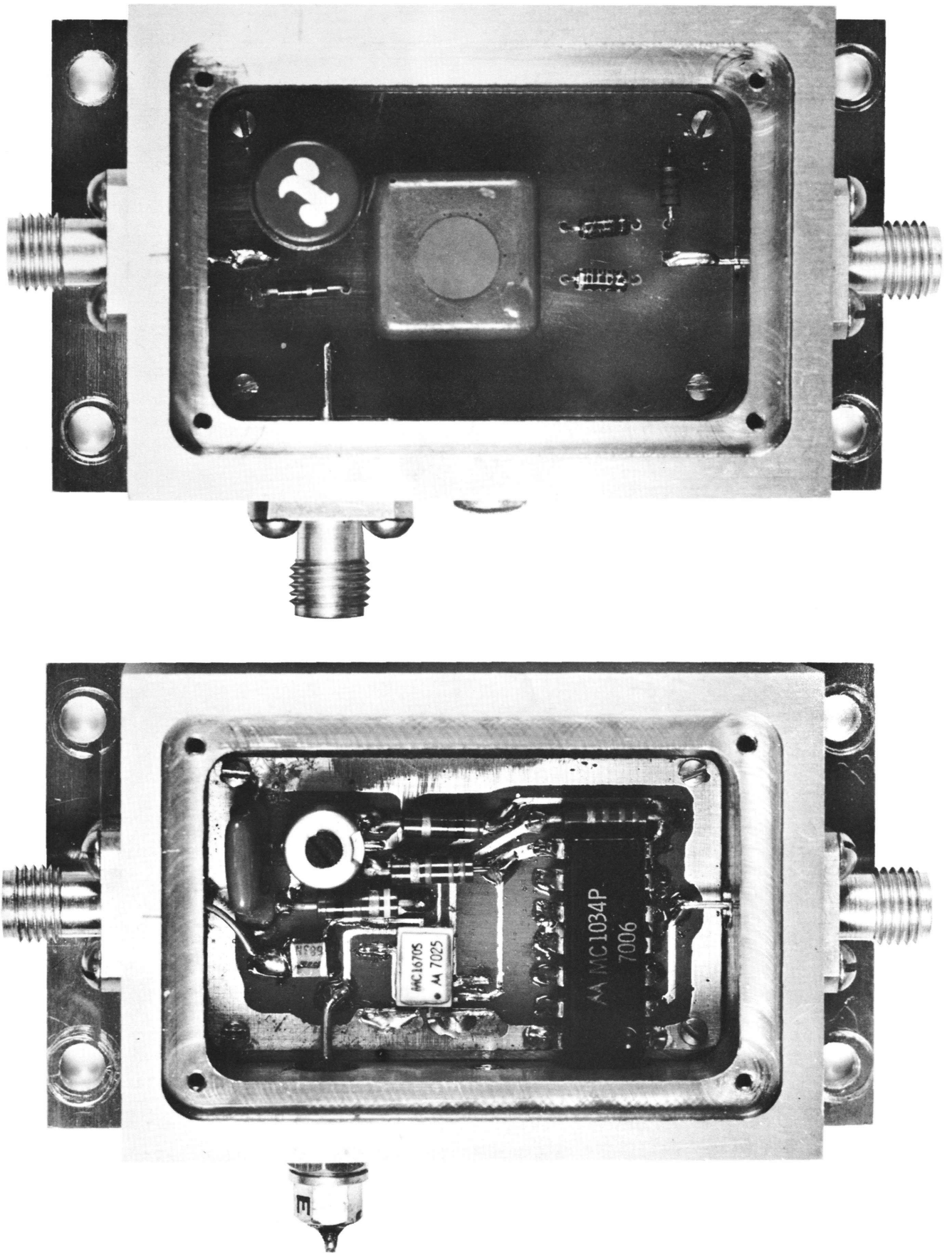
DETAILED BLOCK DIAGRAM OF SYNTHESIZER

FIG. 3



÷4 PRE SCALER

FIG. 4



PHOTOGRAPH OF DOUBLER / PRESCALER

FIG. 5

2) Programmable Divider

A design for a suitable 2-999 programmable divider is described in Motorola Application Note AN 456 (Appendix 1). MECL II logic is used throughout and the maximum speed of operation is 50 MHz. A ML 1034 was included at the input as a ÷ 2 prescaler to reduce the maximum frequency at the input to the programmable divider to 37.5 MHz. (The counter is preset via the front panel Digitran switch.) Figure 6 shows both sides of the divider board.

3) Reference Divider

The reference divider takes the 5 MHz reference signal and divides it down to the required F_R. In this case

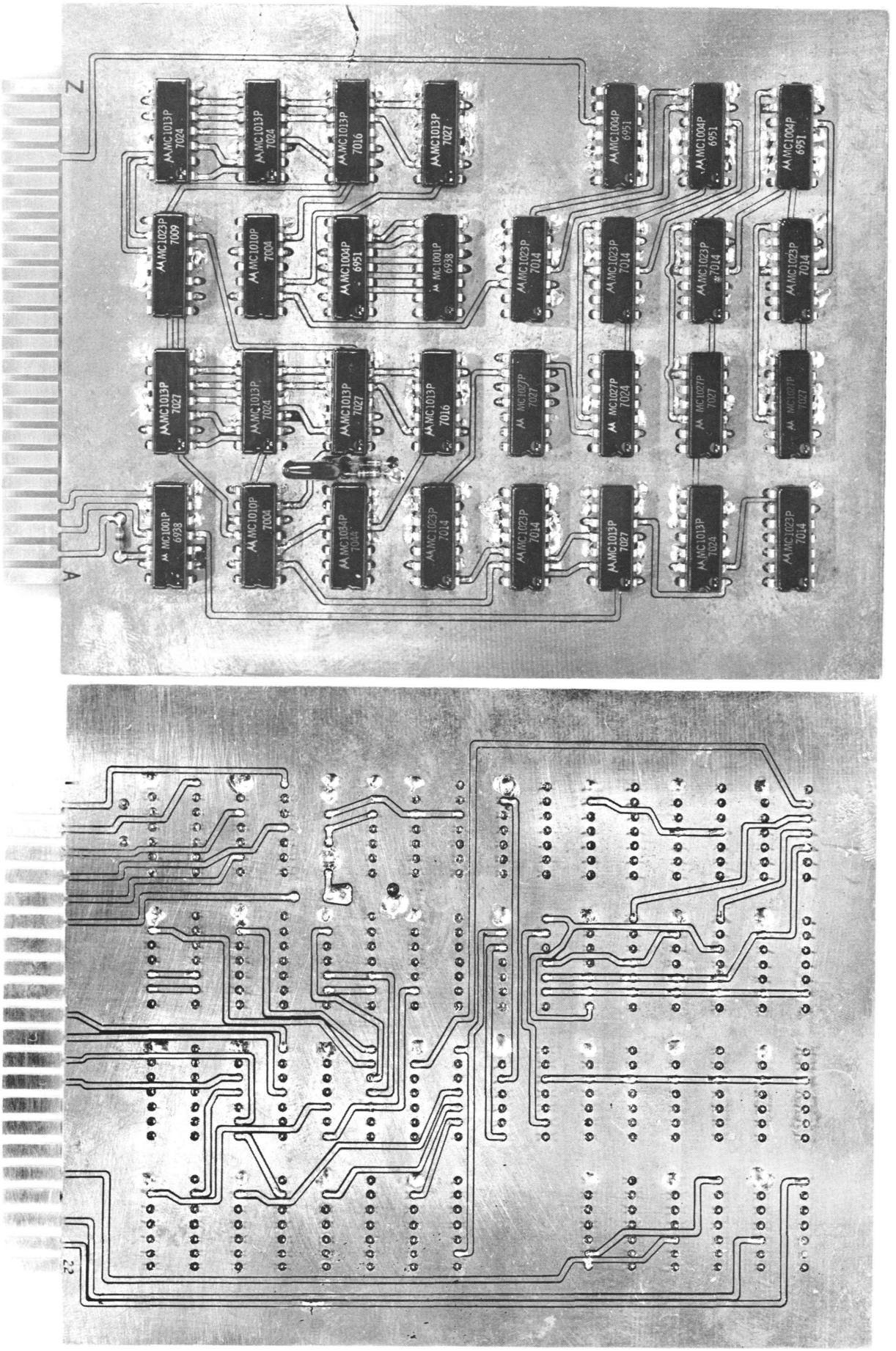
$$F_R = \frac{\text{Minimum Freq Step}}{L \times M} = \frac{10^6}{(4 \times 2)\,2} = 62.5 \text{ kHz.}$$

A further division of two was made to obtain the square wave signal necessary to develop the triangular waveform for the phase detector. (In retrospect the square wave could easily have been produced at 62.5 kHz — this would have simplified the circuit somewhat.) Figure 7 shows the divider chain; the 5 MHz input is on pin C and the reference phase detector drive is on pin N.

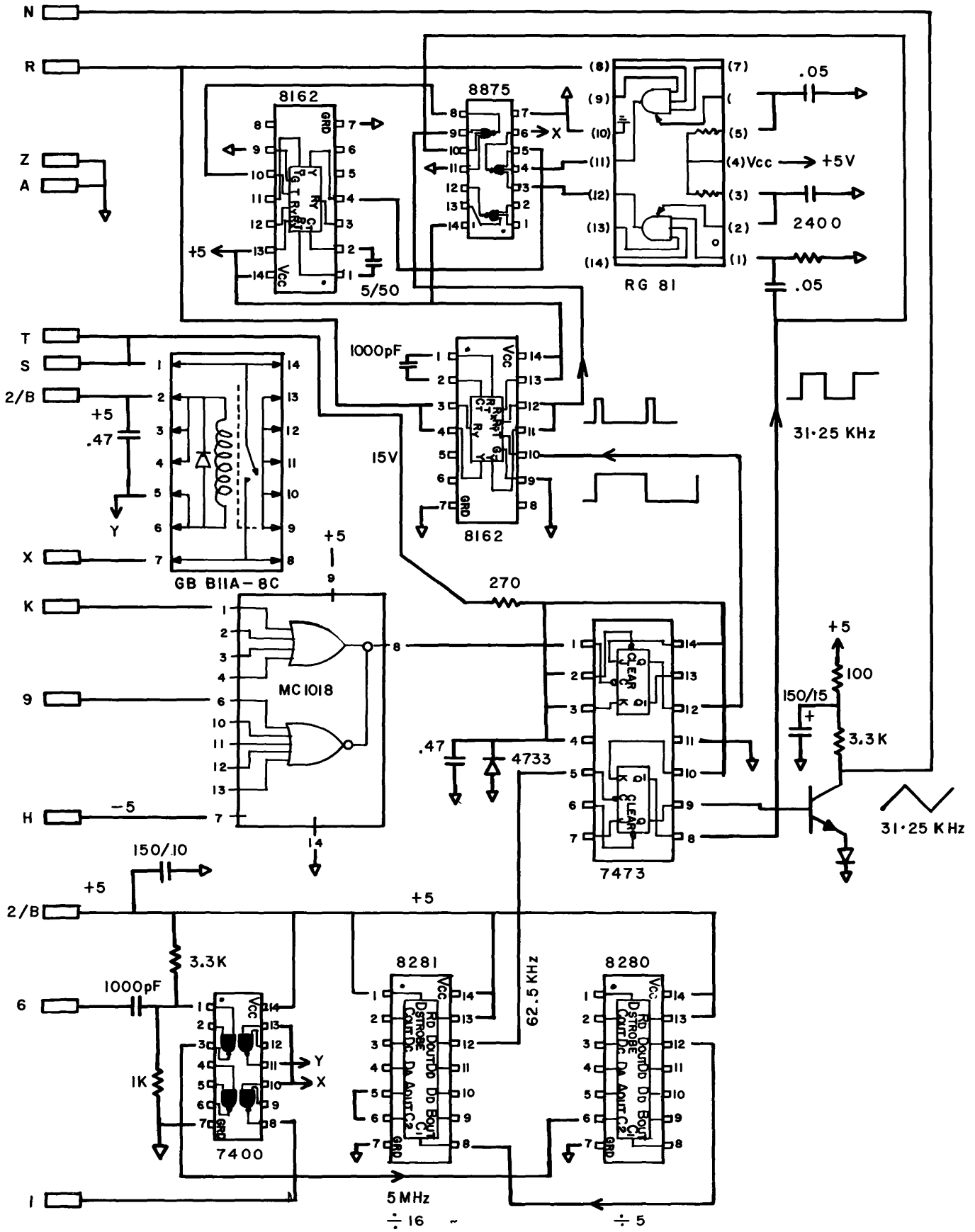
The programmable divider output goes to pins 9 and K on the circuit board shown in Figure 7. The MC 1018 converts the MECL II to T^2L logic levels. The pulse chain is converted to a 1 μs pulse chain with a 31.25 kHz repetition rate (when loop is closed).

III. Phase Detector and Loop Amplifier

A sample and hold phase detector was used (Figure 8); this type is best since the reference signal output is minimal and easily filtered by the following amplifier. The sampling is done with a Teledyne FET gate which is compatible with T^2L logic signals. The output voltage is held by a 1000 pF capacitor; a high input impedance FET amplifier follows. The voltage developed across this capacitor depends on the relative phase of the signal pulse chain and the triangular reference signal.

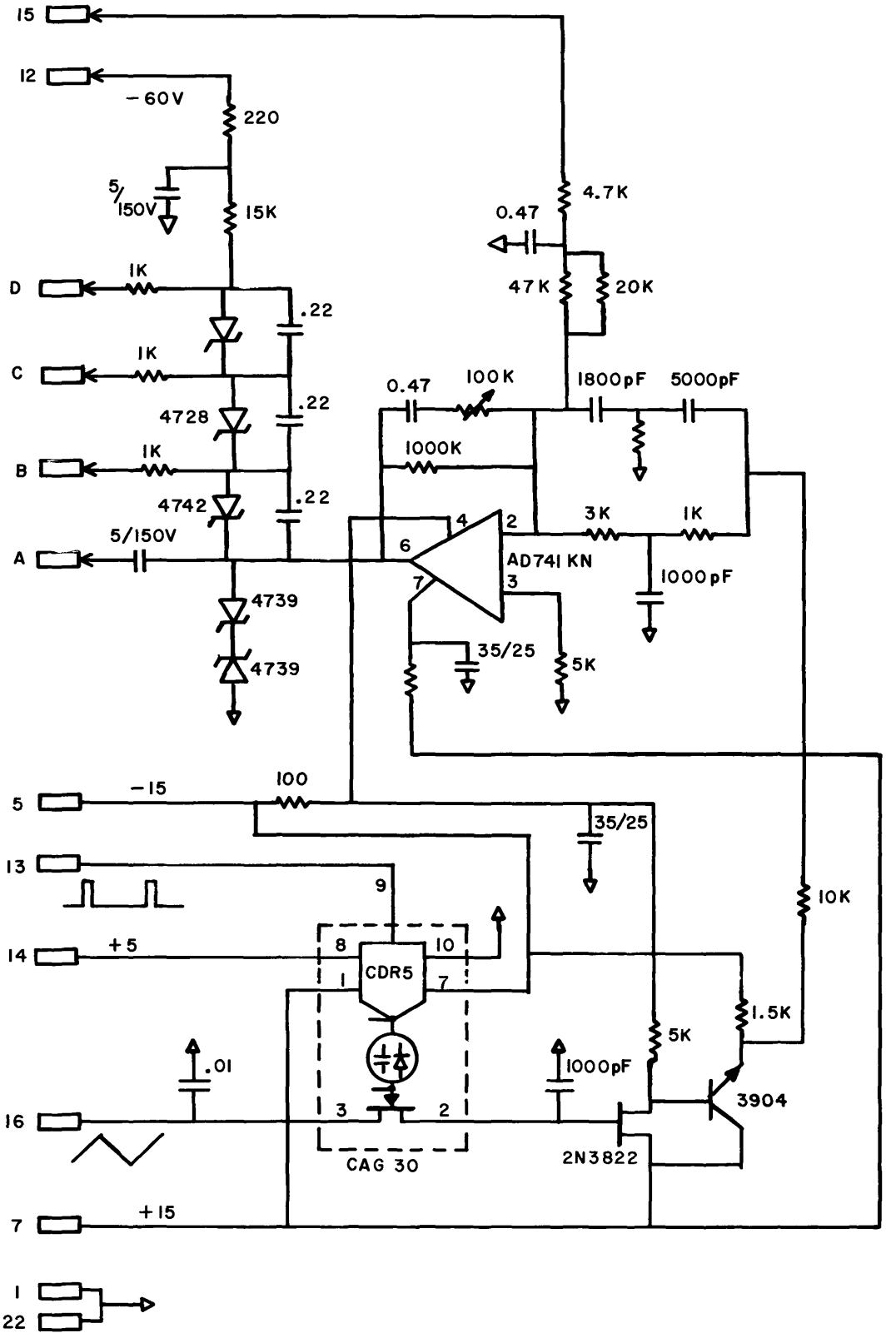


PHOTOGRAPH OF PROGRAMMABLE DIVIDER
FIG. 6



REFERENCE DIVIDER & LOCK INDICATOR

FIG. 7



PHASE DETECTOR & LOOP AMPLIFIER

FIG. 8

The following operational amplifier has a notch at 31.25 kHz to reject the phase detector ripple which causes AM sidebands on the VCO output signal. The DC output from the AD 741 KN has a ± 10 V swing which is insufficient to time the VCO over its full range (requires -10 V ⟶ -50 V). The VCO was coarse tuned from a zener diode voltage divider chain by the 100's of MHz on the Digitran switch. The final diode was connected to the AD 741 KN output; consequently at each of the three taps the voltage can be swung ± 10 V. A front panel control was found to be desirable to fine tune the oscillator to the correct frequency. A lock light indicates when the PLL is locked.

IV. Lock Indicator

The three integrated circuits at the top of Figure 7 form the lock indicator circuit. The 8875 senses when the signal and reference pulse trains are at different frequencies; the RG-81 confirmes the presence of the two pulse trains. Provided there are two pulse trains and they are at the same repetitive rate, a lock is indicated by the front panel light. Fifteen volts are also applied to the output signal amplifier.

V. Power Supplies and Interconnection Wiring

Power supplies and interconnection wiring are shown in Figure 9; they are self-explanatory.

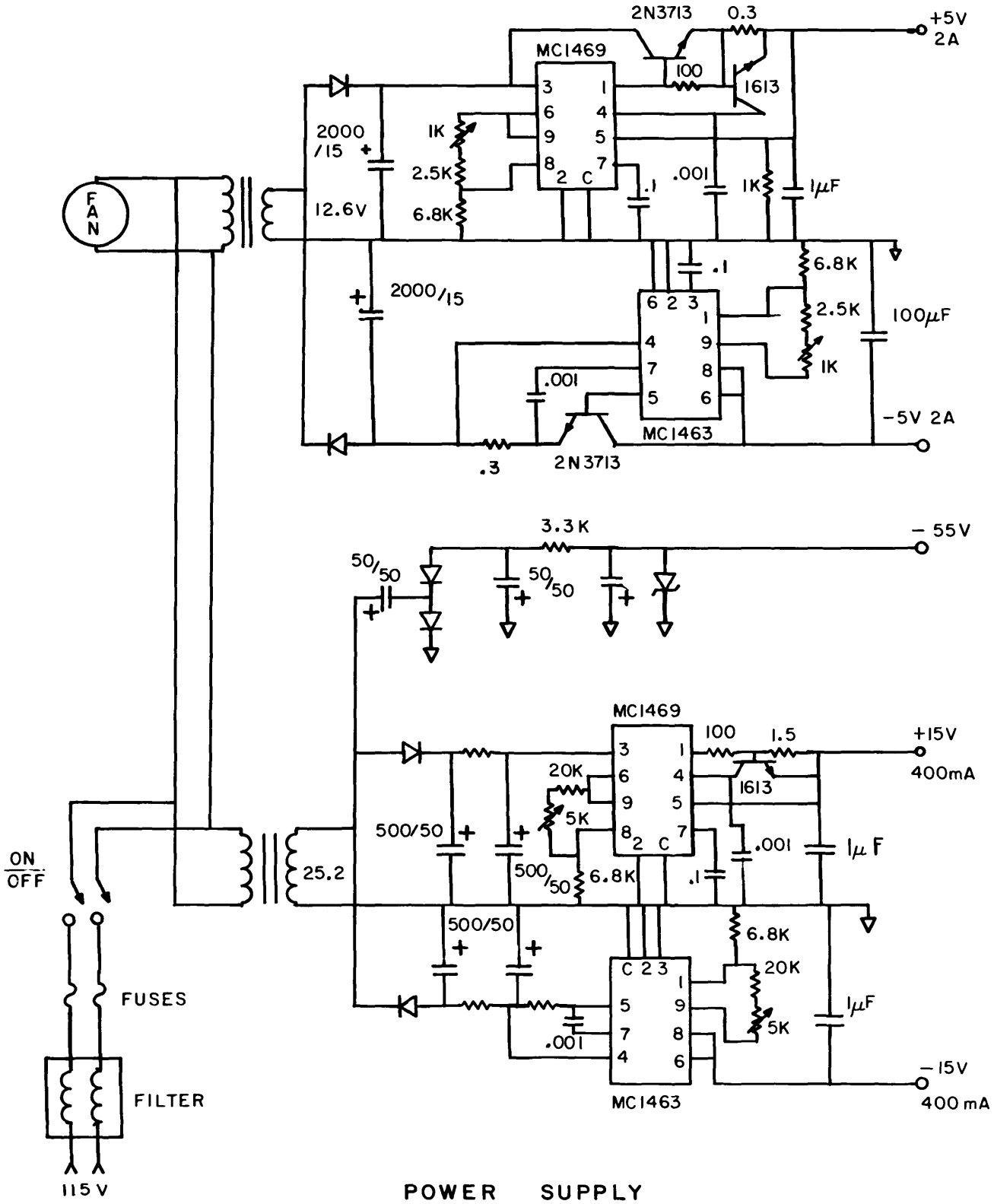
Figure 10 shows the interconnections between the circuit boards and components.

VI. Conclusion

Two units have been constructed. Figure 11 shows the RF spectrum at 300, 400 and 500 MHz of the second unit. The fundamental and 2nd harmonic breakthrough of the VCO was $\leq$ 30 dB below the carrier.

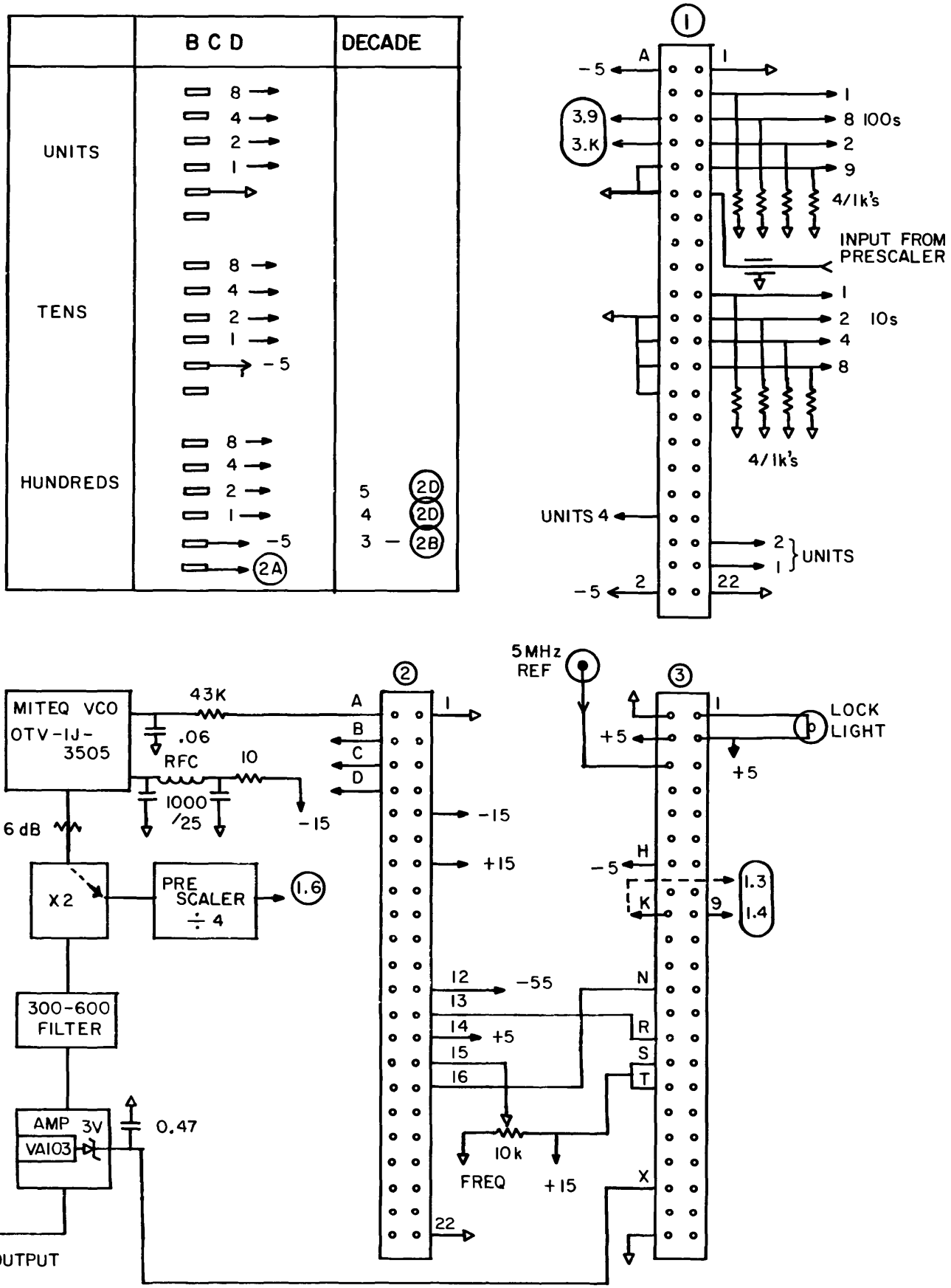
Figure 12 shows the output power variation with frequency for both units.

Figure 13 is a photo showing the completed unit.



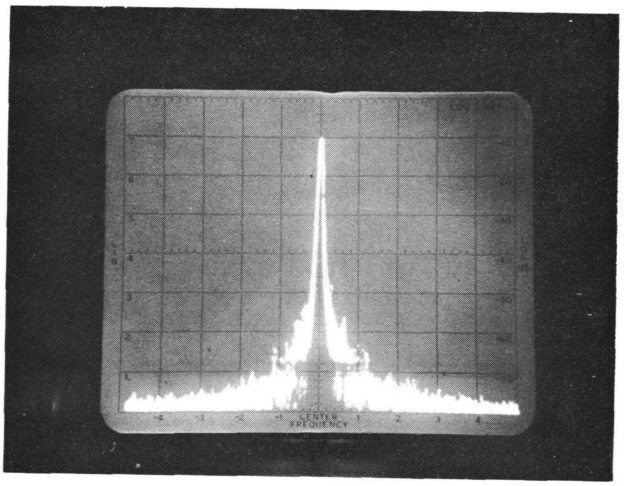
POWER SUPPLY

FIG. 9

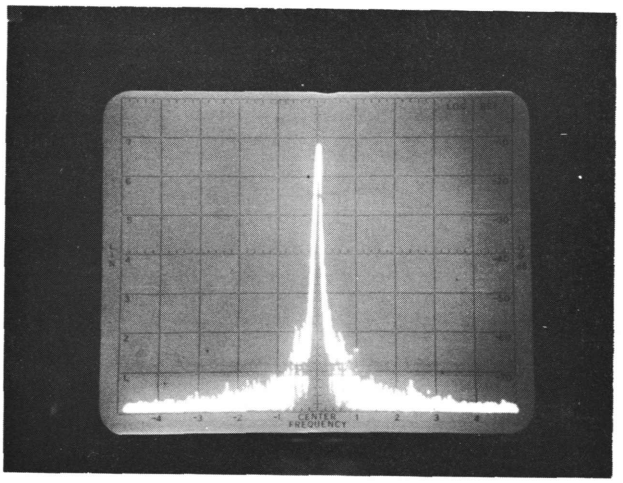


INTERCONNECTION DIAGRAM
FIG. 10

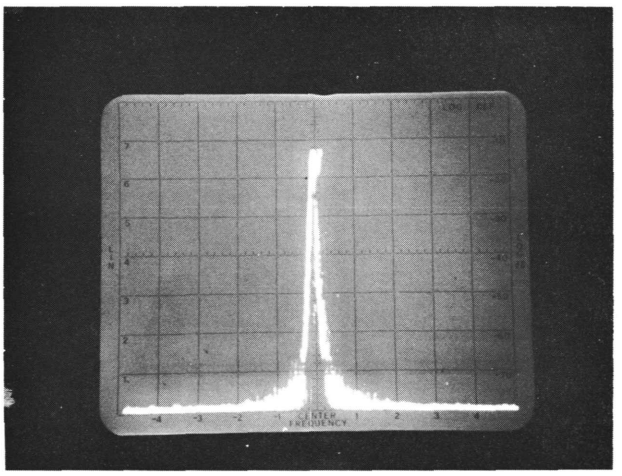
300MHz



400MHz



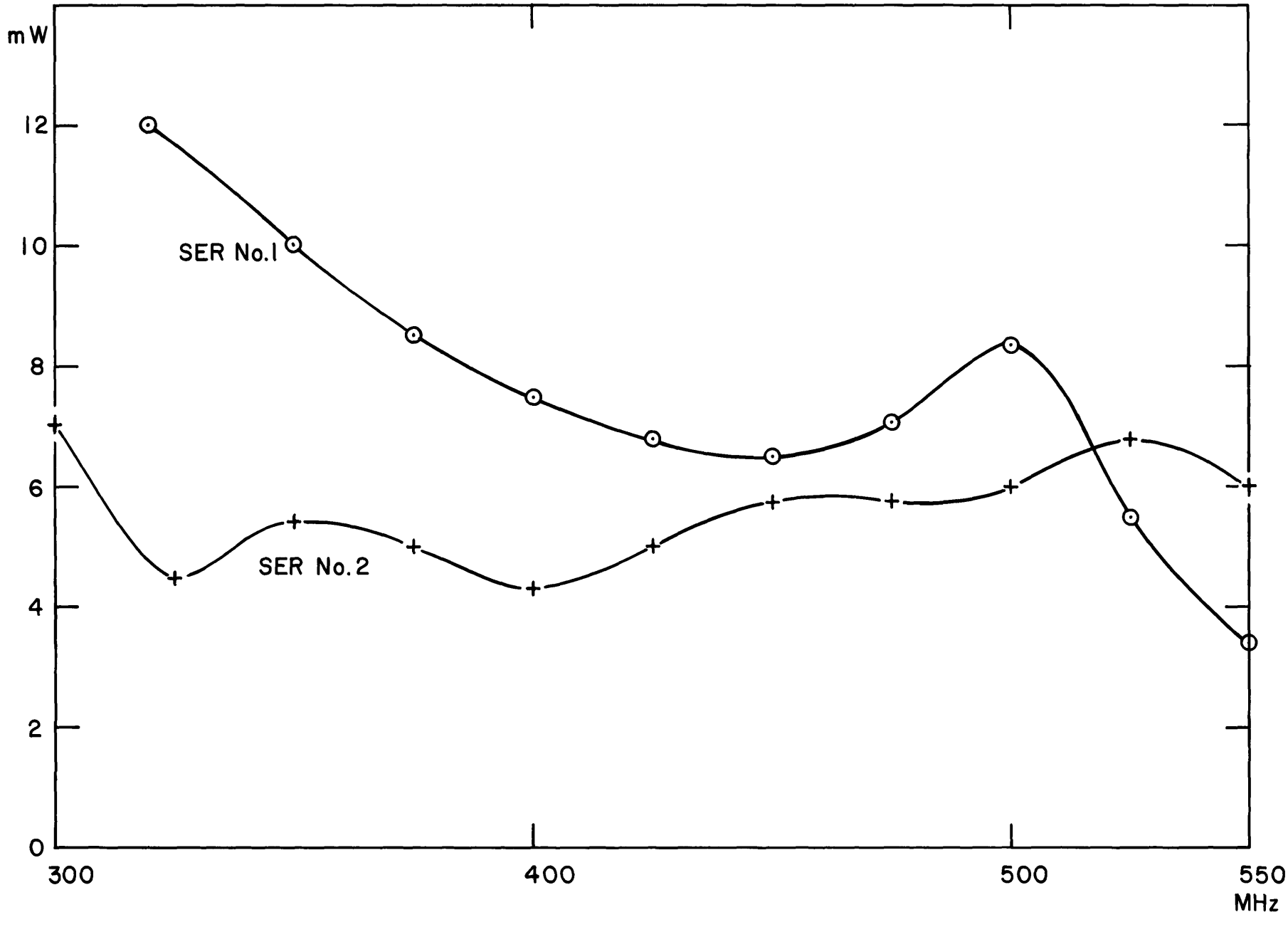
500MHz



OUTPUT SPECTRA

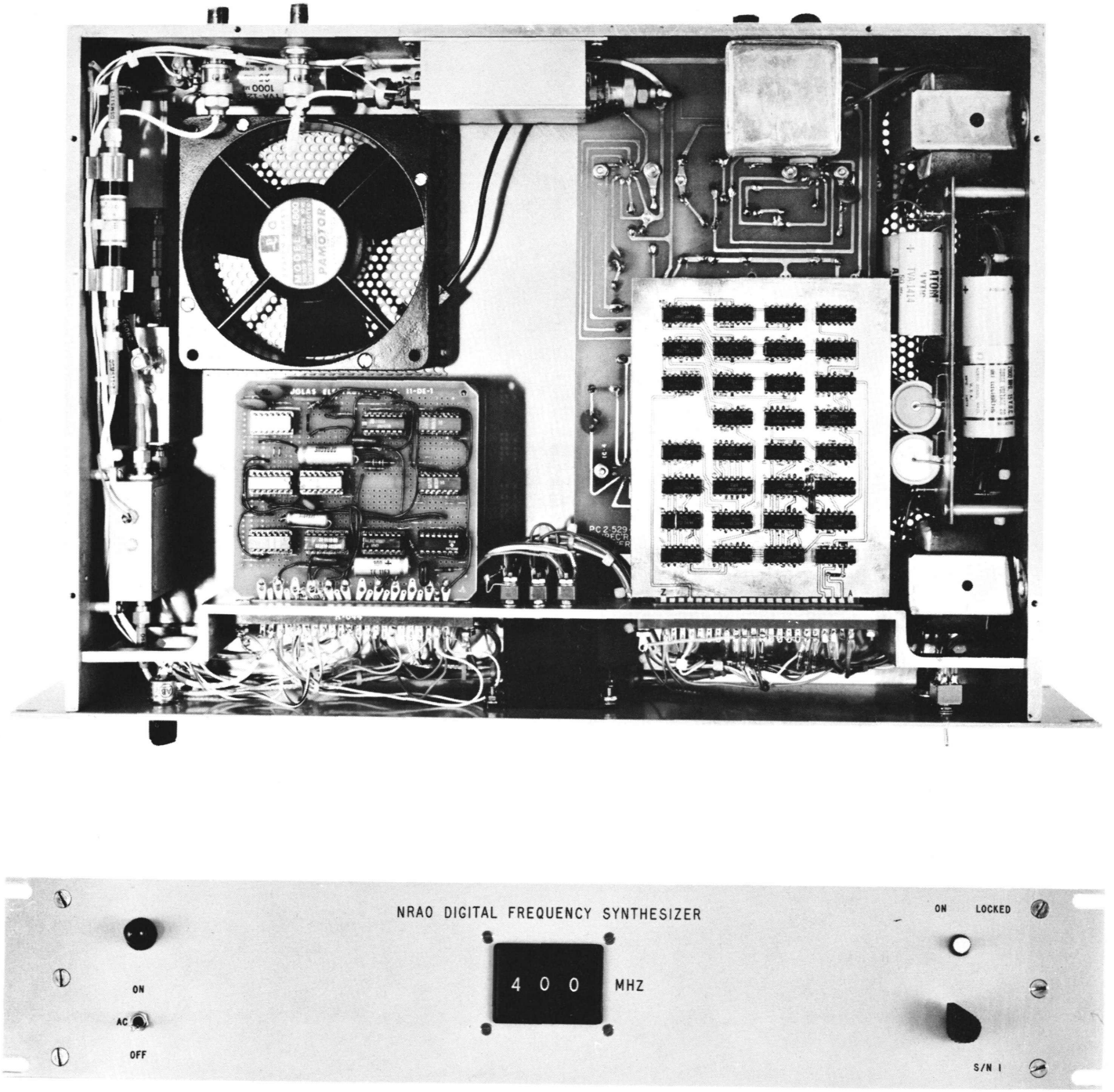
HORIZ. 50kHz/cm
VERT. 10dB/cm
FILTER 3kHz

OUTPUT SPECTRA
FIG. 11



OUTPUT POWER / FREQUENCY CURVE

FIG. 12



PHOTOGRAPH OF SYNTHESIZER
FIG. 13

APPENDIX

AN-456
Application Note

A 50 MHz PROGRAMMABLE COUNTER DESIGNED WITH MECL II INTEGRATED CIRCUITS

Prepared by
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Applications Engineering

A high speed programmable counter using the MECL II family of logic is discussed. The counter is designed to accept an input frequency up to 50 MHz and divide it by any number from 2 to 999. This number is programmed into three decades of synchronous down counters. These decades with additional decoding and control logic comprise a complete high speed divide-by-N counter system.

MOTOROLA *Semiconductor Products Inc.*

A 50 MHz PROGRAMMABLE COUNTER DESIGNED WITH MECL II INTEGRATED CIRCUITS

INTRODUCTION

This note illustrates a programmable counter designed with elements of the MECL II digital logic family. The Divide-by-N Counter will receive any input frequency up to 50 MHz and produce a selected output frequency of F_{in}/N for any N from 2 through 999. Divide-by-N counters find applications in frequency synthesizers and other forms of digital processing instruments. The outstanding feature of the counter is its high input frequency capability that in many cases eliminates the need for any prescaling of a frequency before it is applied to the ÷N counter.

The note is organized with an explanation of system operation followed by detailed design of each of the major sections of the counter.

SYSTEM OPERATION

Figure 1 is a block diagram showing the operation of the 50 MHz ÷N counter. The logic diagram of the counter is illustrated in Figure 2. The divisor N is programmed into the counter by three decades of BCD input data. This can be accomplished with decimal-to-BCD encoding thumb wheel switches or any other type of decimal-to-BCD data input methods. The binary encoded divisor is gated into the decade counters while the clock line is held high by the control section. When the high level is removed from the clock line the counter begins counting down. Near the end of the countdown, the control logic decodes the binary number six (0110) and initiates a sequence that: 1) inhibits the clock line, 2) while generating an output pulse and strobing the preset gating section to condition the decade counters for the next countdown, 3) then removes the inhibit level on the clock line so that the counting sequence can begin again.

DOWN COUNTERS DESIGNS

The counter design uses MECL II JK flip-flops, the MC1013 or the MC1027, that toggle at a typical 85 MHz and 120 MHz, respectively. Their four J and four K inputs and short propagation delays make these flip-flops highly versatile in logic designs. The pin configuration of the MC1013/MC1027 is shown in Figure 3.

Three decade counters are used in the ÷N counter design: two 9-0 BCD down-counters and a 13-4 down-counter. The two counter types are designed in a conventional manner as illustrated in Application Note AN-257 and Tables 1-5.

The use of four flip-flops in a down counter produces sixteen possible states as illustrated in Table 3. To form a

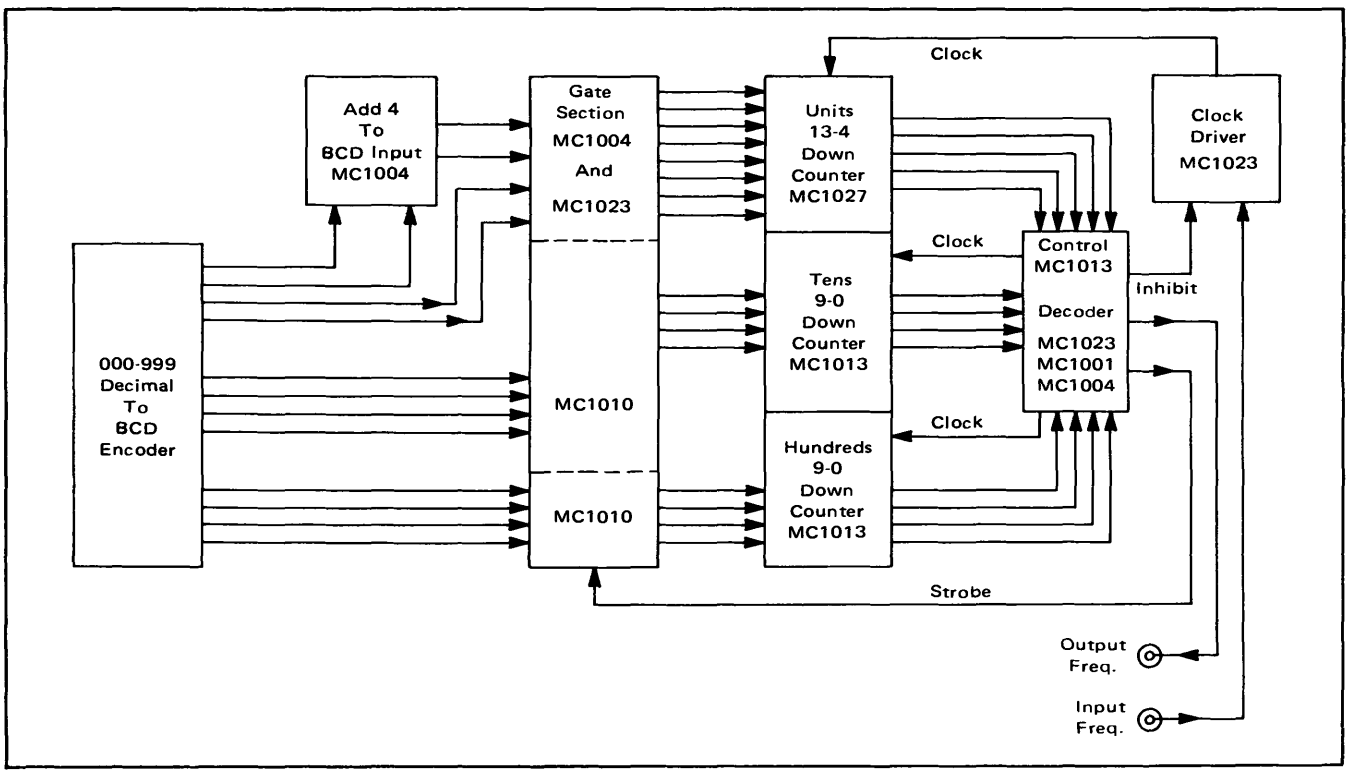

FIGURE 1 – Divide by N Counter Block Diagram

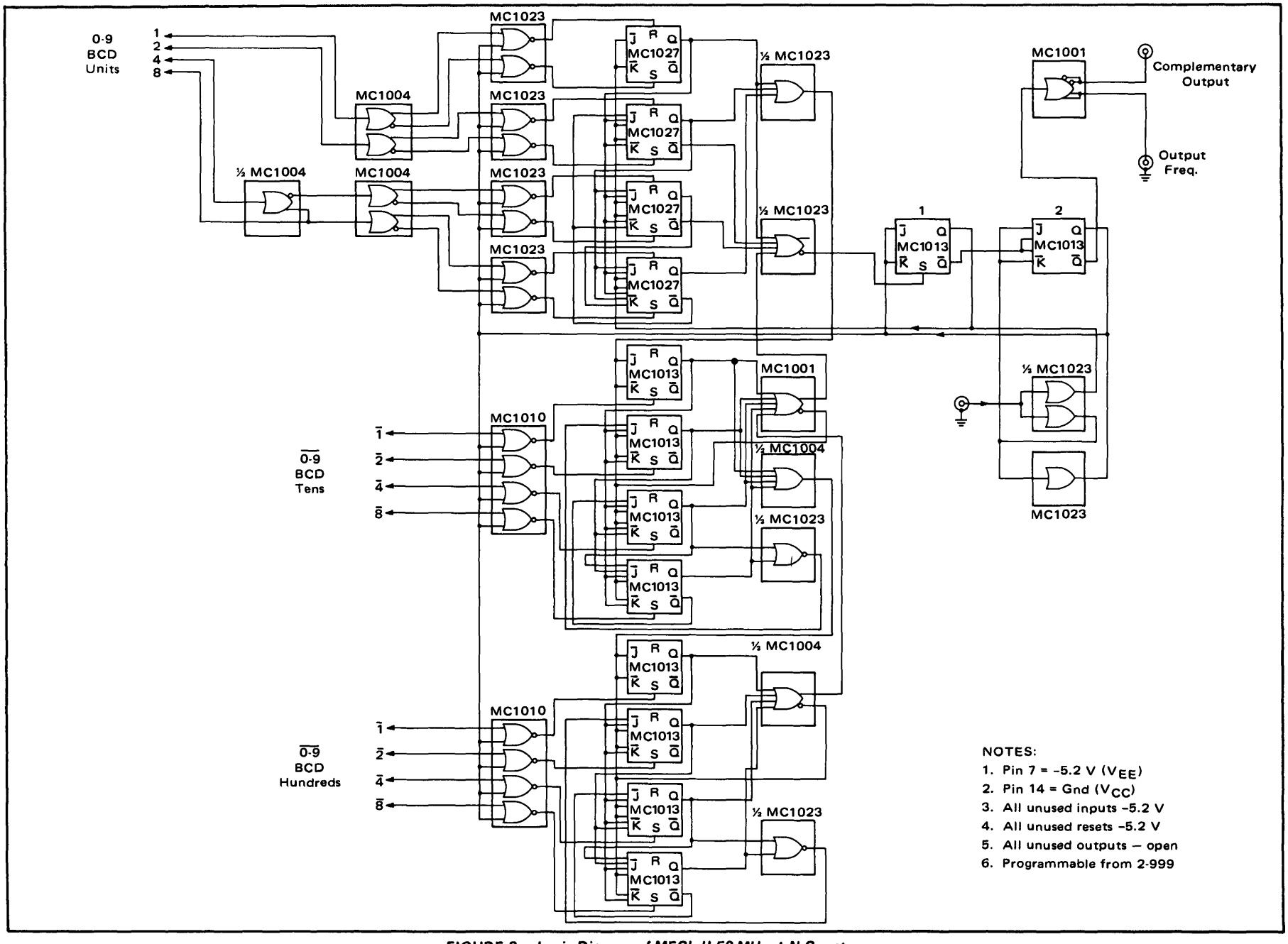

FIGURE 2 — Logic Diagram of MECL II 50 MHz ÷N Counter

counter of modulus ten, six of the possible states must be discarded. The counter must cycle through the ten desired states and, if started in an unused state, it must cycle back into one of the ten desired states to prevent lockup.

The 9-0 down counter input conditions listed in Table 4, can be transformed into a Boolean expression and simplified to the following equations by standard mapping techniques:

$$A\bar{J} = 0 \qquad A\bar{K} = 0$$
$$B\bar{J} = \bar{C}\,\bar{D} + A \qquad B\bar{K} = A$$
$$C\bar{J} = A + \bar{D} \qquad C\bar{K} = A + B$$
$$D\bar{J} = A + B + C \qquad D\bar{K} = A$$

These equations result in the 9-0 synchronous down counter shown in Figure 4. Note that an additional NOR gate is necessary to implement the $\bar{C}\,\bar{D}$ portion of the $B\bar{J}$ equation. The following worst case calculations determine the maximum operating frequency of the 9-0 down counter at 75°C.

Required down time of the clock	= 7 ns
t_{pd++} of the MC1013 flip-flop	= 9 ns
t_{pd+-} of the MC1023 gate	= 4 ns
Worst case clock period	= 20 ns
Worst case frequency of operation	= 50 MHz

The 9-0 down counter design of Figure 4 is used for both the tens and hundreds decades and may also be used in the units decade, but with some loss in maximum frequency of operation. By using the faster MC1027 flip-flops in the 9-0 down counter in place of the MC1013 flip-flops the calculated worst case frequency of operation at 75°C becomes 55 MHz.

An unusual 13-4 down counter was used in the units decade. This design yields a decade requiring no additional gating, resulting in an improvement in operating frequency. By using Table 5 and mapping techniques the following equations are obtained:

$$A\bar{J} = 0 \qquad A\bar{K} = 0$$
$$B\bar{J} = A + \bar{D} \qquad B\bar{K} = A$$
$$C\bar{J} = A + B \qquad C\bar{K} = A + \bar{D}$$
$$D\bar{J} = A + B \qquad D\bar{K} = A + B + C$$

Implementation of these input logic equations results in the down counter of Figure 5. The following worst case calculations determine the maximum operating frequency for the 13-4 down counter at 75°C

Required down time of the clock	= 7 ns
t_{pd++} of the MC1013 flip-flop	= 9 ns
Worst case clock period	= 16 ns
Worst case frequency of operation	≈ 65 MHz

TABLE 1 – Clocked $\bar{J}$-$\bar{K}$ Truth Table

Pin #	$\bar{J}$	$\bar{K}$	$\bar{C}_D$	Q^{n+1}
	•	•	••	13
	ϕ	ϕ	0	Q^n
	0	0	1	$\bar{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

All other $\bar{J}$-$\bar{K}$ inputs and the R-S inputs are at a "0" level

TABLE 2 – $\bar{J}_D$-$\bar{K}_D$ Truth Table

Pin #	$\bar{J}_D$	$\bar{K}_D$	Q^{n+1}
	•	•	13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\bar{Q}^n$

All other $\bar{J}$-$\bar{K}$ inputs and the R-S inputs are at a "0" level

NOTES:
1. *Any one of the $\bar{J}$ or $\bar{K}$ inputs may be used.
2. **Any $\bar{J}$ and $\bar{K}$ inputs may be tied together to form $\overline{C_D}$.
3. -0.75 V nominal is defined as a logic "1" or high level and -1.55 V nominal is defined as a logic "0" or low level. $\bar{J}$ and $\bar{K}$ refer to static levels while $\bar{J}_D$, $\bar{K}_D$, $\bar{C}_D$ refer to dynamic positive-going transitions for a "1".

A high level on a $\bar{J}$ input inhibits the flip-flop from being set by a $\bar{J}_D$ input. Likewise a "1" level on a $\bar{K}$ inhibits a $\bar{K}_D$ from resetting the flip-flop. The $\bar{J}$ and $\bar{K}$ inputs perform the "OR" function in preventing a $\bar{J}_D$ or $\bar{K}_D$ from setting or resetting the flip-flop.

TABLE 3 – Possible States

Binary Weight:	8	4	2	1
Decimal Number	D	C	B	A
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

TABLE 4 – 9-0 Counter Input Requirements

F/F	B		C		D	
STATE	$\bar{J}$	$\bar{K}$	$\bar{J}$	$\bar{K}$	$\bar{J}$	$\bar{K}$
9	1	+	1	+	+	1
8	0	+	0	+	+	0
7	+	1	+	1	1	+
6	+	0	+	1	1	+
5	1	+	+	1	1	+
4	0	+	+	0	1	+
3	+	1	1	+	1	+
2	+	0	1	+	1	+
1	1	+	1	+	1	+
0	1	+	1	+	0	+

$J_A = K_A = 0$
+ = Don't care condition

TABLE 5 – 13-4 Counter Input Requirements

F/F	B		C		D	
STATE	$\bar{J}$	$\bar{K}$	$\bar{J}$	$\bar{K}$	$\bar{J}$	$\bar{K}$
13	1	+	+	1	+	1
12	0	+	+	0	+	1
11	+	1	1	+	+	1
10	+	0	1	+	+	1
9	1	+	1	+	+	1
8	0	+	0	+	+	0
7	+	1	+	1	1	+
6	+	0	+	1	1	+
5	1	+	+	1	1	+
4	1	+	+	1	0	+

$J_A = K_A = 0$
+ = Don't care condition

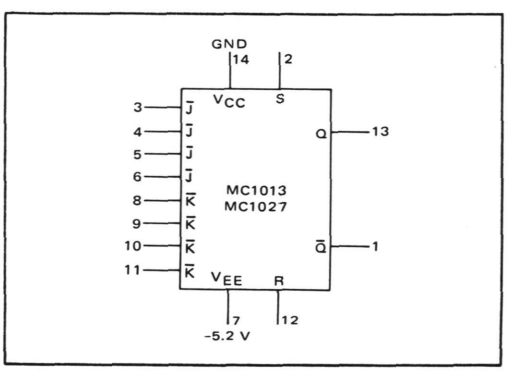

FIGURE 3 – Pin Configuration of MC1013/MC1027

If the faster MC1027 flip-flops are used in place of the MC1013 flip-flops the calculated worst case frequency of operation at 75°C is 72 MHz. All worst case frequencies are for the decade counters only, and do not include any output decoding delays. With good layout techniques the total ÷ N counter system will operate at 50 MHz over a temperature range of 0°C to +75°C.

PRESET GATING SECTION

The function of the gating section is to preset the divisor N into the set and reset terminals of the counter flip-flops when strobed by the decoder control section. The use of the 13-4 counter in the units decade requires that both the set and reset inputs of the four flip-flops be capable of being updated. There are two reasons for this requirement. First, the counter's lowest binary count is 0100 (binary 4) and not 0000 (binary 0) precluding the simple setting of the four units flip-flops as is the case in the tens and hundreds decades. The second reason is the inhibiting of the clock at count 0110 (binary 6) by the control section. This results in the toggling of Flip-Flop A (Figure 5) to a "1" level and Flip-Flop B to a "0" level. Therefore, it may be necessary to reset flip-flops A or C for certain divisors. Only the set terminals in the tens and hundreds decades need be gated at the end of a count cycle since, at strobe time, these decades have already been counted down to zero. The unused reset terminals are returned to V_{EE} (-5.2 V) on these two counters. The input gating section is illustrated in Figure 6. Note that the 9-0 down counter input gates require the 1-2-4-8 complements on their inputs.

INPUT LINE CODE TRANSLATOR FOR 13-4 COUNTER

The use of a 4-13 decade counter circuit to improve operating frequency requires that the units place of the

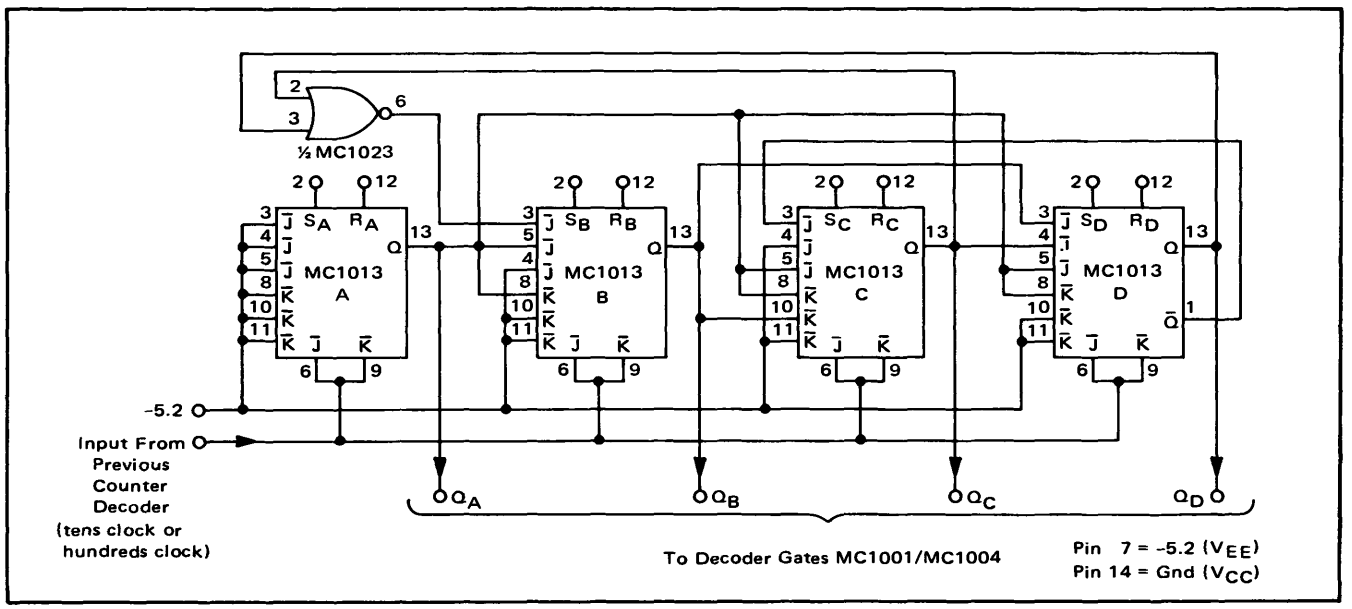

FIGURE 4 — 9-0 BCD Down Counter Tens or Hundreds Decades

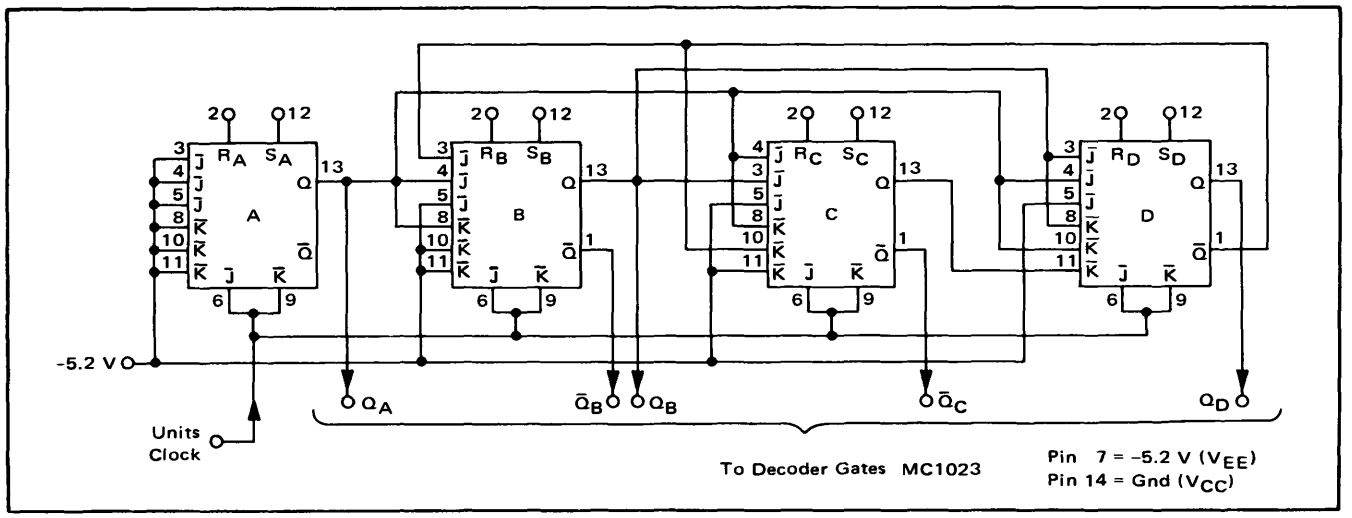

FIGURE 5 — 13-4 Down Counter Units Decade 4-MC1013 or 4-MC1027

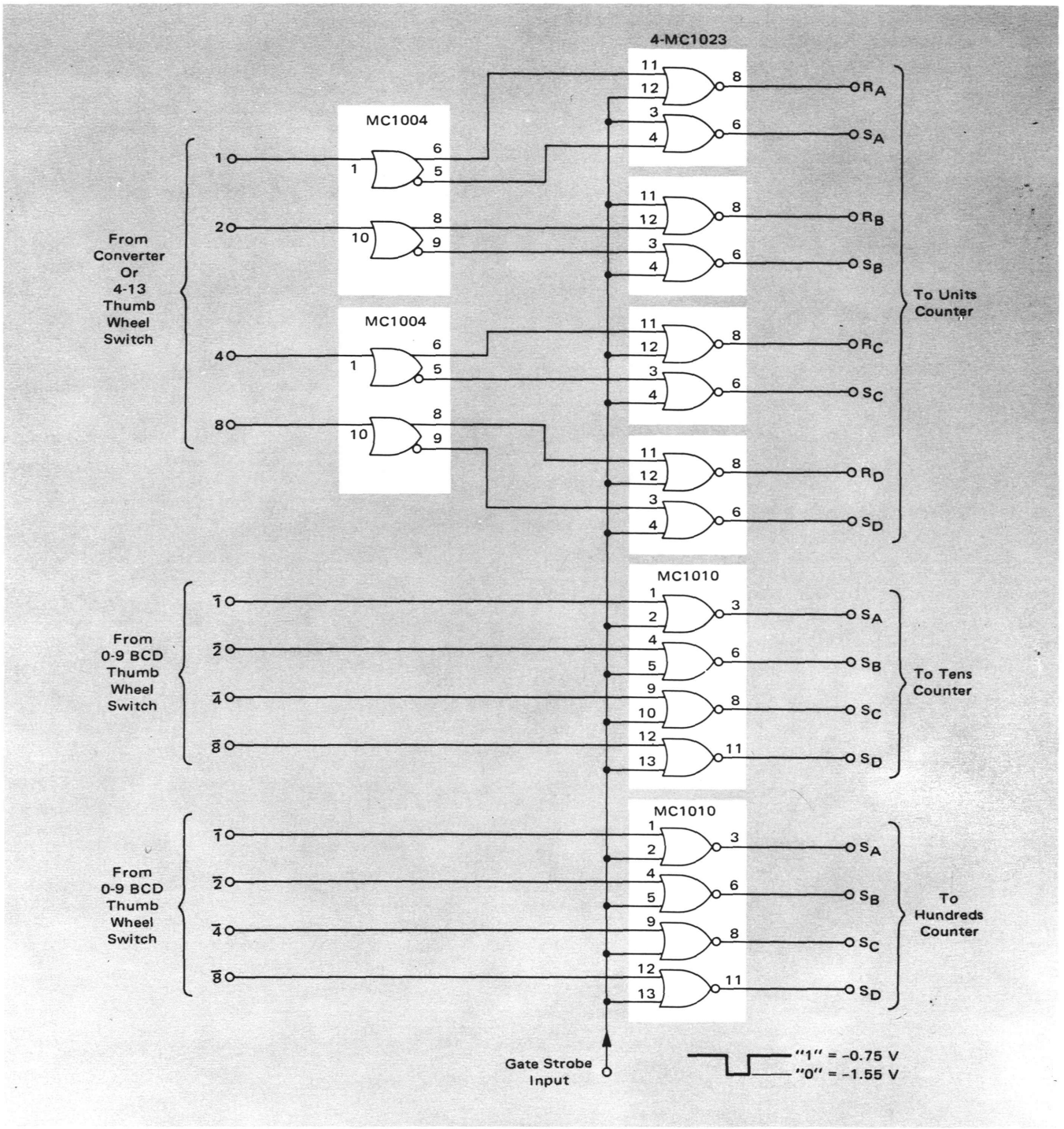

FIGURE 6 — Gating Section

TRUTH TABLE

	D	C	B	A		D′	C′	B′	A′
0	0	0	0	0	4	0	1	0	0
1	0	0	0	1	5	0	1	0	1
2	0	0	1	0	6	0	1	1	0
3	0	0	1	1	7	0	1	1	1
4	0	1	0	0	8	1	0	0	0
5	0	1	0	1	9	1	0	0	1
6	0	1	1	0	10	1	0	1	0
7	0	1	1	1	11	1	0	1	1
8	1	0	0	0	12	1	1	0	0
9	1	0	0	1	13	1	1	0	1

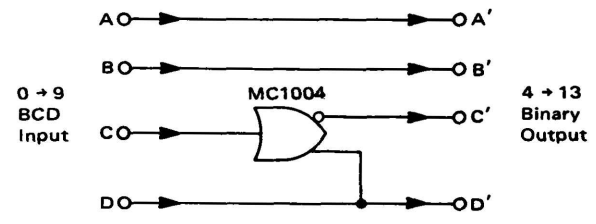

FIGURE 7 — 0-9 to 4-13 Converter

divisor, encoded in a 0-9 BCD code, be converted to a 4-13 code. This is readily done by the use of an MC1004 OR/NOR gate. This circuit, illustrated in Figure 7, could be eliminated by having the 4-13 binary code externally available, as from a special thumb-wheel switch. In addition, Figure 8 illustrates a decimal-to-BCD encoder using three 10-position switches and supplementary gating that could be used to provide the three required decades of BCD. In this encoder both the function and its complement are available.

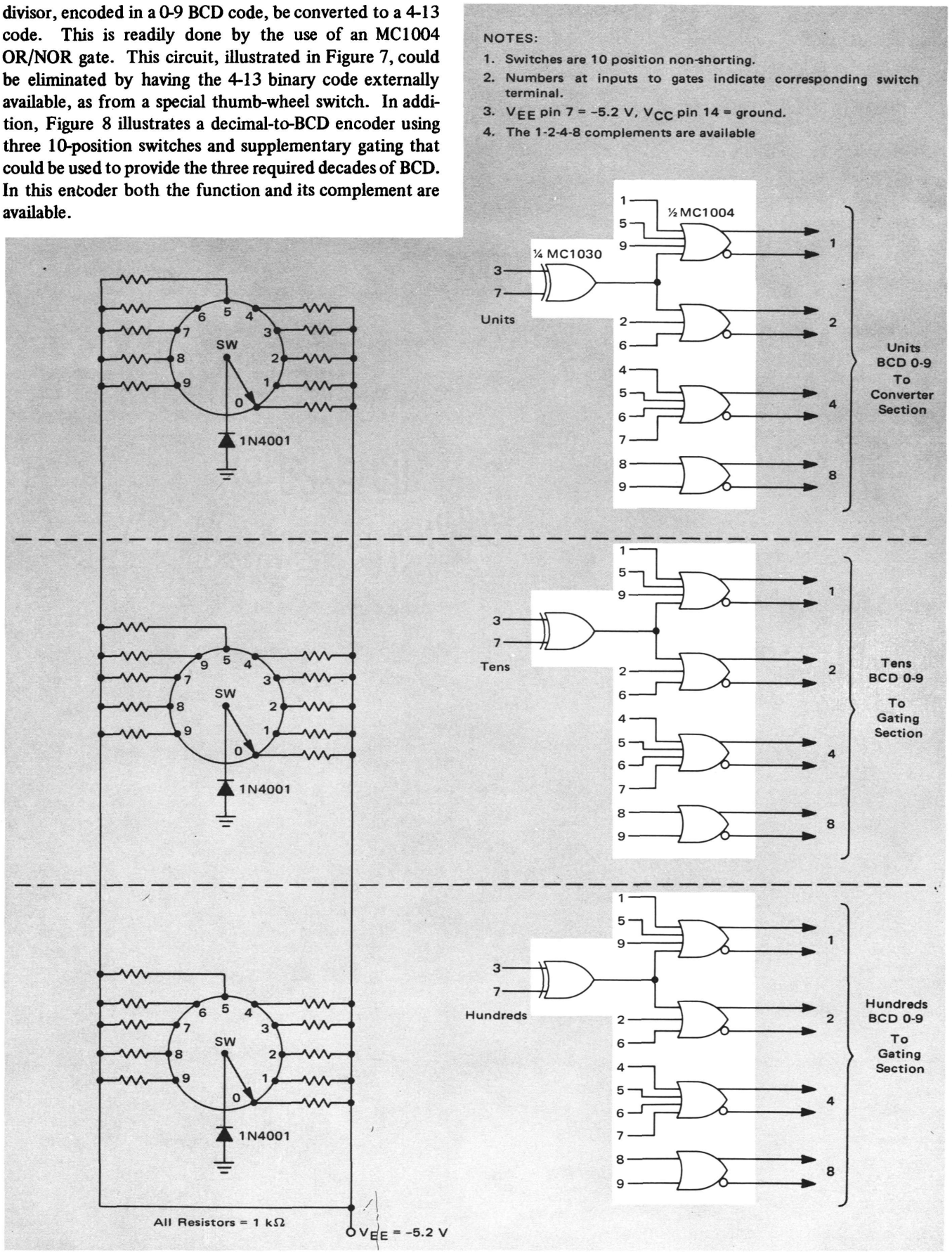

FIGURE 8 – 3 Decade Decimal to BCD Encoder

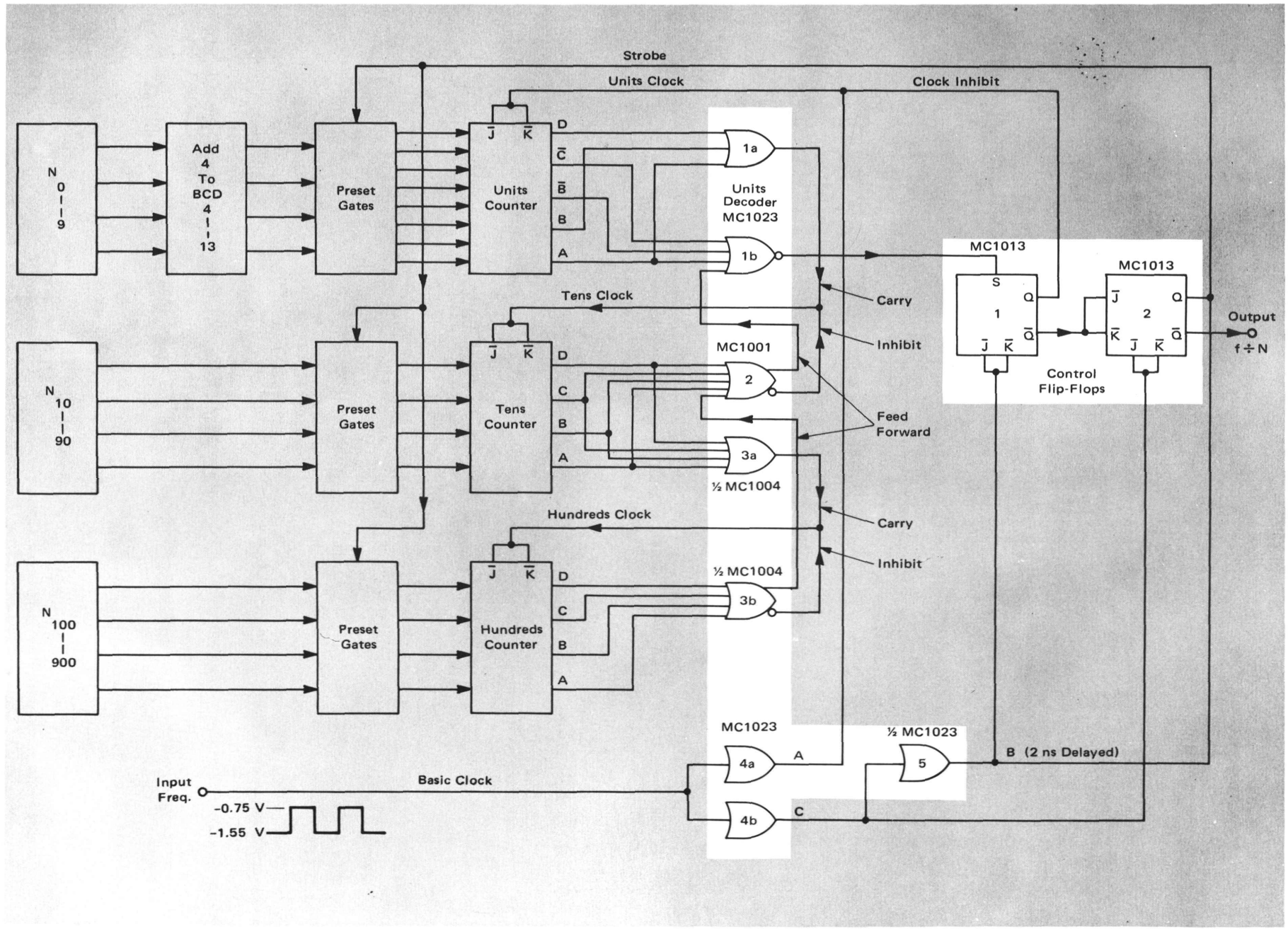

FIGURE 9 – Control Section

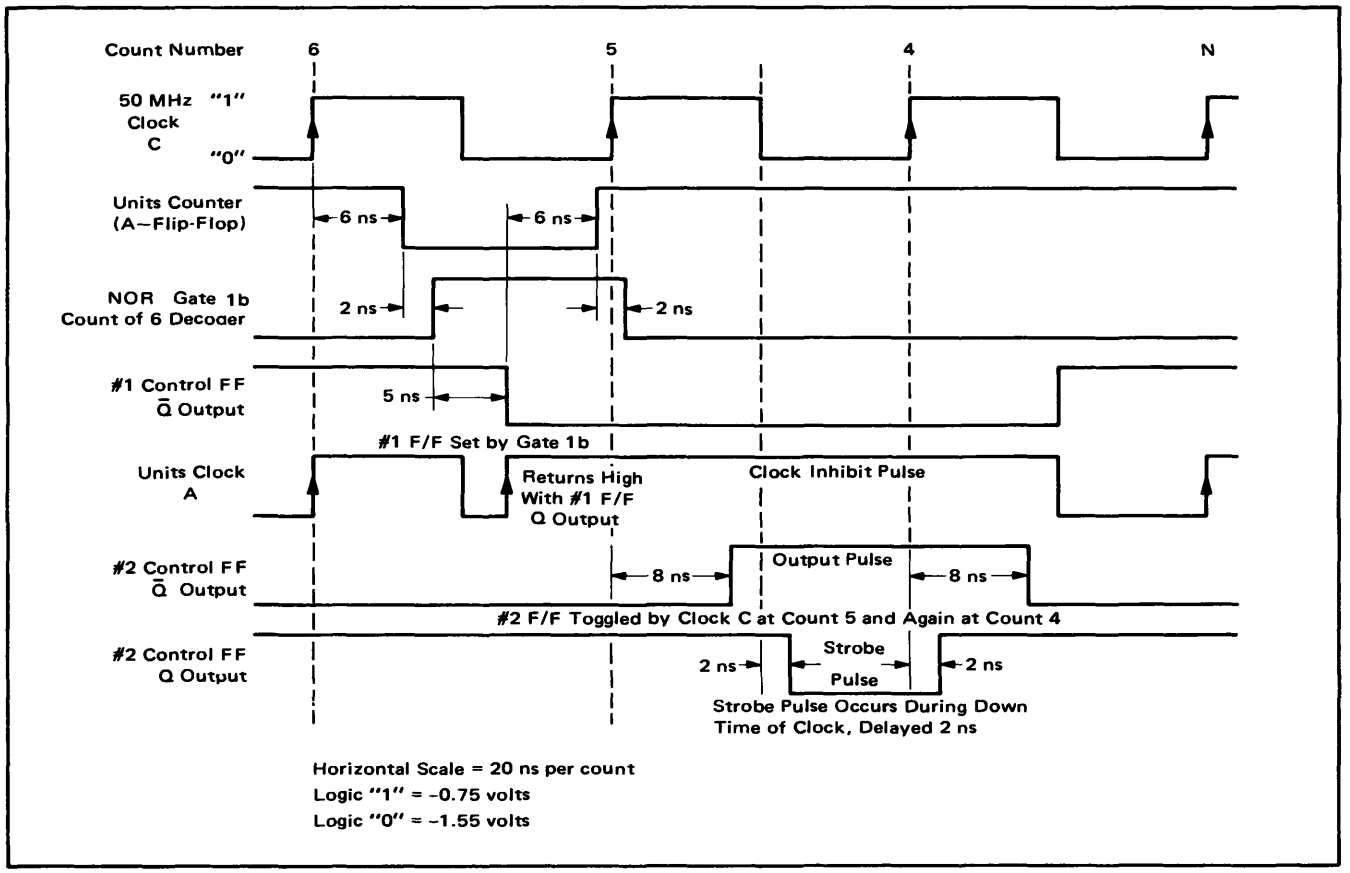

FIGURE 10 – Control Timing Diagram

CLOCK DRIVER AND DECODER

The input frequency is fed into an MC1023 clock driver, one half of which drives the four flip-flops in the units decade. The other half drives control Flip-Flop #2 and gate #5. (see Figure 9). Another MC1023 (gates 1a and 1b in Figure 9) is used in the units decade to decode a 0100 (binary 4) for the carry output, which drives the next decade counter, and a 0110 (binary 6) for the overall output decoding sequence. The sequence of events can be followed more easily by referring to Figures 9 and 10. This timing diagram represents the last portion of the decoding sequence for the units decade after previous decades have counted down to zero.

As the ÷N system counts down from its preset number (the divisor, N), the units decade repeatedly cycles through its 13 to 4 sequence. When the hundreds and tens decade have counted down to zero, a feed-forward signal is produced by an MC1001 six input OR/NOR gate connected to the tens decade as a four place binary zero (0000) decoder. This low feed-forward signal enables the decoder in the units decade (1b in Figure 9) to detect the next count of six.

Six nanoseconds after the count of six reaches the units decade clock input, the Q output of Flip-Flop A goes low. Then, two nanoseconds later, (typical MC1023 delay) the NOR output of the count of six decoder goes high. This high level sets the Q output of control Flip-Flop 1 to a logical "1" level and the $\bar{Q}$ output to a logical "0" level, after a five nanosecond delay. (Typical delay from set/reset inputs to Q/$\bar{Q}$ outputs).

Prior to this time, the Q output of Flip-Flop 1, which is wire ORed with clock A, remained at a low level and did not affect the toggling of the units counter by the positive transitions of the clock. (In a MECL system if any of the input paths to a wired OR connection are at a high level, the OR connection is maintained high). When the Q output of control Flip-Flop 1 is set to a "1" by the NOR output of the count of six decoder, the OR connection changes from low to high. The counter is thus inhibited while the strobe pulse presets the counters. Although the units counter is inhibited, the final events are sequenced by the control section so that no count is lost.

The logical "0" level on the $\bar{Q}$ output of control Flip-Flop 1 enables control Flip-Flop 2 to toggle on the next positive transition of clock C (count 5), after an eight nanosecond delay. At this time the Q output of Flip-Flop 2 goes low and its $\bar{Q}$ output goes high. The $\bar{Q}$ transition is the start of the counter output pulse.

Since the Q output is wire ORed with clock B, (the MC1023 clock driver, gate 5 in Figure 9) which is still in the positive portion of count 5, the OR connection is held high until the negative transition. The fall of clock B then serves as the leading edge of the strobe pulse. The strobe

pulse is terminated ten nanoseconds later at the positive transition of clock B entering count 4.

The count 4 positive transition on clock C will toggle control Flip-Flop 2, after an eight nanosecond delay. The change of state of the $\bar{Q}$ output terminates the 20 nanosecond output pulse. The same count 4 positive transition, that occurs two nanoseconds later on clock B than clock C, also toggles control Flip-Flop 1, after an eight nanosecond delay, to end the control sequence.

Expansion of the ÷ N counter to accept larger divisors can be accomplished in the following manner. By duplicating the decoding design employed in the tens decade, the hundreds decade can accept a feed forward decoding pulse and also generate a carry pulse. This is the only modification necessary for the addition of more BCD decade counters.

SUMMARY

This note has illustrated the use of emitter coupled logic as applied to a divide-by-N counter system. The use of this logic family provides a considerably higher operating frequency than is obtainable in a ÷ N counter system using a saturated logic family. The worst case data given in this note are conservative and, therefore, intended for system design. Due to the high frequencies of operation, performance depends heavily upon system layout and the counter will work best when used with two-sided printed circuit cards where lead lengths have been minimized. Since the introduction of higher speed MECL III, the ÷ N counter can be fabricated to operate in the 100 MHz + area.

ACKNOWLEDGMENT

The author wishes to thank Al Collum for the comprehensive data and laboratory checkout that was done in support of this note. He also wishes to convey acknowledgment to Chuck Byers for his work on the 13-4 counter.

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