NATIONAL RADIO ASTRONOMY OBSERVATORY

ELECTRONICS DIVISION TECHNICAL NOTE NO. 105

TITLE: DIGITAL CONTINUUM RECEIVER HARDWARE MODIFICATIONS

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DATE: January 6, 1982

This technical note is intended to describe the changes to the digital continuum receiver hardware. The continuum receiver was designed by J. Ray Hallman and is described in EDIR No. 188.

After some use of the receiver it became apparent that some changes could improve its performance. The two main changes were:

1. Make sure the DCR always starts observing some fixed time after the host computer starts the observing.
2. Interrupt the host computer at the center of an integration period.

The first change was a major change in the hardware and software. Before the change the calculator program would check one bit in a data word to see if the host computer wanted to start a new scan. This was checked during the normal program flow, which could cause the receiver to delay as much as one integration period before starting a new scan. This delay varied more than was desired for observing.

The program had to be changed so that it could determine in a reasonable amount of time when to start a new scan. This was accomplished through the addition of two status bits. (See Figure 1.) These two status bits enabled

the calculator to wait for a start scan condition, after the scan has stopped. The disadvantage of this approach is that a display of receiver parameters is not displayed between scans. In order that the calculator could guarantee a stop scan condition at start up, a new command was added. This command, WTC 15, 32. forces a stop scan. When the receiver is in a stop scan condition it spends all of its time waiting for a start scan. When the scan is started, all of the time base counters (EDIR 188, page 49) are reset (Figure 2) and the calculator is now waiting on data ready or another stop scan. Being able to wait on a start scan condition reduced the time from the host computer's request to a start scan to the cycle time of the calculator.

The addition of the WTC 15, 32 command caused another problem. This problem was corrected by the logic change in Figure 4. Before this cahnge it was not possible to turn the cal off, due to the fact that when the control word was set to turn the cal off it also stopped the scan. The solution was to move the cal control to a write binary bit (1024) to control the cal.

To generate a center of integration interrupt was rather an involved hardware addition. This was complicated by the fact that the host computer (300-ft DDP 116) only had one interrupt line that had to be shared as a data and center of integration interrupt. The approach used was to provide a flag $\overline{CI}$ (reference Figure 5) to tell the host computer that it was a center of integration interrupt.

This flag caused a problem in that if a data interrupt should happen to occur while the flag was still set the host computer would interpret that interrupt as another center of integration interrupt. The logic in Figure 3 takes care of this problem by forcing the data interrupt to occur after the $\overline{CI}$ flag is gone.

The logic of Figure 5 was implemented to generate a center of integration interrupt. The basic idea of the logic was to provide a duplicate phase counter (EDIR 188, page 49) and the samples/integration counter (page 55) and run these

counters at twice the frequency as in the normal counters. When these counters count down to zero it would be half way through the integration period and would generate an interrupt.

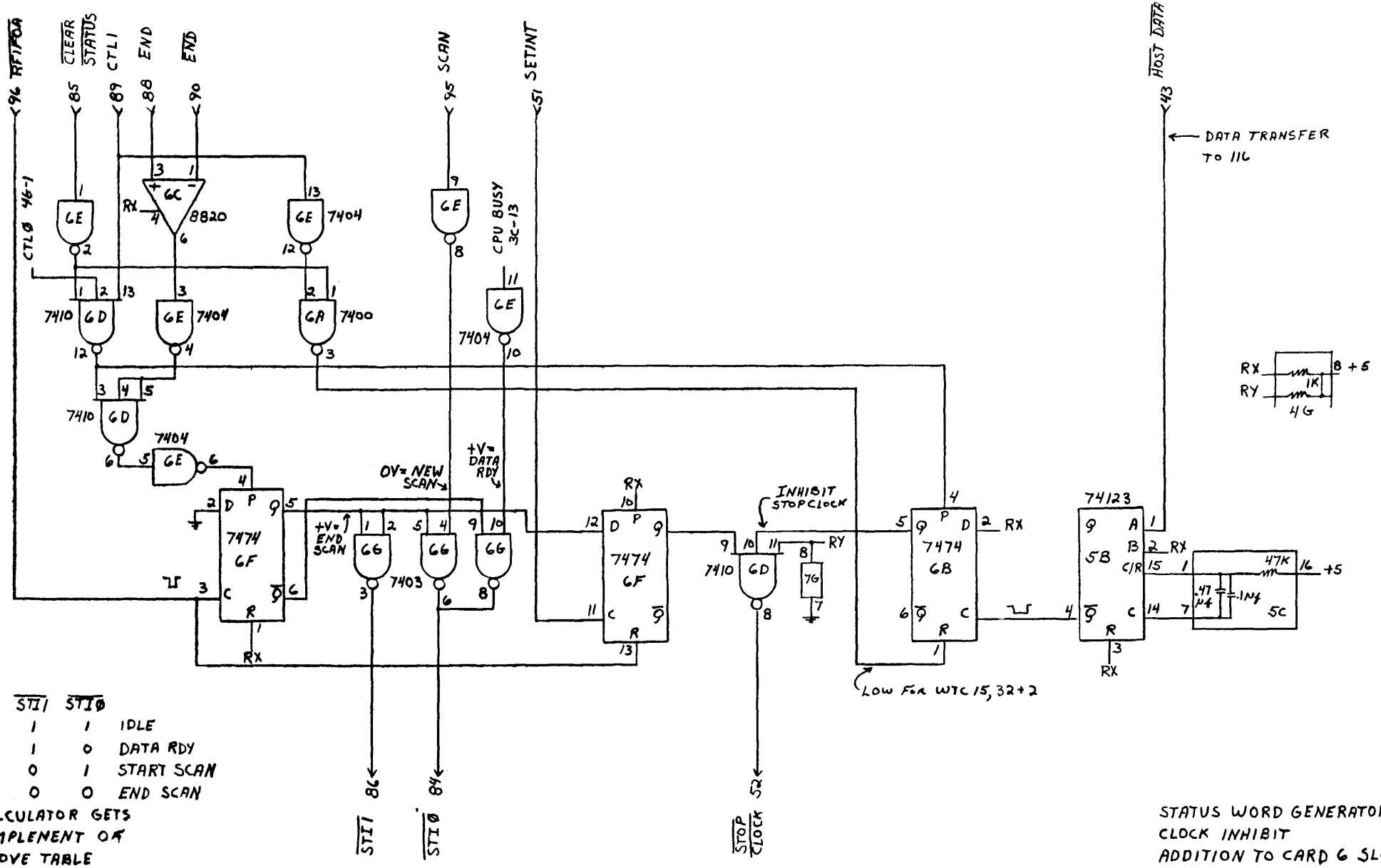
The host computer interrupt structure was changed a great deal as far as the receiver hardware was concerned. First the data interrupt occurs only when data is ready and the new center of integraiton interrupt has passed. In addition, an extra interrupt (required by 300-ft DDP 116 program) is generated at the end of the scan.

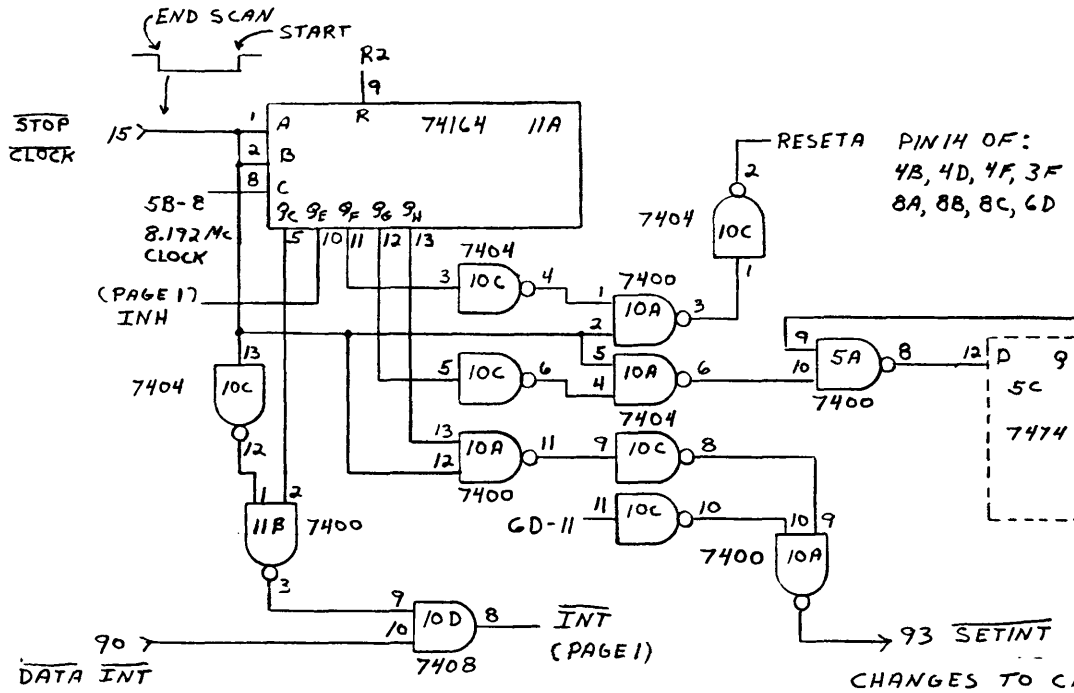
The last observing run with this receiver proved to be favorable and no more hardware changes are anticipated.

There are a few more things that would be nice to have on the receiver, such as a phase period increment of less than one millisecond and more control bits for front-end control. These changes would not be practical with the present hardware. To implement these changes would require a redesign of the receiver. I think some of the wire wrap cards could be used as is and the rest redesigned. If we did a redesign, some of the changes in this note would also be changed.

Attachments:
Figures 1-5

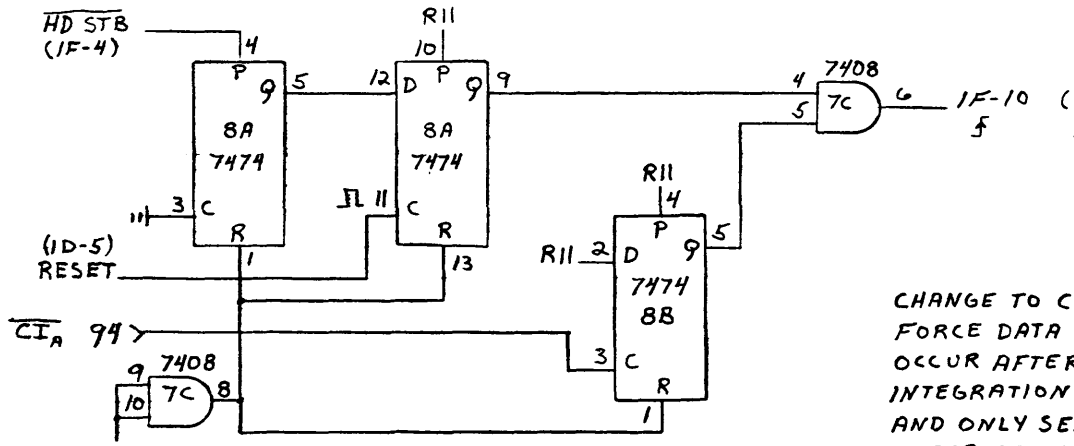
Distribution:
GB Library
CV Library
VLA Library
TUC Downtown File
Mountain File
M. Balister
C. Burgess
H. Hvatum
P. Napier
J. Payne
S. Weinreb
R. Lacasse
R. Weimer


96 RFTPOA
CTLØ 46-1
85 CLEAR STATUS
89 CTL1
88 END
90 END
95 SCAN
51 SETINT
43 HOST DATA
DATA TRANSFER TO 11C
CPU BUSY 3C-13
RX
8820
7404
7410
7400
7474 6F
7403
OV= NEW SCAN
+V= DATA RDY
+V= END SCAN
INHIBIT STOPCLOCK
RY
7474 6B
74123 5B
5C
RX
RY
1K
4G
8 +5
47K
+5
.47 µf
.1Mf
LOW FOR WTC 15, 32+2
STI1 86
STIØ 84
STOP CLOCK 52
STI1 STIØ
1 1 IDLE
1 0 DATA RDY
0 1 START SCAN
0 0 END SCAN
CALCULATOR GETS COMPLEMENT OF ABOVE TABLE
STATUS WORD GENERATOR CLOCK INHIBIT ADDITION TO CARD 6 SLOT 11
(REF PAGE 59)
FIG 1



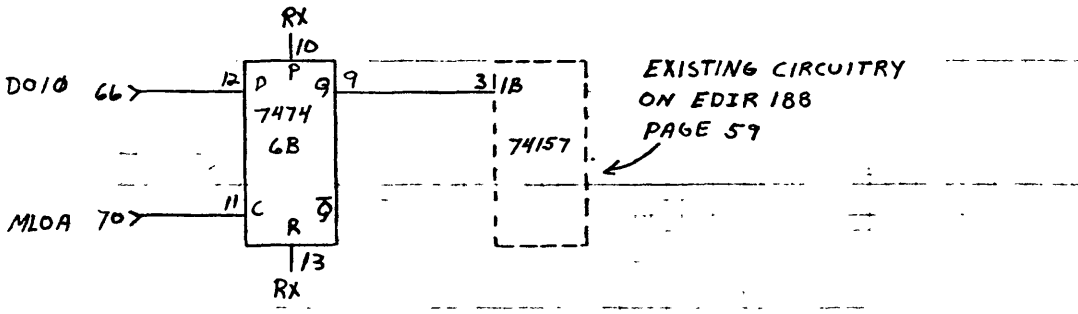
CHANGES TO CARD 1 SLOT 3 TO: RESET TIME BASE COUNTERS AT START OF SCAN AND GENERATE AN INTERRUPT AT END OF SCAN PAGE 2 OF 2

FIG 2



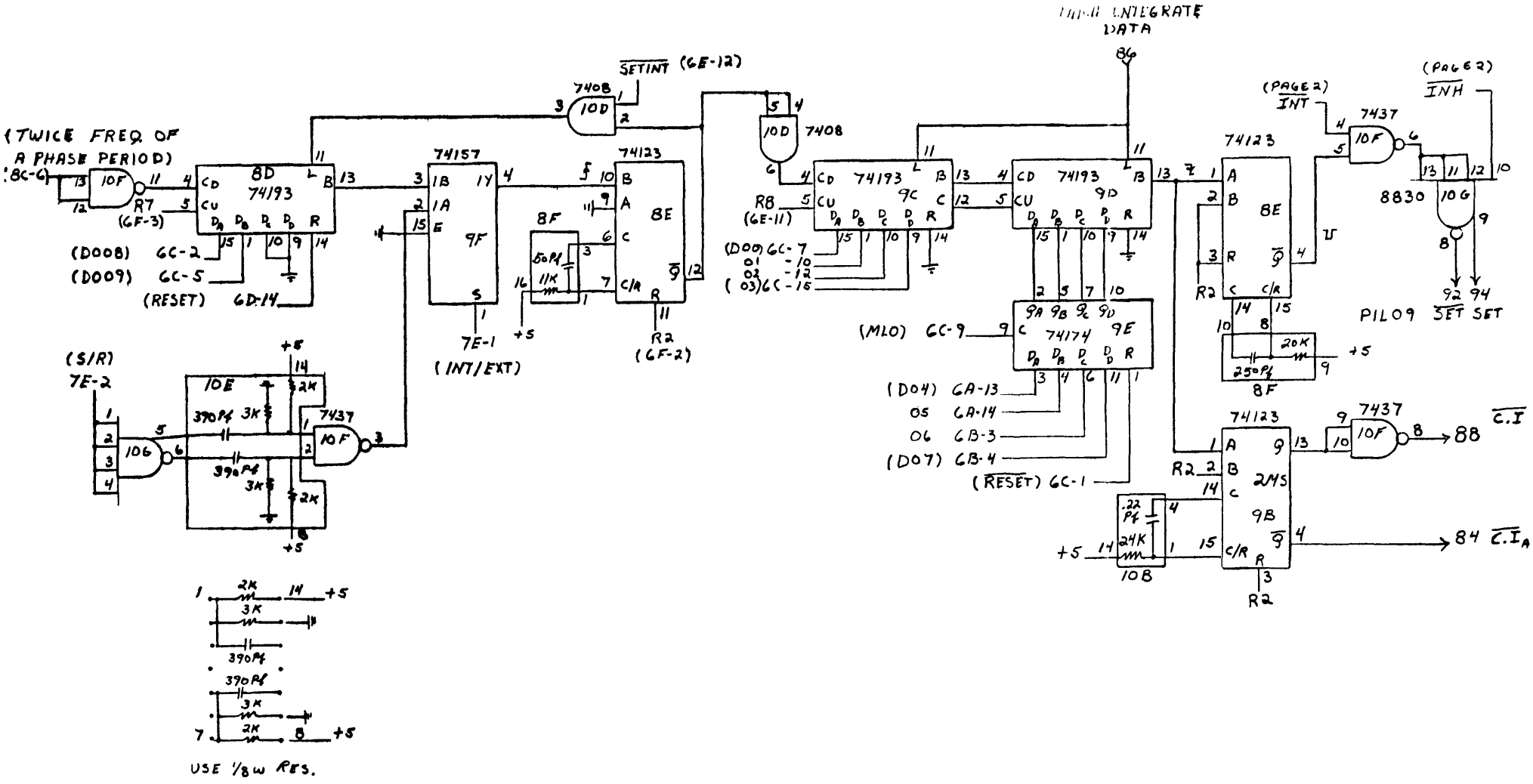
CHANGE TO CARD 4 SLOT 9 TO FORCE DATA INTERRUPT TO OCCUR AFTER CENTER OF INTEGRATION INTERRUPT AND ONLY SEND DATA INTERRUPT WHEN DATA IS READY. (REF. EDIR 188 PAGE 55)

FIG. 3



CHANGE TO CARD 6 SLOT 11 TO BE ABLE TO CONTROL CAL WITH "WTB 15, 1024" INSTEAD OF "WTC 15, 1"

FIG 4



ADDITION TO CARD 1 (SLOT 3)
TO GENERATE CENTER OF
INTEGRATION INTERRUPT
PAGE 1 OF 2
(REF. PAGE 49)

FIG 5