NATIONAL RADIO ASTRONOMY OBSERVATORY
Charlottesville, Virginia

ELECTRONICS DIVISION TECHNICAL NOTE NO. 153

Title: **RECEIVER MONITOR CONTROL**

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Date: April 24, 1989

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RECEIVER MONITOR CONTROL

Ronald B. Weimer

Introduction

Jim Coe is developing a new set of front-ends for use on the interferometer system. The first one was installed on the 85-3 for use as a VLBI receiver. An AST 286 PC was purchased to control the telescope observing and the receiver system. We decided to use the VLBA monitor and control (M/C) card for input-output in the receiver. This report describes the electronics necessary to implement this system. Two small Shalloway cards and one M/C card were placed in a RFI-tight box. Input and output lines were filtered using filter connectors supplied by Coe. The link from the PC uses a fiber optic cable (described in another report) instead of the balanced pairs used in the VLBA stations.

Electronics

Analog Card.

Since we wanted to monitor around 30 DC voltage points we needed to multiplex the analog signals before the M/C card. The individual voltages were routed through a dip carrier that provided voltage division, if necessary, and clamping action to ± 10 volts. Clamping was necessary to prevent crosstalk in the multiplexers. Figure 1 is a schematic for the analog card. Figure 2 shows some of the discrete circuitry on the analog card and lists the components on the various divider/clipper carriers. Figures 3 and 4 are the layout of the analog card. A data sheet for the mux is included. Address and control signals are generated on the digital card.

Digital Card.

Figures 5, 6, 7 and 8 are the schematic for the digital card. Figure 5 contains the M/C ID circuit (5A, 4A) and the Relative address decoding (3A, 3C, 4B). Figure 6 contains further address decoding (3B) and Tri-State digital input multiplexing (2A, 2B). Figure 7 contains more address decoding (1C), output data latch (1B) and a data buffer (1A). A power up circuit (3C) opens the data buffer outputs until the first data is strobed into the latch. This sets the receiver to a nominal operating condition until the PC starts operating. Figure 8 shows the optical interface electronics. This is also described in the fiber optic cable note (EDTN #152) Chip 4D output goes to the M/C card and chip 5F input is the return data out of the M/C card. A data sheet on the optical multiplexer CAF-H2B is included. Figures 9 and 10 are the layout for the digital card. A wire list for the chassis is included.

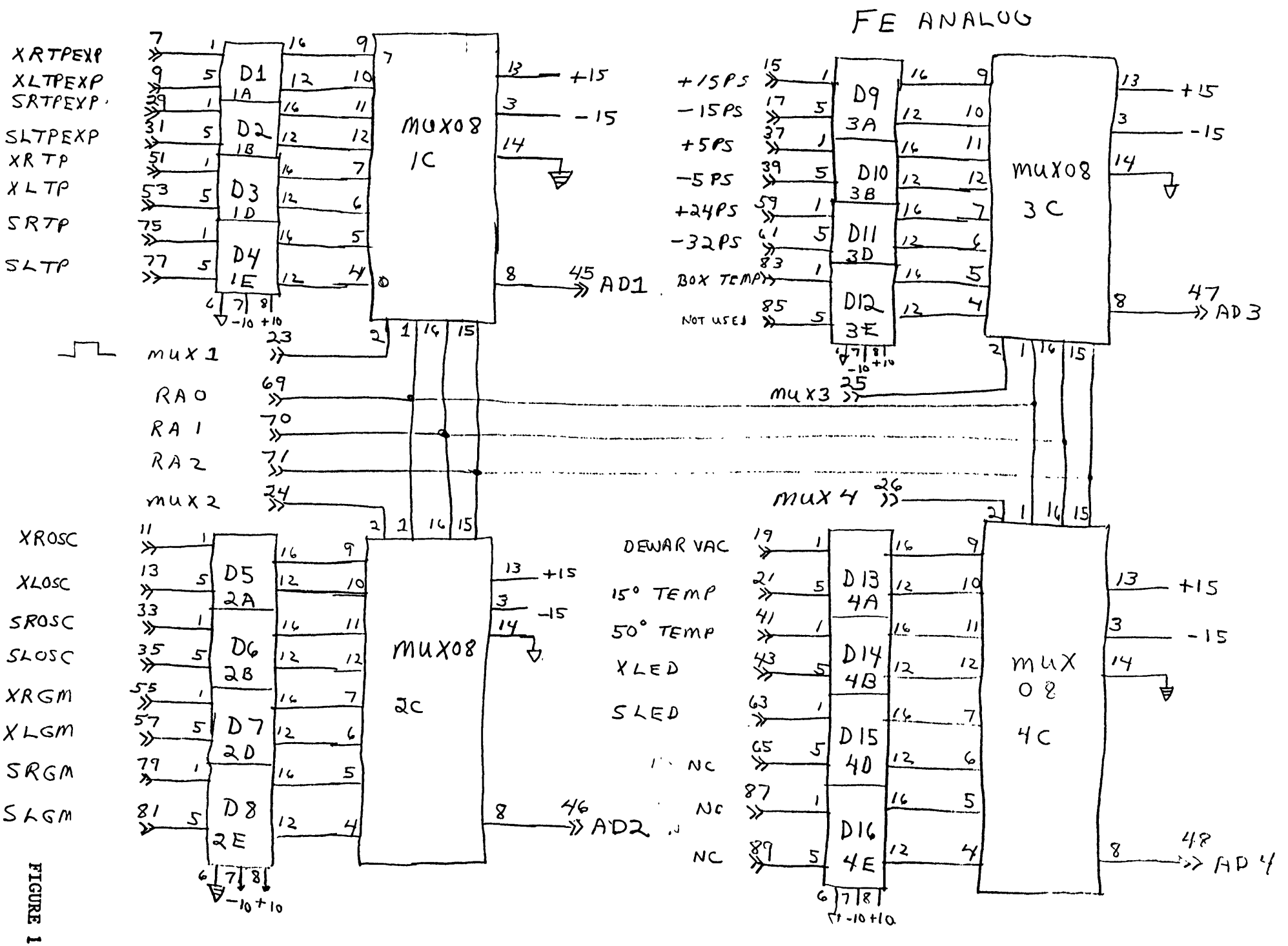
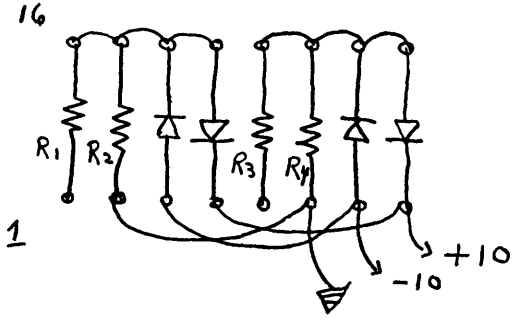
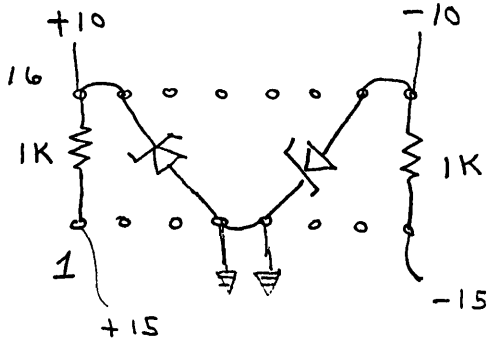

FE ANALOG
XRTPEXP
XLTPEXP
SRTPEXP
SLTPEXP
XRTP
XLTP
SRTP
SLTP
D1 1A
D2 1B
D3 1D
D4 1E
MUX08 1C
+15
-15
AD1
+15PS
-15PS
+5PS
-5PS
+24PS
-32PS
BOX TEMP
NOT USED
D9 3A
D10 3B
D11 3D
D12 3E
MUX08 3C
AD3
mux1
mux3
RA0
RA1
RA2
mux2
mux4
XROSC
XLOSC
SROSC
SLOSC
XRGM
XLGM
SRGM
SLGM
D5 2A
D6 2B
D7 2D
D8 2E
MUX08 2C
AD2
DEWAR VAC
15° TEMP
50° TEMP
XLED
SLED
NC
NC
NC
D13 4A
D14 4B
D15 4D
D16 4E
MUX 08 4C
AD4

FIGURE 1

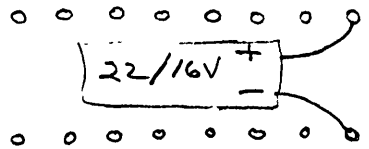


DIODES = IN914
D1 to D16



D17

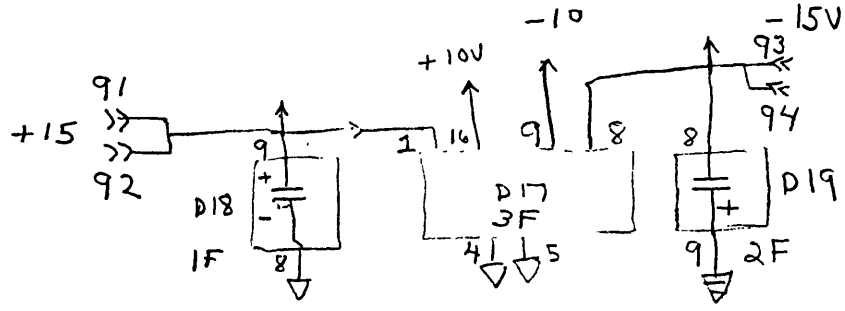
SELECT ZENER FOR
9.5V to 9.7V
1N4740



D18, D19

FIGURE 2

MODULE	R1	R2	R3	R4
D1	511	1 MEG	511	1 MEG
D2	511	1 MEG	511	1 MEG
D3	511	1 MEG	511	1 MEG
D4	511	1 MEG	511	1 MEG
D5	511	1 MEG	511	1 MEG
D6	511	1 MEG	511	1 MEG
D7	511	1 MEG	511	1 MEG
D8	511	4.99K	10.0K	4.99K
D9	10.0K	1 MEG	511	1 MEG
D10	511	4.99K	26.7K	4.99K
D11	19.1K	1 MEG	511	100K
D12	511	1 MEG	511	1 MEG
D13	511	1 MEG	511	100K
D14	511	1 MEG	511	100K
D15	511	1 MEG	511	100K
D16	511	100K	511	100K



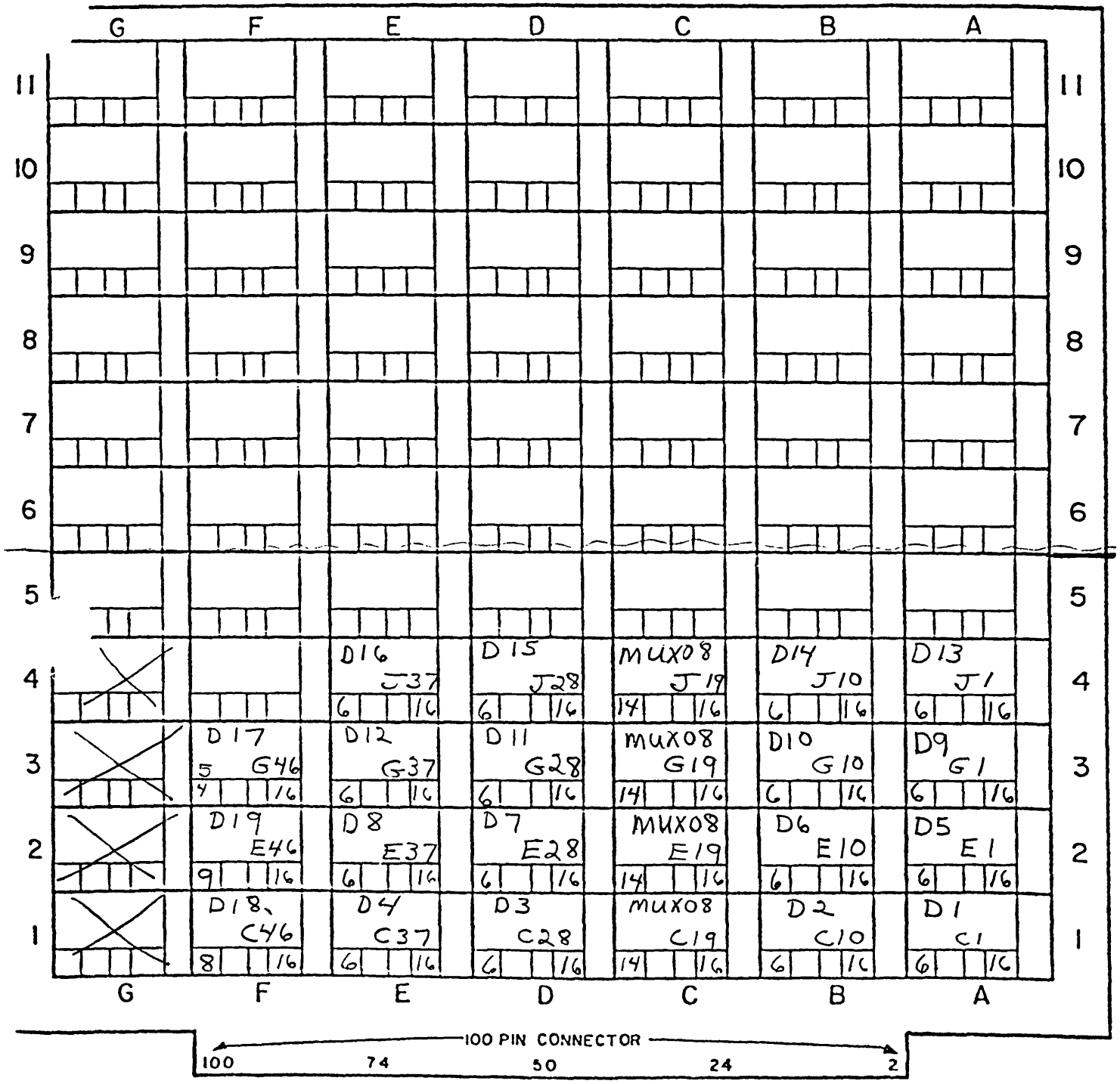
+5 not used on card

FIGURE 2

FE ANALOG

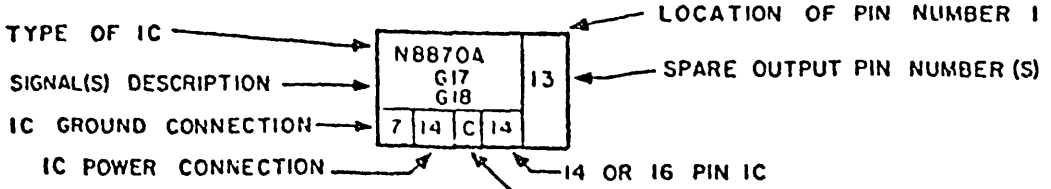
NRAO LOCATION

BY _____ DATE _____



OTES:

1. SAMPLE BOX



2. VIEW, COMPONENT SIDE OF BOARD
3. THIS COLUMN NOT AVAILABLE
4. VCC CONNECTOR PINS: P2, 4, 98, 100 - GND. CONNECTOR PINS: P 1, 3, 27, 49, 73, 97, 99

FIGURE 3

FEANALOG - MUX/DISCRETE

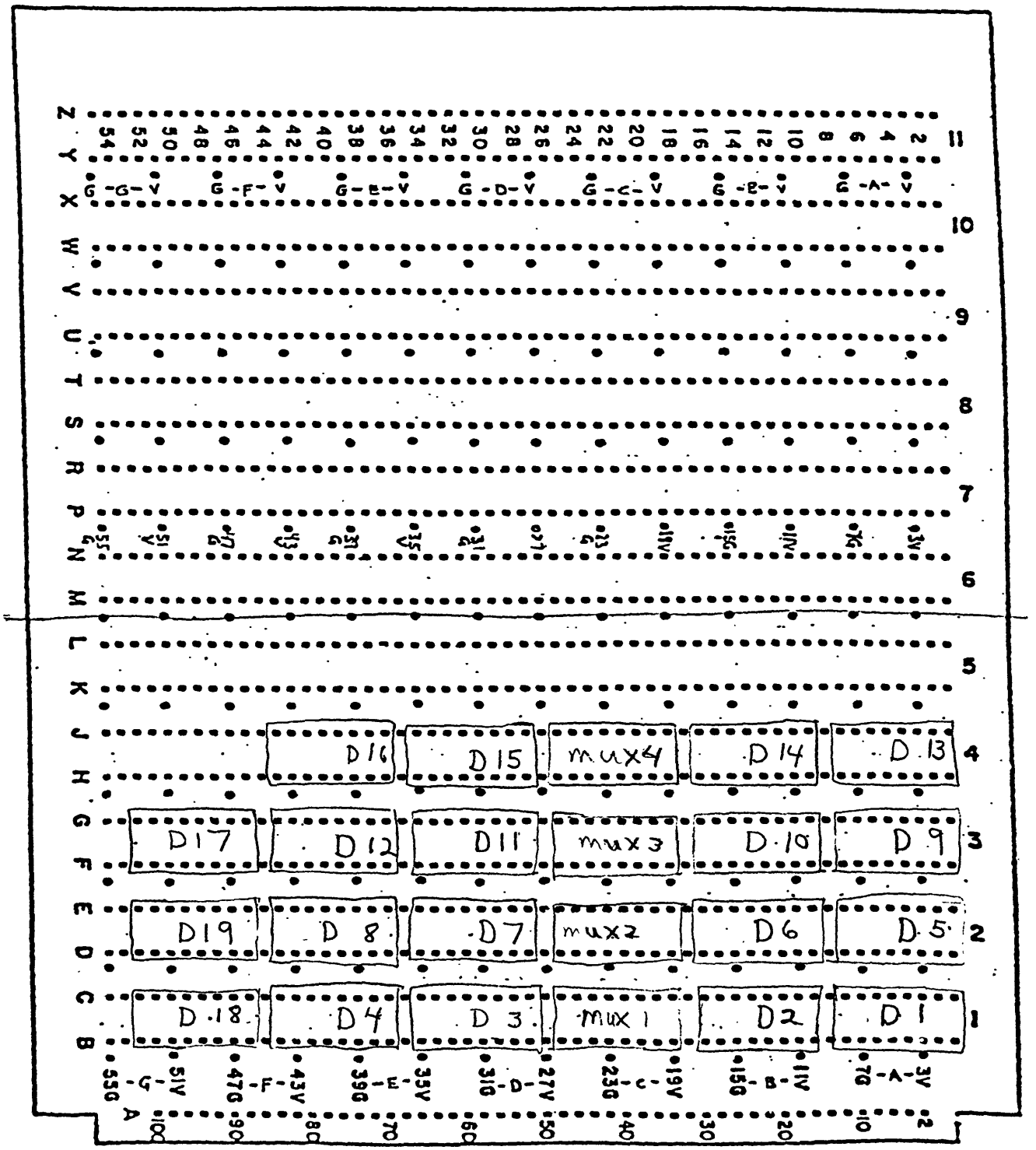


FIGURE 4

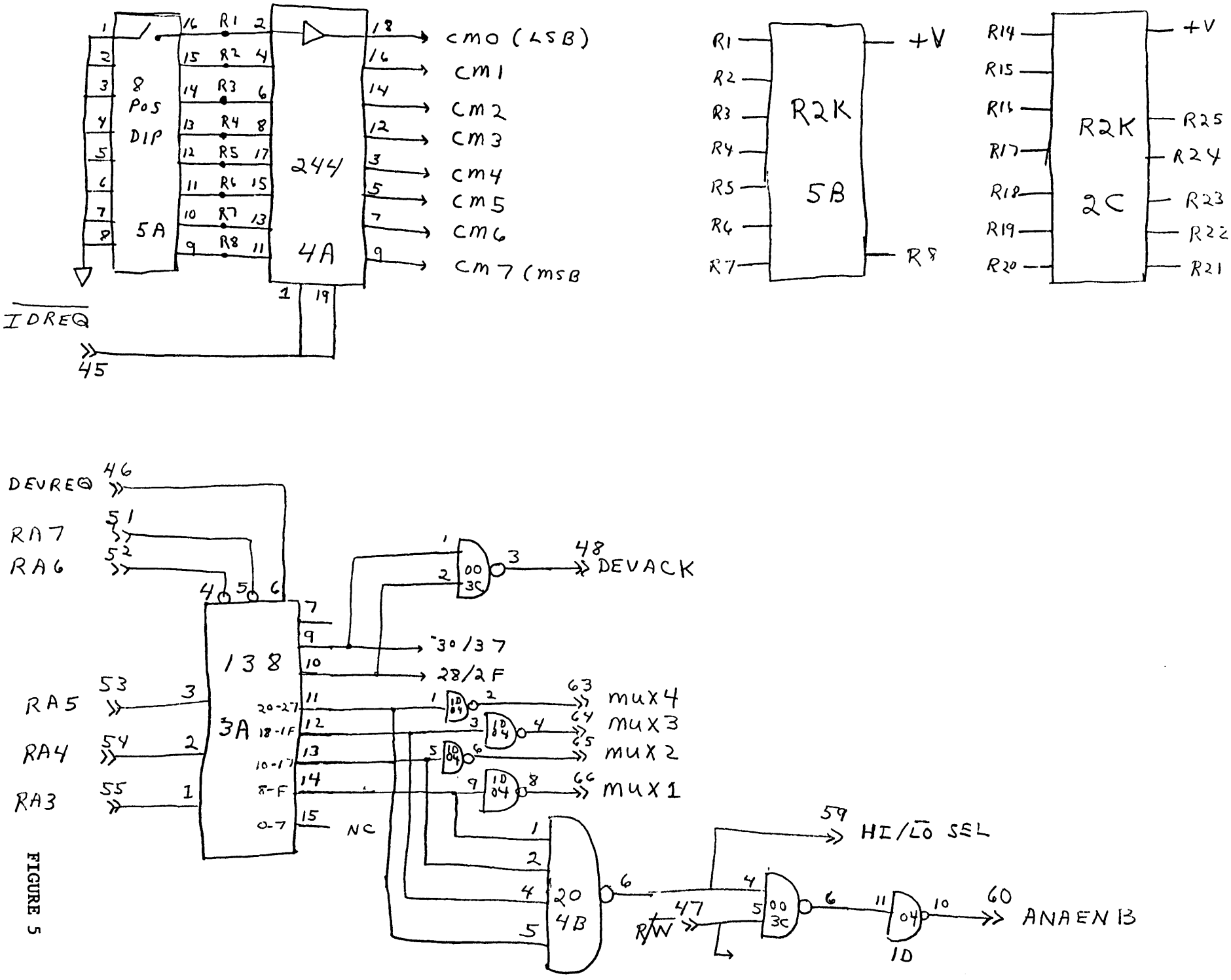

8 Pos DIP
5A
244
4A
R1
R2
R3
R4
R5
R6
R7
R8
cm0 (LSB)
cm1
cm2
cm3
cm4
cm5
cm6
cm7 (msb
IDREQ
45
R2K
5B
+V
R2K
2C
R14
R15
R16
R17
R18
R19
R20
R25
R24
R23
R22
R21
DEVREQ
46
RA7
51
RA6
52
RA5
53
RA4
54
RA3
55
138
3A
20-27
18-1F
10-17
8-F
0-7
NC
48
DEVACK
30/37
28/2F
63
mux4
64
mux3
65
mux2
66
mux1
20
4B
59
HI/LO SEL
47
R/W
60
ANAEN13
1D

FIGURE 5

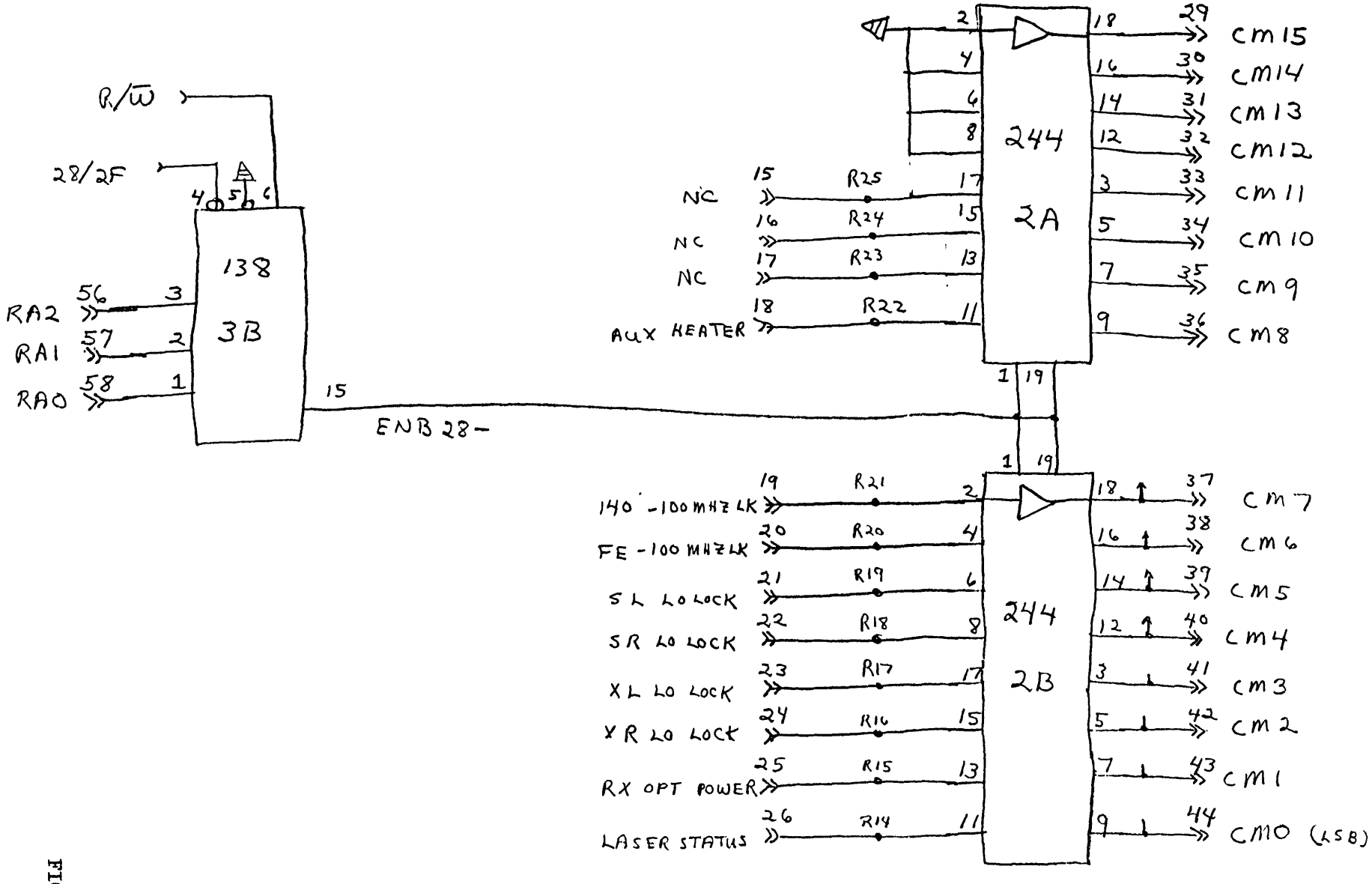

R/W
28/2F
4
5
6
138
3B
RA2
RA1
RA0
56
57
58
3
2
1
15
ENB 28-
244
2A
NC
NC
NC
AUX HEATER
15
16
17
18
R25
R24
R23
R22
17
15
13
11
2
4
6
8
18
16
14
12
3
5
7
9
29
30
31
32
33
34
35
36
CM15
CM14
CM13
CM12
CM11
CM10
CM9
CM8
1
19
244
2B
140 -100 MHZ LK
FE -100 MHZ LK
SL LO LOCK
SR LO LOCK
XL LO LOCK
XR LO LOCK
RX OPT POWER
LASER STATUS
19
20
21
22
23
24
25
26
R21
R20
R19
R18
R17
R16
R15
R14
2
4
6
8
17
15
13
11
18
16
14
12
3
5
7
9
37
38
39
40
41
42
43
44
CM7
CM6
CM5
CM4
CM3
CM2
CM1
CM0 (LSB)

FIGURE 6

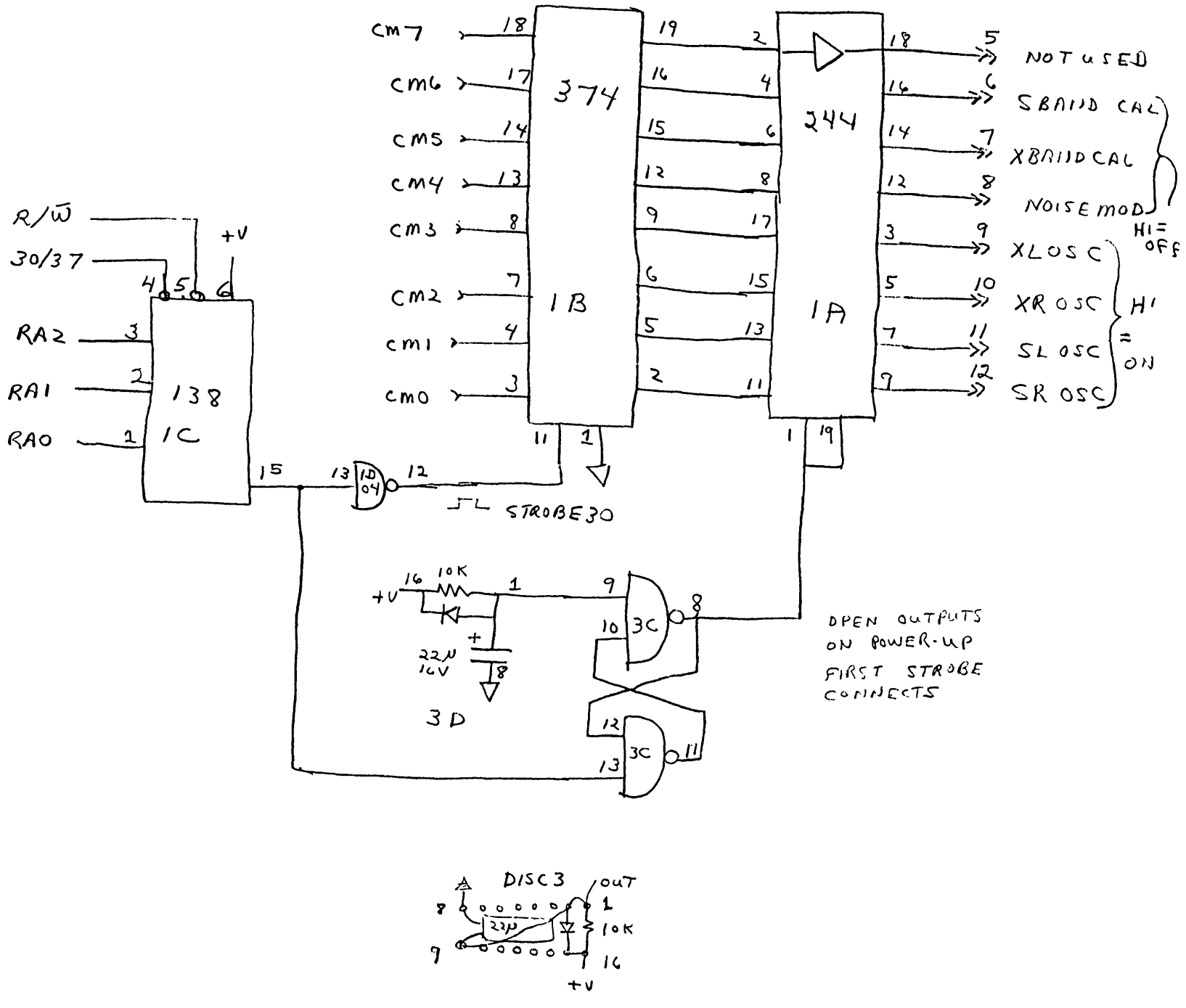

CM7
CM6
CM5
CM4
CM3
CM2
CM1
CM0
374
1B
244
1A
NOT USED
SBAUD CAL
XBAUDCAL
NOISE MOD
HI = OFF
XLOSC
XROSC
SLOSC
SROSC
HI = ON
R/W
30/37
+V
RA2
RA1
RA0
138
1C
1D 04
STROBE30
10K
22µ 16V
3D
3C
3C
OPEN OUTPUTS ON POWER-UP
FIRST STROBE CONNECTS
DISC3
OUT
22µ
10K
+V

FIGURE 7

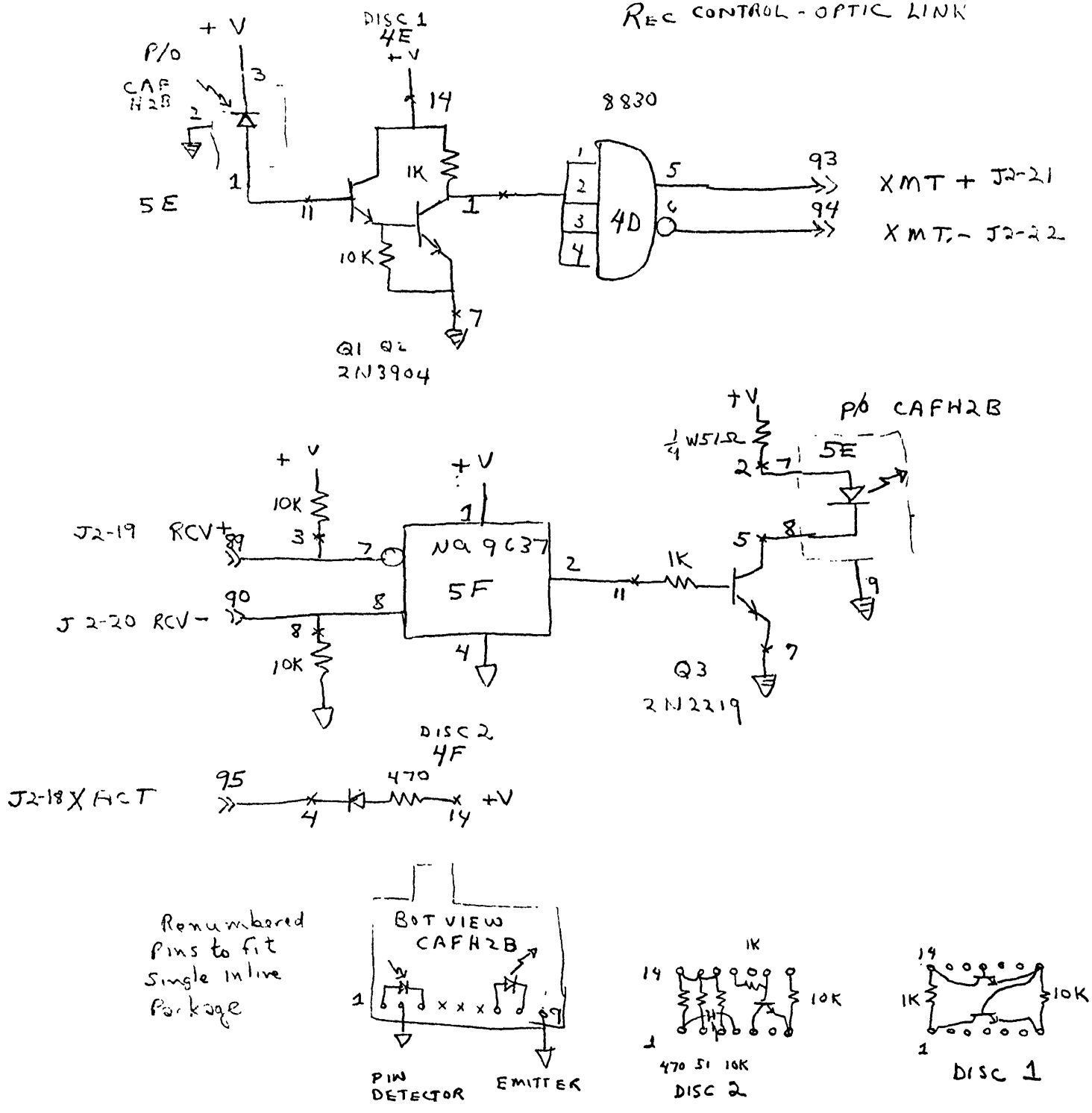
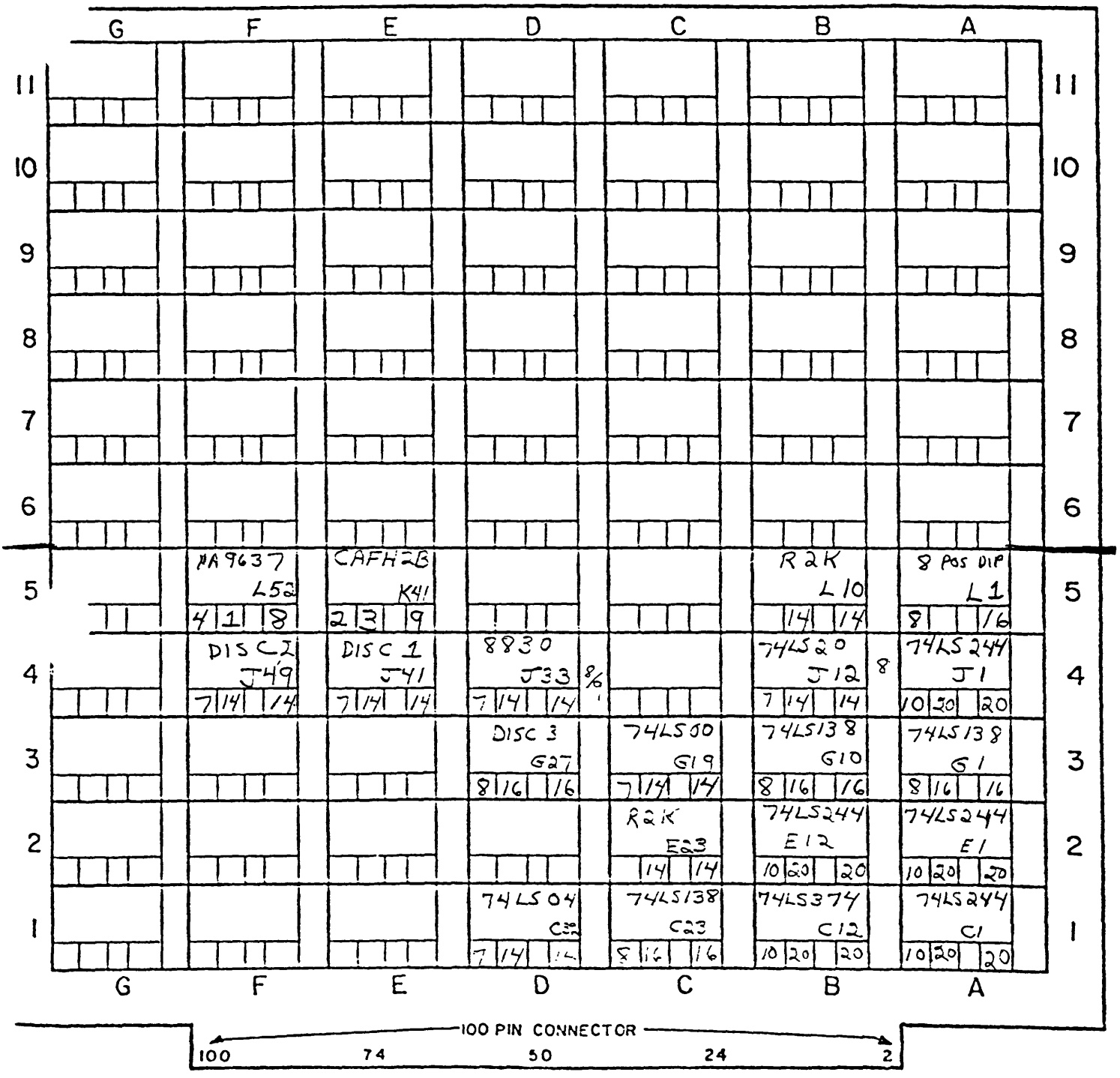

REC CONTROL - OPTIC LINK
+V
P/O
CAF H2B
DISC 1
4E
+V
14
8830
1K
5E
11
1
10K
7
Q1 Q2
2N3904
1
2
3
4
4D
5
6
93
94
XMT + J2-21
XMT - J2-22
+V
P/O CAFH2B
1/4 W 51Ω
2
7
5E
5
8
9
+V
10K
3
J2-19 RCV+
99
7
+V
1
NQ 9637
5F
2
11
1K
90
J 2-20 RCV -
8
8
10K
4
Q3
2N2219
DISC 2
4F
J2-18 XMT
95
4
470
14
+V
Renumbered
Pins to fit
Single Inline
Package
BOT VIEW
CAFH2B
1
PIN
DETECTOR
EMITTER
1K
14
10K
1
470 51 10K
DISC 2
14
1K
10K
1
DISC 1

FIGURE 8

REC CONTROL

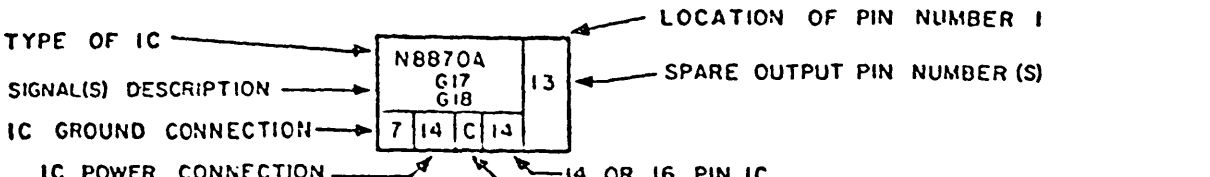
NRAO LOCATION

BY _____ DATE _____



NOTES:

1. SAMPLE BOX



2. VIEW, COMPONENT SIDE OF BOARD
3. THIS COLUMN NOT AVAILABLE
4. VCC CONNECTOR PINS: P2, 4, 98, 100 - GND. CONNECTOR PINS: P 1, 3, 27, 49, 73, 97, 99

FIGURE 9

REC CONTROL

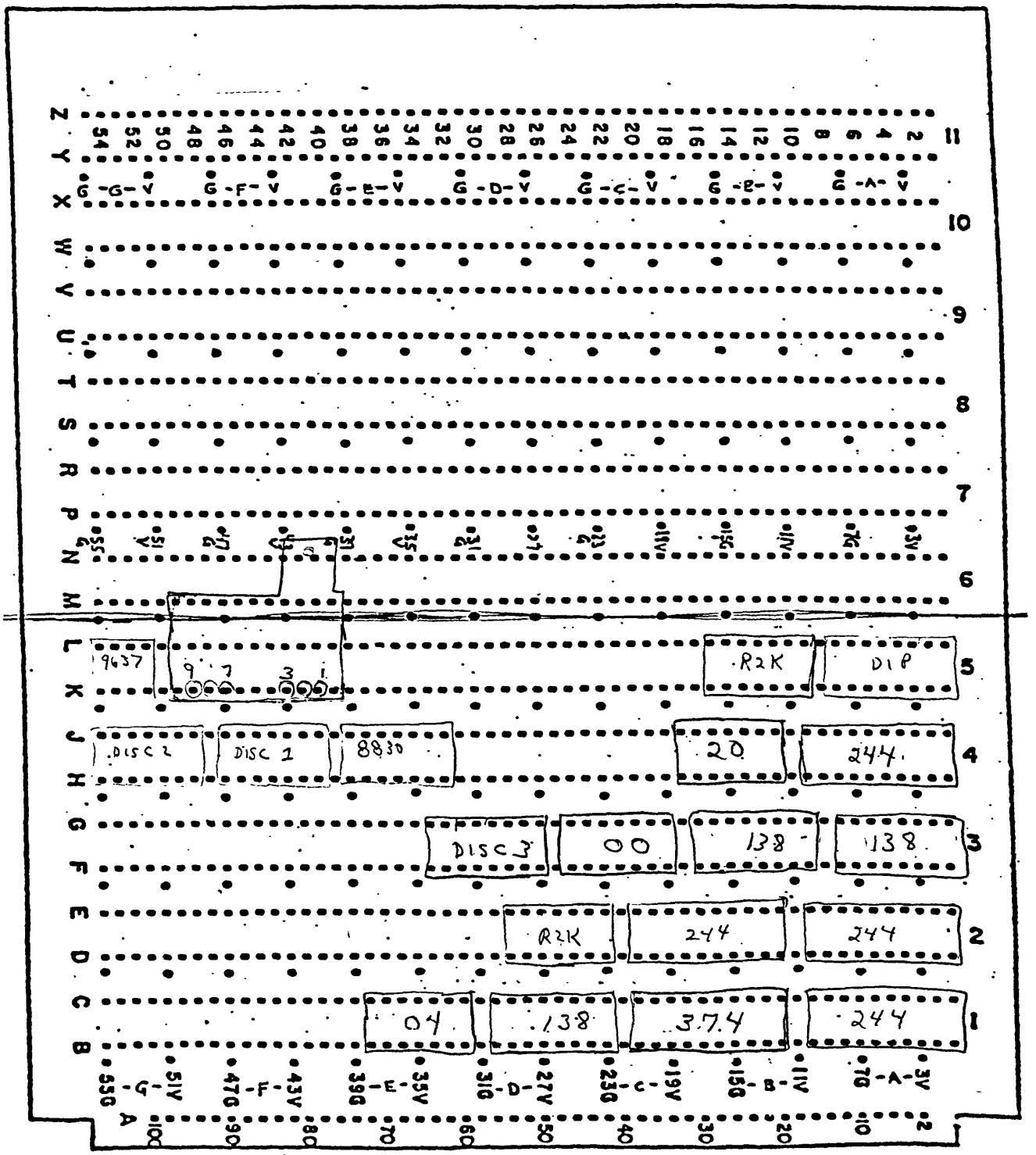
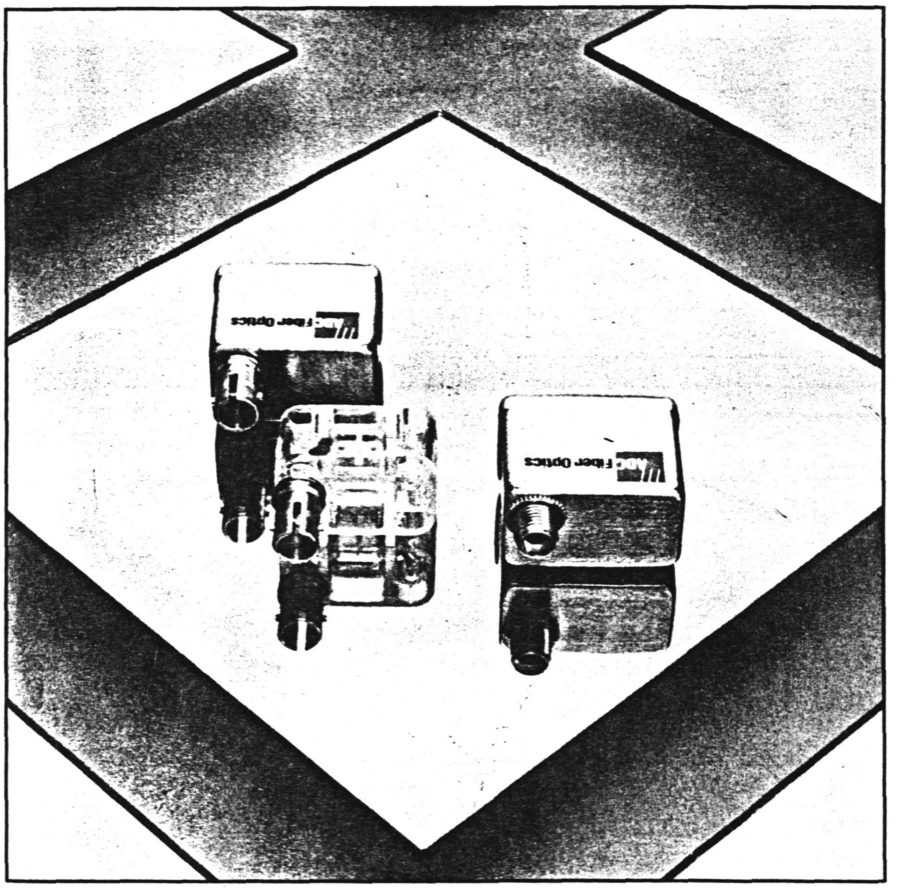


FIGURE 10

ADC®
Fiber Optics

Bidirectional
Connectorized Active Full Duplex Coupler
Model CAF



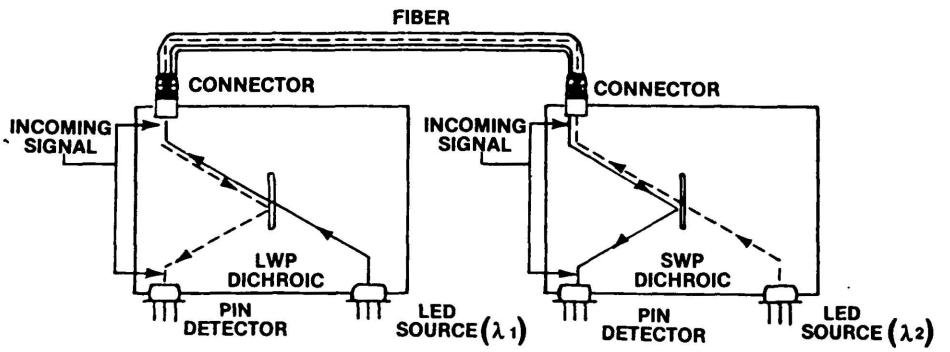
ADC's CAF component permits bidirectional full duplex signal transmission over a single fiber. The CAF operates at dual wavelengths employing a WDM beam separation technique. The transmit and receive signals, operating at different wavelengths, are separated by the use of the CAF's internal reflective surfaces and specially designed optical coatings that result in excellent optical isolation. The CAF's premounted LED source, PIN detector and SMA or ST connector make it compatible with almost any fiber or cable type. Through the high precision plastic molded body used in this design ADC has simplified the technology of combining and distributing optical signals.

ADC's model CAF, full duplex coupler can be used in a wide range of multimode optical network applications, including, various optical local area networks, data bus extenders, single fiber communication links and optical sensors.

CAF Full Duplex Operation

λ_1 = ————————

λ_2 = – – – – – – – – – – –



Features

Single fiber bidirectional communication

Small PC Board mountable package

Single package that incorporates the LED, PIN, SMA or ST compatible connector and fiber optic coupler

Benefits

Lower system costs; flexible system design; increased system reliability

No fiber pigtail routing or termination problems; reduced P.C. Board real estate requirements

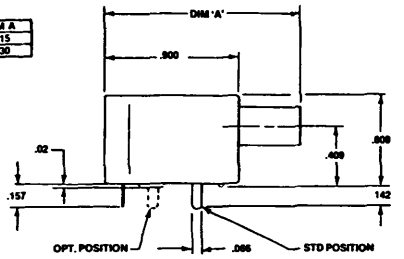
Fewer separate components; more efficient system performance

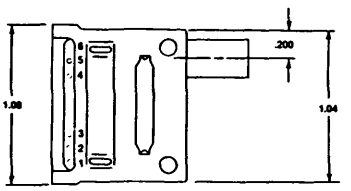
CAF FULL DUPLEX

Electro-optical Specifications		MIN	TYP	MAX	UNIT
Optical Power Coupled into Fiber (1) (I_f = 100 mA)	50/125 G.I.	−19.2 (12)	−17.0 (20)	−15.2 (30)	dBm (μW)
	62.5/125 G.I.	−17.0 (20)	−14.0 (40)	−12.2 (60)	dBm (μW)
	100/140 G.I.	−13.0 (50)	−10.0(100)	−8.2(150)	dBm (μW)
	200/240 S.I.	−7.0(200)	−4.6(350)	−2.6(550)	dBm (μW)
Coupled Power Variation (Over temperature range)					
−40°C to +80°C.		—	+0.5	+1.0	dB
		—	−1.0	−1.5	dB
0°C to +60°C		—	+0.5	+1.0	dB
(Emitter I_f = 100 mA at 50% duty cycle)		—	−0.5	−1.0	dB
Coupler Responsivity		0.35	0.45	0.55	A/W
Responsivity Variation (Over operating temperature range)					
−40°C to +80°C		—	±0.25	±1.0	dB
0°C to +60°C		—	±0.25	±1.0	dB
Crosstalk Current to Detector (Over operating temperature range)					
(Emitter I_f = 100 mA, Detector Bias = −5V)		—	2	20	nA
Operational Wavelength	Type 01	715	730	745	nm
	Type 02	845	865	890	nm
Emitter Bandwidth (+20 mA P-P, I_f = 100 mA)					
−1.5dB from 1 MHz	Type 01	10	20	—	MHz
	Type 02	10	30	—	MHz
−3.0dB from 1 MHz	Type 01	—	40	—	MHz
	Type 02	—	70	—	MHz
Detector Bandwidth (−3dB @−5V Bias)		50	70	—	MHz
Operational Temperature Range		−40	—	+80	°C
Emitter Forward Current (I_f)	Type 01	—	—	120	mA dc
	Type 02	—	—	120	mA dc
Detector Bias Voltage		−5	—	−50	V
Detector Dark Current (@−5V Bias)		—	1	5	nA
Storage Temperature		−40	—	+85	°C

Note (1): Optical Power measured after 1 meter of specified fiber. Connector: SMA (Amphenol 905 style or equivalent) or ST (AT&T type) compatible.

TYPE	DIM A
SMA	1.15
ST	1.30





PIN IDENTIFICATION	
PIN NO.	DESCRIPTION
1	EMITTER CASE
2	EMITTER CATHODE NEG
3	EMITTER ANODE POS
4	DETECTOR CATHODE POS
5	DETECTOR CASE
6	DETECTOR ANODE NEG

Above specifications are for coupler using ADC Fiber Optics standard emitters and detectors. Other devices may be substituted to obtain various operational characteristics. Consult ADC Fiber Optics for further information.

Ordering Information

CAF-X X X - XX

NOT APPLICABLE (ALWAYS X)

NOT APPLICABLE (ALWAYS X)

01 = 730nm Transmission, SMA Connector
02 = 865nm Transmission, SMA Connector
03 = 730nm Transmission, ST Connector
04 = 865nm Transmission, ST Connector

WAVELENGTH

H = 730/865nm, Full Duplex

843 1/87

ADC Telecommunications
Telecommunications

ADC Telecommunications, Inc.
4900 West 78th Street
Minneapolis, Minnesota 55435

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London, U.K. (0734) 441 955 • Montreal, Quebec (514) 677-9166 • Vancouver, BC (604) 270-1675 • Toronto, Ont. (416) 964-2192 • Ottawa, Ont. (613) 596-9937 • Singapore 225-8228

MUX-08/MUX-24

8-CHANNEL/DUAL 4-CHANNEL JFET ANALOG MULTIPLEXERS
(OVERVOLTAGE AND POWER SUPPLY LOSS PROTECTED)

Precision Monolithics Inc.

FEATURES

- **JFET Switches Rather Than CMOS**
- **Low "ON" Resistance ..... 220Ω Typ**
- **Highly Resistant to Static Discharge Damage**
- **No SCR Latch-Up Problems**
- **Digital Inputs Compatible With TTL and CMOS**
- **125° C Temperature Tested Dice Available**
- **MUX-08 Pin Compatible With DG508, HI-508A, IH5108, IH6108, LF11508/12508/13508, AD7506**
- **MUX-24 Pin Compatible With DG509, HI-509A, IH5208, IH6208, LF11509/12509/13509, AD7507**

ORDERING INFORMATION†

25°C ON RESISTANCE	PACKAGE HERMETIC DIP	PLASTIC DIP	LCC	TEMPERATURE RANGE
220Ω	MUX08AQ*	—	—	MIL
	MUX08EQ	—	—	IND
	—	MUX08EP	—	COM
300Ω	MUX08BQ*	—	MUX08BRC/883	MIL
	MUX08FQ	—	—	IND
	—	MUX08FP	—	COM
220Ω	MUX24AQ*	—	—	MIL
	MUX24EQ	—	—	IND
	—	MUX24EP	—	COM
300Ω	MUX24BQ*	—	—	MIL
	MUX24FQ	—	—	IND
	—	MUX24FP	—	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

The MUX-08 is a monolithic eight-channel analog multiplexer which connects a single output to one of the eight analog inputs depending upon the state of a 3-bit binary address.

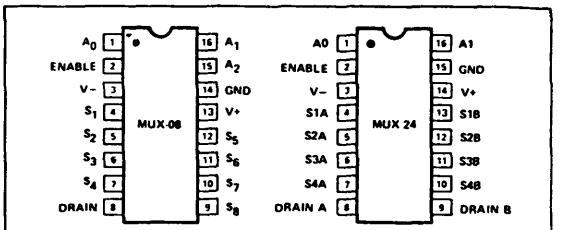
The MUX-24 is a monolithic four-channel differential analog multiplexer configured in a double pole, four-position (plus OFF) electronic switch array. A two-bit binary input address connects a pair of independent analog inputs from each four-channel input section to the corresponding pair of independent analog outputs.

All switches in the MUX-08/MUX-24 are turned OFF by applying logic "0" to the ENABLE pin, thereby providing a package select function.

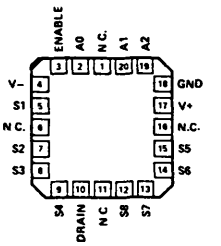
Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, these devices offer low, constant "ON" resistance, low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors over the full operating temperature range.

For single sixteen-channel and dual eight-channel models, refer to the MUX-16/MUX-28 data sheet.

PIN CONNECTIONS

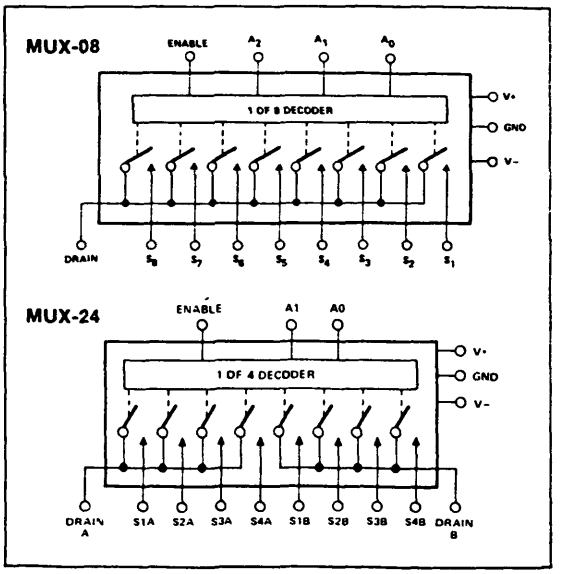


16-PIN DUAL-IN-LINE PACKAGE
(Q or P Package)



MUX-08BRC/883
LCC
(RC-Suffix)

FUNCTIONAL DIAGRAMS



ABSOLUTE MAXIMUM RATINGS (Note)

Operating Temperature Range
- MUX-08/24-AQ, BQ, BRC ..... −55°C to +125°C
- MUX-08/24-EQ, FQ ..... −25°C to +85°C
- MUX-08/24-EP, FP ..... 0°C to +70°C

DICE Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
- P-Suffix ..... −65°C to +125°C

Power Dissipation 500mW
- Derate above 100°C ..... 10mW/°C

Lead Temperature (Soldering, 60 sec) ..... 300°C
Maximum Junction Temperature ..... 150°C
V+ Supply to V− Supply 36V
Logic Input Voltage ..... (−4V or V−) to V+ Supply
Analog Input Voltage ....V− Supply −20V to V+ Supply +20V
Maximum Current Through Any Pin 25mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V+ = +15V, V− = −15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-08A/E MUX-24A/E MIN	TYP	MAX	MUX-08B/F MUX-24B/F MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_S \le 10V$, $I_S \le 200\mu A$		—	220	300	—	300	400	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \le V_S \le 10V$, $I_S = 200\mu A$		—	1	5	—	3	7	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 200\mu A$		—	7	15	—	9	20	%
Analog Voltage Range	V_A	(Note 6)		+10 −10	+10.4 −15	— —	+10 −10	+10.4 −15	— —	V
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)		—	0.01	1.0	—	0.01	2.0	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	MUX-08 MUX-24	— —	0.1 0.05	1.0 1.0	— —	0.1 0.05	2.0 2.0	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$ $+I_{S(ON)}$	$V_D = 10V$ (Note 1)	MUX-08 MUX-24	— —	0.1 0.05	1.0 1.0	— —	0.1 0.05	2.0 2.0	nA
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		—	1	10	—	1	10	μA
Digital "0" Enable Current	$I_{INL\ EN}$	$V_{EN} = 0.4V$		—	4	10	—	4	10	μA
Digital Input Capacitance	C_{DIG}			—	3	—	—	3	—	pF
Switching Time	t_{TRAN}	(Notes 2, 5) Figure 1 (Test Circuit)		—	1.8	2.1	—	1.8	2.1	μs
Output Settling Time	t_S	10V Step to 0.10% 10V Step to 0.05% 10V Step to 0.02%		— — —	1.3 1.5 2.3	— — —	— — —	1.7 1.9 2.5	— — —	μs
Break-Before-Make Delay	t_{OPEN}	Figure 3 (Test Circuit)		—	0.8	—	—	1.0	—	μs
Enable Delay "ON"	$t_{ON\ EN}$	(Note 5) Figure 2 (Test Circuit)		—	1	2	—	1	2	μs
Enable Delay "OFF"	$t_{OFF\ EN}$	(Note 5) Figure 2 (Test Circuit)	MUX-08 MUX-24	— —	0.1 0.2	0.4 0.5	— —	0.2 0.3	0.4 0.6	μs
"OFF" Isolation	ISO_{OFF}	(Note 4) Figure 5 (Test Circuit)	MUX-08 MUX-24	— —	60 66	— —	— —	60 66	— —	dB
Crosstalk	CT	(Note 3) Figure 4 (Test Circuit)	MUX-08 MUX-24	— —	70 76	— —	— —	70 76	— —	dB
Source Capacitance	$C_{S(OFF)}$	Switch "OFF", $V_S = 0V$, $V_D = 0V$	MUX-08 MUX-24	— —	2.5 2	— —	— —	2.5 2	— —	pF
Drain Capacitance	$C_{D\ OFF}$	Switch "OFF", $V_S = 0V$, $V_D = 0V$	MUX-08 MUX-24	— —	7 4	— —	— —	7 4	— —	pF
Input to Output Capacitance	$C_{DS(OFF)}$	(Note 4)	MUX-08 MUX-24	— —	0.3 0.15	— —	— —	0.3 0.15	— —	pF
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I+	V+ = 15V V+ = 5V		— —	10 8	12 —	— —	6 5	12 —	mA
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I−	V+ = −15V V+ = −5V		— —	3.0 2.5	3.8 —	— —	2.0 1.8	3.8 —	mA

NOTES: See next page.

J1 FECONTROL/MONITER.

Parallel I/O - P1
Type: Cinch or Amphenol DD-50PC
Mating type: DD-50S

Pin	Signal	SOURCE/DEST	
1	ANLG-0H	NC	
2	ANLG-1H	J4-45	
3	ANLG-2H	J4-46	
4	ANLG-3H	J4-47	
5	ANLG-4H	J4-48	
6	ANLG-5H	NC	
7	ANLG-6H	NC	
8	ANLG-7H	NC	
9	CON/MON-15	J3-29	
10	CON/MON-13	J3-31	
11	CON/MON-11	J3-33	
12	CON/MON-9	J3-35	
13	CON/MON-7	J3-37	
14	CON/MON-5	J3-39	
15	CON/MON-3	J3-41	
16	CON/MON-1	J3-43	
17	HI/LO SEL	J3-59	
18	ANLG-0L	J4-97	15V GND
19	ANLG-1L		
20	ANLG-2L		
21	ANLG-3L		
22	ANLG-4L	J4-99	15V GND
23	ANLG-5L		
24	ANLG-6L		
25	ANLG-7L		
26	CON/MON-14	J3-30	
27	CON/MON-12	J3-32	
28	CON/MON-10	J3-34	
29	CON/MON-8	J3-36	
30	CON/MON-6	J3-38	
31	CON/MON-4	J3-40	
32	CON/MON-2	J3-42	
33	CON/MON-0	J3-44	
34	5V COMM	NC	
35	DEV REQ	J3-46	
36	DEV ACK	J3-48	
37	ANENB	J3-60	
38	HIQ GND	J5-15	15V GND
39	-15V	-15 Feed	
40	+15V	+15 Feed	
41	RA-7	J3-51	
42	RA-6	J3-52	
43	RA-5	J3-53	
44	RA-4	J3-54	
45	RA-3	J3-55	
46	RA-2	J3-56	
47	RA-1	J3-57	
48	RA-0	J3-58	
49	R/-W	J3-47	
50	+5V	NC	

J2 FE CONTROL/MONITOR

Serial I/O - P2
Type: Cinch or Amphenol DB-25PC
Mating type: DB-25S

Pin	Signal	SOURCE / DEST
1	+5V	5V FEED
2	(reserved)	NC
3	(reserved)	
4	(not used)	
5	(reserved)	
6	(reserved)	
7	(reserved)	
8	(reserved)	NC
9	ID REQ	J3-45
10	DOUT	NC
11	PARX	NC
12	MSG	NC
13	5V COMM	5V GND
14	+5V	5V FEED
15	+15V	+15V FEED
16	-15V	-15V FEED
17	HIQ GND	J5-14 15V GND
18	XACT	J3-95
19	RCV+	J3-89
20	RCV-	J3-90
21	XMT+	J3-93
22	XMT-	J3-94
23	(reserved)	NC
24	BUSY	NC
25	5V COMM	5V GND

SLOT # J2 NAME NEC CONTROL

NAME	BACK PIN #	TO	FROM	NAME	FRONT PIN #	TO	FROM
GROUND	1			+5	2		
GROUND	3			+5	4		
SPARE (D07)	5	J6-30		SBAND CAL (D06)	6	J6-31	
XBANDCAL (D05)	7	J6-32		NOISE MOD (D04)	8	J6-33	
XL OSC (D03)	9	J6-34		XR OSC (D02)	10	J6-35	
SL OSC (D01)	11	J6-36		SR OSC (D00)	12	J6-37	
	13				14		
SPARE (DI 11)	15		J6-18	SPARE (DI10)	16		J6-19
SPARE (DI 9)	17		J6-20	AUX HTR (DI 8)	18		J6-21
140.100 MHZ (DI 7)	19		J6-22	FE 100 MHZ (DI 6)	20		J6-23
SL LO LOCK (DI 5)	21		J6-24	SR LO LOCK (DI 4)	22		J6-25
XL LO LOCK (DI 3)	23		J6-26	XR LO LOCK (DI 2)	24		J6-27
RX OPT. POW (DI 1)	25		J6-28	LASER STATUS (DI 0)	26		J6-29
GROUND	27				28		
CM 15	29	J1-9		CM 14	30	J1-26	
CM 13	31	J1-10		CM 12	32	J1-27	
CM 11	33	J1-11		CM 10	34	J1-28	
CM 9	35	J1-12		CM 8	36	J1-29	
CM 7	37	J1-13		CM 6	38	J1-30	
CM 5	39	J1-14		CM 4	40	J1-31	
CM 3	41	J1-15		CM 2	42	J1-32	
CM 1	43	J1-16		CM 0	44	J1-33	
ID REQ—	45	J2-9		DEV REQ	46	J1-35	
R/$\overline{W}$	47	J1-49		DEV ACK	48	J1-36	
GROUND	49				50		
RA7	51		J1-41	RA6	52		J1-42
RA5	53		J1-43	RA4	54		J1-44
RA3	55		J1-45	RA2	56	J4-71	J1-46
RA1	57	J4-70	J1-47	RA0	58	J4-69	J1-48
HI/$\overline{LO}$ SEL	59	J1-17		ANAENB	60	J1-37	
	61				62		
MUX4	63	J4-26		MUX3	64	J4-25	
MUX2	65	J4-24		MUX1	66	J4-23	
	67				68		
	69				70		
	71				72		
GROUND	73				74		
	75				76		
	77				78		
	79				80		
	81				82		
	83				84		
	85				86		
	87				88		
RCV+	89	J2-19		RCV-	90	J2-20	
	91				92		
XMT+	93	J2-21		XMT—	94	J2-22	
XACT	95	J2-18			96		
GROUND	97			+5	98		
GROUND	99			+5	100		
		89 PINS TOTAL					

SLOT # J4 NAME FEANALJG

NAME	BACK PIN #	To	FROM	NAME	FRONT PIN #	To	FROM
GROUND (15 V)	1		J5-15	+5	2		
~~GROUND~~ (GND)	3		J5-14	+5	4		
	5				6		
XRTPEXP (AI0F)	7		J6-1		8		
XLTPEXP (AI0E)	9		J6-2		10		
XROSC (AI17)	11		J6-9		12		
XLOSC (AI16)	13		J6-10		14		
+15PS (AI1F)	15		+15 feed		16		
-15PS (AI1E)	17		-15 feed		18		
DEWARVAC (AI27)	19		J5-5		20		
15° TEMP (AI26)	21		J5-6		22		
MUX1	23		J3-66	MUX2	24		J3-65
MUX3	25		J3-64	MUX4	26		J3-63
GROUND	27				28		
SRTP EXP (AI0D)	29		J6-3		30		
SLTPEXP (AI0C)	31		J6-4		32		
SROSC (AI15)	33		J6-11		34		
SLOSC (AI14)	35		J6-12		36		
+5PS (AI1D)	37		+5 Feed		38		
-5PS (AI1C)	39		J6-13		40		
50° TEMP (AI25)	41		J5-7		42		
XLED (AI24)	43		J5-8		44		
AD1	45	J1-2		AD2	46	J1-3	
AD3	47	J1-4		AD4	48	J1-5	
GROUND	49				50		
XRTP (AI0B)	51		J6-5		52		
XLTP (AI0A)	53		J6-6		54		
XRGM (AI13)	55		J5-1		56		
XLGM (AI12	57		J5-2		58		
+24PS (AI1B)	59		J6-14		60		
-32PS (AI1A)	61		J6-15		62		
SLED (AI23)	63		J5-9		64		
NC-1 (AI22)	65		J5-12		66		
	67				68		
RA0	69		J3-58	RA1	70		J3-57
RA2	71		J3-56		72		
GROUND	73				74		
SRTP (AI09)	75		J6-7		76		
SLTP (AI08)	77		J6-8		78		
SRGM (AI11)	79		J5-3		80		
SLGM (AI10)	81		J5-4		82		
BOXTEMP (AI19)	83		J6-16		84		
NC-2 (AI18)	85		J6-17		86		
NC-3 (AI21)	87		J5-10		88		
NC-4 (AI20)	89		J5-11		90		
-15	91		+15 feed	+15	92		+15 feed
-15	93		-15 feed	-15	94		-15 feed
	95				96		
GROUND (+15)	97	J1-18	J5-15	+5	98		
GROUND (GND)	99	J1-22	J5-14	+5	100		

189 PINS TOTAL

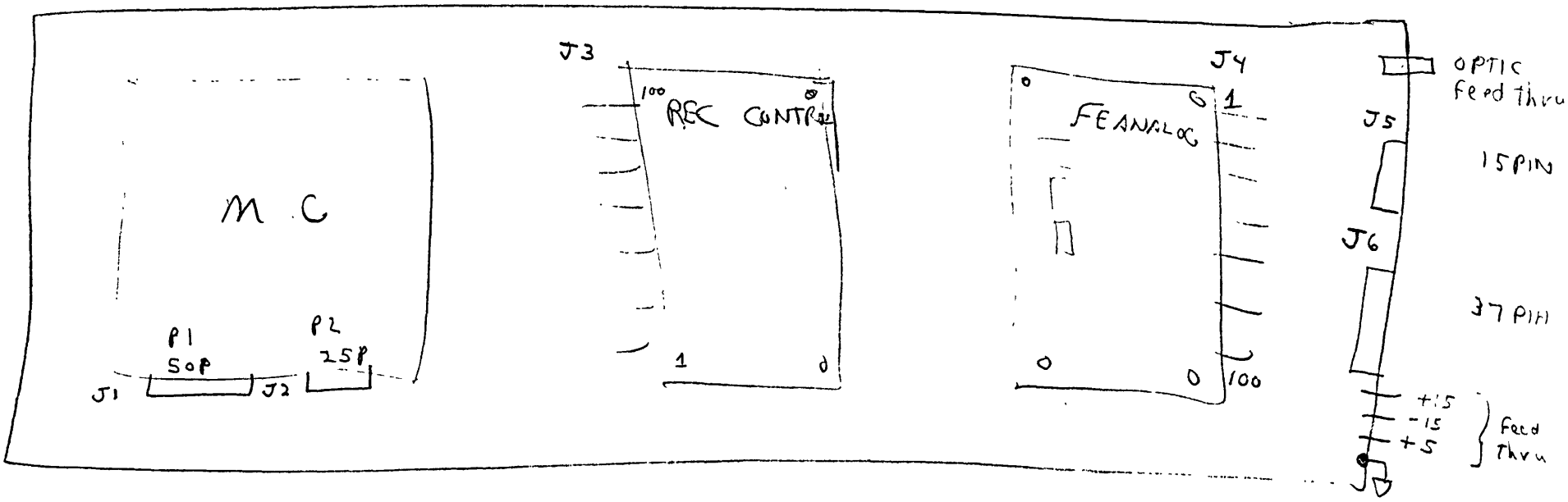
J5 15 PIN I/O

1	J4-55	XRGM
2	J4-57	XLGM
3	J4-79	SRGM
4	J4-81	SLGM
5	J4-19	DEWARVAC
6	J4-21	15° TEMP
7	J4-41	50° TEMP
8	J4-43	XLED
9	J4-63	SLED
10	J4-87	NC3
11	J4-89	NC4
12	J4-65	NC1
13		
14	J4-3, 99+J2-17	15V GND
15	J4-1, 97+J1-38	15V GND

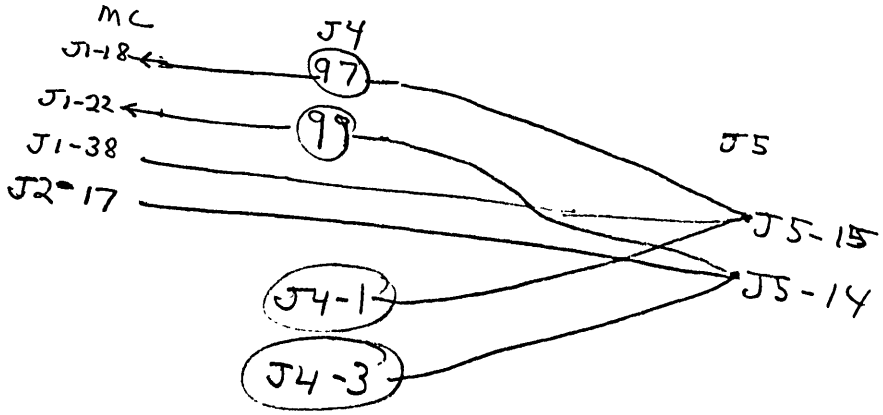
J6 37 PIN IO

PIN#	SOURCE/DEST	SIGNAL NAME
1	J4-7	XR TP EXP
2	J4-9	XL TP EXP
3	J4-29	SR TP EXP
4	J4-31	SL TP EXP
5	J4-51	XR TP
6	J4-53	XL TP
7	J4-75	SR TP
8	J4-77	SL TP
9	J4-11	XR OSC
10	J4-13	XL OSC
11	J4-33	SR OSC
12	J4-35	SL OSC
13	J4-39	-5V PS
14	J4-59	+24V PS
15	J4-61	-32V PS
16	J4-83	BOX TEMP
17	J4-85	NC 2
18	J3-15	SPARE (DI 11)
19	J3-16	SPARE (DI 10)
20	J3-17	SPARE (DI 9)
21	J3-18	AUX HTR (DI 8)
22	J3-19	140-100 MHZ (DI 7)
23	J3-20	FE 100 MHZ (DI 6)
24	J3-21	SL LO LOCK (DI 5)
25	J3-22	SR LO LOCK (DI 4)
26	J3-23	XL LO LOCK (DI 3)
27	J3-24	XR LO LOCK (DI 2)
28	J3-25	REC OPT PWR (DI 1)
29	J3-26	LASER STATUS (DIØ)
30	J3-5	SPARE (DO 7)
31	J3-6	SBANDCAL (DO 6)
32	J3-7	XBANDCAL (DO 5)
33	J3-8	NOISEMOD (DO 4)
34	J3-9	XLOSC (DO 3)
35	J3-10	XROSC (DO 2)
36	J3-11	SLOSC (DO 1)
37	J3-12	SR OSC (DOØ)

ORIG



15V GND



current
no activity

-15V	-	50 ma
+15V		67 ma
+5V		950 ma

7 PIN POWER CONNECTOR
ADDED

A	+15
B	GND
C	-15
D	+5
E	GND
F	-5 (not used)
H	+5