

# ELECTRONICS DIVISION TECHNICAL NOTE 195

## IPG Continuum Data Collection System

Tim Weadon  
8/29/03

The "IPG" Continuum System was designed and built in 1998 by Rick Fisher, Rich Lacasse, Dwayne Schiebel and Tim Weadon. Rick specified the system requirements, Rich designed and built the Filter Amplifier system. Dwayne designed and built the Clock and Switching system and Tim designed and built and specified the computer associated hardware and software. Figure 1 is an over-all block diagram of the system.

The Filter Amplifier has one SMA input and one BNC output. There are three low-pass filters one may choose. The single pole three throw switch (SP3T) allows the user to select either a 50Hz, 500Hz or 5000Hz low-pass filter.

The Clock and Switching system inputs 4 differential signals and routes them, through the ribbon cable, to the computer A/D card. Only one signal was originally requested so the system, presently, only supports one input on the first channel. This system has thumb-wheel switches to set the hardware parameters "sample rate", "switch rate" and "cycles/integration".

The enable/stop switch arms and disarms the system from any spurious signals which could trigger a false start. The thumb-wheel switches should be set when this switch is in the stop position. Once the thumb-wheel switches are set, and the computer system is on and stable, this switch may be set to the enable position. When you wish to begin a new scan the enable/stop switch should be set to stop, the thumb-wheel switches should be set, then the enable/stop switch should be set to enable. The Switch Control LED and the Recording Data LED will be flashing when the clock and switching system is running.

The Clock and Switching system provide an interrupt to the computer A/D for when to sample the data. The computer provides the "go" signal to the Clock and Switching system for when it is to start generating the clock and switching signals.

The Computer and associated hardware provide the user interface for collecting, documenting and analyzing the data. The user enters a filename and description of the data. The number of samples to blank after each switch cycle, the sample rate, switch cycle and cycles/integration. The program generates two files. The first is filename.rf1 and the second is filename.rf2. Filename.rf1 contains the configuration data such as sample rate, switch cycle, samples/integration, etc. Filename.rf2 contains the raw "streamed" data.

When setting up for a scan the user first sets the thumb-wheel switches and enables the Clock and Switching System. Provisions for reading the thumb-wheel switches were not made or requested so the thumb-wheel positions should be repeated on the computer GUI panel. The total number of A/D conversions (samples) is determined from this data and is used by the program for when to quit sampling, so it is important to set the switches correctly or you will not know how many samples to wait for. Otherwise this data does not affect the collection

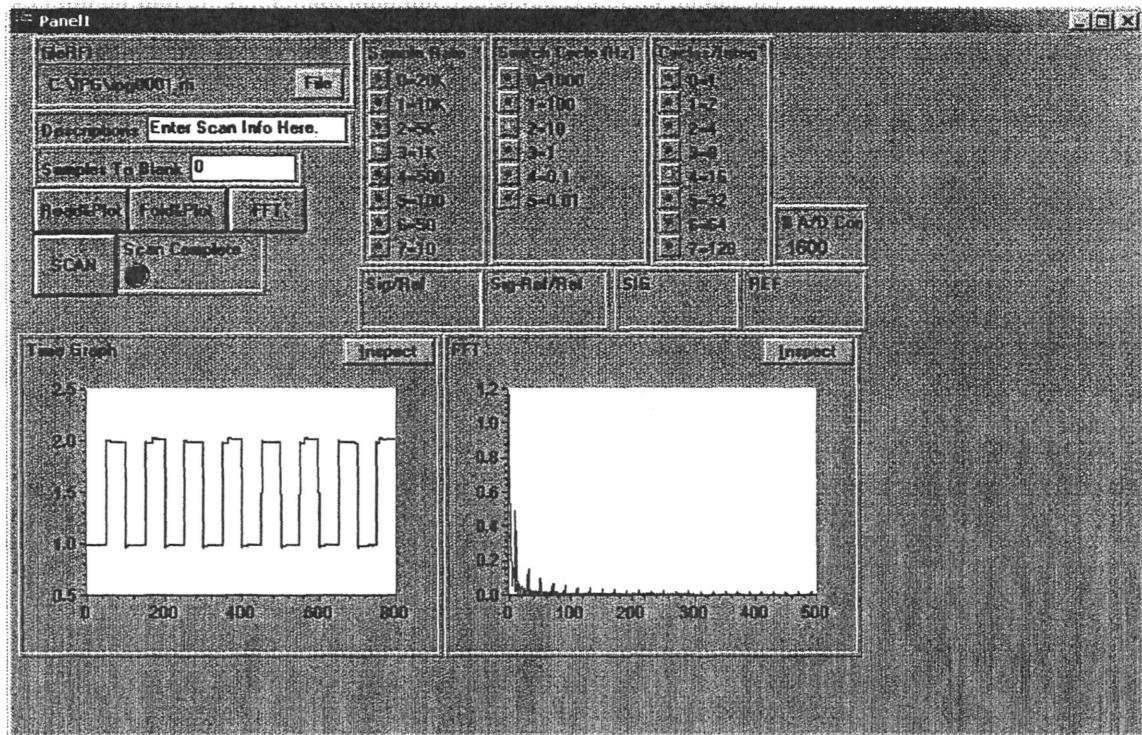
of the data but is used by the plotting and analysis software so it is stored for later reference. The Scan Complete “LED” on the GUI screen will turn green when all the data is collected. (If this LED turns green before the Clock and Switching system LEDs stop switching or if it stays black after the Clock and Switching system stops then you know your thumb-wheel switches do not match your GUI settings.)

The GUI panel allows you to collect, load and plot / analyze data which has just been collected or data which was collected sometime in the past. When you specify the filename then press the “Read&Plot” or “Fold&Plot” or “FFT” switches the computer reads the associated filename and performs the appropriate analysis on the data. A picture of the GUI panel is shown below in figure 2.

“Read&Plot” allows the user to plot out all the data collected. The X-axis is sample number and the Y-axis is the amplitude in volts.

“Fold&Plot” averages each “cycle” of data and plots one cycle of the average of all the data.

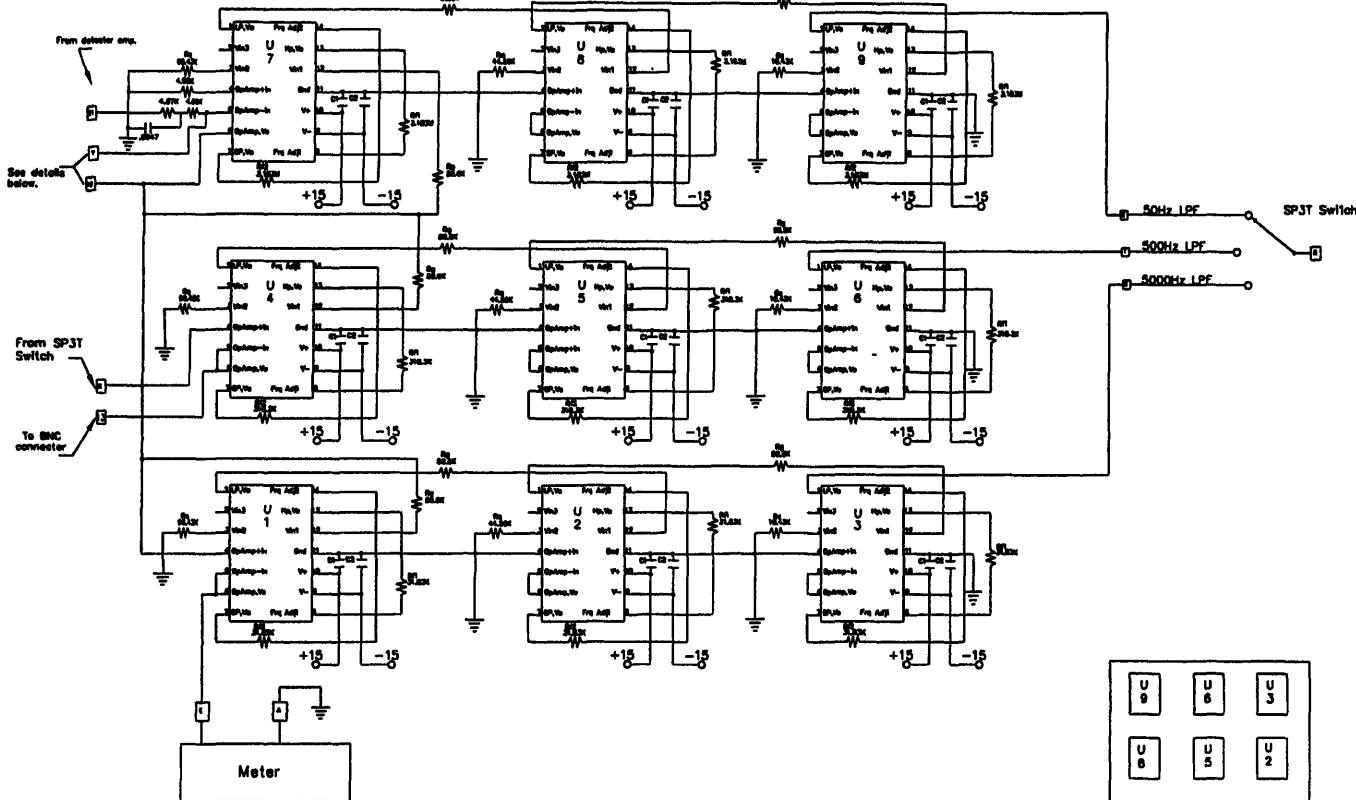
“FFT” performs an FFT on the data. The X-axis is Hz and the Y-Axis is power. The boxes labeled “Sig/Ref”, “Sig-Ref/Ref”, “SIG” and “REF” are the accumulative counts of SIG and REF and the associated equation on that data. It is only filled in when you do the scan, not during post processing.



**Figure 2**

## **Instructions to run the IPG RFI computer software. (Appendix A)**

1. Turn on the computer and associated equipment.
2. Log on to the computer.
3. Double click on the IPG RFI Test Software Icon.
4. Click on the “File” button in the “fileRFI” box.
5. Enter the filename you wish to store your data to or read data from.
6. Fill in the descriptions entry.
7. Set the thumb-wheel switches on the metal box beside the computer to the desired settings and the “Enable/Stop” switch to “Enable”.
8. Set the Radio Buttons on the IPG RFI Panel to what you set the thumb-wheel switches to.
9. Press “SCAN” when you are ready to collect data. (Data is presently only collected on input channel 0.)
10. The Scan Complete light will be black during the scan and it will turn to green when the scan is complete.
11. The “Time Graph” will be plotted when the Scan is complete.
12. The data is now in the file you selected in step 5 above.
13. Press “Read&Plot” to read data from the file and plot it in the “Time Graph Window”.
14. Press “Folt&Plot” to fiod each cycle from the selected file into one cycle and plot the resulting “average” cycle.
15. Press “FFT” to run and plot the FFT on the data in the file selected.



100K  
W  
V  
Y  
X  
Z  
U  
B  
C  
D  
E  
F  
G  
H  
I  
J

Use shielded pair  
and ground to chassis.

+15 → C → 22uF, 15V  
Gnd → C → 22uF, 15V  
-15 → C → 22uF, 15V

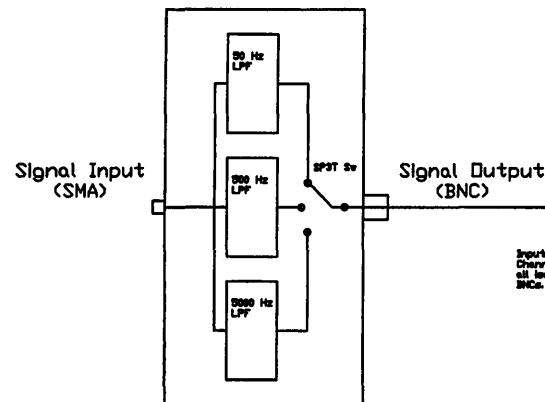
NOTE: C1, C2 are  
0.1uf. Each are  
shown nine places  
in the schematic.  
Place these as  
close to the IC's  
as possible.



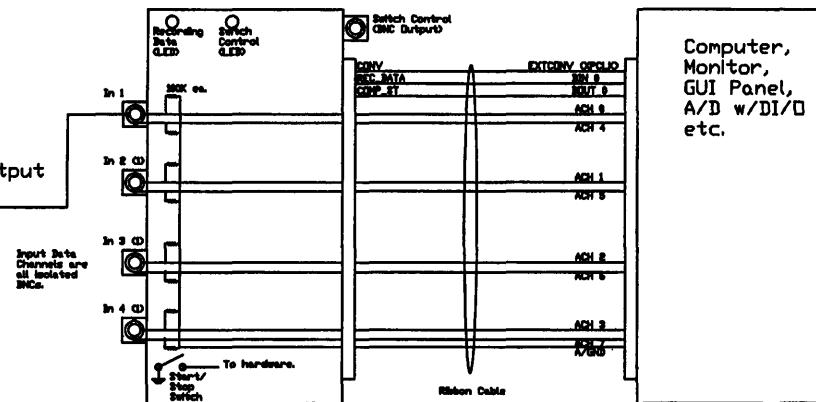
NATIONAL RADIO ASTRONOMY OBSERVATORY		CONTINUUM UNITS CONTINUUM SYSTEM
P.O. BOX E, GREEN BANK, WEST VIRGINIA, 24464		Filter Amplifier
DESIGNED BY	DRAINED BY	REVISED BY
R.Lecocq	J.McMahon	R.Lecocq
DATE	03/03/1999	DATE
REVIEWED BY	DOUGLAS CARD	REVIEWED BY
FILE: schematic.dwg		FILE: schematic.dwg
MATERIAL: 1 OF 1		MATERIAL: 1 OF 1
REVISION: 1		REVISION: 1
XXXXXX		XXXXXX

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

Continuum  
System  
Filter  
Amplifier  
(Lacasse)



Continuum  
System  
Clock and  
Switching Hardware  
(Schiebel)



Continuum  
System &  
Computer &  
Hardware  
(Weadon)

	IPG Continuum System			
	SIZE	FSCM NO.	DWG NO.	REV
Dwg: T. Weadon		XXXXXXXXXX		
Date: 8/29/03	SCALE N/A		SHEET 1/1	

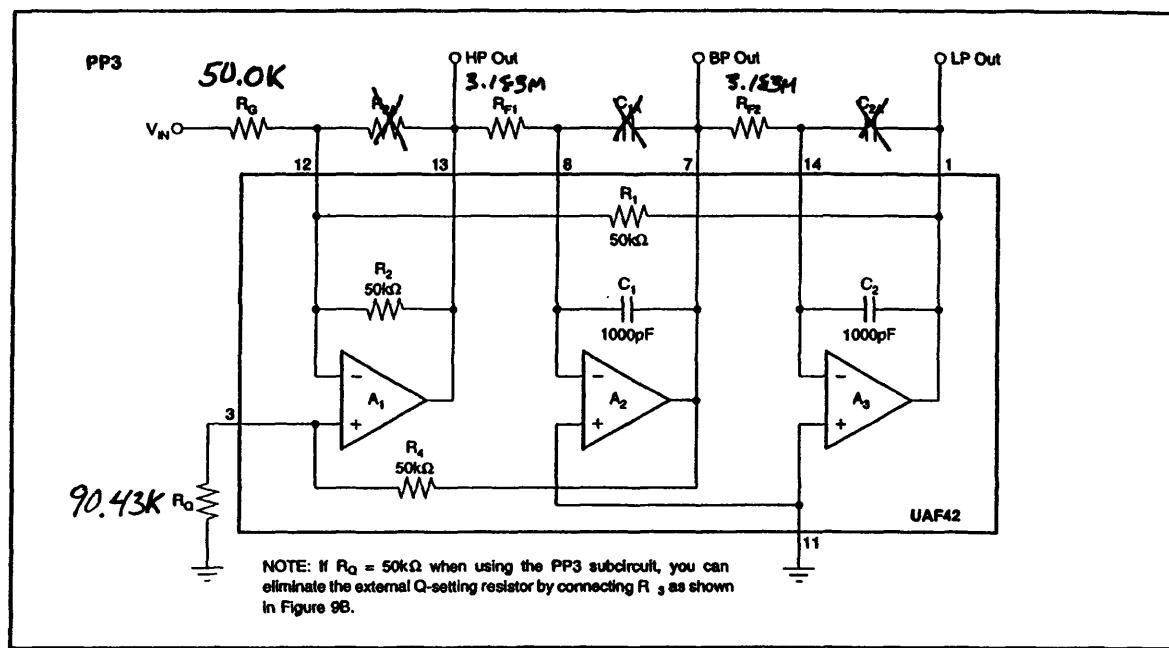


FIGURE 9A. PP3 Inverting Pole-Pair Subcircuit.

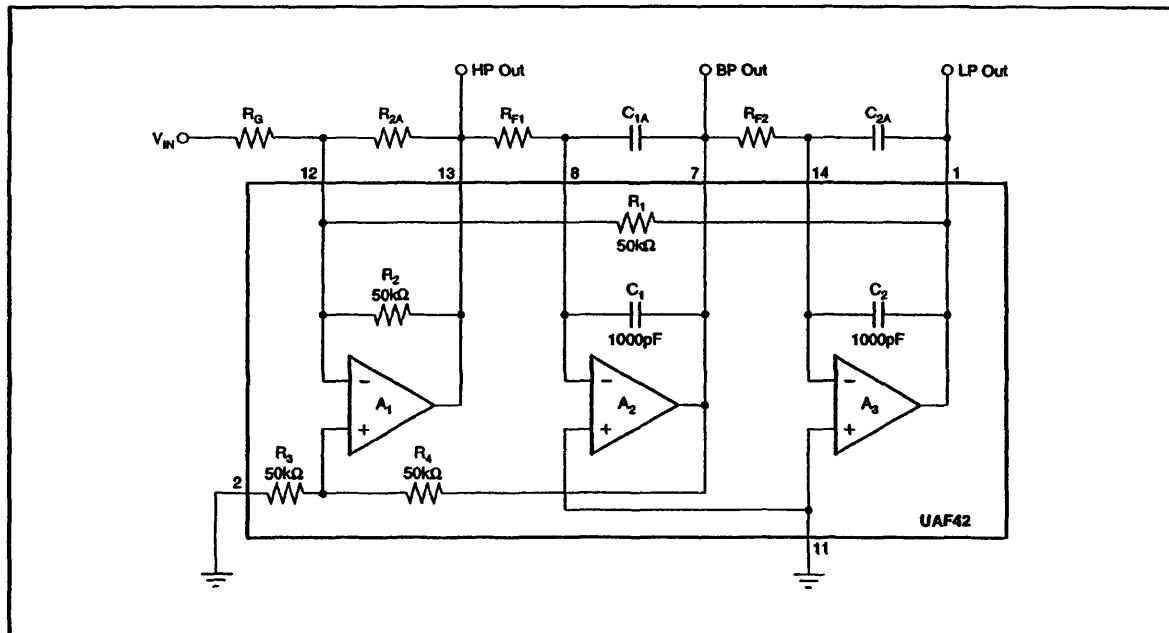


FIGURE 9B. Inverting Pole-Pair Subcircuit Using  $R_3$  to Eliminate External Q-Setting Resistor  $R_g$ .

### UAF42 Filter Component Values

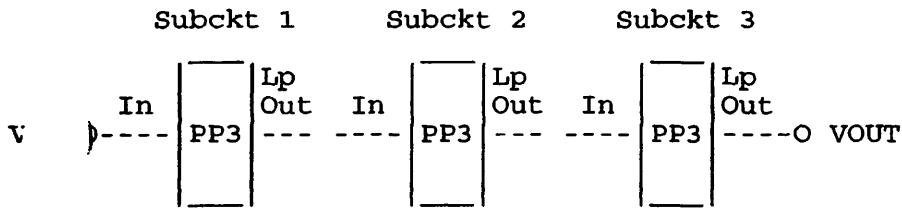
R **Type** : Lowpass  
Type : Butterworth

**Topology:** Inverting

f-3dB : 50.00Hz  
Order n : 6  
Resistors : exact

	Subckt C ext	fo Rp	Q Cp	fz Rz1	RF1,2 Rz2	RQ Rz3	RG Ckt-gain	R2A
Sub Ckt 1	PP3	50.00Hz	517.6m	----	3.183M	90.43k	50.00k	----
Sub Ckt 2	PP3	50.00Hz	707.1m	----	3.183M	44.59k	50.00k	----
Sub Ckt 3	PP3	50.00Hz	1.932	----	3.183M	10.43k	50.00k	----

### Filter Block Diagram



Build this filter by connecting filter subcircuits in order as shown in the 'Filter Block Diagram' above. See Application Bulletin AB-035 for detailed schematics of subcircuits. When no value is shown for a component in the 'Filter Component Values' table, omit the component.

Passband gain : 1.00 V/V (0 dB)  
Max Input : 10.00 V (Vs=+-15V)

Freq(Hz)	Gain (dB)	Vout * Insert 1VPP
10	0	1
40	-3	.97
50	-2.85	.72
60	-9.6 db	.33
70	-17	.14
80	-24	.063
90	-30	.032
100	-36	.016

$$\frac{V_{out}}{V_{in}} = 20 \log \frac{V_{out}}{V_{in}}$$

$$20 \log \frac{V_o}{V_{in}} = n \text{ dB}$$

$$\log \frac{V_o}{V_{in}} = \frac{n}{20}$$

$$\frac{V_o}{V_{in}} = 10^{\frac{n}{20}}$$

$$^* V_{in} = 1 \text{ volt (p-p or RMS)}$$

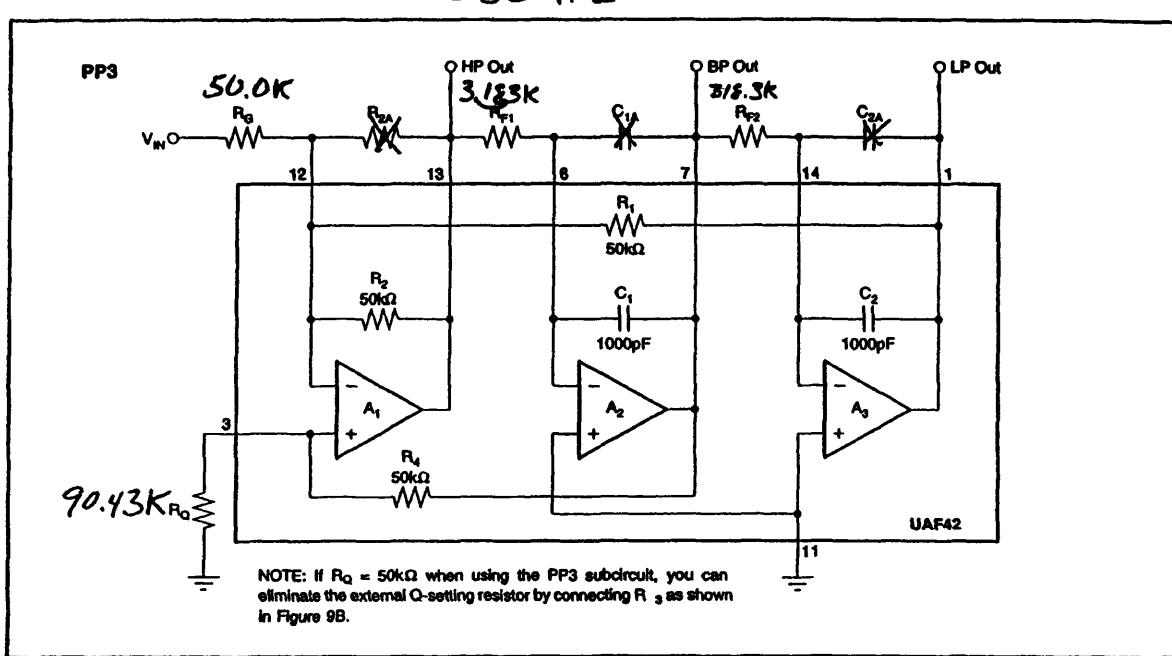


FIGURE 9A. PP3 Inverting Pole-Pair Subcircuit.

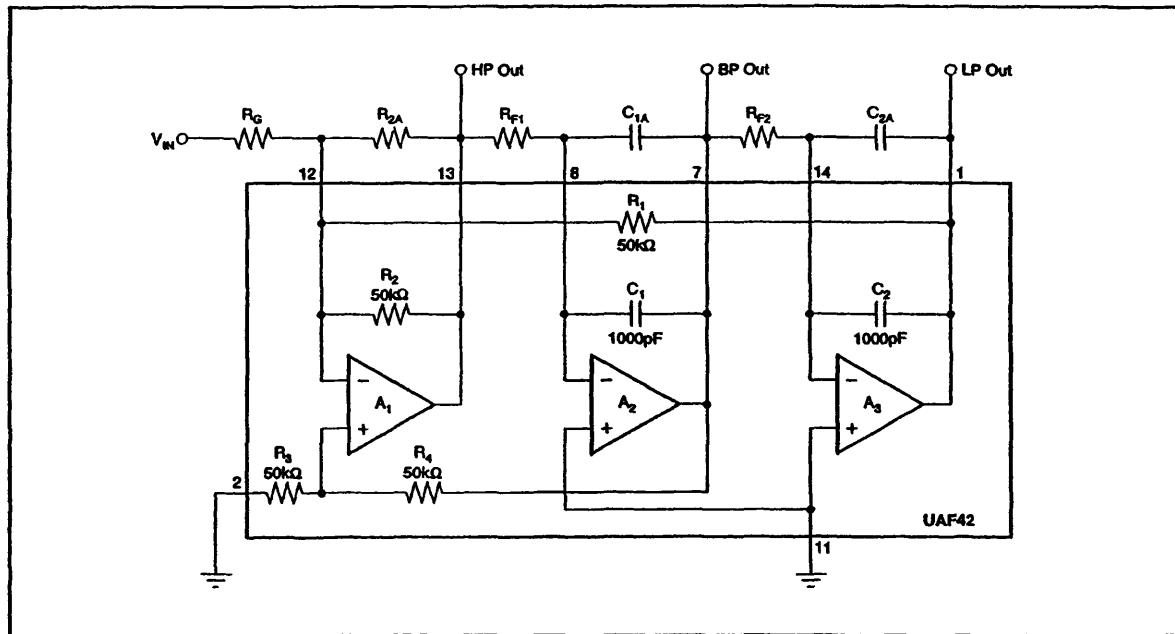


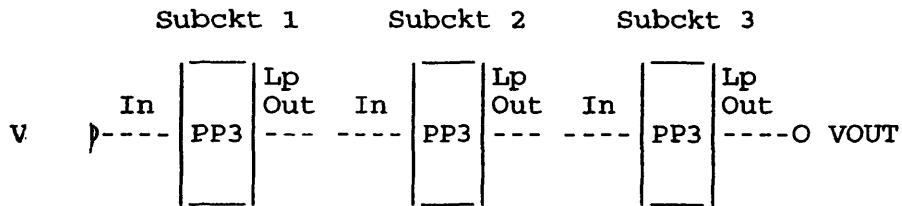
FIGURE 9B. Inverting Pole-Pair Subcircuit Using  $R_3$  to Eliminate External Q-Setting Resistor  $R_G$ .

### UAF42 Filter Component Values

R. Inse: Lowpass  
 Type : Butterworth      Topology: Inverting      f-3dB : 500.0Hz  
 Order n : 6  
 Resistors : exact

	Subckt C ext	fo Rp	Q Cp	fz Rz1	RF1, 2 Rz2	RQ Rz3	RG Ckt-gain	R2A
Sub Ckt 1	PP3	500.0Hz	517.6m	----	318.3k	90.43k	50.00k 1.000	----
Sub Ckt 2	PP3	500.0Hz	707.1m	----	318.3k	44.59k	50.00k 1.000	----
Sub Ckt 3	PP3	500.0Hz	1.932	----	318.3k	10.43k	50.00k 1.000	----

Filter Block Diagram



Build this filter by connecting filter subcircuits in order as shown in the 'Filter Block Diagram' above. See Application Bulletin AB-035 for detailed schematics of subcircuits. When no value is shown for a component in the 'Filter Component Values' table, omit the component.

Passband gain : 1.00 V/V (0 dB).  
 Max Input : 10.00 V (Vs=+-15V)

Freq(Hz)	Gain (DB)	Vout/T (acc.)	Vout/T (meas.)
100	0	1	1
400	-0.3	.97	.96
500	-2.85	.72	.69
660	-9.6	.33	.33
700	-17	.14	.13
800	-24	.063	.072
900	-30	.032	.043
1000	-36	.016	.021

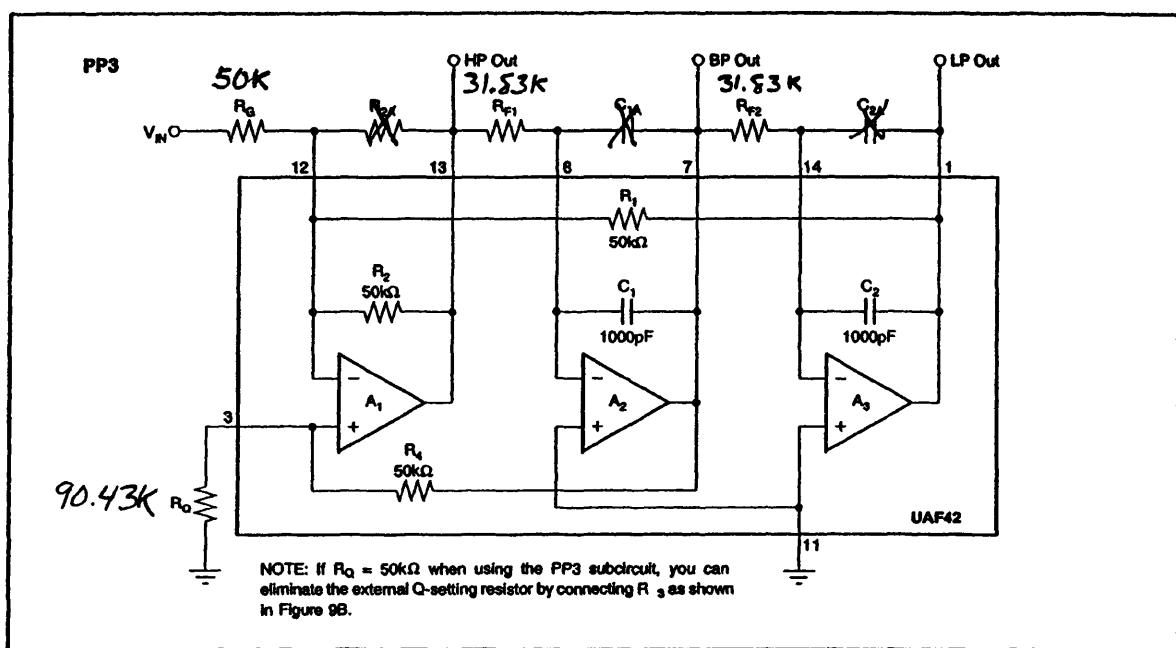


FIGURE 9A. PP3 Inverting Pole-Pair Subcircuit.

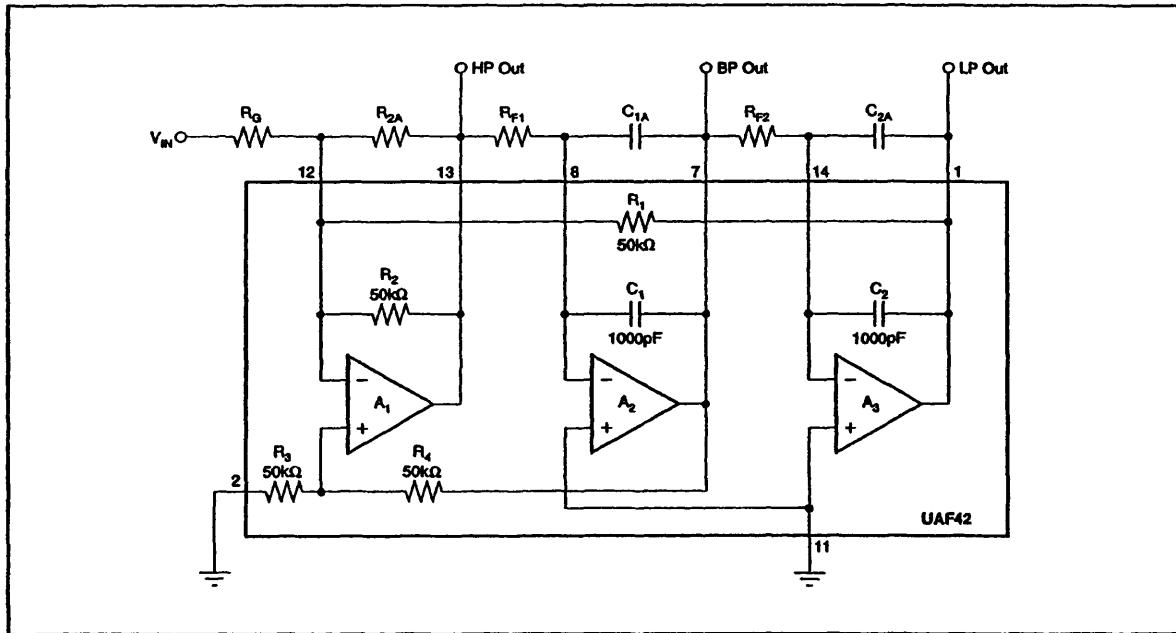


FIGURE 9B. Inverting Pole-Pair Subcircuit Using  $R_3$  to Eliminate External Q-Setting Resistor  $R_g$ .

### UAF42 Filter Component Values

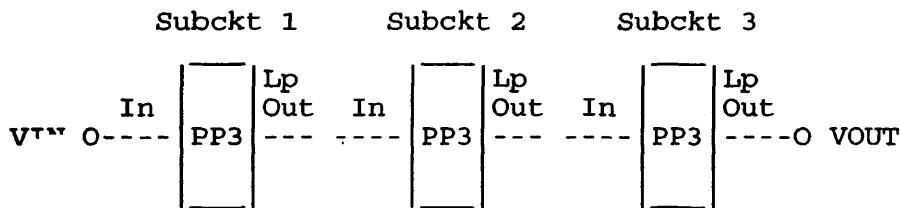
Response: Lowpass  
Type : Butterworth

Topology: Inverting

f-3dB : 5.000kHz  
Order n : 6  
Resistors : exact

	Subckt C ext	fo Rp	Q Cp	fz Rz1	RF1,2 Rz2	RQ Rz3	RG Ckt-gain	R2A
Sub Ckt 1	PP3	5.000kHz	517.6m	----	31.83k	90.43k	50.00k	----
Sub Ckt 2	PP3	5.000kHz	707.1m	----	31.83k	44.59k	50.00k	----
Sub Ckt 3	PP3	5.000kHz	1.932	----	31.83k	10.43k	50.00k	----

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Passband gain : 1.00 V/V (0 dB)  
Max Input : 10.00 V (Vs=+-15V)

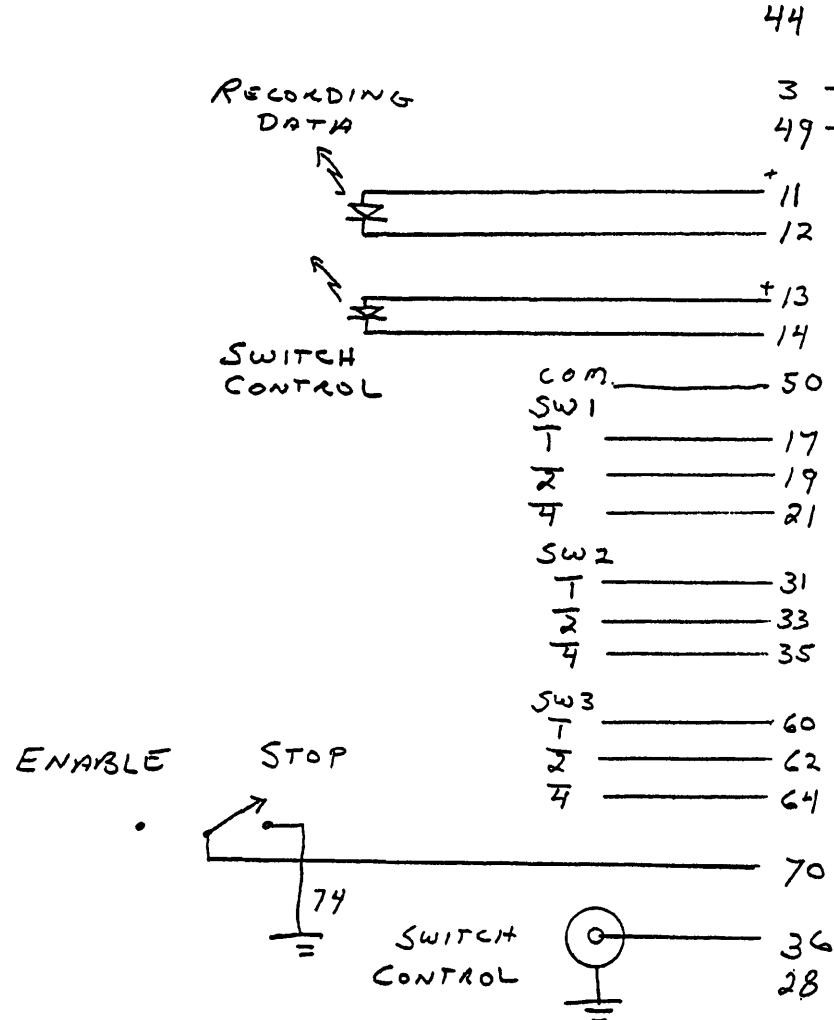
Freq(Hz)	Gain	Vout (V)	Vout (mV)
1000	0	1	1
4000	-3	.97	.96
5000	-2.85	.72	.70
6000	-9.6	.33	.33
7000	-17	.14	.13
8000	-24	.063	.066
9000	-30	.032	.031
10000	-36	.016	.020

# RFI A/D TEST

CARD CONN

50 PIN RIBBON

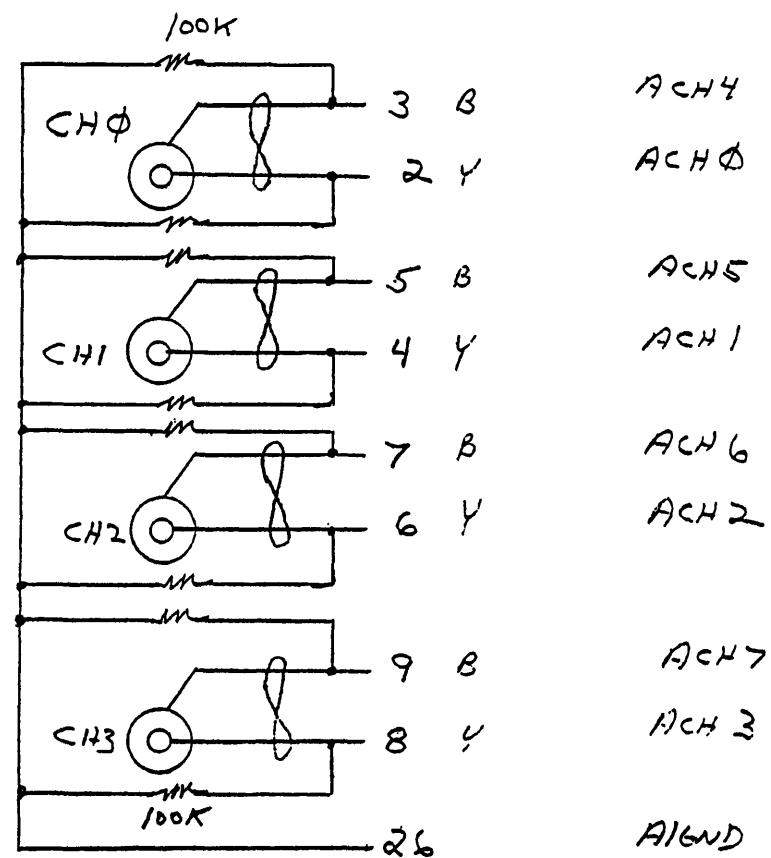
7 - CONV	38 (XPCLK)	EXTCONN
8 - REC - DATA	30	DIN $\emptyset$
54 - COMP - ST	34	DOUT $\emptyset$



44 NOT AVAILABLE NOW

3 — GND	27
49 — GND	49

1MHz
DGND
DGND
DGND



ISOLATED BNC'S

5/26/98

IN SWITCHING TO A KIEHLY A/D HAVE TO  
GENERATE A 1MHZ CLOCK SINCE ONE IS  
NOT AVAILABLE FROM THE A/D. HAVE TO ADD TWO  
CHIPS U31 + U32.

U31 LS19C

1 C40	14 B40
2 41	13 41
3 42	12 42
4 43	11 43
5 44	10 44
6 45	9 45
7 C4C	8 B4C

U32 OSC

1 C49	14 B49
2 50	13 50
3 51	12 51
4 52	11 52
5 53	10 53
6 54	9 54
7 C55	8 B55

ADD

U31-14 TO +5  
U31-7 TO GND

ADD

B40 - B43V  
C4C - B47G

U32-14 TO +5  
U32-7 TO GND

B49 - B51V  
C55 - B55G

U31-1 TO U31-13  
U31-1 TO U30-4

C40 - B41  
C40 - L4C

U31-12 TO U31-8

B42 - B4C

U32-8 TO U31-6

B55 - C45

REMOVE

U5-1 TO PIN 44

REMOVE

C23 - A44

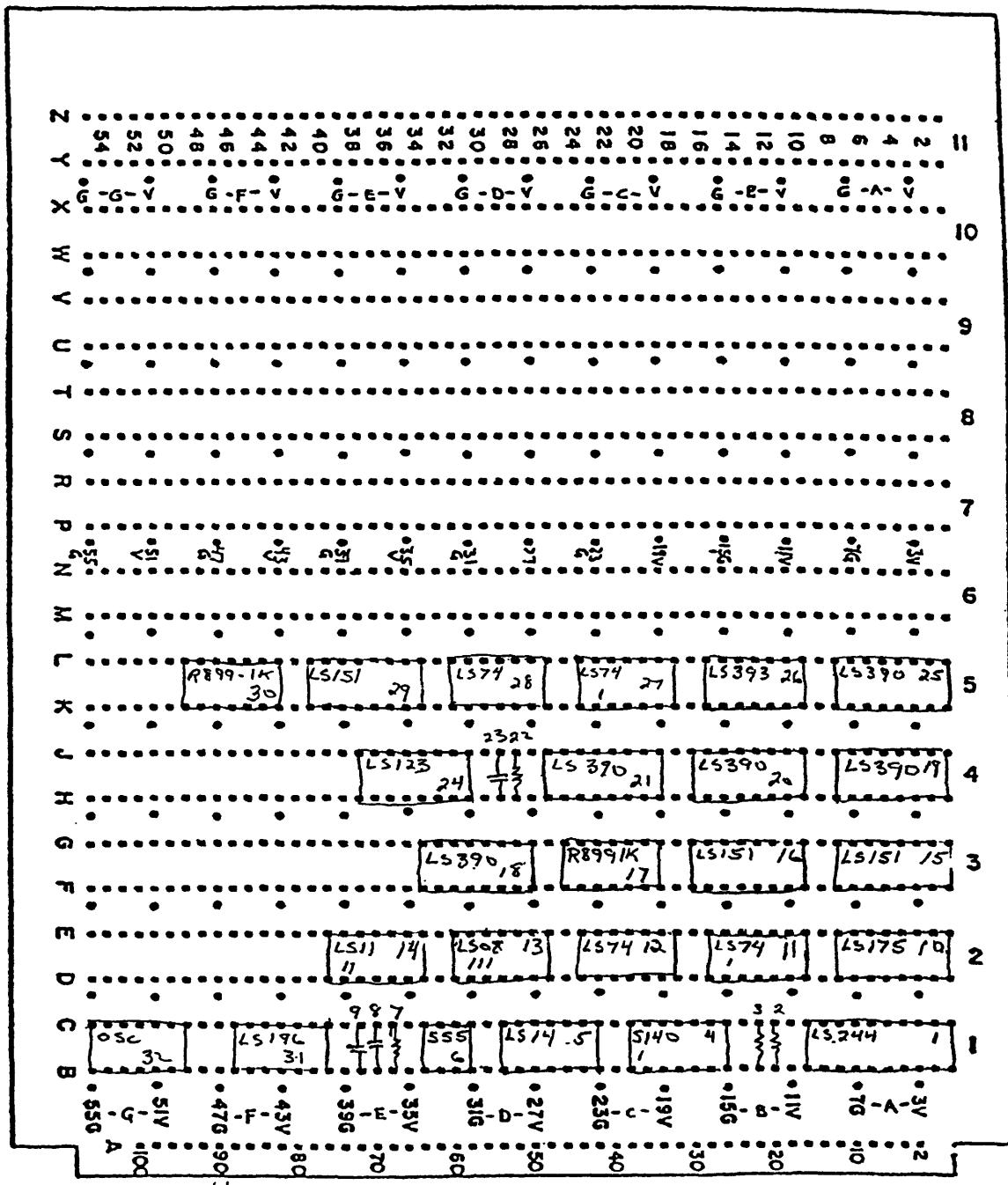
ADD

U5-1 TO U31-5

ADD

C23 - C44

RFI TEST A/D CONTROL



4	S140	1	U2+3	470-2
11	74	/	U7	1M
13	08	111	U8	1M
14	11	11	U9	.01N2
24	123	1	U22	39K
27	74	1	U23	680P1

## STA-1800U I/O Connectors J1 and J2

Pin assignments for I/O connectors J1 and J2 of the STA-1800U screw terminal accessory are shown in Figure B-2.

(User Common Mode) U_CM MD - 01	■ ■	02 - CH00 HI
CH00 LO or CH08 HI - 03	■ ■	04 - CH01 HI
CH01 LO or CH09 HI - 05	■ ■	06 - CH02 HI
CH02 LO or CH10 HI - 07	■ ■	08 - CH03 HI
CH03 LO or CH11 HI - 09	■ ■	10 - CH04 HI
CH04 LO or CH12 HI - 11	■ ■	12 - CH05 HI
CH05 LO or CH13 HI - 13	■ ■	14 - CH06 HI
CH06 LO or CH14 HI - 15	■ ■	16 - CH07 HI
CH07 LO or CH15 HI - 17	■ ■	18 - LL GND
ODAC2 (Note 2) - 19	■ ■	20 - ODAC0 (Note 1)
ODAC3 (Note 2) - 21	■ ■	22 - ODAC1 (Note 1)
+15 V - 23	■ ■	24 - -15V
±15 V Return - 25	■ ■	26 - ±15 V Return
D GND - 27	■ ■	28 - GEXT
DI 1 - 29	■ ■	30 - DI 0
DI 3 - 31	■ ■	32 - DI 2
DO 1 - 33	■ ■	34 - DO 0
DO 3 - 35	■ ■	36 - DO 2
DOSTB - 37	■ ■	38 - XPCLK
TGOUT - 39	■ ■	40 - SSHO
MUX 03 - 41	■ ■	42 - TGIN
MUX 05 - 43	■ ■	44 - MUX 04
MUX 07 - 45	■ ■	46 - MUX 06
+5V - 47	■ ■	48 - +5 V
D GND - 49	■ ■	50 - D GND

Notes:

<sup>1</sup> DAS-1701ST-DA, DAS-1702ST-DA, DAS-1702HR-DA,

DAS-1701AO, and DAS-1702AO boards only

<sup>2</sup> DAS-1701ST-DA and DAS-1702ST-DA boards only

Figure B-2. STA-1800U I/O Connectors J1 and J2

