EDTN Memo 223

ADC Characterization

Stephen Wunduke

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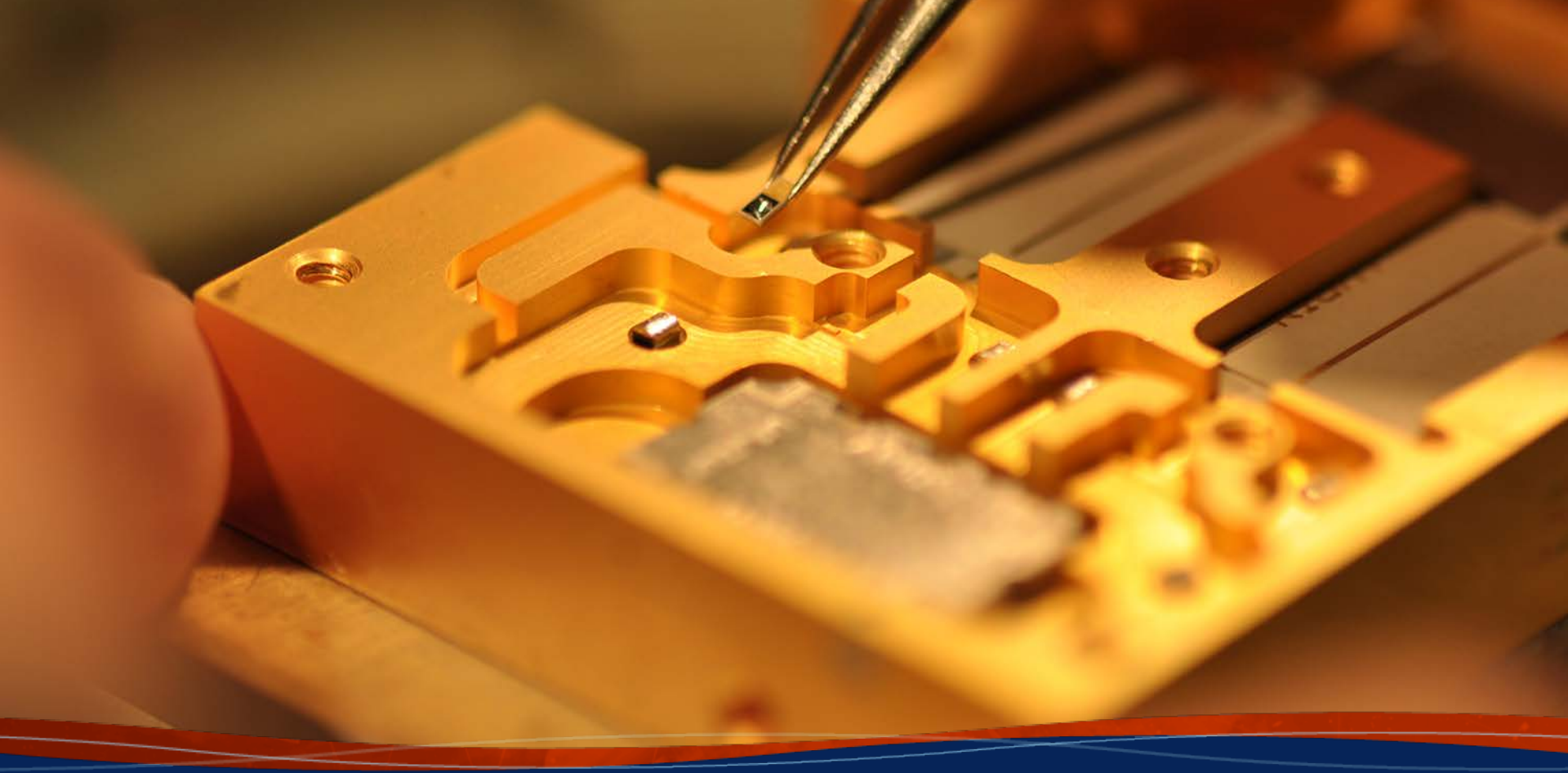

ADC Characterization

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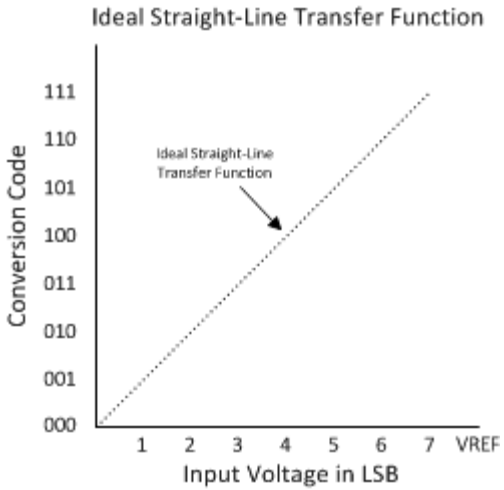
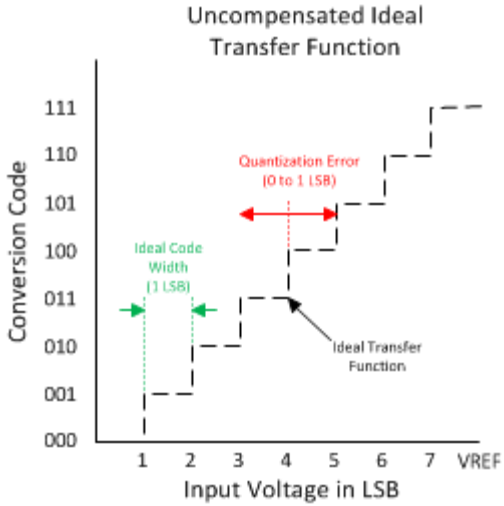
ADC Characterization

Converter Terminology

- **Ideal Transfer Function** – The ideal converter provides for equally spaced digital output codes over the entire analog input range.
  - Each digital output code represents a fractional value of the reference voltage (Vref).





ADC Characterization

Converter Terminology

- **Code Width** – The width of a given output code is the range of analog input voltages for which that code is produced by the converter.
  - Code widths are referenced to the weight of 1 LSB which is defined by the resolution of the converter.
    - 1 LSB = $\frac{Vref}{2^n-1}$, where n is the number of bits of resolution
- **Resolution** – is specified in the number of bits and determines how many distinct output codes (2^n) the converter is capable of producing.
  - Since the first (zero) step and the last step are only one half of a full width, the full-scale range (FSR) is divided into 2^n-1 step widths.

ADC Characterization

Converter Terminology

- **Accuracy** – determines how close the actual digital output is to the theoretically expected digital output for a given analog input.
  - The accuracy of the ADC determines how many bits in the digital output code represent useful information about the signal.
    - No missing codes
    - Offset error
    - Gain error
    - DNL
    - INL

ADC Characterization

Converter Terminology

- **Acquisition Time** - is the time required to charge and discharge the holding capacitor on the front end of an ADC.
  - The holding capacitor must be given sufficient time to settle to the analog input voltage level before the actual conversion is initiated.
  - If sufficient time is not allowed for acquisition the conversion result will be inaccurate.

- **Aperture Error** – is caused by the uncertainty in the time at which the sample/hold goes from sample mode to hold mode.
  - This variation is typically caused by noise on the clock
    - Jitter
    - Slew Rate

ADC Characterization

Converter Terminology

- **Conversion Time** - is the time required to obtain the digital result after the analog input is disconnected from the holding capacitor
  - Usually specified in ADC clock cycles and the minimum period for the clock is specified to obtain the specified accuracy for the ADC.

ADC Characterization

Converter Terminology

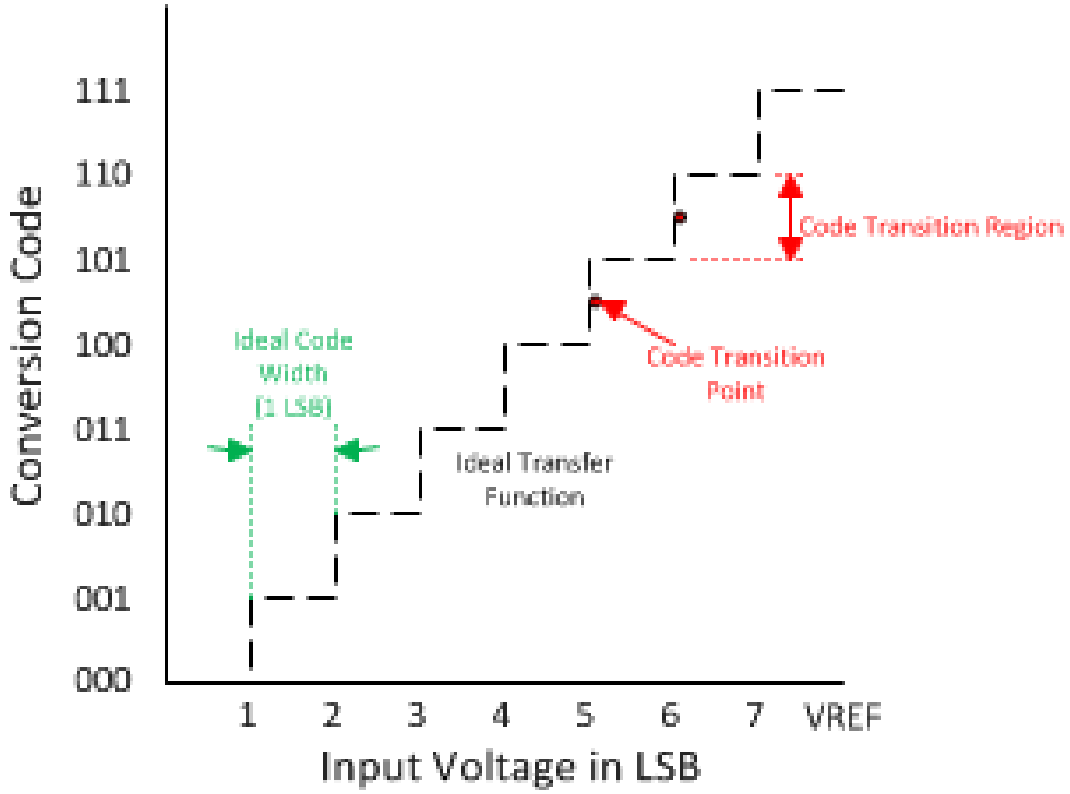
- **Code Transition Points** – the transition points of the ADC are the analog input voltages at which the output code switches from one code to another.
  - For the ideal ADC it is the analog input level for which the probability of producing either output code is 50% and would occur at distant, evenly spaced locations.
  - The code transition points must be accurately determined, since the error specifications for the ADC are derived from them.

- **Code Transition Region** – the analog range that produces either code and can be expressed statistically by averaging the results of many conversions.

ADC Characterization

Converter Terminology

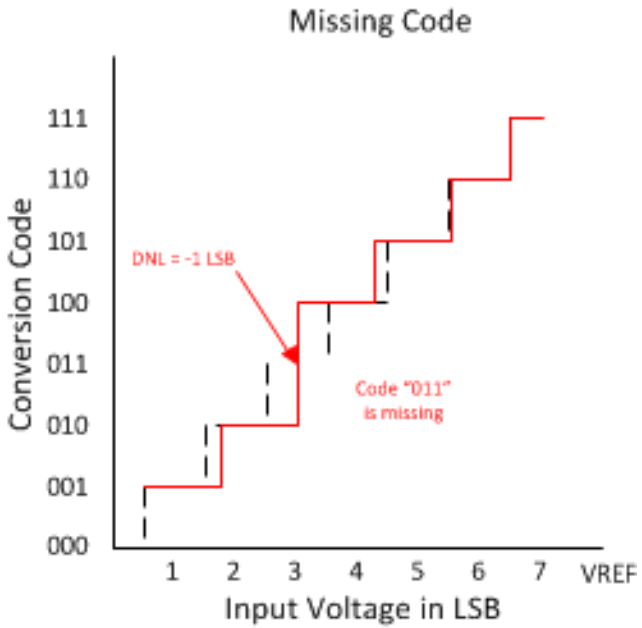
- Code Transition Point and Region



ADC Characterization

Converter Terminology

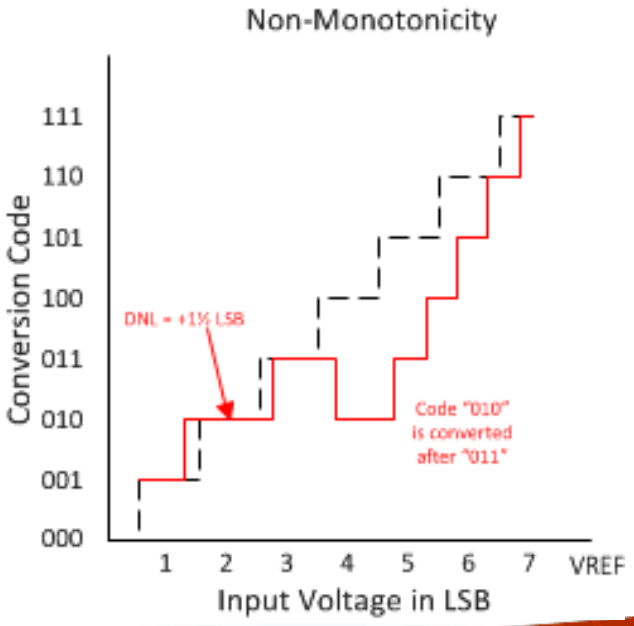
- **Missing Codes** - An ADC has missing codes if a small change in voltage causes a change in result of two codes, with the intermediate code never being set.
  - A DNL of –1.0 LSB indicates the ADC has missing codes.



ADC Characterization

Converter Terminology

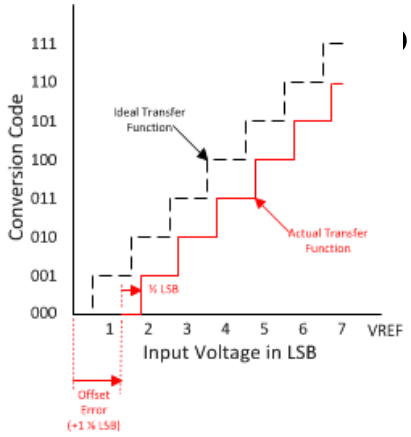
- **Monotonicity** - An ADC is monotonic if it continually increases conversion result with an increasing voltage (and vice versa).
  - A non-monotonic ADC may give a lower conversion result for a higher input voltage, which may also mean that the same conversion may result from two separate voltage ranges.



ADC Characterization

DC Specifications

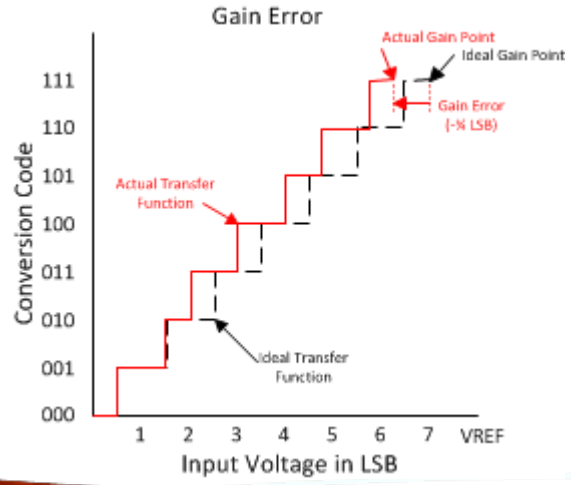
- **Offset Error** – the deviation of the actual first code transition to the expected code transition of the ideal converter. Also referred to as "Zero Scale Error".
  - Offset error has the effect of shifting the entire transfer function to the "right" or to the "left" and represents a deviation of the code transition points across all output codes.
  - Once the offset error has been determined, it can be subtracted from the digita) that the correct conversion result is obtained.



ADC Characterization

DC Specifications

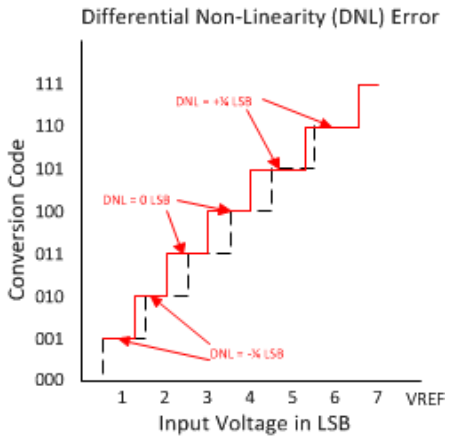
- **Gain Error** – the deviation of the location of the actual last code transition to the expected last code transition of the ideal converter. Also known as "Full Scale Error"
  - Determines the amount of deviation from the ideal slope of the ADC transfer function.
  - The offset error must first be measured and subtracted from the code result before utilizing gain error.



ADC Characterization

DC Specifications

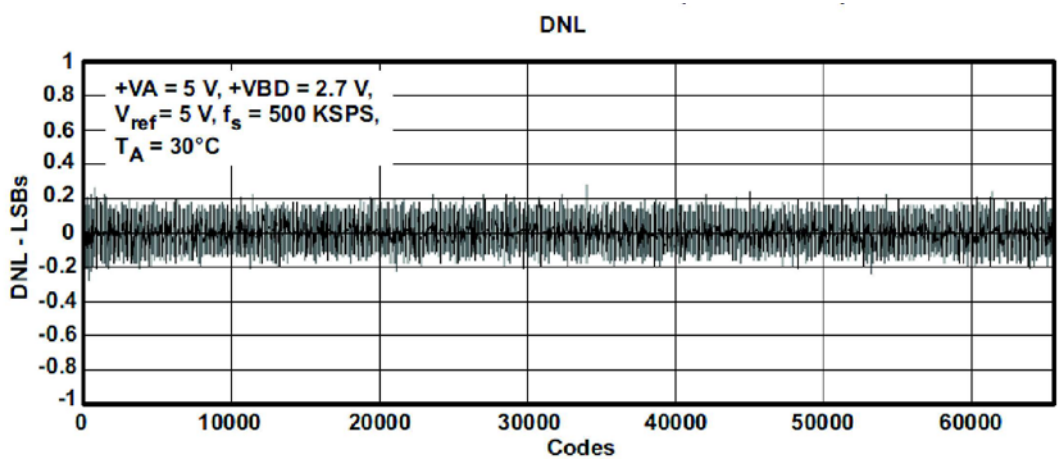
- **Differential Nonlinearity (DNL)** – specifies the deviation between actual step-size to idea step-size observed for each ADC output code.
  - DNL is determined by subtracting the locations of successive code transition points after compensating for an offset and gain errors.
    - A positive DNL implies that a code is longer than the ideal code width.
    - A negative DNL implies that a code is shorter than the ideal code width.



ADC Characterization

DC Specifications

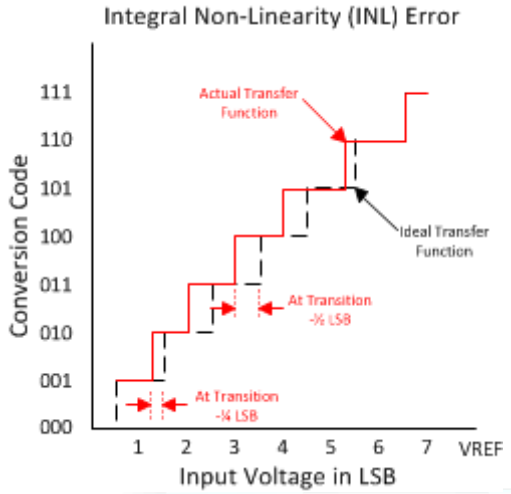
- **<u>Differential Nonlinearity (DNL)</u>** – value is usually specified in units of LSB's.



ADC Characterization

DC Specifications

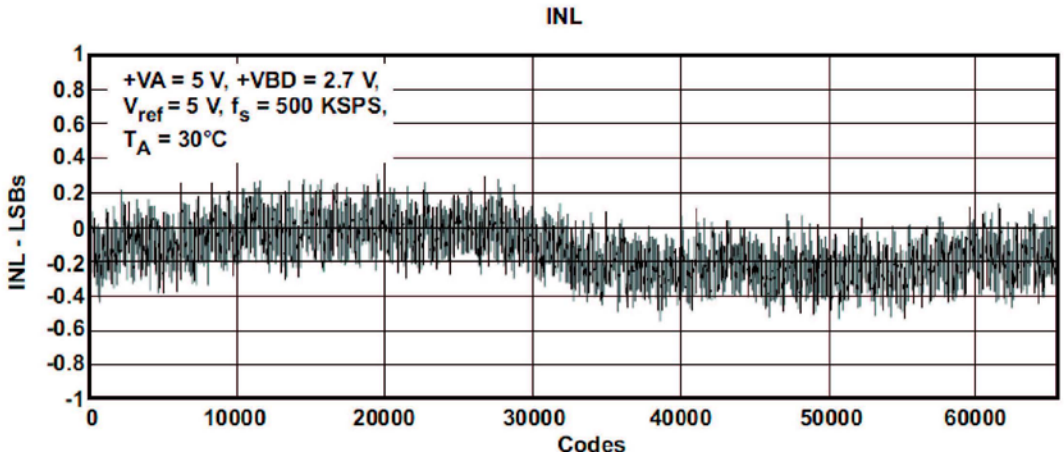
- **Integral Nonlinearity (INL)** – specifies how much the overall transfer function deviates from a linear response.
- INL is the distance of the actual code centers in the ADC from the ideal code centers
  - Tells the designer the best accuracy that the ADC will provide after calibrating for offset and system gain errors.
  - If all code centers "land" on the idea line, the INL is zero.



ADC Characterization

DC Specifications

- **Integral Nonlinearity (INL)** – usually specified in units of LSB's.



ADC Characterization

DC Specifications

- **Absolute Error** – is the sum of the offset, gain, and INL errors and is also called the "Total Unadjusted Error (TUE)".
  - This is an indication of the ADC's worst RMS error without compensating for gain and offset errors.
  - TUE $= \sqrt{\left((offset\ error)^2 + (gain\ error)^2 + (DNL)^2 + (INL)^2\right)}$

ADC Characterization

DC Specifications

- In addition to the ADC specific DC parameters, the following measurements are needed to complete the DC specifications for the converter.
  - Power Consumption (IDD, IDDQ)
  - Input Voltage Threshold (VIL, VIH)
  - Output Voltage Level (VOL, VOH)
  - Output Short Circuit (IOS)
  - Input Leakage (IIL, IIH)
  - Rise Time/ Fall Time

- Temperature range for testing serial ADC?

ADC Characterization

DC Specifications

- The DC Specifications are listed in a typical datasheet as follows:

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, duty cycle stabilizer (DCS) enabled, unless otherwise noted.

Table 1.

		AD9643-170			AD9643-210			AD9643-250			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	14			14			14			Bits
ACCURACY											
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error	Full			±10			±10			±10	mV
Gain Error	Full			+2/−6			+3/−5			±4	%FSR
Differential Nonlinearity (DNL)	Full			±0.75			±0.75			±0.75	LSB
	25°C		±0.25			±0.25			±0.25		LSB
Integral Nonlinearity (INL)[1]	Full			±1.8			±2			±3.5	LSB
	25°C		±1.5			±1.5			±1.5		LSB
MATCHING CHARACTERISTIC											
Offset Error	Full			±13			±13			±13	mV
Gain Error	Full			±2.5/ +3.5			−2/ +3.5			−2.5/ +3.5	%FSR
TEMPERATURE DRIFT											
Offset Error	Full		±5			±5			±5		ppm/°C
Gain Error	Full		±70			±80			±100		ppm/°C
INPUT REFERRED NOISE											
VREF = 1.75 V	25°C		1.33			1.33			1.33		LSB rms
ANALOG INPUT											
Input Span	Full		1.75			1.75			1.75		V p-p
Input Capacitance[2]	Full		2.5			2.5			2.5		pF
Input Resistance[3]	Full		20			20			20		kΩ
Input Common-Mode Voltage	Full		0.9			0.9			0.9		V
POWER SUPPLIES											
Supply Voltage											
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current											
I_{AVDD}[1]	Full		196	250		217	265		256	275	mA
I_{DRVDD}[1]	Full		145	160		160	185		180	210	mA
POWER CONSUMPTION											
Sine Wave Input (DRVDD = 1.8 V)	Full		614			680			785		mW
Standby Power[4]	Full		90			90			90		mW
Power-Down Power	Full		10			10			10		mW

ADC Characterization

AC Specifications

- The AC specifications for the converter inform the designer of how much noise and distortion has been introduced into the sampled signal and the accuracy of the converter for a given frequency and sampling rate.

- Dynamic specifications are usually expressed in the frequency domain using the Fast Fourier Transform (FFT).

ADC Characterization

AC Specifications

- **Signal-to-Noise Ration (SNR)** – is defined as the ratio of the RMS level of the input signal to the RMS value of the root-sum-square of all noise components in the FFT analysis, except for the DC components and harmonics of the input.
  - In practice, only the first several harmonics of the input are used for the calculation of the SNR, since the higher order harmonics are usually insignificant when compared to the FTT of the noise floor.

- Ideal SNR = 6.02N + 1.76 dB, where N is the number of bits
- Actual SNR = $20\log_{10}(\frac{signal_{rms}}{total\_noise_{rms}})$

ADC Characterization

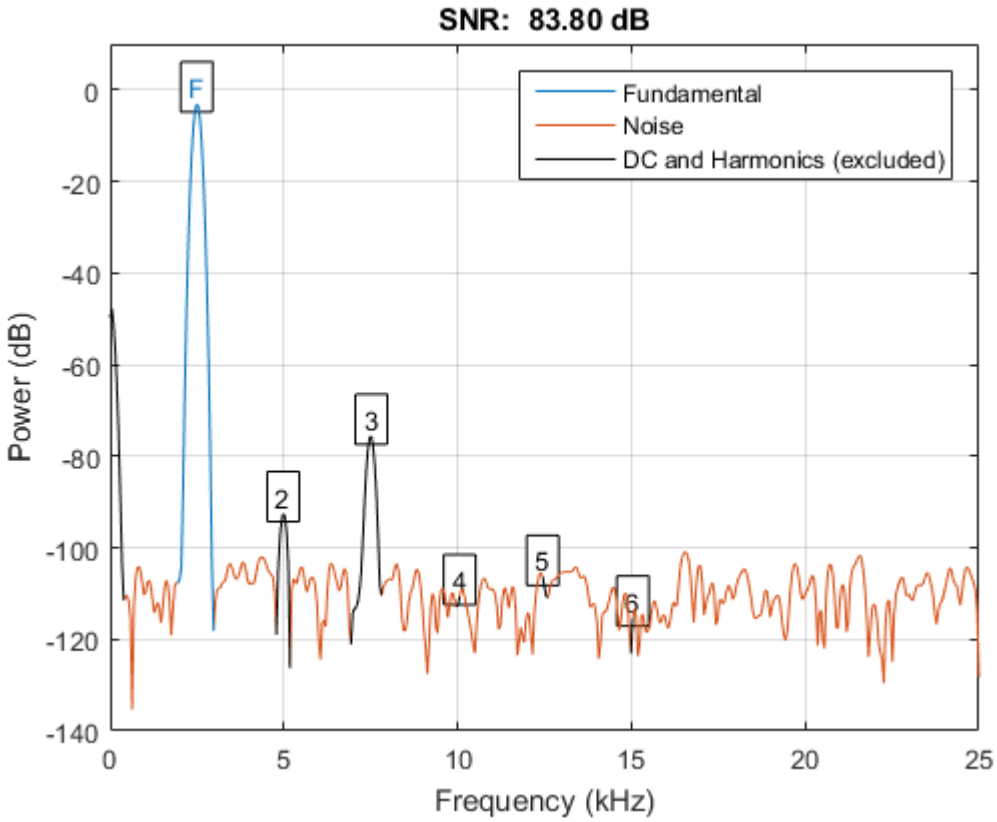
AC Specifications

- **SNR for an ADC is a contribution of noise from many sources:**
  - Quantization noise
  - Thermal Noise
  - Power supply hum
  - RF Interference
  - Switching noise
  - Jitter Noise
    - Clock Input Jitter
    - ADC Aperture Jitter

ADC Characterization

AC Specifications

- **Example ADC spectrum plot**



ADC Characterization

AC Specifications

- **Signal-to-Noise Ratio plus Distortion (SINAD) –** is measured with a sinusoidal input near full-scale applied to the converter.
  - The SINAD is found by computing the ration of the RMS level of the input signal to the RMS value of the root-sum-square of all noise and distortion components in the FFT analysis, except for the DC component.
  - The SINAD is a useful measure of converter performance, because it includes the effect of all noise, distortion, and harmonics introduced by the ADC.

ADC Characterization

AC Specifications

- **Effective Number of Bits (ENOB)** – The effective number of bits (ENOB) is a way of quantifying the quality of an analog to digital conversion. A higher ENOB means that voltage levels recorded in an analog to digital conversion are more accurate.
- Noise contributes directly to a degradation of the SNR of the ADC. A non-linearity results in harmonics which also reduce the achieved SNR. Thus, a 12 bit ADC might be specified with an ENOB of 10.5. This means that even though the ADC outputs 12 bits, the achieved SNR corresponds to that of an ideal ADC with 10.5 bits.
- ENOB = $\frac{(SINAD - 1.76)}{6.02}$

ADC Characterization

AC Specifications

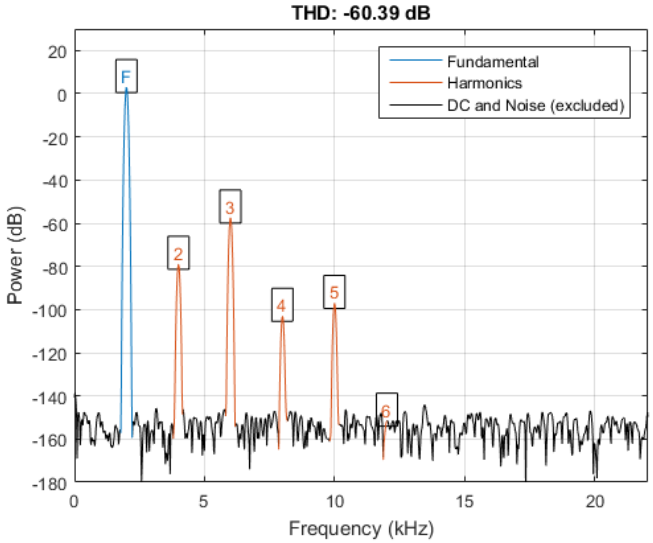
- **Harmonic Distortion –** is the ratio of the RMS signal to the RMS value of the n^{th} harmonic in question.
  - $\boldsymbol{d_n = 20log_{10}\left(\frac{V_{rms,n}}{V_{rms,total}}\right) dB}$

ADC Characterization

AC Specifications

- **Total Harmonic Distortion (THD) –** is the ratio of the RMS value of the signal to the root-sum-square of it's harmonics, generally only the first 5 harmonics are significant.

- $$d_n = 20 \log_{10} \left[\frac{\sqrt{(V_{RMS,2})^2 + (V_{RMS,3})^2 + (V_{RMS,4})^2 + (V_{RMS,5})^2}}{V_{RMS,total}} \right] dB$$



ADC Characterization

AC Specifications

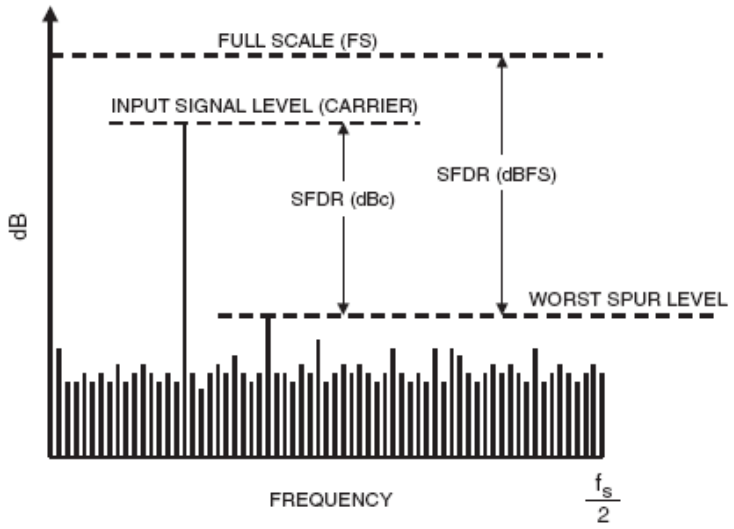
- **Total Harmonic Distortion plus Noise (THD + N) –** is the ratio of the RMS value of the input signal to the mean value of the root-sum-square of it's harmonics plus all noise components, excluding DC.
  - The bandwidth over which noise is measured must be specified and is usually DC -> fs/2

- ***THD + N = SINAD***

ADC Characterization

AC Specifications

- **Spurious Free Dynamic Range (SFDR) -** is defined as the ratio of the RMS signal amplitude to the RMS value of the *peak spurious spectral content* (measured over the entire first Nyquist zone, DC to fs/2).
  - SFDR is generally plotted as a function of signal amplitude and may be expressed relative to the signal amplitude (dBc) or the ADC full-scale (dBFS)



ADC Characterization

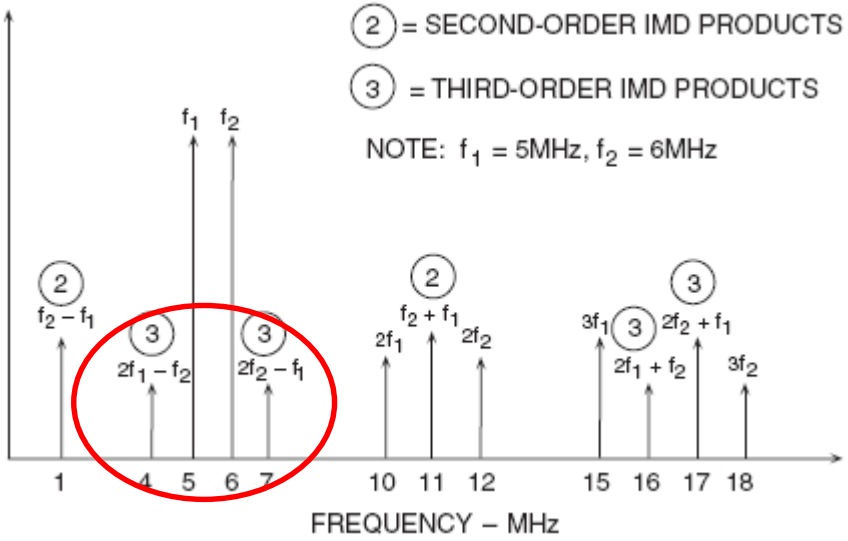
AC Specifications

- **Two-Tone Intermodulation Distortion (IMD) -** Two-tone IMD is measured by applying two spectrally pure sine waves to the ADC at frequencies f1 and f2, usually relatively close together. The amplitude of each tone is set slightly more than 6 dB below full scale so that the ADC does not clip when the two tones add in-phase.

ADC Characterization

AC Specifications

- **<u>Two-Tone Intermodulation Distortion (IMD)</u>**
  - The third-order products 2f2–f1 and 2f1–f2 are close to the original signals and are more difficult to filter.
  - Two-tone IMD refers to these third-order products.



ADC Characterization

AC Specifications

- **Transient Response Test –** Settling time for the ADC to full accuracy after a step in input voltage from zero to full-scale.
- **Overvoltage Recovery Test –** Settling time for the ADC to full accuracy after a step in input voltage outside the full-scale value. Example input of 1.5 V_{fs} to 0.5 V_{fs}.
- **Crosstalk** - The typical measurement is usually where no power is input into the channel of interest and a full power tone is injected into a neighboring 'aggressor' channel.
  - Best approach is two signals of differing strength and frequency are injected into a multi-channel ADC with the outputs analyzed for noise, harmonic and mixed signal components, similar to intermodulation distortion measurements (IMD).

ADC Characterization

AC Specifications

- AC specifications are usually given in a data sheet for several reference frequencies and specific temperatures as shown below.

Parameter[1]	Temperature	AD9643-170 Min	AD9643-170 Typ	AD9643-170 Max	AD9643-210 Min	AD9643-210 Typ	AD9643-210 Max	AD9643-250 Min	AD9643-250 Typ	AD9643-250 Max	Unit
SIGNAL-TO-NOISE-RATIO (SNR)											
f_{IN} = 30 MHz	25°C		72.6			72.6			72.0		dBFS
f_{IN} = 90 MHz	25°C		72.2			72.2			71.6		dBFS
	Full	70.8			70.6						dBFS
f_{IN} = 140 MHz	25°C		71.8			71.3			71.2		dBFS
f_{IN} = 185 MHz	25°C		71.2			70.6			70.6		dBFS
	Full							68.8			dBFS
f_{IN} = 220 MHz	25°C		70.7			69.9			69.9		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)											
f_{IN} = 30 MHz	25°C		71.6			71.5			70.9		dBFS
f_{IN} = 90 MHz	25°C		71.1			71.2			70.5		dBFS
	Full	70.4			69.9						dBFS
f_{IN} = 140 MHz	25°C		70.5			70.1			69.9		dBFS
f_{IN} = 185 MHz	25°C		69.6			69.2			69.4		dBFS
	Full							67.5			dBFS
f_{IN} = 220 MHz	25°C		69.1			68.1			68.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)											
f_{IN} = 30 MHz	25°C		11.6			11.6			11.5		Bits
f_{IN} = 90 MHz	25°C		11.5			11.5			11.4		Bits
f_{IN} = 140 MHz	25°C		11.4			11.4			11.3		Bits
f_{IN} = 185 MHz	25°C		11.3			11.2			11.2		Bits
f_{IN} = 220 MHz	25°C		11.2			11.0			11.1		Bits
WORST SECOND OR THIRD HARMONIC											
f_{IN} = 30 MHz	25°C		−95			−90			−90		dBc
f_{IN} = 90 MHz	25°C		−92			−90			−88		dBc
	Full			−78			−80				dBc
f_{IN} = 140 MHz	25°C		−88			−88			−86		dBc
f_{IN} = 185 MHz	25°C		−83			−87			−85		dBc
	Full									−80	dBc
f_{IN} = 220 MHz	25°C		−83			−85			−85		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)											
f_{IN} = 30 MHz	25°C		95			90			90		dBc
f_{IN} = 90 MHz	25°C		92			90			88		dBc
	Full	78			80						dBc
f_{IN} = 140 MHz	25°C		88			88			86		dBc
f_{IN} = 185 MHz	25°C		83			87			85		dBc
	Full							80			dBc
f_{IN} = 220 MHz	25°C		83			85			85		dBc
WORST OTHER (HARMONIC OR SPUR)											
f_{IN} = 30 MHz	25°C		−98			−95			−94		dBc
f_{IN} = 90 MHz	25°C		−97			−95			−93		dBc
	Full			−78			−80				dBc
f_{IN} = 140 MHz	25°C		−97			−93			−92		dBc
f_{IN} = 185 MHz	25°C		−96			−92			−92		dBc
	Full									−80	dBc
f_{IN} = 220 MHz	25°C		−94			−90			−88		dBc

ADC Characterization

ADC Test Methodologies & Software

- IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters
  - define the main characteristics of the testing procedures, but cannot determine every detail of them.
    - IEEE STD 1241-2000
    - IEEE STD 1057-94
- MATLAB Data Acquisition Toolbox - MathWorks
  - Support for NI Hardware
- ADC Testing Toolbox for MATLAB
  - https://www.mit.bme.hu/projects/adctest/
- ADC Testing Toolbox for LabVIEW
  - Based on MATLAB Toolbox

ADC Characterization

Basic Test Requirements for DC Parameters

- DC characterization of the ADC requires either a static or essentially slow moving input signal to the converter.
- Since we are concerned with determining the code widths, code transition regions, and code transition points a high-precision, programmable voltage source is required.
  - Possible use of a NI System Measurement Unit (SMU)
- A low-jitter, lockable clock generator to minimize jitter effects.
  - Clock Jitter << 1ps
  - Improving the SNR of the ADC can be directly related to aperture jitter.
    - Aperture jitter is ultimately improved by optimizing the slew rate of the clock signal.

ADC Characterization

DC Test Methodology

- As mentioned previously, the code transition points and code widths must be accurately determined, since the error specifications for the ADC are derived from them.
- To accurately determine both, a precision, slow moving ramp signal is input to the ADC and the output codes are recorded. This operation is performed over thousands of iterations to determine offset and gain error using actual value minus ideal.
- The following slide will show an example of calculating DC errors for a 3-bit ADC.

ADC Characterization

DC Error Calculations (Offset Error and Gain Error)

- Example for 3-bit ADC

Transition Code	Ideal Transition (V)	Actual Transition (V)
001	0.05	0.02
010	0.15	0.17
011	0.25	0.2
100	0.35	0.37
101	0.45	0.42
110	0.55	0.50
111	0.65	0.68

(1) Offset Error = (Actual - Ideal) = (0.02V - 0.05V) = -0.03V

Offset Error = -0.03/0.1V per LSB = -0.3 LSB

Offset Error = -0.3LSB

*** Negative Offset Error indicates code transition is shorter than ideal and thus the ideal transfer function is shifted "left".**

(2) Full-Scale Error = (Actual - Ideal) = (0.68V -0.65V) = 0.03V

Full-Scale Error = 0.03/0.1V per LSB = 0.3 LSB

Full-Scale Error = 0.3LSB

(3) Gain Error = LSB = (Last Transition - First Transition)/(2^n-2)

Gain Error = LSB = (0.68V-0.02V)/(2^3-2) = 0.66/6 = 0.11V

LSB = 0.11V

VFS = 2^n * 0.11V = 2^3 * 0.11V = 0.88V (Actual)

VFS = 2^n * 0.10V = 2^3 * 0.10V = 0.80V (Ideal)

(4) Gain = Ideal VFS/Actual VFS = 0.8V/0.88V = 0.91

Gain = 0.91

ADC Characterization

DC Error Calculations (DNL and INL)

- Example for 3-bit ADC

Transition Code	Actual Transition (V)	Width = (Transition [K+1] - Transiition [K])	DNL (LSB)	Normalized DNL	DNL (LSB)
001	0.02	(0.17V - 0.02V = 0.15V	0.15V / 0.11 V per LSB = 1.36	1.36 - 1 = 0.36	0.36
010	0.17	(0.20V - 0.17V = 0.03V	0.03V / 0.11 V per LSB = 0.27	0.27 -1 = -0.73	(-0.73 + 0.36) = -0.37
011	0.20	(0.37V - 0.20V = 0.17V	0.17V / 0.11 V per LSB = 1.55	1.55 -1 = 0.55	(-0.37 + 0.55) = 0.18
100	0.37	(0.42V - 0.37V = 0.05V	0.05V / 0.11 V per LSB = 0.45	0.45 - 1 = -0.55	(-0.55 + 0.18) = -0.37
101	0.42	(0.50V - 0.42V = 0.08V	0.08V / 0.11 V per LSB = 0.73	0.73 -1 = -0.27	(-0.27 + -0.37) = -0.64
110	0.50	(0.68V - 0.50V = 0.18V	0.18V / 0.11 V per LSB = 1.64	1.64 - 1 = 0.64	(0.64 + 0.64) = 0
111	0.68				

DNL = deviation of each actual code wifth from ideal code width

* MAX DNL = -0.73

INL = is the cummulative sum of DNL

* MAX INL = -0.64

ADC Characterization – DC Parameters

Code Density or Histogram Test for DNL and INL

- A code density or histogram test helps determine nonlinearity parameters such a DN and INL. The relative number of occurrences of each distinct digital output code is termed code density.
  - The histogram indicates how many times, or the code density, each different digital code word appears on the ADC output for a given analog input voltage.
  - The best and most utilized method involves using a ramp signal that is sampled and sorted into "bins".
    - Each code "bin" represent a single ADC code output.
    - For an Ideal ADC each "bin" width is equal to 1 LSB width.
    - Real world ADC will have unequal bin widths and you will have different counts of output code per bin.

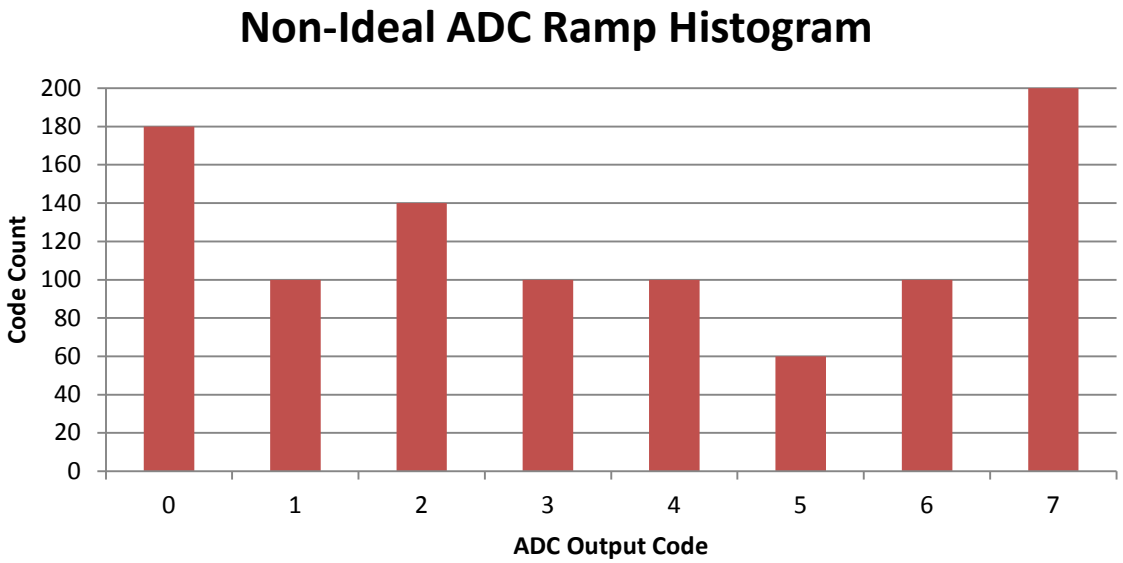
ADC Characterization – DC Parameters

Code Density or Histogram Test for DNL and INL

- For the histogram test, the number of sample depends on the resolution of the ADC, the desired confidence level of he measurement, and the size of the DNL error.
  - For a 0.01 LSB resolution in measurement, you need 100 counts for each ADC output code.
    - For an 8-bit ADC
      - 256 code bins and 100 counts = 25,600 samples
  - Ramp test is typically performed on ADC < 10 bits
  - Sinusoidal test is used for ADC >10 bits, but can be used in place of ramp for lower resolution ADC's as well.

ADC Characterization – DC Parameters

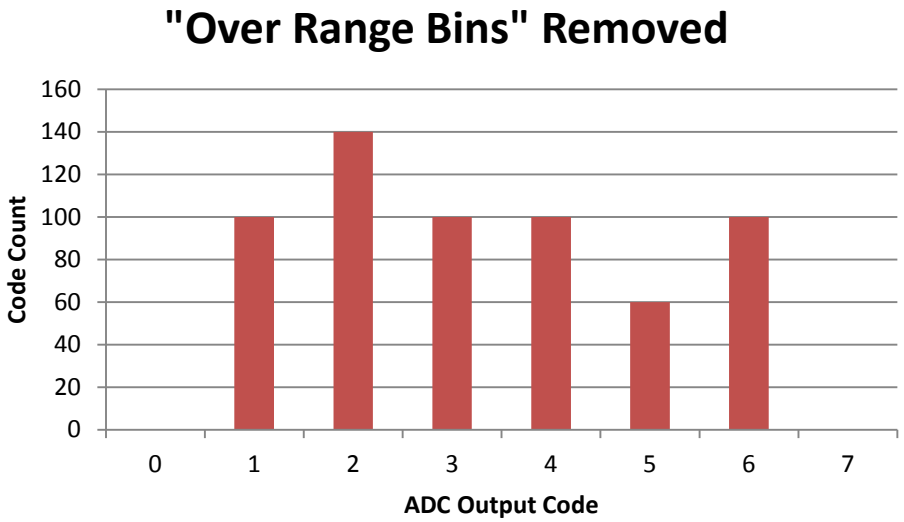
Code Density or Histogram Test for DNL and INL



- Code Count Plotted for each ADC Output Code

ADC Characterization – DC Parameters

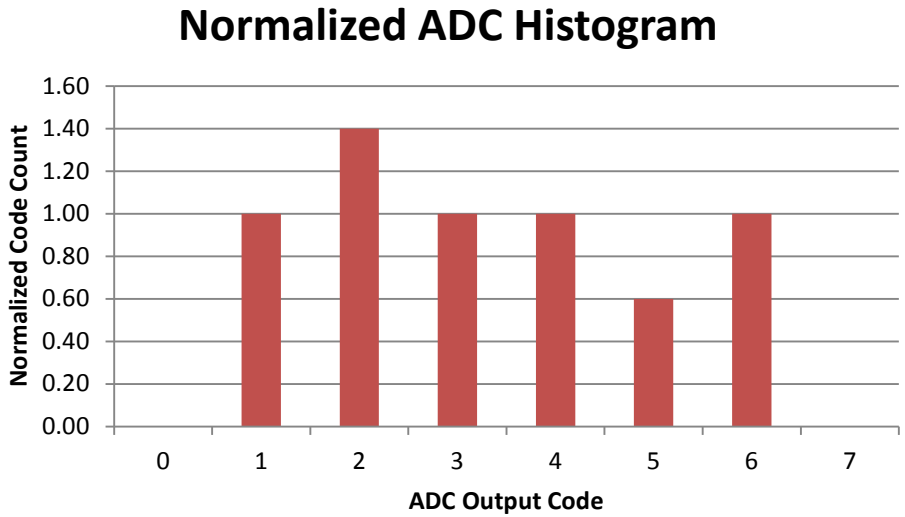
Code Density or Histogram Test for DNL and INL



- Over Range Bins Bin 0 and Bin 7 are special case as code 0 does not have the lower transition edge and code 7 does not have an upper transition ridge.
- Total all counts for bins and determine the average = 100 counts

ADC Characterization – DC Parameters

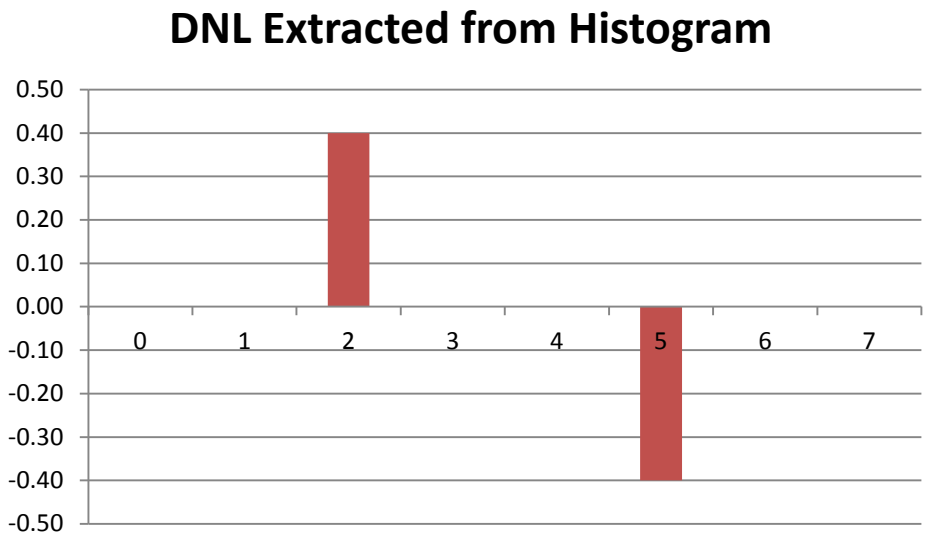
Code Density or Histogram Test for DNL and INL



- Divide histogram by average count per bin to normalize

ADC Characterization – DC Parameters

Code Density or Histogram Test for DNL and INL



- **DNL = +- 0.4 LSB**

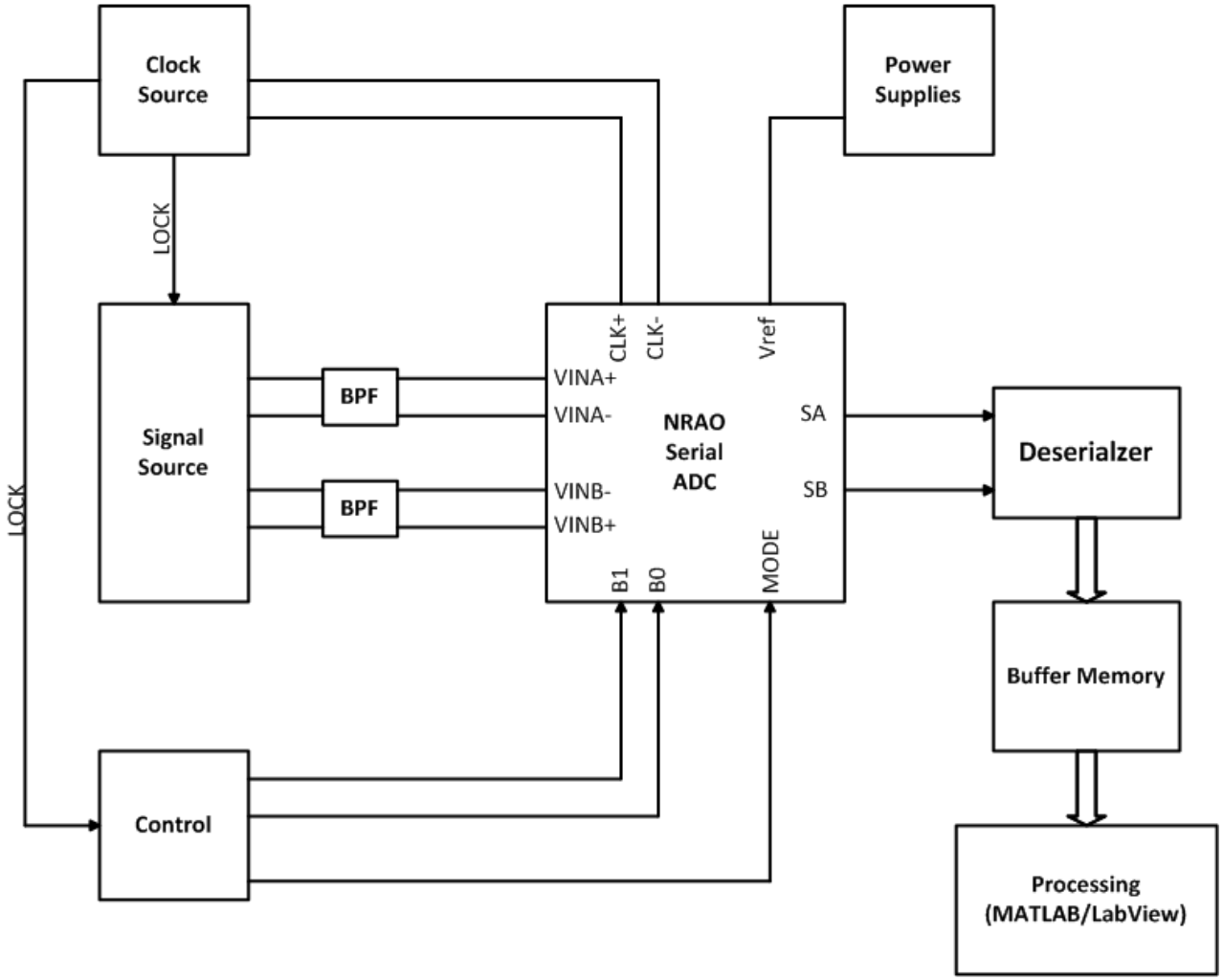
ADC Characterization

Basic Test Requirements for AC Parameters

- AC characterization of the ADC requires a low noise, low-distortion, lockable sine-wave source(s).
  - Note the sine-wave source must have lower noise and distortion than the converter being tested.
- A low-jitter, lockable clock generator to minimize jitter effects.
- ADC Sample buffer to store data for FFT processing.
- FFT engine (FPGA or Processor/PC) to calculate the FFT results and output graphically.

ADC Characterization

Basic Test System Configuration for DNL, INL, SNR, SINAD, ENOB, THD, SFDR



ADC Characterization

Basic Test System Configuration for two-tone Intermodulation Distortion (IMD)