# THE EVLA TRANSITION FILTER

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**Abstract**

An important requirement of the EVLA project is to maintain VLA operations during the period when antennas are being modified and before the EVLA correlator becomes operational. This requires that modified EVLA antennas be able to supply data to the VLA correlator. This memo describes the digital filter which process the 1GHz bandwidth EVLA data stream and makes it suitable for the VLA baseband system.

## 1 Introduction

The functionality to accomplish this is implemented in the transition converter. The transition converter is physically located in the EVLA fiber-optic receiver module. It consists of a high speed digital to analog converter (DAC) on the board and a digital filter implemented in the FPGAs on the receiver module board.

This document describes the transition filter that is implemented in the receiver module FPGAs. This document is intended to document the design of the filter and as an aid to persons who must understand and maintain the VHDL code which implements the filter. The EVLA fiber-optic receiver module description document provides descriptions of the underlying hardware.

## 2 General Description

The transition converter uses the 8-bit data stream from the EVLA antennas. The 8 bit data stream contains 1GHz of bandwidth digitized at a rate of 2048 Megasamples per second (Msa/s). This data are processed in a digital filter

which then drives a high speed DAC. This analog signal is introduced to the VLA baseband system at the input to the baseband filter module. The transition filter selects a 50 MHz band from the input and drives the DAC at a clock rate of 128MHz. Further bandpass shaping is done in the VLA baseband filter.

The transition filter is a three stage finite impulse response (FIR) design. The first stage selects a 128MHz wide sub-band from the 1 GHz input bandwidth and reduces the input sample rate by a factor of 8. The second stage selects half the stage one output and determines the DC cutoff properties and the spectral sense of the transition converter output. The third stage is a phase compensator which matches the phase response of the EVLA IF, LO, and data transmission systems to the VLA.

The VLA correlator digitizers operate at a sample rate of 100 MHz using a three level quantization scheme. The EVLA 8-bit digitizers operate at a sample rate of 2048 MHz. The inputs to the 8-bit digitizers are in the second Nyquist zone at 1024 to 2048 MHz.

In addition to reducing the bandwidth of the signal the transition converter must also accomplish a sample rate conversion. The 100 MHz rate of the VLA system is not a simple sub-multiple of the EVLA rate.

The output sample rate of the transition converter is 128 MHz which is the smallest sub-multiple of the EVLA rate that can accomodate the required 50 MHz bandwidth. The conversion to analog before introduction to the VLA baseband system is necessary because of the relatively high data rates involved and the need for additional bandpass shaping.

There are three Altera Stratix FPGAs on the fiber-optic receiver board. The Stratix family of FPGAs provides dedicated hardware resources for high performance input and output and digital signal processing (DSP). The data sheet for the Stratix family is over two hundered pages.

Stage one of the filter is a 128 tap 8:1 decimation polyphase FIR. The filter uses integer two's complement arithmetic with 8 bit input data and 8 bit tap coefficients. The filter is implemented using the DSP blocks in the FPGAs. The Stratix DSP blocks implement the input shift registers, multipliers, and the first two stages of a fully pipelined adder tree. Additional stages of the adder tree are implemented in FPGA general purpose logic resources.

Following stage one is a gain adjustment block and a requantizer. The gain adjustment block is implemented using hardware multipliers and allows the on-line computer system to optimize dynamic range in subsequent stages.

After the gain adjustment is a requantizer which reduces the 22 bit wide output of stage one down to the 4 bit input width of stage two. The requantizer is designed to saturate on overflow. There is an overflow flag which can be read by the on-line computer system.

Stage two is a 511 tap 2:1 decimation polyphase FIR. The filter uses integer two's complement arithmetic with 4 bit input data and 10 bit tap coefficients. The

filter is implemented using lookup table (LUT) multipliers in general purpose logic resources. The clock speed of stage two is 128 MHz.

After stage two the data stream is again requantized, this time to 8 bits, for input to stage three. Stage three is a 64 tap all pass FIR implemented using DSP blocks. Stage three performs the phase matching between the EVLA transmission system and the VLA system. There is a multiplexer which bypasses the phase compensator. The gain of the bypass path is matched to the nominal gain of the compensator so no gain adjustment is necessary when switching between compensated and uncompensated signal paths. The output width of stage three is 20 bits of which 10 are selected to drive the DAC.

# 3 The Data Transmission System

In 8 bit mode the EVLA data transmission system moves the data over two of three OC-192 fiber-optic channels. The third channel transmits test pattern data but is used to synchronize the receivers in the data carrying channels.

The channels are arbitrarily labeled top, middle, and bottom. The top and bottom channels carry 8 bit samples which alternate in time. The top channel carries the even samples.

The basic frame rate of the data processing in the deformatter is 64 million frames per second. The data are multiplexed by a factor of 4 up to the 256 MHz clock rate of stage one.

# 4 Polyphase Filters

If the output of a filter meets certain restrictions on passband width and location the output will meet the Nyquist criterion at reduced clock speed. In such a case the output sample rate may be reduced by keeping every N-th sample where N is a small power of 2, a process referred to as decimation.

Some mathematical manipulation reveals that in this case there are a large number of results being computed that are not used and consequently requires a lot less hardware. Reference 1 presents a good development of this result. More importantly the clock speed of the filter circuitry may be reduced by a factor of N, so the stage one clock runs at one eighth of the digitizer clock.

The process of decimation divides the filter input band into N sub-bands. In this case N in stage one is eight and in stage two is two. The requirement for a polyphase filter to work is that the output passband must fit entirely within one of the N sub-bands. Any filter transmission outside the desired sub-band will be aliased into the filter output.

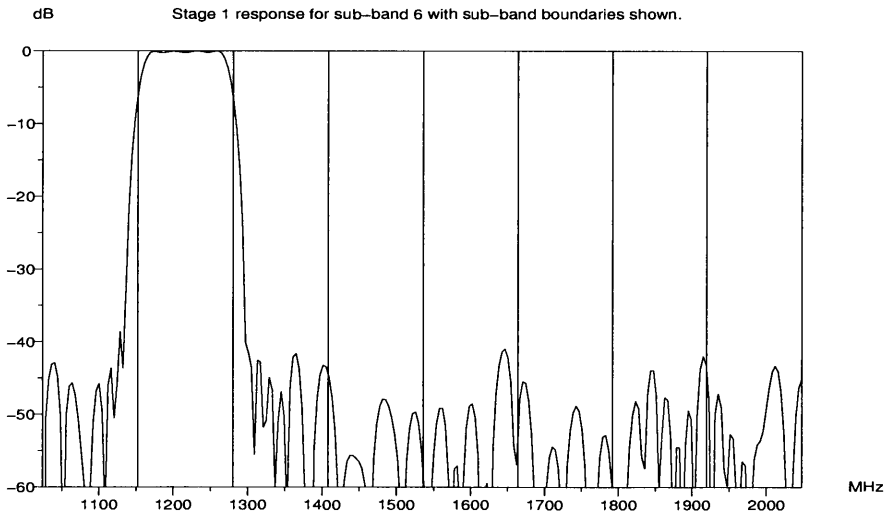
A further consequence of the decimation process is that the spectral sense of the successive sub-bands is inverted. Numbering sub-bands from 0 the even numbered sub-bands will have normal spectral sense, with respect to digitizer output, and the odd ones will be inverted.

# 5 Stage One

The primary function of stage one is as an anti-alias filter to stage two. It decimates the input data by a factor of eight and selects one of eight sub-bands. The selected sub-band may be changed by loading an appropriate set of tap coefficients into the filter hardware.

Figure 1 shows the stage one magnitude response computed from the quantized filter coefficients used in the hardware. The coefficent set was obtained using standard FIR filter design software for a Kaiser windowed filter with a parameter of 3.0. The horizontal axis labels are frequency in MHz at the digitizer analog input. The vertical axis is relative response in dB. The irregular appearance of the stop-band attenuation is due to quantization of the filter tap coefficients to 8 bits. Because this is sub-band 6 and the analog input to the digitizer is in the first Nyquist zone the output of stage one will spectrally inverted relative to the digitizer analog input.

Figure 1: Stage 1 sub-band six magnitude response.

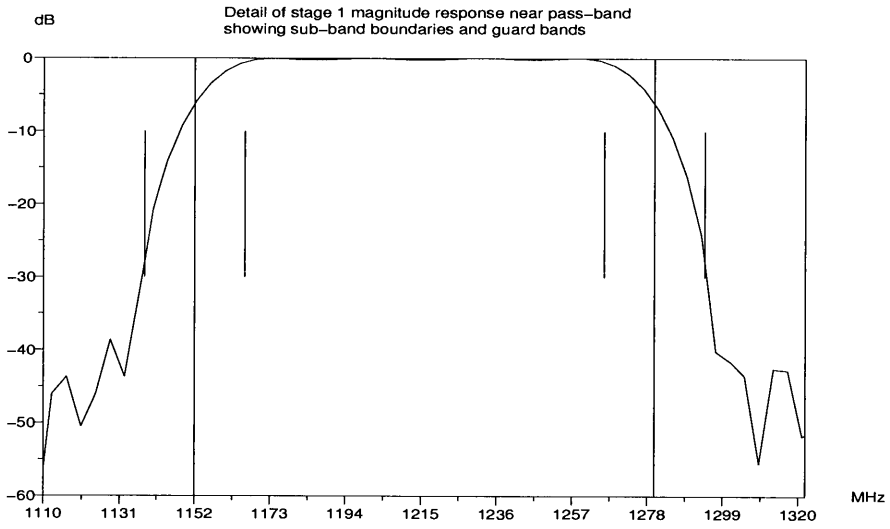



The sub-bands are 128 MHz wide. The required bandwidth to the input of the

VLA baseband system is 50 MHz. In order to obtain a final analog output with either spectral sense the center 100 MHz of the stage 1 output is required.

At either end of the center 100 MHz of the selected sub-band is a 14 MHz wide guard band. These are frequencies which are not needed in the final output. To minimize the required filter size this 14 MHz plus the 14 MHz adjacent sub-bands are used as guard bands. The partial response in adjacent sub-bands is aliased into the filter output. These aliased signals are not used in the final filter output. Figure 2 is a detail showing the area near the passband with sub-band and guard-band boundaries shown.

Figure 2: Stage one sub-band six magnitude response detail.




Stage one is implemented using the DSP block resources in the top and bottom FPGAs. There are 10 DSP blocks available in each FPGA which each provide 8 8x8 bit multipliers. Two blocks are cascaded to provide a 16 tap chain. Four chains are implemented in each of the top and bottom FPGAs to obtain a total of 128 taps.

In the DSP block mode used the block provides 8 multipliers, the first two pipelined adder tree stages and two shift register chains at the multiplier inputs. One of the shift register chains is used for the data and is clocked at 256 MHz. The other is used to hold the filter coefficients. The coefficient chains are cascaded in the hardware. The chains are loaded through a single register by the online computer. The coefficients must be split even and odd and further shuffled by the computer in order for them to end up in the correct places in the coefficient inputs to the multipliers. This task is handled by the monitor/control

computer software. Refer to the VHDL source code and the control program soruce for the exact implementation of this.

The stage one implementation is split between two FPGAs. The adder trees in the filter are allowed to grow in width as data propogates up the tree. In order to obtain the required speed in the filter the adder tree is fully pipelined. At the output of one half the filter the word width is 22 bits. This is truncated to 10 bits and demultiplexed by a factor of two for transmission to the middle FPGA where the signals are combined.

The two streams from the outside FPGAs are added to obtain the two inputs to the stage two chains. These are input to a gain adjust block. The gain is set by the online computer system through an 8 bit register. The output of the gain adjust block is requantized to 4 bits. The requantizer is designed to saturate on overflow. Part of this logic is an overflow flag which can be read by the online computer system to determine the optimum gain setting.

The logic compiler used to produce the FPGA configuration file from the VHDL source code is very efficient at removing unnecesary logic. Unused logic resulting from allowing the adder tree to grow naturally is automatically removed.

# 6 Stage Two

Stage two is a 511 tap decimation two polyphase FIR. The magnitude response is symmetric about mid-band. The half-band symmetric odd length filter has the property that nearly half the coefficients are zero. This provides a large savings in hardware. Further, for the case of the decimation two filter the zero coefficients all appear in one pipeline leaving only one nonzero coefficient. The filter gain can be scaled such that this coefficient is one.

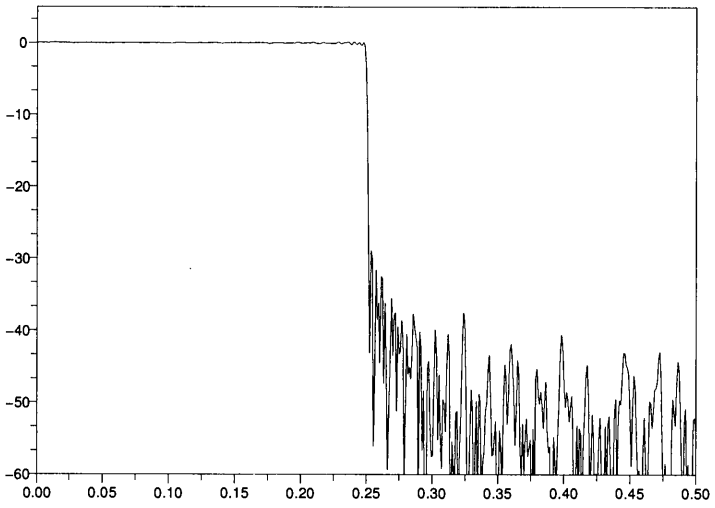
In order to obtain both spectral senses out of the transition filter the second stage can be used in either low-pass or high-pass mode. The filter is designed with standard FIR design software using a Kaiser window low-pass FIR with window parameter 3.0. To obtain the high-pass equivalent The two's complement is obtained for data entering one of the filter pipelines. This is equivalent to inverting every other filter coefficient.

Figure 3 shows the magnitude response of stage two. The horizontal scale is frequency expressed as a fraction of the filter clock frequency. The response is symmetric about frequency 0.25.

Stage two is implemented as a constant coefficient filter with lookup table multipliers in the general purpose logic resources of the middle FPGA. The stage two clock frequency is 128 MHz. The outputs of the two pipelines are added together and requantized to 8 bits for input to stage three.

The cutoff of the DC end of the analog output is important to the performance of the VLA in narrow bandwidth modes. The transition band of the second

Figure 3: Stage two magnitude response.




stage is moved to DC by spectraly inverting the output of stage two. This is accomplished by computing the two's complement of alternating samples. This spectral inversion is performed in all modes. There is a bit in the FGPA which turns off the spectral inversion. It is for diagnostic purposes only.

# 7 Stage Three

The VLA analog transmission system and baseband system has a phase response which is well matched between the VLA antennas but does not match the linear response of the wide band digital system of the EVLA. In order to make the EVLA transition system work with the VLA correlator in continuum mode the phase response of the EVLA transition system must be matched to the VLA.

Stage three is a 64 tap all pass FIR with a phase response which compensates for the VLA phase response. It is implemented using DSP block resources in the middle FPGA.

The required phase response is obtained by fitting a functional form to VLA calibration data obtained with no phase compensation in the EVLA transition system. The function has the following form with the result $y$ in degrees and the input $x$ in MHz.

$$y = a_0 e^{-a_1 x} + a_2 + a_3 x + a_4 x^2 + a_5 x^3 + a_6 x^4$$

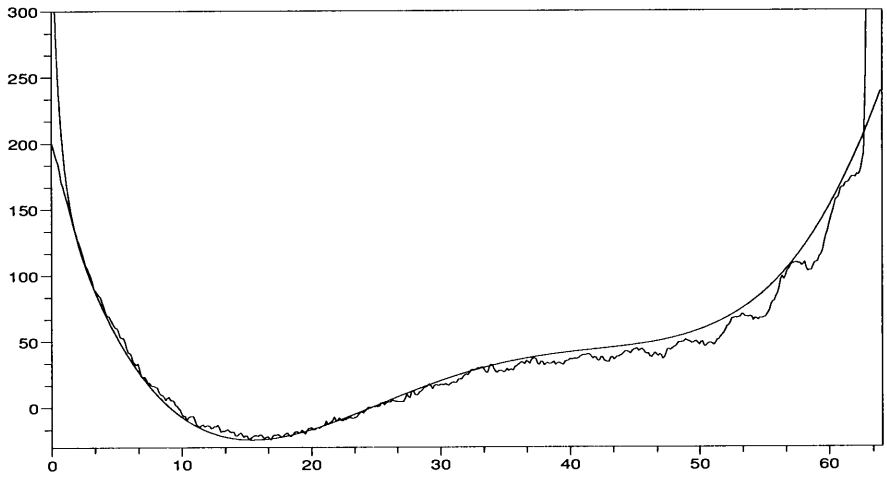
The parameters have the values shown in .

Table 1: Parameter values

| | value |
|---|---|
| $a_0$ | 196.011 |
| $a_1$ | 1.808 |
| $a_2$ | 181.518 |
| $a_3$ | -34.058 |
| $a_4$ | 1.889 |
| $a_5$ | $-4\times10^{-2}$ |
| $a_6$ | $2.98 \times 10^{-4}$ |

Figure 4 is a plot of the above function with the measured response of the equalizer.

Figure 4: Stage 3 phase sesponse specification and measured response.




The measured data were obtained by setting up two EVLA transmission systems. Identical wide band noise was input to both. One system had the stage three coefficients obtained from the specification function the other had a linear response with compensating delay. Data from both were captured into memory in the FPGAs and dumped to computer files. These files were then correlated in a special computer program. The resulting measured phase data were then compensated for residual delay error by subtracting a linear function.

# 8 Summary

The hardware required to supply data to the VLA correlator from modified EVLA antennas consists of a single high speed digital to analog converter on the EVLA fiber-optic receiver module and a somewhat larger FPGA than would have otherwise been necessary. The required signal processing is implemented digitally as described above.

# 9 References

1. P.P. Vaidyanathan, Multirate Systems and Filter Banks, 1993, Prentice Hall, ISBN 0-13-605718-7