The EVLA 8-Bit Digitizer Performance

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Abstract

Performance measurements of the EVLA 8-bit digitizer are presented. The measured performance is consistent with the manufactuer's data sheet for the primary component used in the design.

1 Introduction

For operation in bands where RFI is expected to be a problem the EVLA design incorporates 8-bit resolution digitizers operating at a speed of 2.048 Gsa/sec to obtain a bandwidth of 1.024 GHz and large dynamic range. The attainable dynamic range is limited by the performance of the basic chip used.

To simplify the design of the analog IF system the analog inputs to the digitizer are down-converted to the band between 1024 and 2048 MHz which eliminates the need for complex mixer based down-converters.

The EVLA 8-bit digitizer design is based on the TS83102G0B analog to digital converter part from Atmel and a companion 1:4 demultiplexer chip, the AT84CS001. The digitizer chip is a 10-bit 2 Gsa/sec device. In the EVLA design the least significant 2 bits are left unconnected. The design therefore has 8-bit resolution with the quantization threshold accuracy of a 10-bit device.

2 Methodology

A standard technique for evaluating digitizer components is to input a signal of known spectral characteristics, typically sine waves, and evaluate the frequency spectra of the digital data produced. The most useful signals consist of single

frequencies at various levels to evaluate spurious products generated by various system nonlinearities and two closely spaced tones to detect intermodulation products generated in system nonlinearities.

All plots are logarithmically scaled power spectra normalized to the converter output full scale. For 8-bit converters the full-scale is 256 counts. The output range is -128 through 127.

The data used here were captured in the EVLA data transmission system (DTS) receiver module. The DTS receiver has the capability to capture data at full speed into memory which can then be read out by the monitor and control system and stored into disk files. These files are then read by data reduction software.

All plots presented here are 256K point FFTs of the captured data. The data are unwindowed. The plots have a basic resolution of about 8KHz. The plot scales are not adjusted for frequency resolution so the amplitude scale can be interpreted as the power per resolution bandwidth integrated over the time to acquire 256K samples (about 128 microseconds).

The primary performance measure obtained is the Spurious Free Dynamic Range (SFDR). SFDR is the range expressed in dB from full scale to the highest unwanted spurious response. A related figure of merit is ENOB which is the number of bits in an ideal digitizer which gives the same dynamic range. This ideal digitizer may have a non-integer number of bits.

3 Results

For reference, the manufacturer's data sheet for the TS83102G0B specifies an ENOB of 6.5 bits at 2 Gsa/sec. This provides a signal to noise of 41dB.

Figure 1 shows the result from a signal at 1730 MHz at -40 dBm into the DTS module. This results in an output signal around -32 dBFS (dB referenced to full scale). This signal is representative of the operating level of the digitizer when RFI is not present. In this case the highest spurious signals are around -65 dBFS or -35 dBc (dB referenced to carrier).

Figure 1: -40dBm input level at 1730MHz.

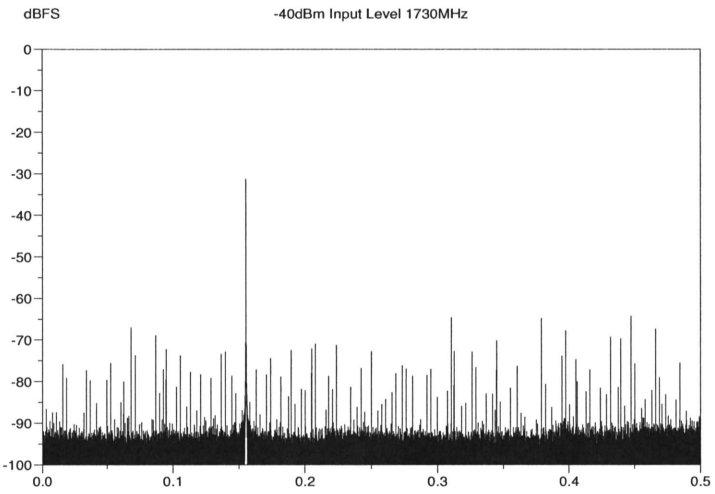


Figure 2 is at the same frequency with the input level increased to just bel saturation. The highest spurious signal is around -46 dBFS. This yeilds ENOB of 7.3 which is consistent with or better than the data sheet specificat of 6.5 ENOB.

Figure 2: -10dBm input level at 1730MHz.

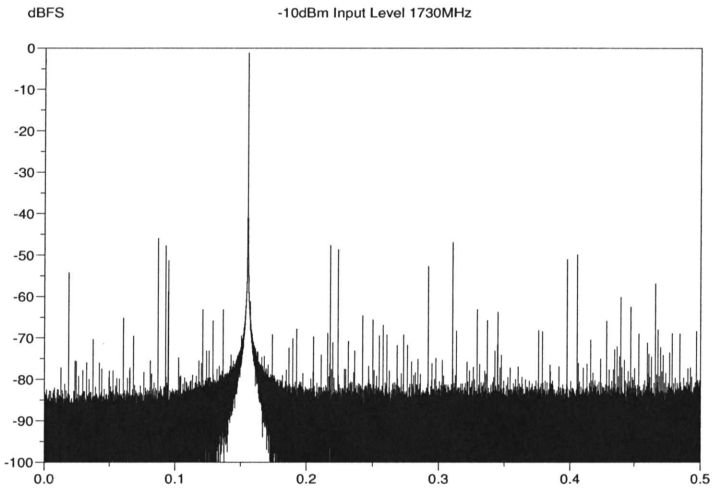


Figure 3 shows the result of a -40dBm signal at 2047MHz which is 1MH from the digitizer clock frequency. The spurious signals are at similar lev now cluster around the signal DC and Nyquist frequencies.

Figure 3: -40dBm input level at 2047MHz.

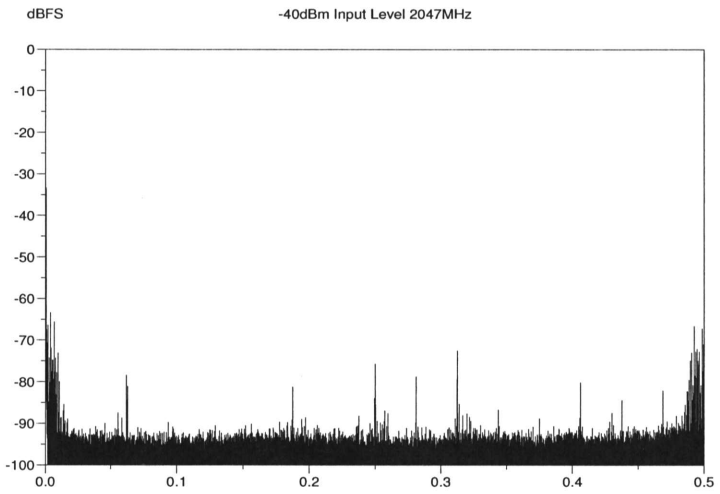


Figure 4 shows the result of a signal near full scale at 1024MHz which is the Nyquist frequency. The peak is not visible because it coincides with the plot frame. There appear to be fewer spurious signals because they now lie on top of each other or coincide with the main peak. The maximum spurious signal is still around -45dBFS.

Figure 4: -10dBm signal at Nyquist frequency.

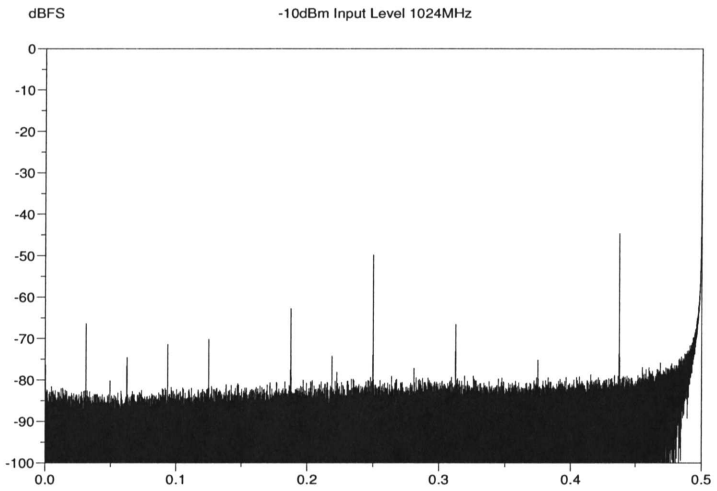
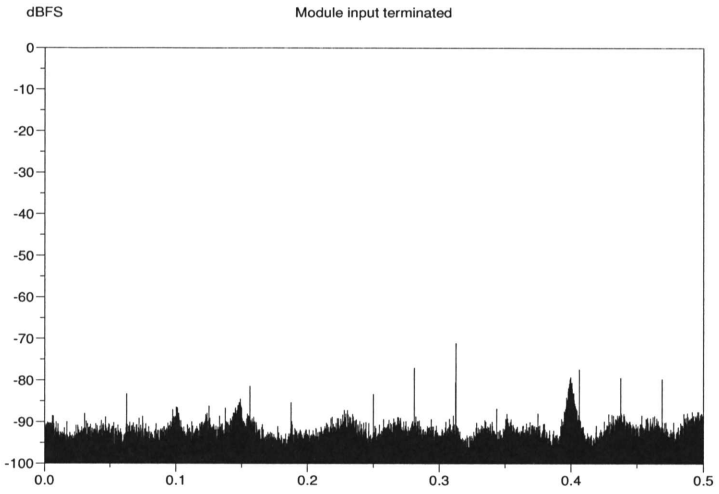


Figure 5 was obtained with the module input terminated at 50 ohms. This represents the noise floor from the digitizer, input amplifiers and crosstalk from other signals inside the module. The highest peak in this plot is below -70dBFS with the bulk of the noise below -90dBFS.

Figure 5: Module noise floor.



Figures 6 and 7 are the results of two tone tests. This test looks for intermodulation products between input signals caused by mixing in nonlinearities in the digitizer. Figure 6 shows two input signals at low levels. In Figure 7 the two signals are adjusted to just below saturation. There are new spurious signals but none are above those noted in single tone tests.

Figure 6: Low level two-tone test.

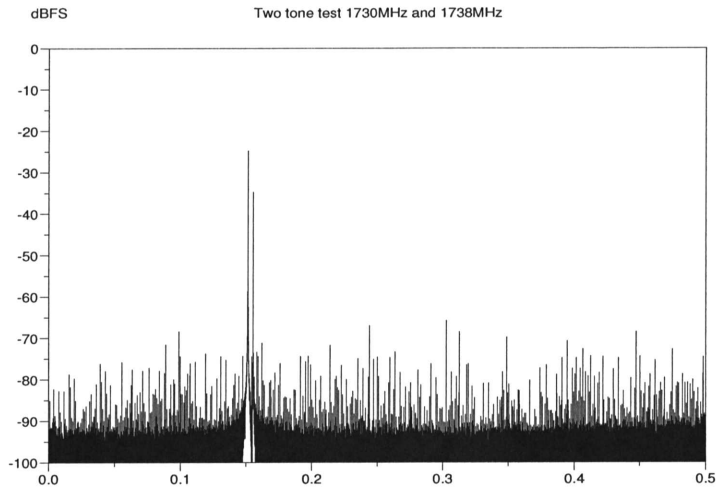
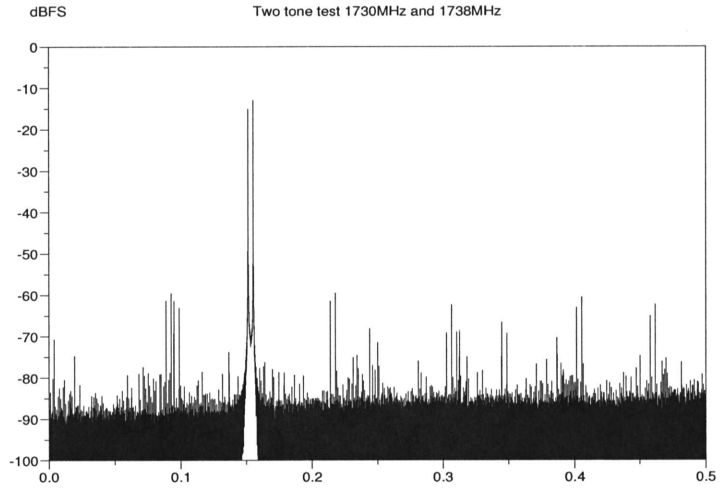


Figure 7: High level two-tone test.



4 Summary

The measured performance of the EVLA 8-bit digitizer design is consistent with the manufacturer's published specifications for the part the design is based on.