GBT Technical Report No. 2

LO Reference Distribution System

Maintenance Manual

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September 15, 2004

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Abstract

The purpose of this report is to provide users of the LO Reference Distribution System with detailed procedures for periodic maintenance, and guidance for troubleshooting in the event of a subsystem failure. Some background information and important system design considerations are also given.

Those readers who already have a basic understanding of the System may choose to proceed directly to section II – Maintenance Procedures. New users, or users wishing to modify or redesign any part of the System, are recommended to read the introductory section of this document.

I. System Description

The LO Reference Distribution System transmits 10 MHz and 500 MHz from the Timing Center to various remote user stations, over single-mode optical fiber. A simplified schematic block diagram is shown in figure 1 (for a detailed schematic, refer to D35260K003 in the GBT drawing archive).

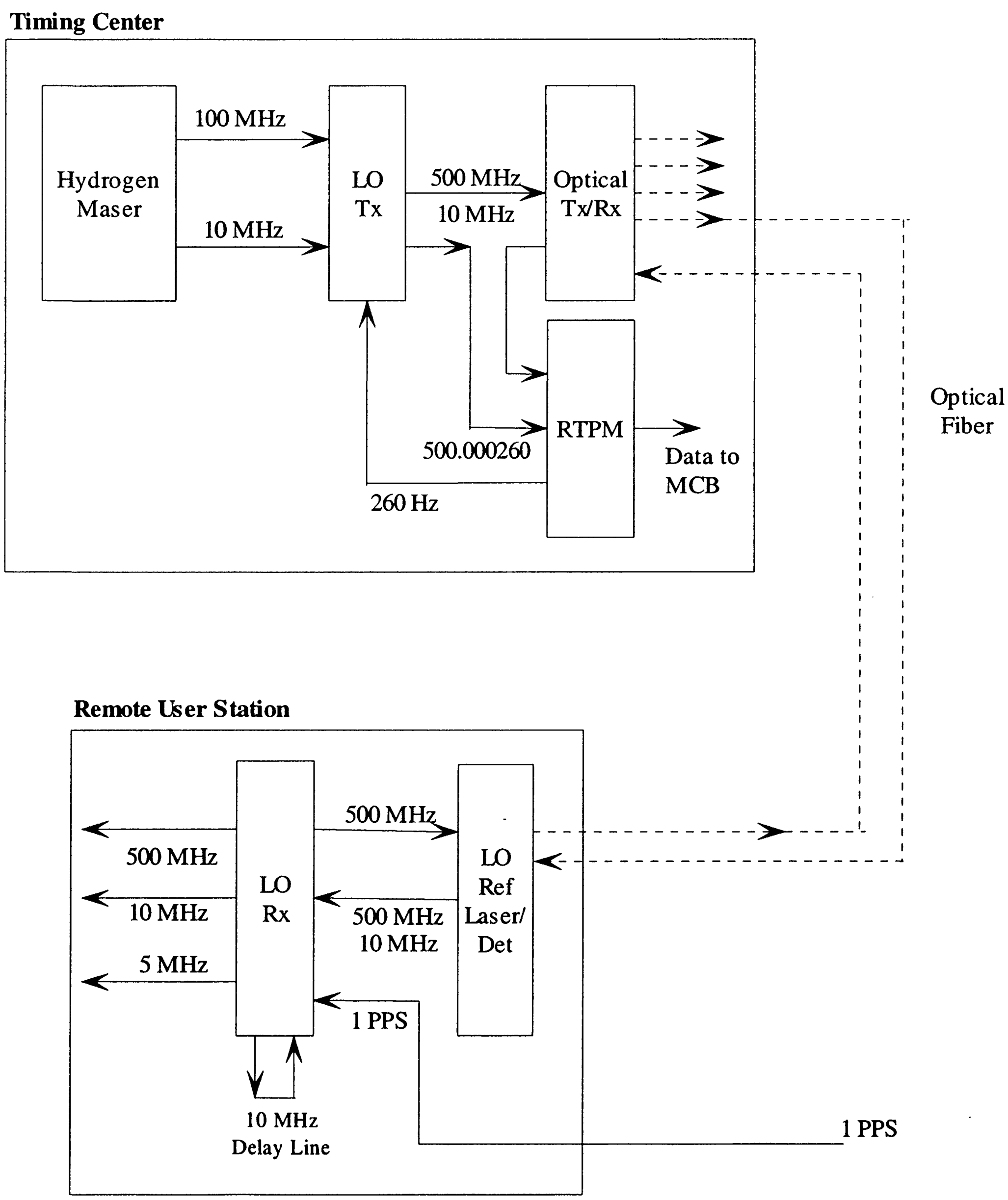


Figure 1. A simplified block diagram of the LO Reference Distribution System.

Overall System Architecture

From the hydrogen maser, the LO Transmitter module accepts 10 MHz and 100 MHz, each with nominal levels of +10 dBm. Inside the LO Tx module, the 100 MHz is frequency multiplied to 500 MHz, filtered, combined with the 10 MHz, and sent out to the Optical Tx/Rx module where it modulates a laser. The laser output is optically split, with each of the four outputs spliced to SM fibers which carry the modulated light to each user station.

At the user station, the optical signal is detected in the LO Ref Laser/Detector module, and its output is transmitted via coax cable to the adjacent LO Rx module. Inside the LO Rx module, the incoming 500 and 10 MHz is separated (coming into the module on a single coax cable, the signals are put onto individual coax cables using a power divider and filters). The module's 500 MHz input is used as a reference in a PLL, whose output is split four ways; two of the outputs are brought to the module's rear panel for general use, another is used internally for clocking the incoming 10 MHz, a third establishes a feedback path for the PLL, and the fourth is output to the module's rear panel for use as the returned 500 MHz – part of the round-trip measurement subsystem.

Inside the LO Rx module, the clocked 10 MHz (ECL) is voltage-shifted and filtered to provide a +2 dBm (50 Ohm) sine wave at the module's rear panel. A sample of the ECL 10 MHz is applied to a divide-by-two circuit, producing 5 MHz which is also shifted, filtered, and output to the rear panel (+2 dBm).

Round-Trip Phase Monitoring

Within the LO Tx module at the Timing Center, a sample of the 500 MHz is used, together with 260 Hz from the RTPM module in a PLL, to create an offset reference frequency of 500.000260 Hz (more precisely, 10 MHz divided by 38400) to be used in the RTPM for phase detection. The offset reference is mixed (in the RTPM module) with the returned 500 MHz from a user station, translating the phase drift information to 260 Hz. The 260 Hz signal is then input to an exclusive-OR gate along with a reference 260 Hz, which produces at its output a 260 Hz square wave whose duty cycle is an indirect measure of relative phase drift on the 500 MHz round-trip path. By running a digital counter on the XOR output, the duty cycle can be accurately measured. The counters are latched and reset once every three seconds, and the transformation from counts to picoseconds is done in software.. The RTPM module contains its own SIB, providing an interface to the MCB over which the RT phase, and other information can be exchanged.

History of the GBT RTPM Design

The GBT round-trip phase monitor was modeled after the OVLBI RTPM, which in turn was taken from the original VLBA design [1]. The VLBA RTPM was designed to accept a 5 MHz reference, however, the architecture of the OVLBI system made it more convenient to use a 10 MHz reference instead of 5 MHz. This design change was carried on to the GBT RTPM in order to maintain compatibility; neither the OVLBI nor the GBT designs are interchangeable with the VLBA modules, while they still have many of the component parts in common.

Important Considerations for the Optical Subsystems

The 500 MHz and 10 MHz together (in the documentation referred to as 500/10 MHz) are input to the Optical Tx/Rx module via a single coax cable. It is very important that the combined power of the 500/10 not exceed -2.5 dBm to avoid nonlinear operation, and damage to the laser. The Optical Tx/Rx module contains one laser, followed by an optical four-way splitter – for providing up to four remote user stations. The noise margin of the System will not allow for an increase in the number of user stations, or for a significant increase in the distance between the Timing Center and a user station; 5 kilometers is the predicted limit. Expansion of the System, either in the number of user stations or distance of transmission, will require the upgrade of laser transmitters from the Fabry-Perot to a DFB type. The module also houses four PINFET optical detectors, for converting the returned light to an electrical signal to be used for round-trip phase detection.

At a remote user station, the incoming light (modulated with 500/10) is input to the LO Ref Laser/Detector module, where it's detected, and sent out on coaxial cable to the LO Rx module. The incoming optical power level is nominally -9 dBm, however the System will continue to function without significant degradation, with optical power levels anywhere in the range -10 dBm to -8 dBm.

It is important to keep in mind that the input power to the optical detectors must not exceed -7 dBm. Optical power incident on the detectors at user stations is attenuated by not only the fiber loss (typically on the order of 1 dB), but also by the four-way optical splitter within the Optical Tx/Rx module in the Timing Center. Since the returned optical signal is not optically split, additional attenuation was needed. The System makes use of hand-wound (NRAO) optical attenuators in each LO Ref Laser/Detector module.

LO Reference Signal Synchronization

The LO Rx module receives 500 MHz and 10 MHz (500/10) signals from the LO Ref Laser/Det module on a single coaxial cable, and separates them. The 500 MHz is used as a reference in a PLL within the module, and is subsequently divided four ways in a 1:4 splitter. One of the splitter outputs is used as a clock input to a resynchronization circuit, where it clocks the incoming 10 MHz using a D flip-flop, as shown in figure 2. Two of the splitter outputs are brought to the module's rear panel to provide 500 MHz for general use (+8 dBm each). A sample of the synchronized 10 MHz is then applied to a divide-by-two circuit (the center D flip-flop of figure 2) to generate 5 MHz. The ECL 10 MHz and 5 MHz are DC-shifted, then low-pass filtered to provide +2 dBm outputs at the module's rear panel.

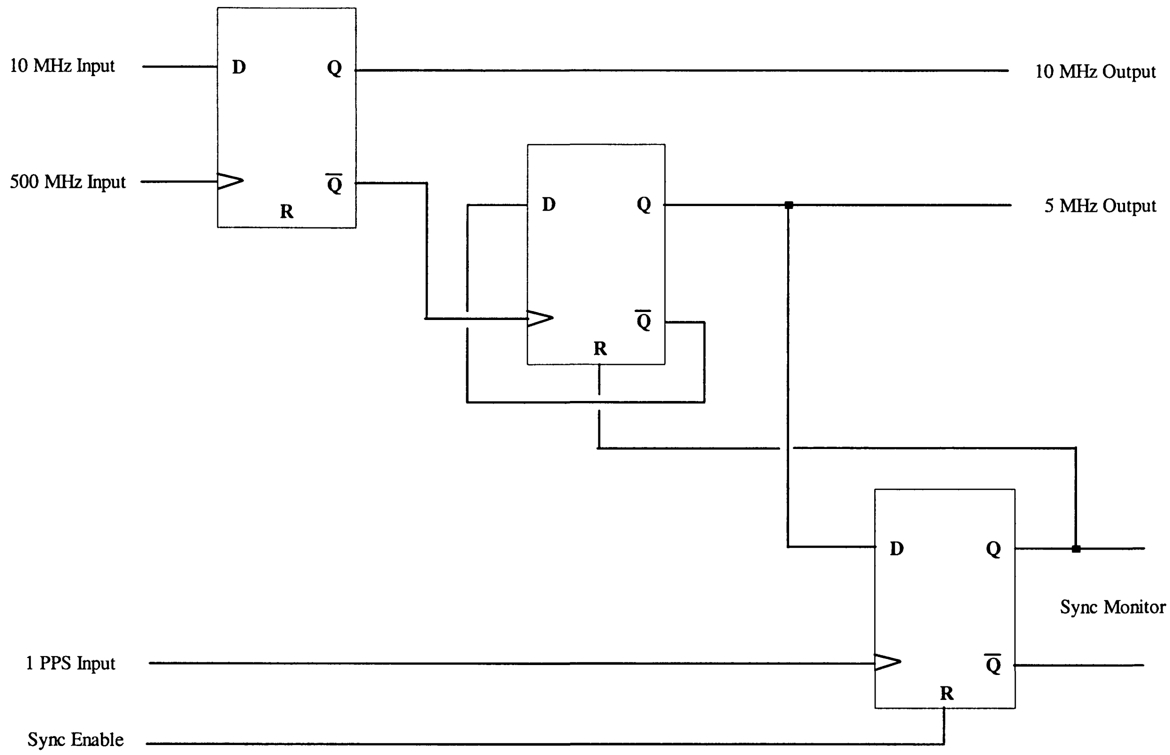


Figure 2. A simplified schematic of the synchronization circuits in the LO Rx module.

Since some applications require a 5 MHz reference having unambiguous phase, the 5 MHz is sampled at the rising edge of the 1PPS, and phase inverted if necessary. The *phase* of the 5 MHz, with respect to the rising edge of the 1PPS, is a parameter that is constantly monitored using again a D flip-flop (on the right-hand side of figure 2). If the 5 MHz square wave should come up in the "wrong" phase during power up of the module, the output of the third D flip-flop will reset the divide-by-two circuit, thereby forcing the 5 MHz phase to be "low" at the rising edge of the 1PPS. The output of the third flip-flop, the *sync monitor*, is latched and is able to be read over the MCB. Two other events can also lead to the latching of the *sync fault*: (a) the interruption of the 1PPS signal, or (b) disabling the sync circuit (setting sync enable to a logic "high"). If any one of these three basic events occurs, a *sync fa*ult will be latched and reported over the MCB. The fault latched by the sync monitor (the D flip-flop which monitors the phase relationship between the 5 MHz and 1PPS) is of most concern, as there are many possible causes. These are:

- The randomness of initial conditions on the flip-flop inputs upon power-up.
- The absence of 10 MHz. Since the 5 MHz is made from the 10 MHz, a loss of 10 MHz input will naturally lead to the loss of 5 MHz.
- The loss of 500 MHz reference. If the module's 500 MHz reference input level drops by more than 6 dB, the module's VCXO will lose phase lock – creating a ramping phase modulation on both the 10 MHz and 5 MHz.

- Loss of 500 MHz VCXO. If the module's 500 MHz VCXO output level decreases by 6 dB, the 10 MHz will not be clocked through the first flip-flop.
- A drop in optical power input to the LO Ref Laser/Detector will reduce the amplitude of 500 MHz and 10 MHz input to the LO Rx module.
- A loss of 1PPS signal.
- Ambient temperature drift. As temperature changes, two critically-timed signals may experience different changes in propagation delay, and eventually resulting in the violation of required setup and hold times at the flip-flop inputs.. If this occurs between the 500 MHz and the 10 MHz, the LO Rx module's 10 MHz output spectrum will be noisy (discussed in detail later in this report), and the noise will trigger a sync fault. If there is a drift in relative delay between the 5 MHz and the 1PPS, the required phase relationship can be violated.

The 1PPS/5MHz sync fault can be cleared remotely, or by pressing a button on the module's front panel.

II. Maintenance Procedures

The LO Reference Distribution System requires occasional cable length adjustments. Due to seasonal variations in the outdoor temperature, the length of the optical fibers – between the Timing Center and the GBT, for example – will change enough to misalign critical signals in the LO Rx module. Critical timing exists between the 500 MHz and the 10 MHz, and between the 5MHz and the 1PPS signals in the LO Rx module. Both pairs of signals are input to D flip-flops (data, and clock inputs) which have well-defined set-up and hold requirements.

In addition to the cable length adjustments at the LO Rx module needed for meeting the setup and hold requirements for the flip-flops, the 500 MHz return path length must be varied at the input to the RTPM module, just prior to a VLBI run, to center the delay data in the center of its range. The current data processing software calculated one-way dealy modulo 1000 psec. In other words, if the data increases beyond 1000 psec, it will automatically wrap around to zero psec. Similarly, data decreasing below zero will wrap around to 1000. The VLBI data processing is not able to handle the discontinuities in RTPM data across the zero-1000 psec boundary, therefore, a path length must be changed in order to place the current data near 500 psec – the middle of its range. To avoid disturbing other critical delays in the system, it is important to do this alignment by varying the length of the 500 MHz return path. This is most conveniently done at the Timing Center, at the 500 MHz input to the RTPM module.

In summary, there are two cable length adjustment procedures: One set of adjustments is done at the LO Rx module (at each user station, such as the GBT LO Rack), and the other adjustment is done at the RTPM module in the Timing Center just prior to a VLBI run. Detailed procedures for the cable length adjustments are given in the following two sections.

LO Rx Module Cable Length Adjustments

If the 500 MHz and 10 MHz become sufficiently misaligned – to the extent that the set-up or hold time is violated, the 10 MHz and 5 MHz outputs from the LO Rx module will be noisy. To illustrate the increased noise on the 10 MHz output, a coaxial line stretcher was inserted in the 10 MHz signal path – after the signal separation (500/10) but ahead of the D flip-flop. As the line was stretched, noise on the 10 MHz module output was seen to rise and fall cyclically, according to an electrical length of pi radians at 500 MHz (a half wavelength). Figure 3 below shows the difference between a clean and noisy 10 MHz spectrum, obtained by changing the 10 MHz path length within the LO Rx module..

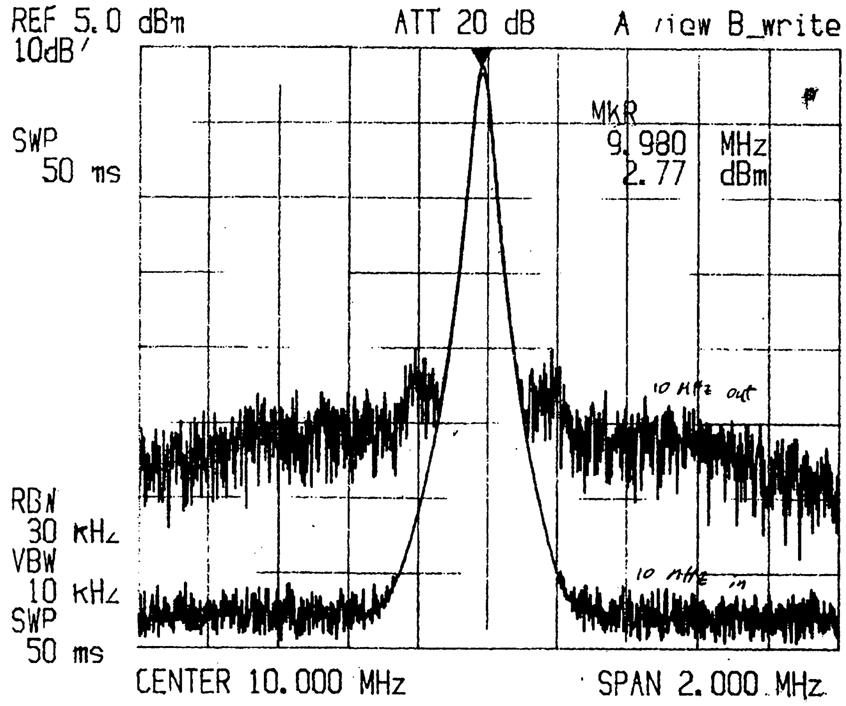


Figure 3. Clean and high-noise spectra, obtained by varying 10 MHz path length.

If the 10 MHz becomes noisy, so will the 5 MHz. Noise on the 5 MHz will trigger a fault on the 1PPS/5MHz Sync monitor.

Adjusting the relative delay between the 10 MHz and 500 MHz will of course affect an equal delay differential between the 5 MHz and 1PPS signals in the LO Rx module. Care must be taken to ensure that the setup and hold times at the 1PPS/5MHz flip-flop are satisfied, with maximum margin. After adjusting the relative delay between the 10 MHz and the 500 MHz, proceed immediately to the adjustment of 1PPS cable length. A procedure for alignment of both critical signal pairs (500 MHz and 10 MHz, and 5 MHz and 1PPS) is as follows:

1. Connect a spectrum analyzer to the LO Rx module's 10 MHz output, and set up the spectrum analyzer as follows:

Center frequency	10 MHz
Span	2 MHz
RBW	auto
VBW	auto
Sweep time	auto
Reference level	+10 dBm
Input attenuation	auto, or 10 dB

2. Locate the coaxial jumper on the rear panel of the LO Rx module, labeled "10 MHz Loop". Vary the length of this jumper, using the semi-rigid coax jumpers supplied with the module, while observing the 10 MHz spectrum. Notice that the spectrum will be noisy with certain jumper lengths, and clean for other lengths. If a given jumper length produces a noisy spectrum, another jumper – either 8 inches longer or 8 inches shorter (corresponding to a half-wavelength at 500 MHz) will also produce a noisy spectrum. Verify that this is true.

3. After finding two different coax jumper cable lengths (differing by approx 8 inches) that result in a noisy spectrum, install a jumper cable length that is approximately 4 inches shorter than the longer cable which produced a noisy spectrum. After installing this cable, the spectrum should be clean.

4. Using a 2-channel oscilloscope, view the rising edge of the 1PPS (at the input to the LO Rx module) and the module's 10 MHz output signal (use two coax cables of equal length, to carry the 1PPS and 10 MHz signals from the LO Rx module to the oscilloscope, so as to not introduce additional differential delay). Verify that the rising edge of the 1PPS coincides with a maxima or minima of the 10 MHz sine wave (the rising edge should be mid-way between zero crossings of the 10 MHz sine wave). If necessary, vary the length of the 1PPS cable at the input to the LO Rx module.

5. Reset the 1PPS/5MHz Sync Fault monitor by pressing the Sync Fault Reset button on the LO Rx module's front panel. Verify that the module's green 1PPS Sync LED is lit.

RTPM Cable Length Adjustment

This section describes the procedure for changing the 500 MHz path length just prior to a VLBI experiment, as needed to center the RTPM delay in the middle of its range (near 500 psec). Before each VLBI run, it is necessary to check the RTPM delay to make sure the data is between 400 and 600 psec. If it is not, it is necessary to make the adjustment as outlined below.

1. At the Timing Center, find the coaxial cable that is connected the RTPM's front-panel "500 MHz Input", and, at a convenient computer workstation, open a real-time display of the RTPM data. For a real-time display of round-trip delay, launch CLEO or a similar software application. CLEO's menu path is as follows:

CLEO → Utilities/Tools → Site Timing → then select the "GBT" tab.

2. Change the 500 MHz cable length as needed to obtain a delay within the range 400 psec to 600 psec. Note that changing the length of this cable will produce only half of the expected change in the displayed delay, since the signal processing software assumes that the delay change occurred in both the outgoing and return path. For example, changing the cable (having a Teflon dielectric) by 2 inches (245 psec delay) will affect a change of only 122.5 psec on the CLEO display. Using the software application gbtlogview, round-trip delay can be plotted as a function of time. The graph of figure 4 shows typical delay data over a three day period.

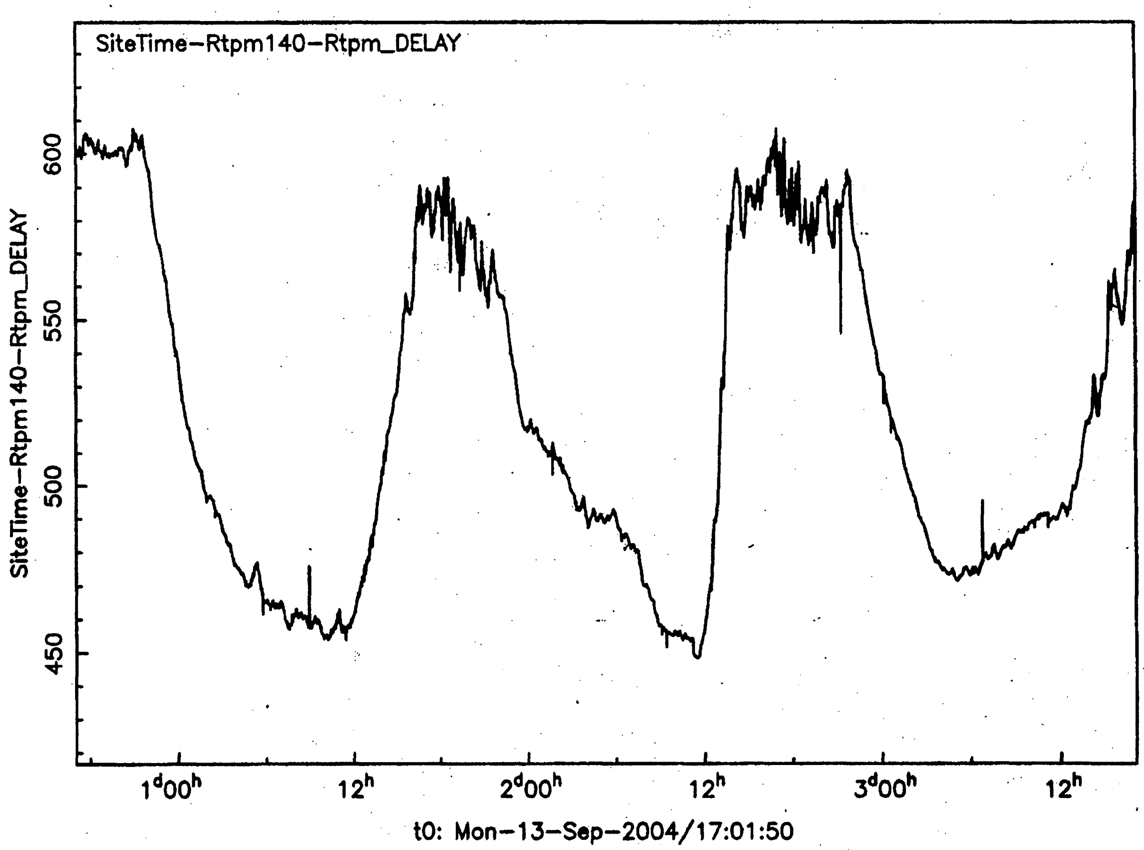
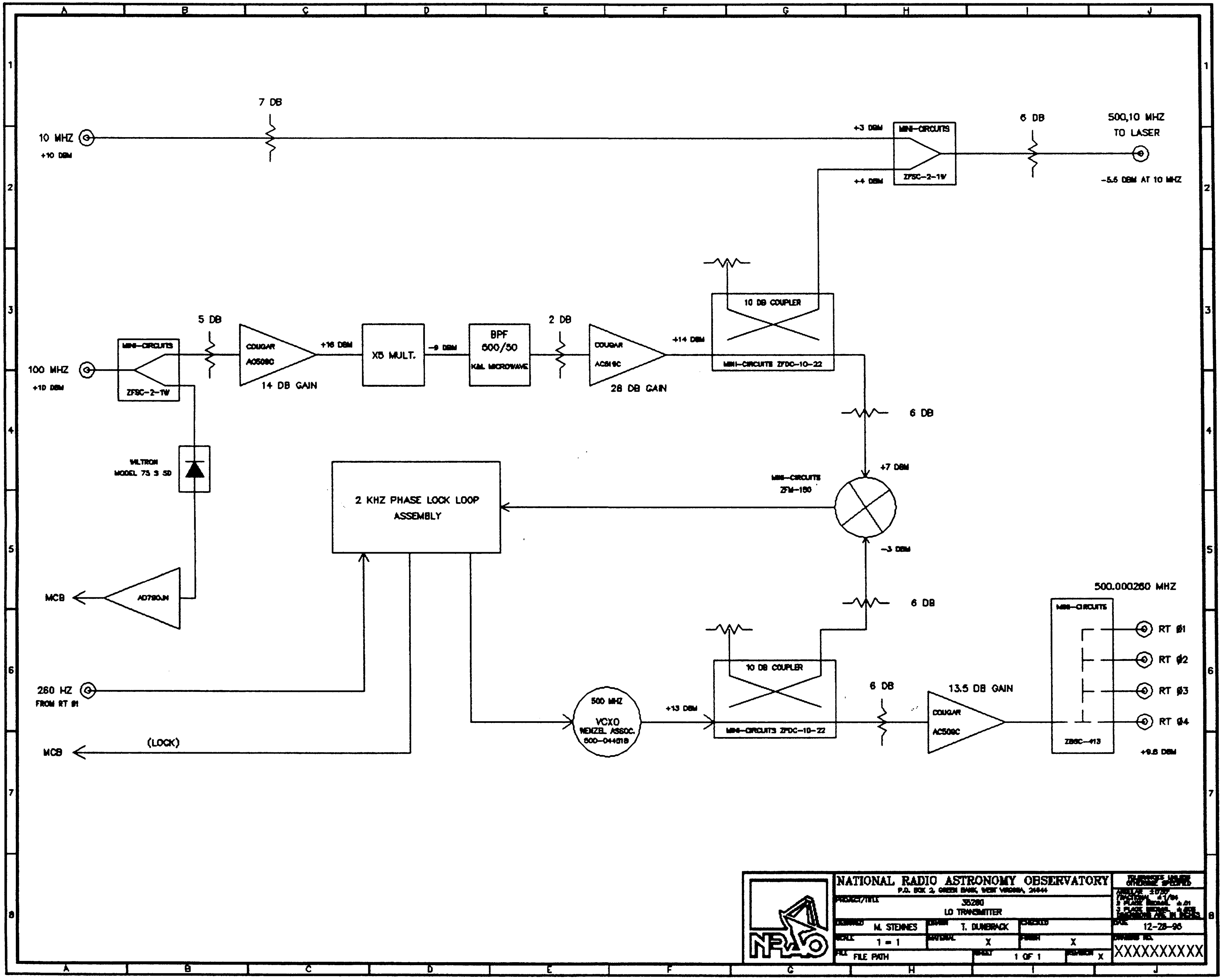
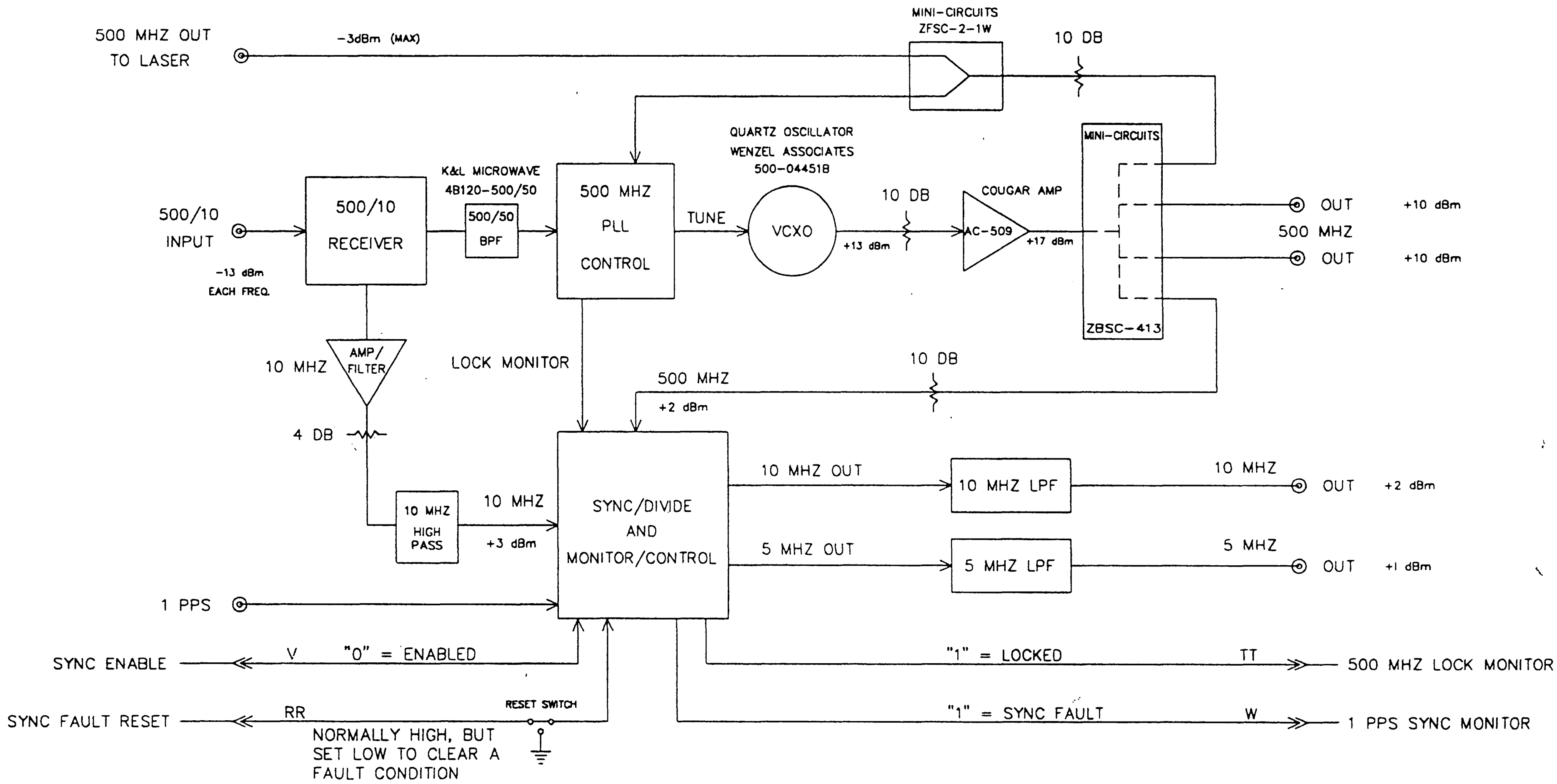


Figure 4. Typical RTPM data over a three day period.

III. Schematics


10 MHZ
+10 DBM
7 DB
+3 DBM
MINI-CIRCUITS
ZFSC-2-1W
+4 DBM
6 DB
500,10 MHZ
TO LASER
-5.5 DBM AT 10 MHZ
100 MHZ
+10 DBM
MINI-CIRCUITS
ZFSC-2-1W
5 DB
COUGAR
AC509C
14 DB GAIN
+16 DBM
X5 MULT.
-9 DBM
BPF
500/50
K&L MICROWAVE
2 DB
COUGAR
AC519C
28 DB GAIN
+14 DBM
10 DB COUPLER
MINI-CIRCUITS ZFDC-10-22
6 DB
WILTRON
MODEL 75 S 50
2 KHZ PHASE LOCK LOOP
ASSEMBLY
MINI-CIRCUITS
ZFM-150
+7 DBM
-3 DBM
6 DB
MCB
AD790JN
500.000260 MHZ
MINI-CIRCUITS
10 DB COUPLER
RT Ø1
RT Ø2
RT Ø3
RT Ø4
260 HZ
FROM RT Ø1
500 MHZ
VCXO
WENZEL ASSOC.
500-04461B
+13 DBM
MINI-CIRCUITS ZFDC-10-22
6 DB
13.5 DB GAIN
COUGAR
AC509C
ZBSC-413
+9.8 DBM
MCB
(LOCK)
NATIONAL RADIO ASTRONOMY OBSERVATORY
P.O. BOX 2, GREEN BANK, WEST VIRGINIA, 24944
35280
LO TRANSMITTER
M. STENNES
T. DUNBRACK
12-28-96
1 = 1
X
X
FILE PATH
1 OF 1
X
XXXXXXXXXX

LO RECEIVER MODULE



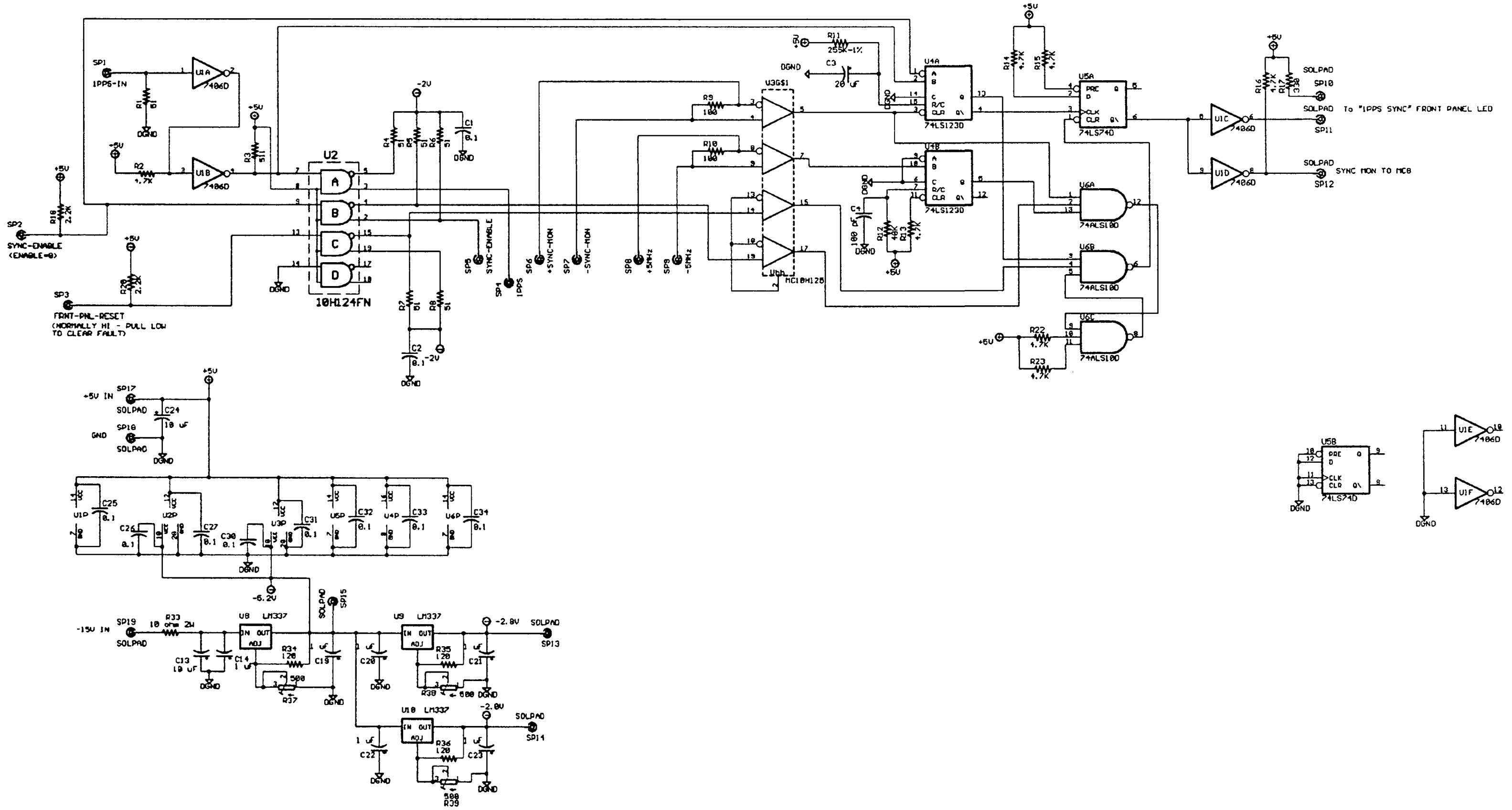
NATIONAL RADIO ASTRONOMY OBSERVATORY

LO RECEIVER MODULE

XXXXXXXXXX

REVISIONS

REVISION#	MADE BY:	DESCRIPTION	ZONE	DATE	APPROVED
A	C. NIDAY	REDREW ORIGINAL SCHEMATIC IN EAGLE; DIVIDED SCHEMATIC INTO 2 PAGES.	ALL	05 NOV 2003	
B	M. STENNES	CHANGED R3 TO 511 OHMS; CORRECTED -5V BUS TO -5.2v; CORRECTED -2V BUSS TO -2.0V.	ALL	21 APRIL 2004	



NOTES

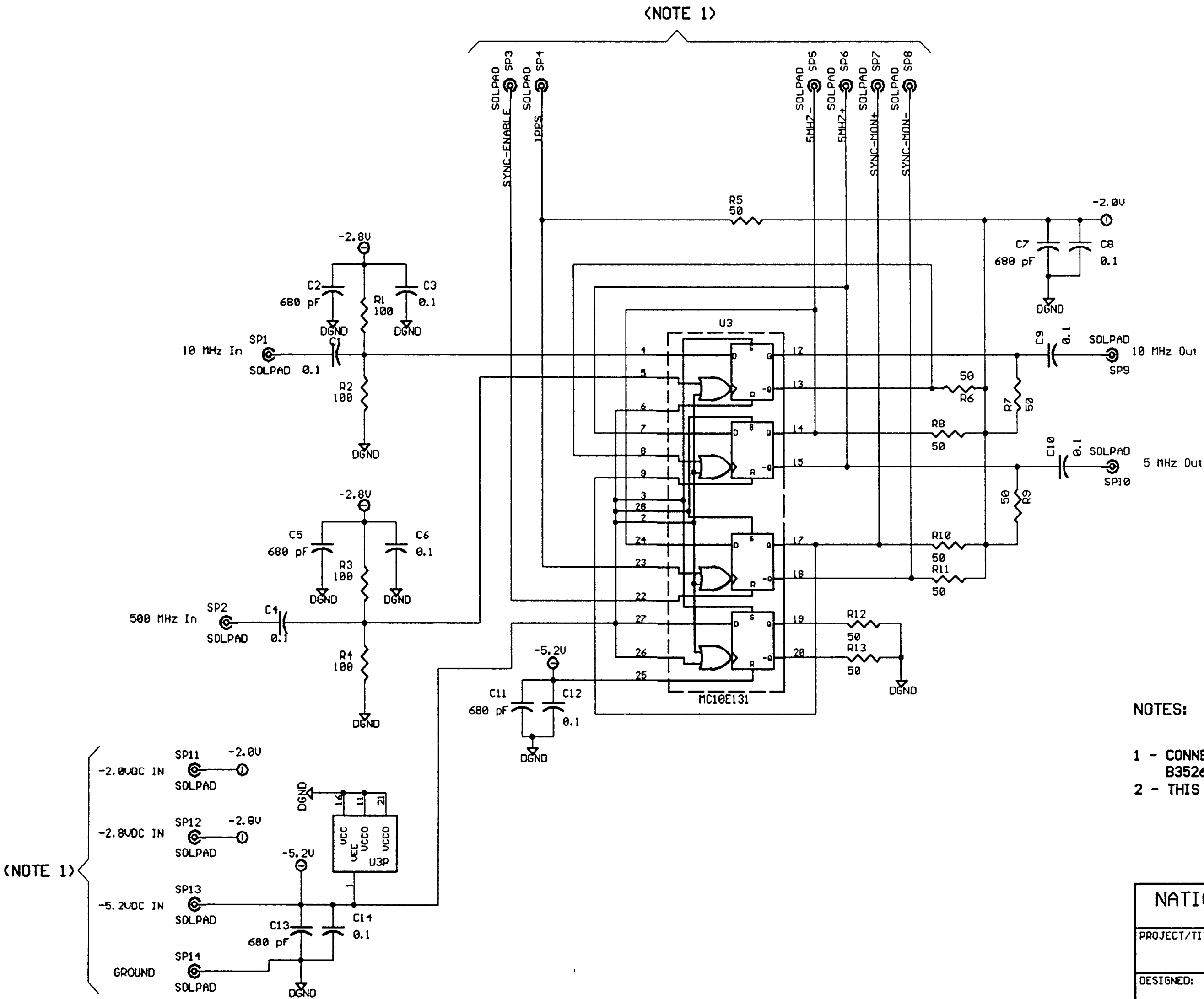
1 - CONNECTS TO BOARD 35260Q010, SCHEMATIC B35260S021A-2

2 - THIS CIRCUIT IS CONTAINED ON PC BOARD A35260Q027

NATIONAL RADIO ASTRONOMY OBSERVATORY P. O. BOX 2, GREEN BANK, WV, 24944		
PROJECT/TITLE: GBT LO RECEIVER SYNC/DIVIDE CIRCUIT (PAGE 1 OF 2)		
DESIGNED: M. STENNES	DRAWN: NIDAY	CHECKED:
DWG #: C35260S021-1	DATE SAVED: 4/21/2004 10:33:51a	REV: B
FILE NAME: LO-Rcvr-Sync-1	Sheet: 1/1	

REVISIONS

REVISION:	MADE BY:	DESCRIPTION	ZONE	DATE	APPROVED
A	C. NIDAY	REDREW SCHEMATIC IN EAGLE & BROKE INTO 2 PAGES.	ALL	04 NOV 2003	
B	M. STENNES	CORRECTED -5V BUSS TO -5.2V, AND -2V BUSS TO -2.0V	ALL	21 APRIL 2004	



NOTES:

1 - CONNECTS TO BOARD 35260Q027, SCHEMATIC B35260S021A-1
2 - THIS CIRCUIT IS FOUND ON PC BOARD 35260Q010.

NATIONAL RADIO ASTRONOMY OBSERVATORY P. O. BOX 2, GREEN BANK, WV, 24944			
PROJECT/TITLE: GBT LO RECEIVER SYNC/DIVIDE CIRCUIT (Page 2 of 2)			
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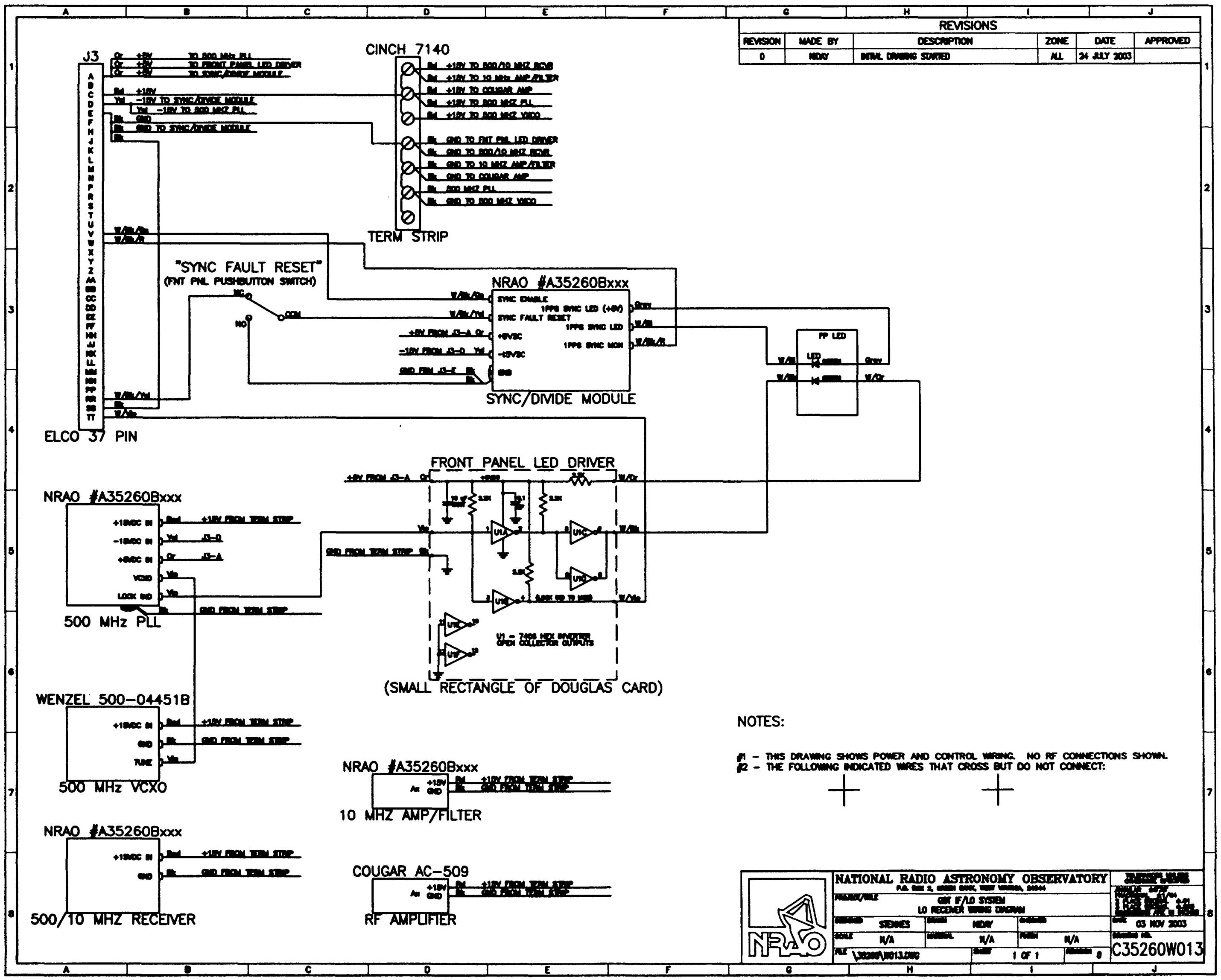
FILE NAME: LO-Rcvr-Sync-2		Sheet: 1/1	


REVISIONS
REVISION | MADE BY | DESCRIPTION | ZONE | DATE | APPROVED
0 | NIDAY | INITIAL DRAWING STARTED | ALL | 24 JULY 2003
J3
CINCH 7140
TERM STRIP
"SYNC FAULT RESET"
(FNT PNL PUSHBUTTON SWITCH)
NRAO #A35260Bxxx
SYNC/DIVIDE MODULE
FP LED
ELCO 37 PIN
FRONT PANEL LED DRIVER
NRAO #A35260Bxxx
500 MHz PLL
(SMALL RECTANGLE OF DOUGLAS CARD)
WENZEL 500-04451B
500 MHz VCXO
NRAO #A35260Bxxx
10 MHZ AMP/FILTER
NRAO #A35260Bxxx
500/10 MHZ RECEIVER
COUGAR AC-509
RF AMPLIFIER
NOTES:
#1 - THIS DRAWING SHOWS POWER AND CONTROL WIRING. NO RF CONNECTIONS SHOWN.
#2 - THE FOLLOWING INDICATED WIRES THAT CROSS BUT DO NOT CONNECT:
NATIONAL RADIO ASTRONOMY OBSERVATORY
GBT IF/LO SYSTEM
LO RECEIVER WIRING DIAGRAM
STENNES
NIDAY
03 NOV 2003
N/A
N/A
N/A
1 OF 1
0
C35260W013

IV. Component Data Sheets

REV	DATE	REVISION RECORD	DWN	AUTH
-	08-06-04	Draft	SS	GP

OUTPUT

Frequency

500 MHz

Level

+13 ±2dBm into 50 ohms

STABILITY

Aging

±1 x 10^{-6} after 30 days year one,

.5 x 10^{-6} year two

±.3 x 10^{-6} years three and beyond

Phase Noise L(f)

100 Hz	-112 dBc/Hz
1 kHz	-142 dBc/Hz
10 kHz	-150 dBc/Hz
20 kHz	-151 dBc/Hz

Temperature Stability

±5 x 10^{-7}, 0° to +50°C (Ref +25°C)

Harmonics and Sub-Harmonics

-30 dBc

MECHANICAL

Dimensions

1.94 x 2.97 x 1"

Connectors

SMA and Feedthru capacitor

Packaging

Solder sealed steel can
with threaded inserts on base

POWER REQUIREMENTS

Warm-Up Power

<6 Watts for 5 minutes

Total Power

3 Watts at +25°C

Supply Voltage

+15 VDC

ADJUSTMENT

Electrical Tuning

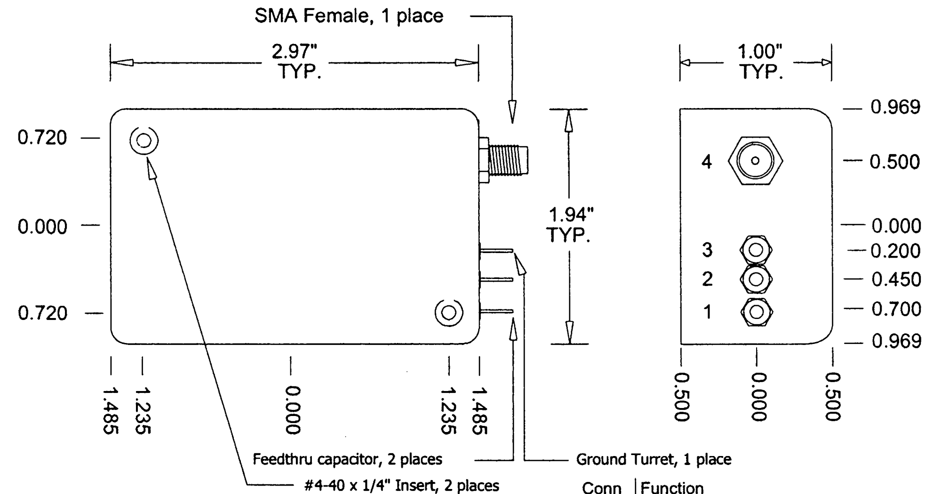
±5 x 10^{-6}, 0 to +6 VDC,

±.1 x 10^{-6} at +3 V at time of shipment,
negative slope, input impedance
>50KΩ, mod. Rate DC to 1 kHz

CRYSTAL

Type

100 MHz SC-cut 5th overtone with x5
multiplier stage



Connector numbers are for reference only, they do not appear on unit.

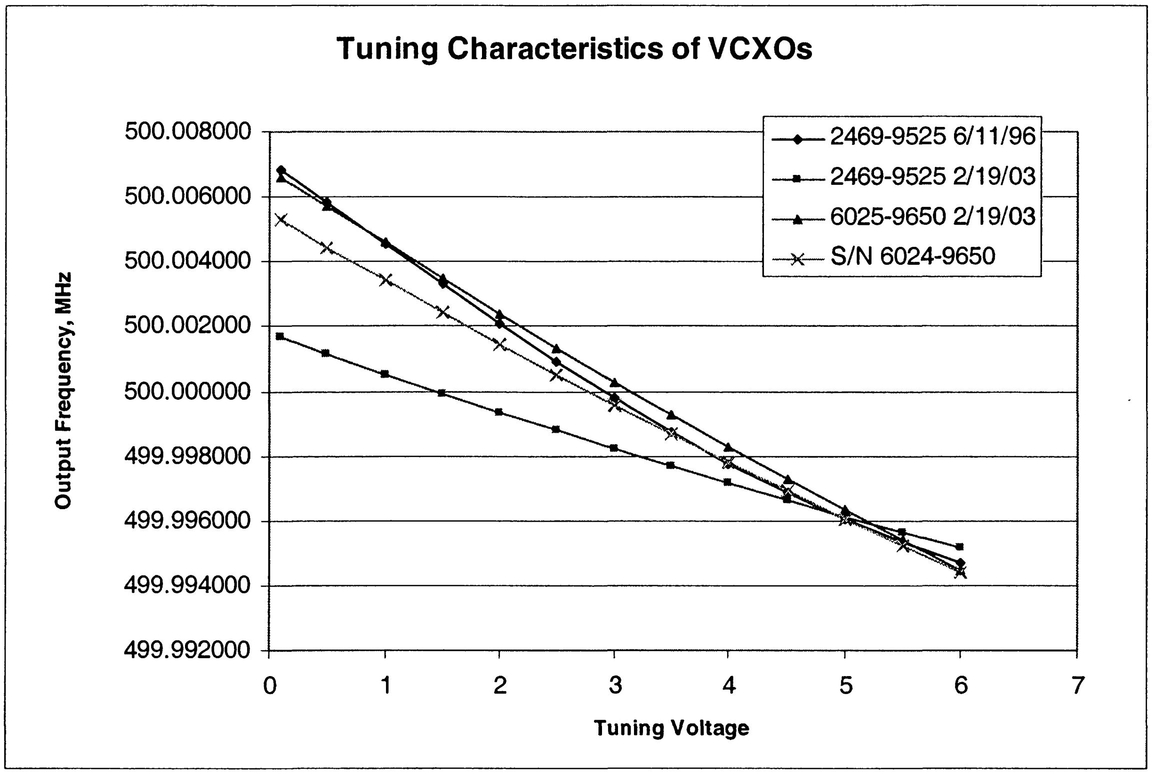
Conn	Function
1	Electrical Tuning
2	Supply Voltage
3	Ground, Case
4	RF Output

Wenzel Associates, Inc.
Austin, Texas

Title: **500 MHz-SC Crystal Oscillator**

P/N:	Rev:	Date:	Drawn:	Ref:
500-13106	-	08-06-04		500-04451

Tolerances: (except as noted) Dimensions are in inches	0.XX Dec:	0.XXX Dec:	FSCM:	
	±0.030"	±0.010"	62821	Page 1 of 1



This graph illustrates the effect of quartz resonator ageing. The tuning characteristic of oscillator serial number 2469-9525 has been monitored over time, from 1996 though the present. Notice the lowest curve, which shows a tuning voltage of 1.5 volts for f = 500.000000 MHz as was measured after approximately six years of operation. The upper curves show acceptable performance, with tuning voltage near 3.0 volts at 500.000000 MHz.

At the time of this writing, a new oscillator is being designed for this application, using an SC-cut resonator, rather than an AT-cut. The SC-cut should offer significantly longer MTBFs.

MC10E131, MC100E131

5V ECL 4-Bit D Flip-Flop

The MC10E/100E131 is a quad master-slave D-type flip-flop with differential outputs. Each flip-flop may be clocked separately by holding Common Clock (C_C) LOW and using the Clock Enable ($\overline{CE}$) inputs for clocking. Common clocking is achieved by holding the $\overline{CE}$ inputs LOW and using C_C to clock all four flip-flops. In this case, the $\overline{CE}$ inputs perform the function of controlling the common clock, to each flip-flop.

Individual asynchronous resets are provided (R). Asynchronous set controls (S) are ganged together in pairs, with the pairing chosen to reflect physical chip symmetry.

Data enters the master when both C_C and $\overline{CE}$ are LOW, and transfers to the slave when either C_C or $\overline{CE}$ (or both) go HIGH.

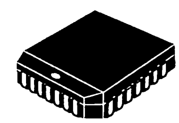
The 100 Series contains temperature compensation.

- 1100 MHz Min. Toggle Frequency
- Differential Outputs
- Individual and Common Clocks
- Individual Resets (asynchronous)
- Paired Sets (asynchronous)
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = –4.2 V to –5.7 V
- Internal Input 50 KΩ Pulldown Resistors
- Metastability Time Constant is 200 ps.
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- ESD Protection: > 2 KV HBM, > 200 V MM
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 240 devices

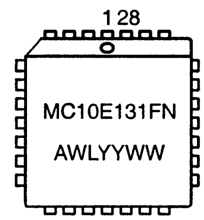
ON Semiconductor®

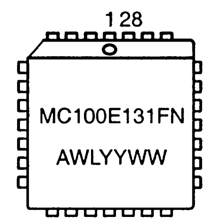
http://onsemi.com

MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776



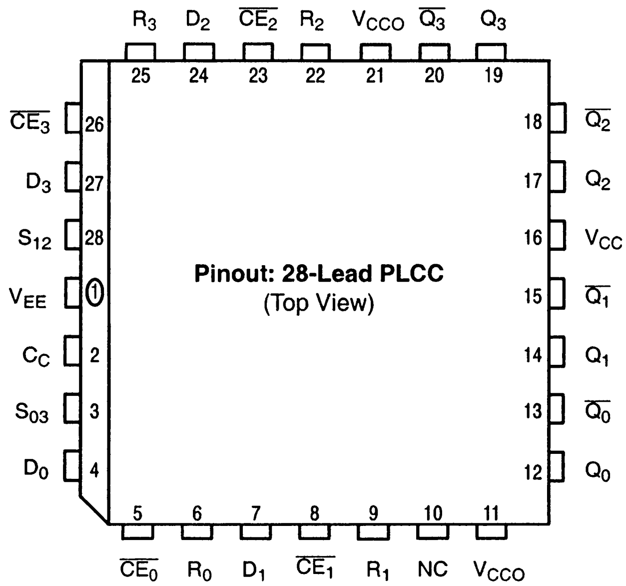


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
MC10E131FN	PLCC–28	37 Units/Rail
MC10E131FNR2	PLCC–28	500 / Tape & Reel
MC100E131FN	PLCC–28	37 Units/Rail
MC100E131FNR2	PLCC–28	500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pinout Diagram

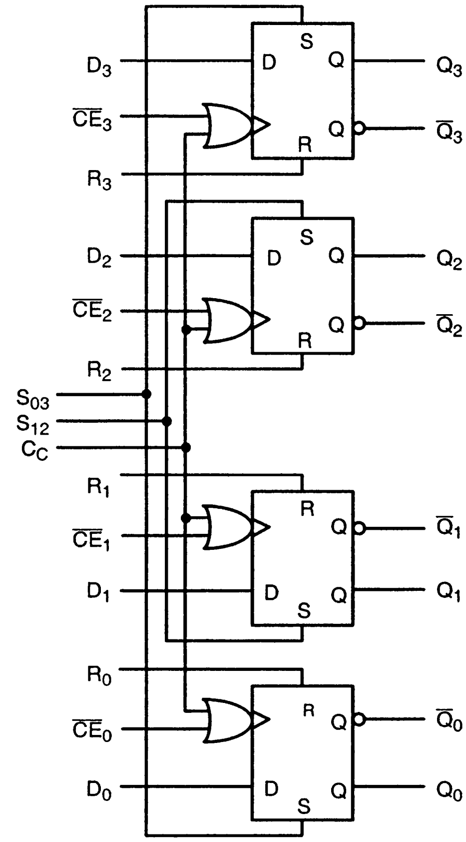


Figure 2. Logic Diagram

PIN DESCRIPTION

PIN	FUNCTION
D_0 – D_3	ECL Data Inputs
$\overline{CE}_0$ – $\overline{CE}_3$	ECL Clock Enables (Individual)
R_0 – R_3	ECL Resets
C_C	ECL Common Clock
S_{03}, S_{12}	ECL Sets (paired)
Q_0 – Q_3, $\overline{Q}_0$ – $\overline{Q}_3$	ECL Differential Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		-8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 −5.7 to −4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V (Note 2)

		−40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		58	70		58	70		58	70		58	70	mA
V_{OH}	Output HIGH Voltage (Note 3)				3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 3)				3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage				3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage				3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current C_C S R, $\overline{CE}$ D			350 450 300 150			350 450 300 150			350 450 300 150			350 450 300 150	μA
I_{IL}	Input LOW Current				0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary −0.46 V / +0.06 V.
3. Outputs are terminated through a 50 ohm resistor to V_{CC}−2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx} = 0.0 V; V_{EE} = –5.0 V (Note 4)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		58	70		58	70		58	70		58	70	mA
V_{OH}	Output HIGH Voltage (Note 5)				–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 5)				–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage				–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage				–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current C_C S R, $\overline{CE}$ D			 350 450 300 150			 350 450 300 150			 350 450 300 150			 350 450 300 150	µA
I_{IL}	Input LOW Current				0.5	0.3		0.5	0.065		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

4. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary –0.46 V / +0.06 V.
5. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V (Note 6)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		58	70		58	70		58	70		67	81	mA
V_{OH}	Output HIGH Voltage (Note 7)				3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 7)				3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage		3975		3835	3975	4120	3835	3975	4120	3835	3975	4120	mV
V_{IL}	Input LOW Voltage		3355		3190	3355	3525	3190	3355	3525	3190	3355	3525	mV
I_{IH}	Input HIGH Current C_C S R, $\overline{CE}$ D			350 450 300 150			350 450 300 150			350 450 300 150			350 450 300 150	µA
I_{IL}	Input LOW Current				0.5	0.3		0.5	0.25		0.5	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

6. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary –0.46 V / +0.8 V.
7. Outputs are terminated through a 50 ohm resistor to V_{CC} – 2 V.

REMEC

15 - 700 MHz

Hybrid Amplifiers

High Dynamic Range

Electrical Specifications [1]:

QBH-132

Parameter	Specification Limit		Units
Temperature	+25	-55 to +85	°C
Frequency Range	15 - 700		MHz
Small Signal Gain	14.8 ± 0.6		dB
Gain vs. Temperature		+0.5 / -1.0	dB Max
Gain Flatness	0.8	1.4	dB Max p-p
Reverse Isolation	27	26	dB Min
VSWR Input	1.7:1	1.8:1	Max
Output	1.7:1	1.8:1	Max
1 dB Compression	+16	+15.5	dBm Min
Output Intercept Point			
3rd Order	+29	+27	dBm Min
2nd Order	+39	+37	dBm Min
Noise Figure	6.5	7.0	dB Max
DC Power @ 15 Vdc ± 1%	44	45	mA Max
Gain vs. Vdc	0.15		dB/Volt Max
Housing	TO-8 (E52-1213)		

Notes:
1. Specifications are guaranteed when tested in a 50 Ohm system. Specifications indicated as typical are not guaranteed.

Absolute Maximum Ratings

Power Supply Voltage
- Sustaining . . . . .16.5 Vdc
- Pulse (transient) . . . . .21.0 Vdc

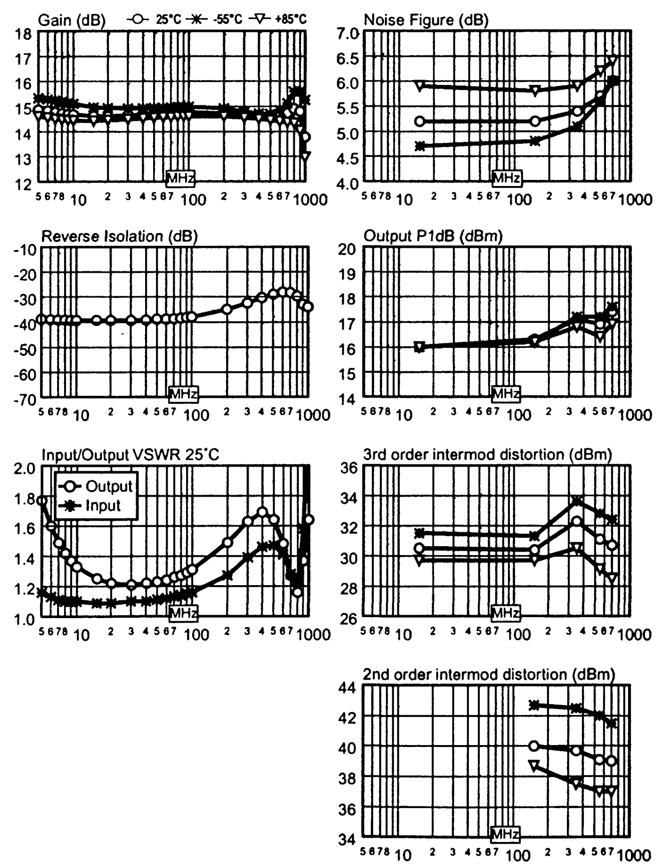
Temperature
- Operating . . . .-55 to +125°C
- Storage . . . .-65 to +150°C

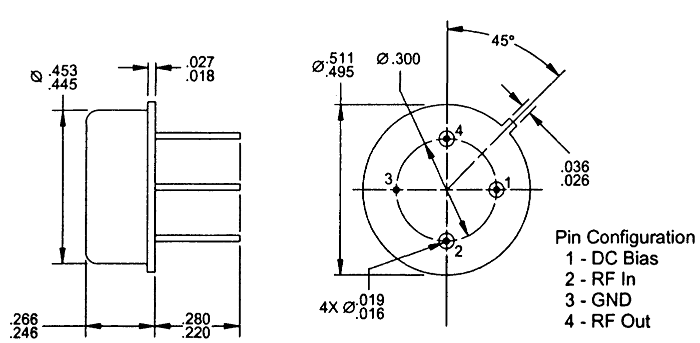
Max Input Drive . . . . .1.4 VRMS

Thermal Rise, junction-to-case . . . .+16°C

Typical S-Parameter Data

	S11		S21		S12		S22	
MHz	dB	Ang	dB	Ang	dB	Ang	dB	Ang
15	-27.3	11.5	14.6	-177.0	-39.3	7.7	-19.1	78.0
40	-26.1	-18.8	14.7	171.2	-39.2	9.1	-20.2	54.7
60	-24.9	-35.5	14.7	164.1	-38.8	10.8	-19.4	44.8
80	-23.7	-48.9	14.7	157.4	-38.5	13.0	-18.4	38.1
100	-22.5	-60.8	14.8	150.9	-37.9	15.0	-17.6	32.9
300	-15.9	-134.3	14.7	87.5	-32.4	2.9	-12.4	-19.1
500	-14.4	170.9	14.6	24.4	-28.9	-33.5	-12.4	-74.4
700	-18.5	100.8	14.7	-41.1	-28.3	-80.6	-18.5	-116.4





Dimensions are in inches

DS-327

M/A-COM Flatpack Two-Way Power Divider, 5 - 1000 MHz

V 3.00

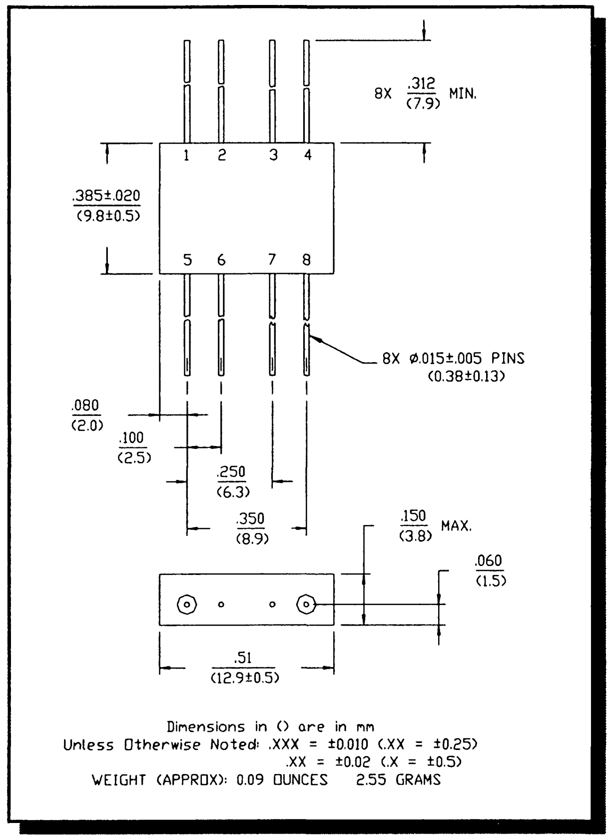
Features

- Broadband, IN Phase Divider
- Low Loss: 0.3 dB Typical
- Amplitude Balance: 0.05 dB Typical
- Impedance: 50 Ohms Nominal
- Maximum Power Rating or Input Power: 1 Watt Max.
- Internal Load Dissipation: 0.05 Watts Max.
- MIL-STD-883 Screening Available

Description

A Power Divider is ideally a loss less reciprocal device which can also perform vector summation of two or more signals and thus is sometimes called a power combiner or summer.

FP-2



Pin Configuration

Pin No.	Function	Pin No.	Function
1	Σ	5	GND
2	GND	6	GND
3	GND	7	GND
4	Output C	8	Output D

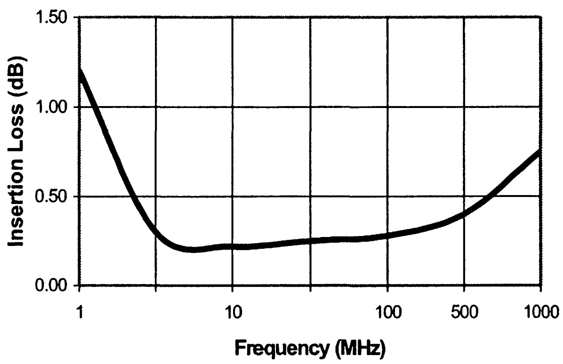
Electrical Specifications[1]: T_A = -55°C to +85°C

Parameter	Test Conditions	Frequency	Units	Min	Typ	Max
Insertion Loss	Less Coupling	5 - 500 MHz 500 - 1000 MHz	dB dB	— —	— —	0.5 1.0
Isolation	—	5 - 500 MHz 500 - 1000 MHz	dB dB	25 20	— —	— —
Amplitude Balance	—	5 - 1000 MHz	dB	—	—	0.2
Phase Balance	—	5 - 500 MHz 500 - 1000 MHz	° °	— —	— —	2 3
VSWR	Input Output	10 - 500 MHz 5 - 1000 MHz	Ratio Ratio	— —	— —	1.3:1 1.5:1

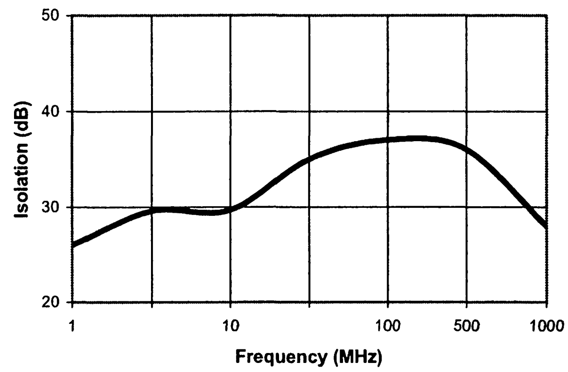
1. All specifications apply with 50 ohm source and load impedance.

Typical Performance Curves

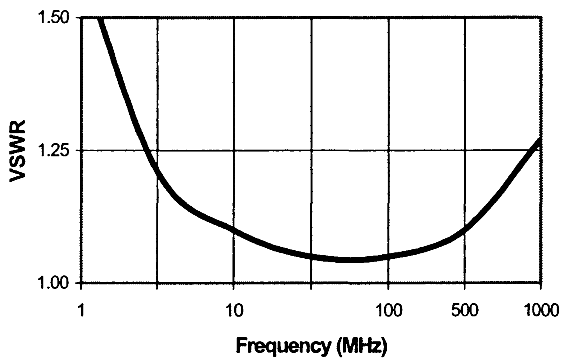
Insertion Loss



Isolation



VSWR



Ordering Information

Part Number	Package
DS-327 PIN	FP-2

- **North America:** Tel. (800) 366-2266
- **Asia/Pacific:** Tel.+81-44-844-8296, Fax +81-44-844-8298
- **Europe:** Tel. +44 (1344) 869 595, Fax+44 (1344) 300 020

tyco / Electronics M/A-COM

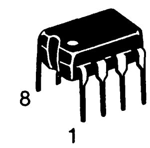
LM393, LM293, LM2903, LM2903V, NCV2903

Low Offset Voltage Dual Comparators

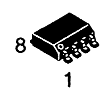
The LM393 series are dual independent precision voltage comparators capable of single or split supply operation. These devices are designed to permit a common mode range–to–ground level with single supply operation. Input offset voltage specifications as low as 2.0 mV make this device an excellent selection for many applications in consumer, automotive, and industrial electronics.

ON Semiconductor®

http://onsemi.com



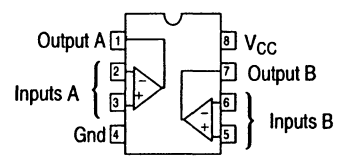
PDIP–8
N SUFFIX
CASE 626



SOIC–8
D SUFFIX
CASE 751

Micro8™
DM SUFFIX
CASE 846A

PIN CONNECTIONS



(Top View)

ORDERING & DEVICE MARKING INFORMATION

See detailed ordering and shipping information and marking information in the package dimensions section on page 6 of this data sheet.

Features

- Wide Single–Supply Range: 2.0 Vdc to 36 Vdc
- Split–Supply Range: ±1.0 Vdc to ±18 Vdc
- Very Low Current Drain Independent of Supply Voltage: 0.4 mA
- Low Input Bias Current: 25 nA
- Low Input Offset Current: 5.0 nA
- Low Input Offset Voltage: 5.0 mV (max) LM293/393
- Input Common Mode Range to Ground Level
- Differential Input Voltage Range Equal to Power Supply Voltage
- Output Voltage Compatible with DTL, ECL, TTL, MOS, and CMOS Logic Levels
- ESD Clamps on the Inputs Increase the Ruggedness of the Device without Affecting Performance
- Pb–Free Packages are Available

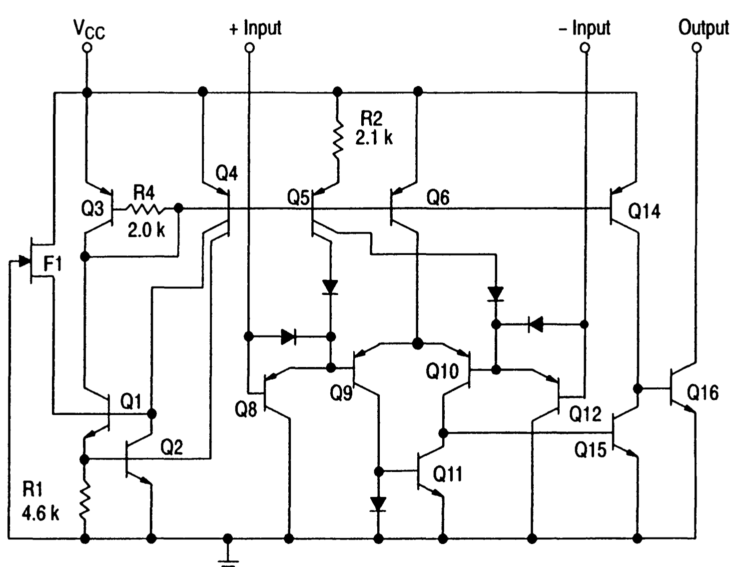


Figure 1. Representative Schematic Diagram
(Diagram shown is for 1 comparator)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	−0.3 to +36	Vdc
Output Short Circuit–to–Ground Output Sink Current (Note 1)	I_{SC} I_{Sink}	Continuous 20	mA
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D $1/R_{\theta JA}$	570 5.7	mW mW/°C
Operating Ambient Temperature Range LM293 LM393 LM2903 LM2903V, NCV2903 (Note 2)	T_A	 −25 to +85 0 to +70 −40 to +105 −40 to +125	°C
Maximum Operating Junction Temperature LM393, 2903, LM2903V LM293, NCV2903	$T_{J(max)}$	 150 150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
ESD Protection at any Pin – Human Body Model – Machine Model	V_{esd}	 2000 200	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. *NCV2903 is qualified for automotive use.*

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ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, $T_{low} \le T_A \le T_{high}$, unless otherwise noted.)

Characteristic	Symbol	LM293, LM393			LM2903, LM2903V, NCV2903			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}							mV
T_A = 25°C		–	±1.0	±5.0	–	±2.0	±7.0	
$T_{low} \le T_A \le T_{high}$		–	–	9.0	–	9.0	15	
Input Offset Current	I_{IO}							nA
T_A = 25°C		–	±5.0	±50	–	±5.0	±50	
$T_{low} \le T_A \le T_{high}$		–	–	±150	–	±50	±200	
Input Bias Current (Note 5)	I_{IB}							nA
T_A = 25°C		–	25	250	–	25	250	
$T_{low} \le T_A \le T_{high}$		–	–	400	–	200	500	
Input Common Mode Voltage Range (Note 5)	V_{ICR}							V
T_A = 25°C		0	–	V_{CC} −1.5	0	–	V_{CC} −1.5	
$T_{low} \le T_A \le T_{high}$		0	–	V_{CC} −2.0	0	–	V_{CC} −2.0	
Voltage Gain $R_L \ge$ 15 kΩ, V_{CC} = 15 Vdc, T_A = 25°C	A_{VOL}	50	200	–	25	200	–	V/mV
Large Signal Response Time V_{in} = TTL Logic Swing, V_{ref} = 1.4 Vdc V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C	–	–	300	–	–	300	–	ns
Response Time (Note 7) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C	t_{TLH}	–	1.3	–	–	1.5	–	μs
Input Differential Voltage (Note 8) All $V_{in} \ge$ Gnd or V– Supply (if used)	V_{ID}	–	–	V_{CC}	–	–	V_{CC}	V
Output Sink Current $V_{in} \ge$ 1.0 Vdc, V_{in+} = 0 Vdc, $V_O \le$ 1.5 Vdc T_A = 25°C	I_{Sink}	6.0	16	–	6.0	16	–	mA
Output Saturation Voltage	V_{OL}							mV
$V_{in} \ge$ 1.0 Vdc, V_{in+} = 0, $I_{Sink} \le$ 4.0 mA, T_A = 25°C		–	150	400	–	–	400	
$T_{low} \le T_A \le T_{high}$		–	–	700	–	200	700	
Output Leakage Current	I_{OL}							nA
V_{in-} = 0 V, $V_{in+} \ge$ 1.0 Vdc, V_O = 5.0 Vdc, T_A = 25°C		–	0.1	–	–	0.1	–	
V_{in-} = 0 V, $V_{in+} \ge$ 1.0 Vdc, V_O = 30 Vdc, $T_{low} \le T_A \le T_{high}$		–	–	1000	–	–	1000	
Supply Current	I_{CC}							mA
$R_L = \infty$ Both Comparators, T_A = 25°C		–	0.4	1.0	–	0.4	1.0	
$R_L = \infty$ Both Comparators, V_{CC} = 30 V		–	–	2.5	–	–	2.5	

LM293 T_{low} = −25°C, T_{high} = +85°C
LM393 T_{low} = 0°C, T_{high} = +70°C
LM2903 T_{low} = −40°C, T_{high} = +105°C
LM2903V & NCV2903 T_{low} = −40°C, T_{high} = +125°C
NCV2903 is qualified for automotive use.

3. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.
4. At output switch point, $V_O \simeq$ 1.4 Vdc, R_S = 0 Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the full input common mode range (0 V to V_{CC} = −1.5 V).
5. Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, therefore, no loading changes will exist on the input lines.
6. Input common mode of either input should not be permitted to go more than 0.3 V negative of ground or minus supply. The upper limit of common mode range is V_{CC} −1.5 V.
7. Response time is specified with a 100 mV step and 5.0 mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.
8. The comparator will exhibit proper output state if one of the inputs becomes greater than V_{CC}, the other input must remain within the common mode range. The low input state must not be less than −0.3 V of ground or minus supply.

LM293/393

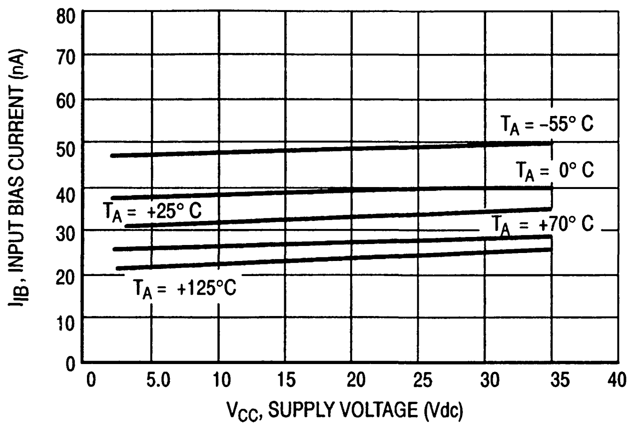


Figure 2. Input Bias Current versus Power Supply Voltage

LM2903

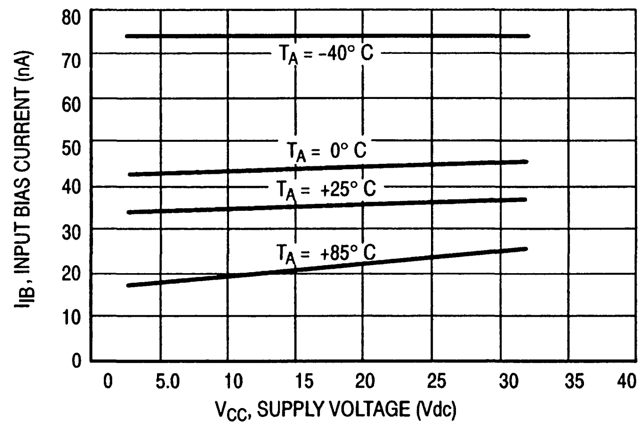


Figure 3. Input Bias Current versus Power Supply Voltage

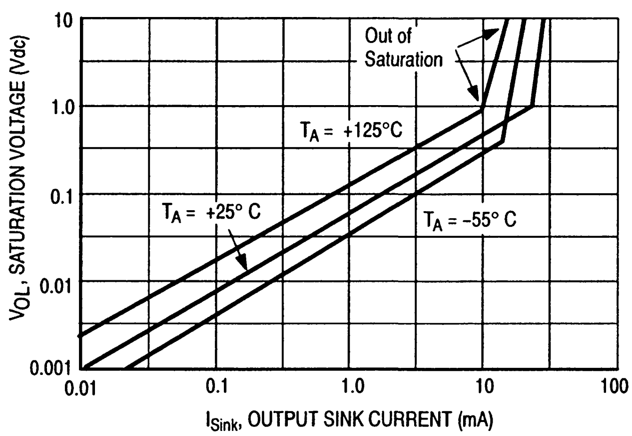


Figure 4. Output Saturation Voltage versus Output Sink Current

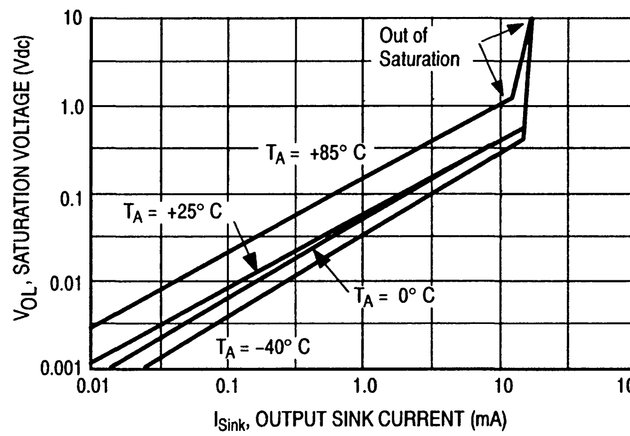


Figure 5. Output Saturation Voltage versus Output Sink Current

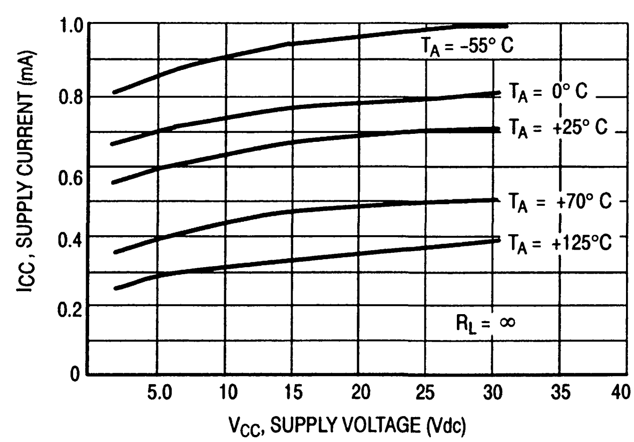


Figure 6. Power Supply Current versus Power Supply Voltage

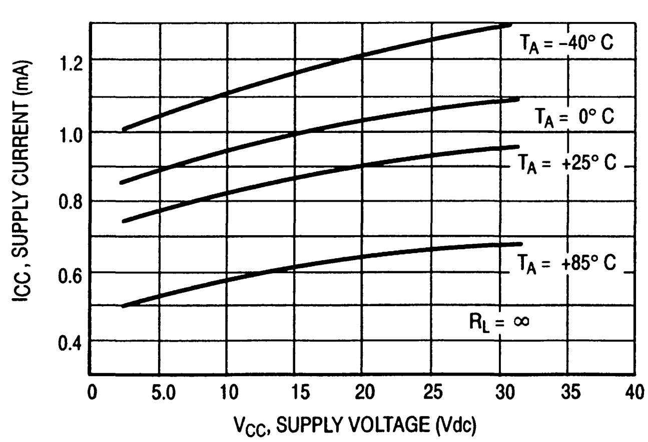


Figure 7. Power Supply Current versus Power Supply Voltage

JH-140

High Frequency Quadrature Hybrid, 500 - 1000 MHz

V 3.00

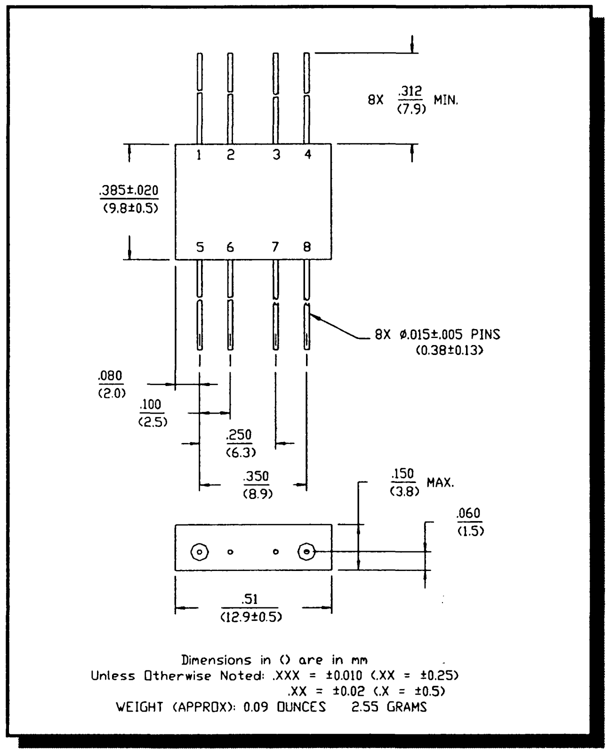
Features

- Octave Bandwidth
- Low VSWR: 1.2:1 Typical
- Miniature Size: 1/2" x 3/8" Flatpack
- Impedance: 50 Ohms Nominal
- Input Power: 25 Watts Max @ +25°C, Derated to 1 Watt @ +85°C
- MIL-STD-202 Screening Available

Description

3 dB Hybrids are ideal for dividing a signal into two signals of equal amplitude and a constant 90° or 180° phase differential and for Quadrature combining or performing summation/differential combining.

FP-2



Phasing Diagram

IN \ OUT	A	B	C	D
A		ISO	-90°	0°
B	ISO		0°	-90°
C	-90°	0°		ISO
D	0°	-90°	ISO	

Pin Configuration

Pin No.	Function	Pin No.	Function
1	A	5	D
2	GND	6	GND
3	GND	7	GND
4	B	8	C

Electrical Specifications[1]: T_A = -55°C to +85°C

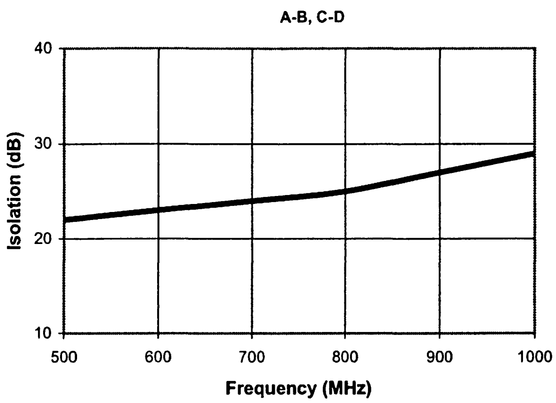
Parameter	Test Conditions	Frequency	Units	Min	Typ	Max
Insertion Loss [2]	Less Coupling	500 - 1000 MHz	dB	—	—	0.3
Isolation	—	500 - 1000 MHz	dB	18	—	—
Amplitude Balance	—	500 - 1000 MHz	dB	—	—	1.0
VSWR	—	500 - 1000 MHz	Ratio	—	—	1.3:1
Deviation from Quadrature	—	500 - 1000 MHz	°	—	—	3

1. All specifications apply with 50 ohm source and load impedance.
2. Average of coupled output less 3 dB.

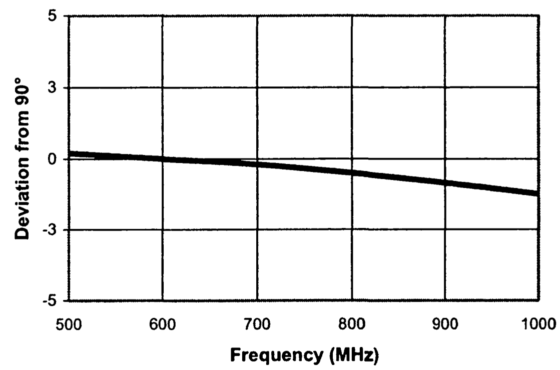
This product contains elements protected by United States Patent Number 3,484,724.

Typical Performance Curves

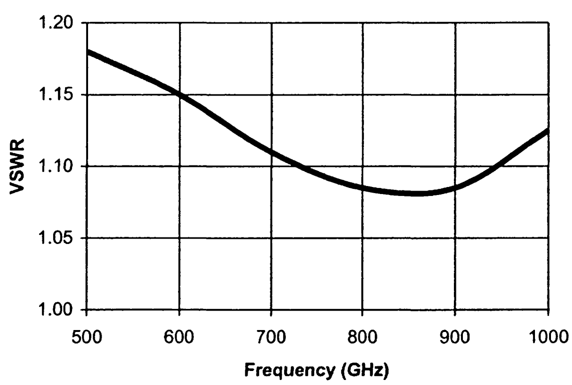
Isolation



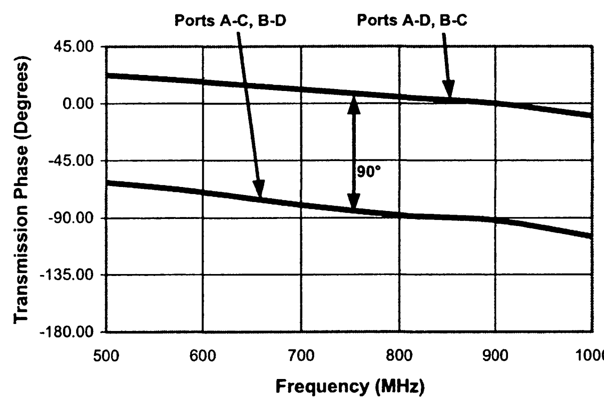
Deviation from Quadrature



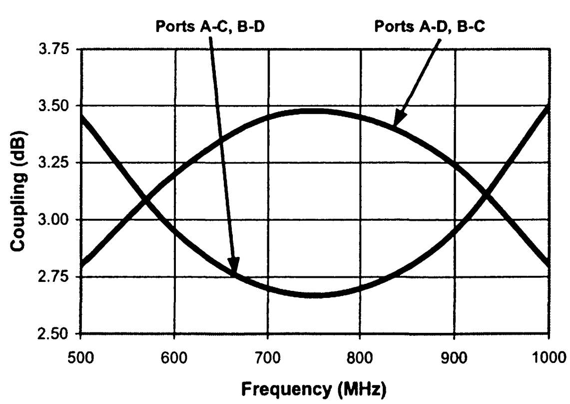
VSWR



Transmission Phase



Coupling



Ordering Information

Part Number	Package
JH-140 PIN	FP-2

- **North America:** Tel. (800) 366-2266
- **Asia/Pacific:** Tel.+81-44-844-8296, Fax +81-44-844-8298
- **Europe:** Tel. +44 (1344) 869 595, Fax+44 (1344) 300 020

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Amplifier

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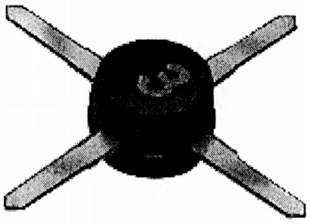


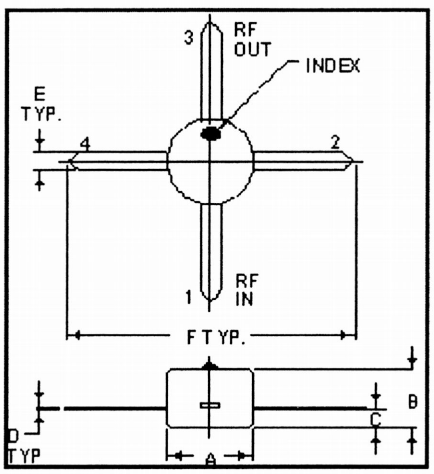
MAV-11

Frequency MHz	GAIN, dB		Maximum Power, dBm		Dynamic Range		VSWR		Absolute Maximum Rating		DC Power		Thermal resistance Øjc °C/W
f_L - f_U	Min.	Typ. Flatness	Output (1 dB Comp.)	Input (no damage)	NF dB Typ.	IP3 dBm Typ.	In Typ.	Out Typ.	I (mA)	P (mW)	Current (mA)	Device Volt(V.)	
50-1000	9.50	±0.70	+18.20	+13.00	4.40	34.00	1.30	1.20	80.00	460.00	60.00	5.50	141.00

L_W=low range(f_L to f_U/2) U=upper range(f_U/2 to f_U)

Pin Connections

Port	RF in	RF Out	DC	Case GND	Not Used
cb	1	3	3	2,4	-



Case Style - BBB123 (inch,mm) weight: 0.015 grams.

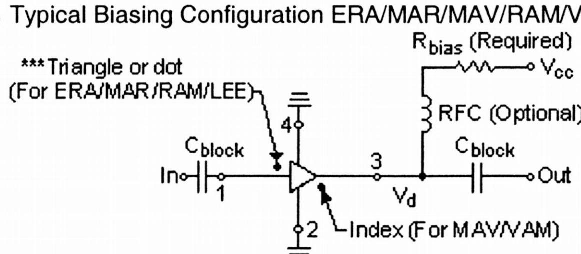
A	B	C	D	E	F	G	H	J
.145	.100	.04	.006	.030	.488			
3.683	2.540	1.016	0.152	0.762	12.395			

K	L	M	N	P	Q	R	S	T

Tolerance: .x ± .1 .xx ± .03 .xxx ± .015 inch.
Material and Finish:
Case material: plastic. Lead finish: tin-lead plate or tin plate.
Marking:
RF output is identified by index mark, model dash number by alphanumeric code.
Special Tolerances:
Lead width ±.010 inch; lead thickness ±.003 inch.

Notes:

- Minimum gain at highest frequency. Full temperature range, except room temperature for Dash-4 models.
- Thermal resistance Øjc is from hottest junction in the device to the mounting surface of the leads.
- Model number designated by alphanumeric code marking.
- Permanent damage may occur if any of these limits are exceeded. These ratings are not intended for continuous normal operation.
- For Amplifier Selection Guide, please click here.
  For Amplifier Environmental Specifications, please click here.
- For Surface Mount Environmental Specifications, please click here.
  Re-flow soldering information is available in "Surface Mount" article.
- Low frequency cutoff determined by external coupling capacitors.
- Frequency at which output power, NF and IP3 are specified: 500 MHz.
- Typical Biasing Configuration ERA/MAR/MAV/RAM/VAM



*** For RAM models, Pin 1 is identified by a diagonally cut lead.

- Prefix letter (optional) designates assembly location.
- Supply voltage must be connected to pin 3 through a bias resistor in order to prevent damage. See Biasing MMIC Amplifiers. Reliability predictions are applicable at specified current and normal operating conditions.
- Aqueous washable.
- General Quality Control Procedures and Environmental Specifications are given in Mini- Circuits Guarantees Quality.
  Hi-Rel, MIL description are given in Hi-Rel and MIL
- Prices and Specifications subjects to change without notice.

Typical Performance Data

FREQ	S_{11} (Input Return	S_{21} (Power	S_{12} (Isolation	S_{22} (

33

(MHz)	Loss)			Gain)		Out-in)			Return Loss)		
	dB	Mag	Ang	dB	Ang	dB	Mag	Ang	dB	Mag	Ang
50.00	-16.79	0.14	-72.26	12.96	167.00	-16.61	0.15	7.30	-18.23	0.12	-81.1
100.31	-21.58	0.08	-72.34	12.60	169.51	-16.53	0.15	2.12	-25.47	0.05	-86.5
150.62	-23.55	0.07	-71.81	12.50	168.94	-16.54	0.15	-0.24	-31.27	0.03	-84.6
200.93	-24.38	0.06	-73.27	12.44	167.50	-16.58	0.15	-1.93	-38.02	0.01	-71.3
251.24	-24.69	0.06	-75.88	12.40	165.73	-16.61	0.15	-3.22	-44.01	0.01	-17.9
301.55	-24.67	0.06	-79.35	12.35	163.77	-16.66	0.15	-4.27	-39.98	0.01	31.8
351.86	-24.51	0.06	-83.79	12.31	161.75	-16.71	0.15	-5.26	-36.10	0.02	46.2
402.17	-24.24	0.06	-88.42	12.26	159.66	-16.76	0.15	-6.19	-33.77	0.02	50.9
452.48	-23.94	0.06	-92.70	12.21	157.55	-16.80	0.14	-6.98	-32.15	0.02	51.7
502.79	-23.60	0.07	-97.36	12.16	155.43	-16.85	0.14	-7.73	-31.02	0.03	51.6
553.10	-23.19	0.07	-101.78	12.11	153.30	-16.90	0.14	-8.48	-30.06	0.03	50.2
603.41	-22.71	0.07	-106.12	12.05	151.17	-16.96	0.14	-9.14	-29.42	0.03	49.5
653.72	-22.31	0.08	-110.84	11.99	149.09	-17.00	0.14	-9.68	-29.03	0.04	50.4
698.44	-21.97	0.08	-114.48	11.93	147.26	-17.02	0.14	-10.26	-28.68	0.04	50.4
704.03	-21.94	0.08	-114.90	11.92	147.03	-17.03	0.14	-10.31	-28.57	0.04	49.9
754.34	-21.57	0.08	-119.11	11.86	144.95	-17.07	0.14	-10.95	-28.16	0.04	49.8
804.65	-21.22	0.09	-122.62	11.79	142.90	-17.11	0.14	-11.54	-27.85	0.04	48.7
854.96	-20.87	0.09	-126.17	11.72	140.87	-17.14	0.14	-12.13	-27.66	0.04	47.7
905.27	-20.53	0.09	-129.53	11.66	138.85	-17.18	0.14	-12.73	-27.37	0.04	46.5
955.58	-20.19	0.10	-132.82	11.59	136.89	-17.22	0.14	-13.25	-27.15	0.04	46.0
1000.30	-19.92	0.10	-135.61	11.52	135.12	-17.24	0.14	-13.79	-26.99	0.04	46.0
1100.92	-19.36	0.11	-141.55	11.38	131.21	-17.31	0.14	-14.92	-26.81	0.05	43.3
1201.54	-18.77	0.12	-146.64	11.24	127.36	-17.38	0.14	-16.02	-26.53	0.05	40.3
1302.16	-18.27	0.12	-151.74	11.09	123.61	-17.45	0.13	-17.12	-26.37	0.05	38.1
1402.78	-17.85	0.13	-156.40	10.95	119.90	-17.52	0.13	-18.22	-26.17	0.05	35.0
1503.40	-17.43	0.13	-160.64	10.80	116.24	-17.59	0.13	-19.31	-26.02	0.05	30.4
1604.02	-17.03	0.14	-164.69	10.65	112.65	-17.67	0.13	-20.38	-25.82	0.05	26.9
1704.64	-16.67	0.15	-168.52	10.50	109.09	-17.75	0.13	-21.46	-25.43	0.05	23.5
1805.26	-16.36	0.15	-172.07	10.36	105.62	-17.83	0.13	-22.51	-25.12	0.06	19.3
1900.29	-16.10	0.16	-175.39	10.23	102.40	-17.91	0.13	-23.49	-24.63	0.06	16.2
2000.91	-15.82	0.16	-179.06	10.08	98.97	-17.99	0.13	-24.60	-24.28	0.06	13.0
2101.53	-15.60	0.17	177.23	9.94	95.57	-18.08	0.12	-25.66	-23.80	0.06	10.5
2202.15	-15.37	0.17	173.45	9.80	92.27	-18.18	0.12	-26.79	-23.39	0.07	8.49
2302.77	-15.13	0.18	169.71	9.65	88.99	-18.28	0.12	-27.82	-22.98	0.07	5.75
2403.39	-14.89	0.18	166.21	9.51	85.77	-18.39	0.12	-28.86	-22.53	0.07	4.51
2504.01	-14.63	0.19	162.21	9.38	82.59	-18.51	0.12	-29.85	-22.04	0.08	4.00
2604.63	-14.34	0.19	158.39	9.25	79.43	-18.63	0.12	-30.79	-21.53	0.08	4.20
2705.25	-14.07	0.20	154.34	9.11	76.28	-18.77	0.12	-31.75	-21.06	0.09	4.72
2800.28	-13.80	0.20	150.57	8.99	73.29	-18.88	0.11	-32.55	-20.59	0.09	5.03
2900.90	-13.49	0.21	146.62	8.86	70.19	-19.02	0.11	-33.47	-20.06	0.10	5.09
3001.52	-13.21	0.22	142.49	8.73	67.06	-19.16	0.11	-34.23	-19.54	0.11	6.37

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References

1. VLBA Technical Report No. 23, "Round-Trip Phase Measurement Module" L103, R. Weimer. February 1994.

2. VLBA Technical Report No. 7, "LO Transmitter Module (L102) and LO Receiver Module (L105)", A. R. Thompson, February 10, 1993.

3. "Transmission of timing references to sub-picosecond precision over optical fiber", L. R. D'Addario and M. J. Stennes, Proc. SPIE, 3357, 1998.