HYSPEC MEMO NO. 1

NATIONAL RADIO ASTRONOMY OBSERVATORY
Charlottesville, Virginia

November 13, 1985

MEMORANDUM:

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SUBJECT: Hybrid Correlator

This memo gives a summary of the Tucson hybrid correlator. Control parameters and input/output signals are described.

I. System Architecture

Figure 1 shows the rack layout of the full system planned. One R.F. rack holds 32 double-sideband filter modules which yield a total of 64 37.5 MHz bandwidth (1 dB bandwidth) signals. Also included in the R.F. rack is one wirewrap digital card that has 64 counters and is used to measure the frequency output of 64 V/F converters driven by power detectors in the filter modules. A 65th counter counts a reference clock and acts as a time base for the frequency measurement. Frequency measurements are taken only when the system data valid line is permissive. Separate frequency accumulations are kept for 8 different conditions (4 possible L.O. frequency settings and signal/reference).

A second digital card in the R.F. rack has a microprocessor that (1) programs the DSB mixer phase-lock-loops, (2) controls zero set and AGC leveling, and (3) scans and digitizes analog points brought out of the DSB filter modules.

The digital rack provides samplers, signal distribution, multiplication, integration, and digital control functions.

The samplers consist of 64 100 mega-sample/sec, three-level quantizers which use Plessy SP9687 high-speed comparators for signal clippers and 10231 flip-flops capturing the asynchronous clipper outputs as samplers.

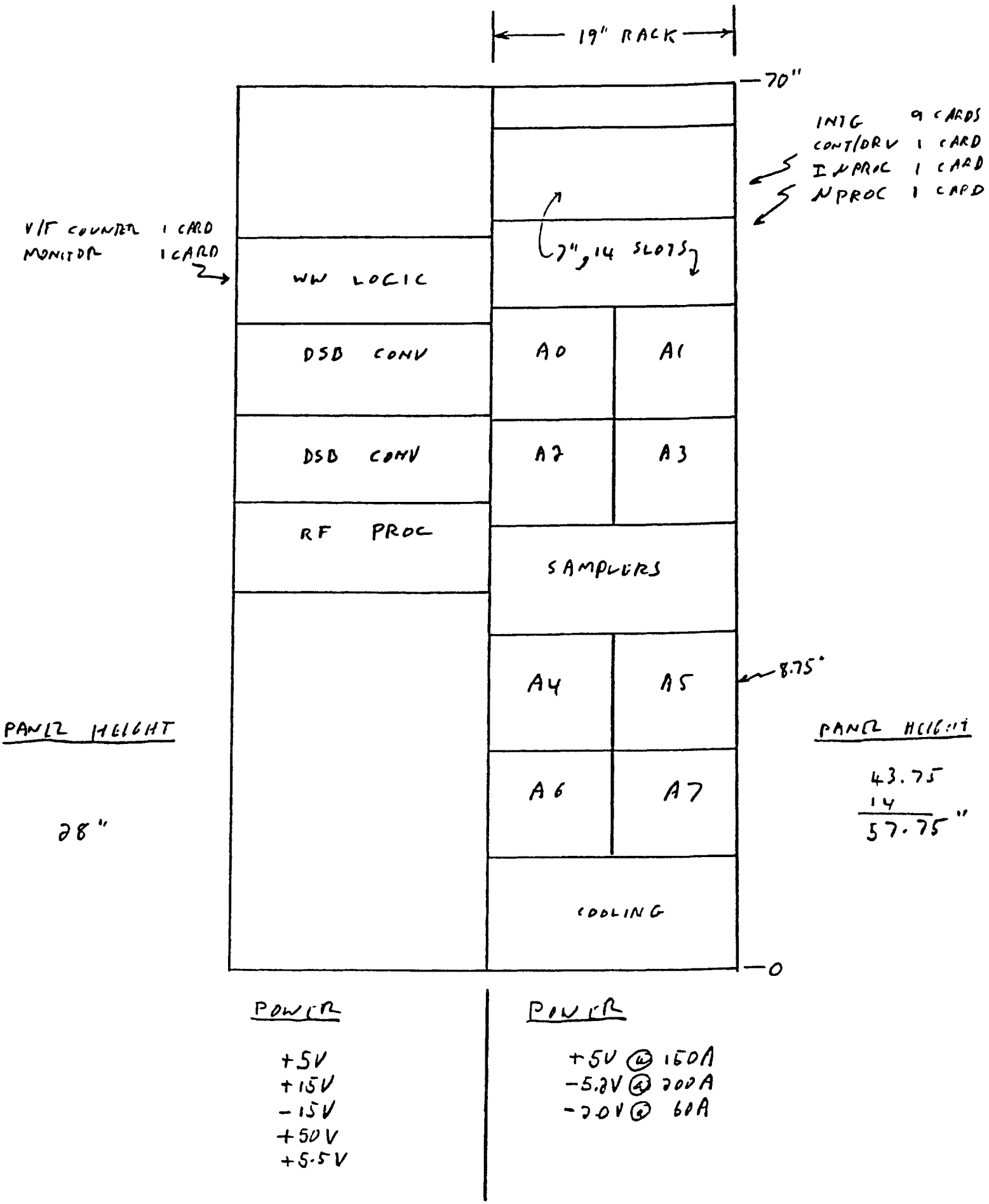
19" RACK
70"
INTG 9 CARDS
CONT/DRV 1 CARD
I PROC 1 CARD
Q PROC 1 CARD
V/F COUNTER 1 CARD
MONITOR 1 CARD
7", 14 SLOTS
WW LOGIC
DSB CONV
DSB CONV
RF PROC
A0
A1
A2
A3
SAMPLERS
A4
A5
A6
A7
8.75"
COOLING
0
PANEL HEIGHT
28"
POWER
+5V
+15V
-15V
+50V
+5.5V
POWER
+5V @ 150A
-5.2V @ 200A
-2.0V @ 60A
PANEL HEIGHT
43.75
14
57.75"

Fig. 1

The clipper levels are set by adjustable voltage dividers driven by + and - voltage reference IC's. POT adjustments on the sampler card panel are available for clipper level trimming. In addition, 128 6-bit D-A converters, programmed by the correlator computer system, are available for automatic level control. The existence of the computer in the loop makes the exact feedback strategy a matter of software.

Sampler threshold settings are monitored by measuring the percentage of time logic one's are detected at each sampler output. Each sampler card has only two circuits to perform this measurement and since each card has 16 digital outputs (2 bits each for 8 analog inputs), two eight-into-one multiplexers are used to circulate the duty cycle measurement among the samplers.

The output of a pseudo-random data generator can be substituted for the sampler output for system testing.

The signal distribution network allows for versatile allocation of the digital multipliers among the sampled analog outputs. The multiplier cards used were designed by A. Shalloway for the Model IV correlator (see EDIR #234) and give lag quanta of 32 lags for distribution among the filter outputs.

Initially, a simple scheme of multiplier card allocation among filters, seen below, is planned. If more complex allocations are desirable (for instance, one filter with 32 cards and 32 others with one card each), they can be implemented via software changes.

# Filters Active	# Cards Per Filter	# Points Across Each Filter Output	Freq. Resolution KHz	Total Bandwidth MHz
64	1	24	1562	2400
32	2	48	781	1200
16	4	96	390	600
8	8	192	195	300
4	16	384	98	150
2	32	768	49	75
1	64	1,536	24.4	37.5

Whether the filters span contiguous or separated bandwidths is a matter of L.O. settings, although the 8 analog outputs of single I.F. processor are more or less confined to span a 300 MHz continuous band.

Short-term integration is performed in the 12-bit VLA custom chips. Long-term integration is performed in high density RAM's. Long-term integration time is programmable from a minimum of about 10 seconds, which is set by how fast the IBM can do the math required by an integration dump, to about 100 seconds (200 seconds for 50% REF, 50% signal) which is when the 32-bit RAM integrators overflow.

The integration system provides 32 bins into which the 2048 multiplier results can be accumulated. These bins are used to keep separate data from:

4	L.O. settings (frequency diversity)
2	For signal/reference
2	For pipelining
2	For future definition (pulsar?)

The "pipelining" factor allows the computer to have a set of results for processing while another integration takes place. The "future definition" factor is a result of RAM's coming in 8k x 8 sizes.

II. System Communication and Timing

Communication with an external computer system and within the correlator is via an IEEE-488 bus. The IBM PC and two internal 6809 microprocessors use the IEEE bus for internal communication, command, and results transfer, and it is planned for a Tucson DEC computer to be part of this network via the same bus. A protocol will be established whereby command, monitoring and results can be interchanged between the hybrid correlator and this Tucson computer.

A single 100 MHz standard is divided internally within the hybrid correlator to generate all necessary timing signals.

The basic macro timing cycle is the 100 μsec VLA-1/VLA-2 integration cycle. During each 100 μsec integration cycle, 9200 samples are correlated in each multiplier producing 14-bit integration results. Correlation is halted for 0.800 μsec at the end of each 100 μsec and 12 of the 14 bits put into secondary storage for later shift out while the two LS bits are discarded.

A second macro timing cycle is the 100 msec cycle. This longer cycle consists of 1,000 100-μsec integrations of which 1 is reserved for self-test and 999 for signal integration. During the self-test cycle, the sampler outputs are discarded and a pseudo-random signal drives the correlator system. The test results are stored in a special long-term storage location for later verification.

The 100 msec cycle sets several system performance characteristics. First, the one of eight sampler threshold measurements (recall that there are 16 circuits to measure the digital duty cycle of the 128 digital sampler outputs) is set to measure a new set of duty cycles each 100 msec. Thus, in 800 msec all sampler output duty cycles are measured. Second, the integrator system bin may be changed only on 100 msec boundaries. Thus L.O. frequency change or signal/reference changes may only be made at 100 msec clock ticks in the initial 1/8th system. When the final system is complete, external signal/reference switches may be permitted on 100 μsec clock ticks. The 100 msec timing cycle also controls the V/F frequency counters and the analog-to-digital scan cycle.

III. Control Parameters

All major system timing cycles are programmable via observation parameters. To start an observation, the user must select a mode of operation, i.e., how many active filters, etc. In addition, a set of timing parameters must be supplied:

A) Frequency diversity, whereby L.O. frequencies are rapidly switched allowing measurement of each frequency point through different filter paths and aiding in splicing the outputs of several digital correlators into a continuous spectra. Four parameters are required.

F1 = Number of 100 msec cycles at L.O. setting 1
F2 = Number of 100 msec cycles at L.O. setting 2
F3 = Number of 100 msec cycles at L.O. setting 3
F4 = Number of 100 msec cycles at L.O. setting 4

An internal timer will flag data invalid for about 1 msec after each L.O. frequency change. If frequency diversity is not desired, set F1=FF, F2=F3=F4=0.

B) Signal/reference. If internal signal/reference is desired, three parameters must be specified.

M1 Number of 100 msec cycles at signal.
M2 Number of 100 msec cycles at reference.
B Number of 100 μsec cycles data will be invalid following signal/reference switch.

A correlator signal/reference output is provided which can be used to control the actual switching between signal and reference. If external signal/reference is desired, set M1≠0, M2=0, AND B=1.

C) Integration time. One additional parameter is required which sets the integration, dump, or FFT rate.

N Number of signal/reference cycles before the integrators are dumped to the IBM PC, cleared, and FFT's performed on integration results.

From these observation parameters, the following operation results:

Frequency diversity cycle time = (F1+F2+F3+F4)100 msec
Signal/reference cycle time = (M1+M2)100 msec
Integration time = N(M1+M2)100 msec

All parameters are 16-bit numbers, and the only limitations are that the integration time be between 10 and 200 seconds. The upper limit depends on M1, M2, F1, F2, F3, F4 since the more bins integrated into, the longer the time to overflow.

IV. Spectrometer Input and Output Signals

Signals into and out of the spectrometer consist of:

1) I.F. input signal. 8 I.F. input signals at a level of -17 dBM per 300 MHz (72 dB above 290K noise) in the 356-656 MHz frequency range.

2) 100 MHz clock (input). A 0 DBM sinewave.

3) Data valid (input). A TTL logic low on this line will cause 100 μsec integration results to be discarded and not accumulated into the integrators. This line is sampled at the change of each 100 μsec cycle and the result of the sample will affect the 12 bit results accumulated during the previous 100 μseconds.

4) External signal/reference (input). This line can be used to separate data into signal or reference accumulation bins. No count of this line is made so the number of signal/reference cycles from this line does not affect in the integration time. In the 1/8th test system, this line can only change on 100 msec cycle boundaries. If data goes invalid for some period following a signal/reference change, the external data valid should be set low for this period to exclude integrations made on bad data from the integrator.

5) Pulsar gate (input). A line is provided to allow keeping two time bins for any reason.

6) Signal/reference (output). This line is a buffered version of the integrator signal/reference bin select.