Long Baseline Antenna Prototype: DBE Concept

ngVLA Antenna Memo #16

07/1/2024

Abstract

This memo explores the key differences between the ngVLA DBE and the ngVLA LBA qualification electronics prototype DBE. It will cover aspects of new or modified DBE functionality, development schedule, band assignment, ADC availability. The document will trade-off key decisions that will be needed to make a DBE to support testing of the ngVLA LBA prototype antenna on the proposed timescale.

1 Introduction

In this memo we consider the conceptual design of the digital backend (DBE) necessary to test the prototype long baseline antenna under development for the US Naval Observatory (USNO). The broader antenna electronics concept to support verification and validation tests is described in ngVLA Antenna Memo #15 [1].

The DBE prototype described here aims to support both single-dish radiometric testing and interferometric characterization as an element of the VLBA. In particular, a demonstration of performance in Earth Orientation Parameter (EOP) observations such as timekeeping (UT1-UTC corrections) is assumed to be included in the associated verification and validation plan.

Another key assumption is that the prototype antenna will be retrofitted to be an operational element of the "ngVLBA" long baseline array. We will use this term to refer to a future operational array that co-observes with the VLBA and is tailored to geodetic use cases. Given this assumed future, this prototype electronics package, inclusive of the DBE, considers the growth path to production electronics and attempts to reduce rework when possible or otherwise support long-term development. However, this goal is considered secondary to supporting the verification and validation activities, and significant future development of the DBE and digitizer platform is anticipated in the transition from the antenna verification and validation phase to any future operational phase.

2 Key Verification & Validation Requirements

The following are key requirements for the antenna electronics, control software, and supporting test systems to support the verification and validation of the antenna performance [1]. Implications for the digital back end system are also noted:

- Systems must support functional radiometric testing of the antenna (pointing, tracking, beam cuts, tipping curves, etc.) Integration of total power data with the Tpoint package is desirable.
    - The DBE can support this not only in collecting high bandwidth data in the proposed Mark VI Data collector, but also by live calculating total power periodically using the DBE monitor and control interface.
- The outfitted antenna must be interoperable as an element of the VLBA. In particular, it must support both current and emerging UT1-UTC EOP observations. This includes the well-established S-X mode used currently on the VLBA, as well as the proposed (and still under development) X-Ka mode.
    - By supporting multiple IRDs simultaneously the DBE facilitates this goal. The DBE will be capable of capturing sub-bands scattered across the available bandwidth on the prototype antenna allowing direct comparison between signals in multiple bands.
    - By supporting VDIF output streaming existing correlators and data collectors can be used.
- It is a goal that the antenna and software systems support the 'real-time' correlation mode of the VLBA. This will facilitate interferometric verification tests such as pointing model determination and pointing offset measurements.
    - The DBE facilitates this goal by providing streaming VDIF ethernet packets. Assuming sufficient bandwidth is available between the antenna and the correlator site, data can be streamed anywhere in the world. The DBE will allow scaling to the available ethernet bandwidth through selection of sub-bands, as well as providing selectable quantization bit depth.
- Software and test systems must include the capability of performing holography for surface verification from GEO beacons in the 11-12 GHz range and/or water masers at 22 GHz. Interoperability with the GBT in a 'VLBI' mode is desired as a reference antenna for holography measurements.
    - Support for 6 IRD basebands allows coverage in multiple frequency bands.
- It is a goal to advance the design of ngVLA electronics concepts and systems when possible, treating this project as a pre-production "pathfinder".
    - The ngVLA-spec DBE will benefit substantially from the use of its core functions on this prototype antenna. This pathfinding will validate the DBE design and reduce risk.

3 Key Functional/Performance Requirements

The receiver bands that must be supported by the prototype electronics are described in Antenna Memo #15 [1] Table 1 and paragraphs 3.1, 3.2, and 3.3. This can be summarized as the following IRD baseband coverage:

Table 1: Proposed Prototype IRD Baseband Tuning and band coverage

IRD Baseband	LO Frequency (GHz)	Frequency Coverage (4.096GSPS ADC, 2.1GHz usable BW)	
		Lower (GHZ)	Upper (GHz)
B1A – LBA Proto	3.2	2.15	4.25
B1B – LBA Proto	9.6	8.55	10.65
B2A – LBA Proto	9.6	8.55	10.65
B2B – LBA Proto	12.8	11.75	13.852
B2C – LBA Proto	22.4	21.35	23.45
B2D – LBA Proto	31.4	30.35	32.45

For production, 8GSPS or faster ADCs should be available. This will allow changes to this band coverage as additional bandwidth will be covered by each IRD and additional bands will be supported as discussed in Table 1 of [1]. Reuse of ngVLA LO Frequencies for coverage above 30GHz is expected in production.

When considering the implementation of the prototype DBE and digitizers, we make the following assumptions:

- As discussed in schedule section below, it may be necessary to use a lower speed ADC for this prototype. The Texas Instruments ADC12DJ5200RF is the currently preferred component.
    - An analog quadrature receiver (e.g. zero-I/F) architecture is assumed. The primary motivation is to have high overlap with the ngVLA electronics architecture in order to decrease development costs and enable reuse of ngVLA-spec IRDs.

Most ngVLA DBE Requirements will be preserved for the long baseline antenna qualification version, though requirements such as safety and security, mechanical/environmental, Reliability etc will be on a best effort basis. However, some new requirements will supersede or modify ngVLA DBE Requirements.

Table 2: Requirement Changes/Additions

Parameter	Related ngVLA Req. #	New Prototype Req. #	Value	Traceability
Input Processor – Sub-band Selection	Replaces DBE0020 and DBE0021	DBE7000	The DBE shall process 2 IRD basebands simultaneously. • The DBE should process 4 IRD basebands simultaneously The DBE prototype must be able to operate in the S-X validation mode, X-KA validation mode, and Ku-K validation mode as described in 3.1, 3.2, and 3.3 of [1]	[1]
Input Processor – IRD Support	<none>	DBE7001	The DBE shall support 6 IRD Modules	[1]
LO Offset Correction – NCO Frequency Programmability	Replaces DBE0223	DBE7003	The DBE shall have better than 500KHz LO offset correction. • The DBE should have a programmable frequency oscillator with resolution better than 1kHz.	[1]
Channelizer – Channel Bandwidth	Replaces DBE0301	DBE7004	The DBE shall split received band data into 32MSPS sub-bands. • The DBE should support 32MSPS, 64MSPS, 128MSPS, 256MSPS, 512MSPS and 1024MSPS	[1]
Channelizer – Channel Selection Minimum	Replaces DBE0302	DBE7005	The DBE shall allow arbitrary (programmable) selection of at least 3.04GHz of dual-pol bandwidth 8-bit I/Q output data (95 Complex channels at 32MSPS)[1]	[1]

[1] This is mostly limited by output bandwidth, and assumes the output bandwidth is 100G Ethernet. If the actual output bandwidth is externally limited lower this requirement need not be met.

Parameter	Related ngVLA Req. #	New Prototype Req. #	Value	Traceability
Channelizer – Rejection	Amends DBE0306	DBE7006	When the channelizer is operating in overlapping mode[2], The DBE sub-band filter shall reject signals more than 0.5625*(Fsout) above or below the sub-band center frequency by at least 60dB (as compared to the passband specified in DBE0304 and further constrained by DBE0305). ● At 250MSPS nominal output rate, this means that signals will be rejected by +/- 140.625MHz from the tuned center frequency preventing an alias signal from aliasing back into the passband (+/- 109.375) ● This requirement does not prevent an alias signal from aliasing into the transition band. ● The DBE should provide 80dB of rejection in these conditions.	Preserved ngVLA support
Channelizer – Nonoverlapping	<N/A>	DBE7007	The DBE shall implement channelization using a non-overlapping channel structure (eg a 32MSPS output shall cover 32MHz of bandwidth). • The DBE should also support an oversampled overlapping mode.	[1]
Output Packetization – Packet Format	Replaces DBE0501	DBE7008	The DBE shall support VDIF packetization. • The DBE should support VITA49.2 packetization.	[1]
Output Packetization – Quantization	Replace DBE0504	DBE7009	The DBE shall support rounding/saturation of data to 2-bit output samples • The DBE should support re-quantization to 4-bits, 8-bits.	[1]

[2] Overlapping channels is a crucial aspect to allow the original DBE0306 to be met. Without overlap, it will be very costly and/or impossible to meet the original DBE0306 adjacent channel rejection requirement. Since the VLBA historically has not used overlapping channels, the adjacent channel rejection requirement from ngVLA's DBE requirements is relaxed to only apply when operating in the optional non-overlapping mode. See DBE7007 as well.

Parameter	Related ngVLA Req. #	New Prototype Req. #	Value	Traceability
Output Packetization – 2SB Real Mode	Extends DBE0504	DBE7010	The DBE shall have sideband separated real output mode (Lower side band in one voltage stream and upper side band in a separate voltage stream). Note: Inputs to the DBE are still in quadrature from the IRD modules. In addition, DBE0131-DBE0138 are still applicable, therefore I/Q calibration should occur prior to 2SB Real separation so that all sideband rejection performance is still maintained even when operating in sideband separated real output mode.	[1]
Output Packetization – Complex Mode	Extends DBE0504	DBE7011	The DBE should support complex (I/Q) output mode	[1]
Output Packetization - Ethernet Speed	<none>	DBE7012	The DBE shall support 100G Ethernet	[1]
Output Packetization - Ethernet Speed Extended	<none>	DBE7013	The DBE should support 10G, 25G, 40G, 100G, or 400G Ethernet	[1]
Input – Processor ADC format	Replaces DBE0052 and DBE0053	DBE7014	The DBE shall support ADC data transfer over fiber optic JESD204C protocol.	As required for ADC Availability

3.1 Key requirement changes from ngVLA

The proposed ngVLA DBE design as documented in [2] and [3] differ in several key ways from the ngVLBA implementation:

Table 3: Requirement Comparison

	ngVLA	LBA Prototype	ngVLBA Production
I/Q balance correction	Required	Required	Required
Equalization Support	Required	Required	Required
IRD Module support	20, 8 simultaneously	6, 2 simultaneously	20, with at least 4 simultaneously, but 8 for full band coverages and compatibility with ngVLA
IRD Bandwidth	5.8GHz, at 7GSPS	>2GHZ, proposed 4.096 GSPS rate (see below)	5.8GHz, 7.168 GSPS Rate with capability to operate at 7GSPS or 8GSPS or 8.192GSPS
Subband Channelization	250MSPS, overlapping with 218.75MHz bandwidth / subband	32MSPS, non-overlapping real-sampled (side-band separated, separate output for lower and upper sideband) Prefer multi rate: 16,32,64,128,256, 512,1024 MSPS[3]	multi rate, non-overlapping real-sampled (side-band separated) at 16,32,64,128,256, 512, and 1024 MSPS
Channelization	Overlapping	Non-overlapping	Overlapping or Non-overlapping
Channel center Frequency Resolutions	~Hz, using coarse FFT tuning and fine NCO tuning on sub-bands after channelization.	~500KHz @ 4.096 GSPS (assumes 8K FFT!)	~500KHz @ 7.168GSPS Can do ~Hz resolution when operating in overlapping mode
Ethernet output bandwidth	2x400Gbit with possible 2x800Gbit future upgrade	100Gbit, with possible 400Gbit upgrade possible	400Gbit Ethernet 2x400Gbit possible if needed
Ethernet output format	VITA49.2	VDIF (real and complex)	VDIF/VITA49.2 Software Selectable output format
Ethernet bitwidths supported	16,12,10,8,6,4,2	2,4,8,16	VDIF: 2,4,8,16 VITA49.2: 16,12,10,8,6,4,2

[3] Expanding to allowing data at up-to 1024MSPS infers that the DBE should support a 16K FFT and 2K IFFT, with the FFT supporting compile-time size changes (8K will be used on the prototype, while 16K will be needed for the production) and the IFFT supporting run-time configurable size changes, with up-to 2048 output cells.

Max Simultaneous dual-pol Bandwidth at 8-bit I/Q output	21.43 GHz (98 Channels at 250MSPS)	3.04 GHz (95 complex channels at 32MSPS)	12.2GHz (382 complex channels at 32MSPS)
Interoperability Goals	Should support interoperability with ngVLBA Production modes to the extent possible with different antenna band structure.	Shall support interoperability with identified VLBA observing modes. Should be a pathfinder to a production unit.	Should support interoperability with ngVLA systems and modes to the extent possible with a different antenna band structure.

However, the ngVLBA production requirements should be considered an absolute floor, it would be better to support both ngVLA and ngVLBA production requirements on the DBE requiring only external changes (eg IRD and LO changes) and software configuration changes (eg to program 8GSPS related settings).

4 Proposed Design Changes

The existing DBE design is largely capable of meeting ngVLBA requirements using the existing conceptual design. The primary differences described above, require the following modifications:

- ADC sample rate needs to be either 3.584, 4.096, 7.168, or 8.192 GSPS to allow the required output data rates
    - This is largely a design change for the IRD, or more specifically the timing system to provide an appropriate sample clock to achieve the required rate.
    - Internal to the DBE FPGA, the clock rate must be higher to achieve 7.168GSPS and/or 8.192GSPS data.
    - If ADC sample rate changes are not possible, the complexity of the rate change in signal processing is non-ideal, as it involves a rate change of up by 1024 and down by 875. The sample rate change will therefore be pursued as the default approach.
    - Recommendation is for the timing subsystem support the following clock as options to the Digitizer (assumes TI ADC12DJ5200RF)

Table 4: Recommended Clock support for TI ADC12DJ5200RF

Sample Rate	Sample Clock	Sysref
4.096GSPS	4.096 GHz	6.4 MHz
7GSPS	3.5 GHz	5.46875 MHz
8GSPS	4 GHz	6.25 MHz
8.192GSPS	4.096 GHz	6.4 MHz

        - With the TI ADC12DJ5200RF, we'll use the part in dual channel mode when operating at <5.2GSPS, so the clock for 8.192 and 4.096 are the same
- Implementation of Multi-rate output support

    - This was conceived as a should for the ngVLA DBE requirements and requires the output IFFT block to be variable size, scaling from an IFFT size of 16 to 2048.
    - The increased max possible IFFT size and variable size of the IFFT have the following effects on the DBE design.
        - Increased FPGA resources to implement a larger (1024 vs 256 IFFT size).
        - Design changes to existing Casper FFT to support.
            - IFFT mode (already required by ngVLA).
            - Variable FFT size support.
- Implementation of Side-band Separation instead of only complex[4] output.
    - Relatively trivial change to I/Q processor to keep upper and lower sideband separated through the channelization and IFFT instead of recombining into Complex data.
- Larger FFT size to support a minimum of 500KHz sub-band spacing in non-overlapping mode
    - 16384 or 8192 FFT size will be Build-Time Configurable as only 8192 will be needed with 4GSPS sampling.
- Implementation of VDIF output Mode.
    - Will support either Real outputs with USB and LSB separated streams, or Complex outputs.

From a hardware perspective, the LBA qualification electronics requirements can be met with 1 DBE PCB stack (ngVLA normally includes 2 instances of the DBE PCB stack), roughly half the BOM cost of the ngVLA DBE. Due to schedule concerns, the initial prototype may use a packaged demo board approach, but these would still use the same FPGA family as the expected production DBE.

[4] While Complex output is I/Q balance corrected on the proposed ngVLA design, arguably when transmitted as complex (Real and Quadrature) the lower and upper sideband (when digitally tuned to the middle of the analog bandwidth) are only "Separable" not "separated", as neither the I nor the Q alone give the information required to detect if a signal is in the upper or lower sideband. Only together, by comparing the relative phase of the I and Q signal, can a CW (for example) be determined to be upper or lower sideband. When operating in side-band separation (real outputs), the lower and upper sideband would be separated, which mathematically can be accomplished with a 90 degree phase shift and adder (in the time domain) or in the frequency domain by considering only the frequency cells in the upper or lower sideband.

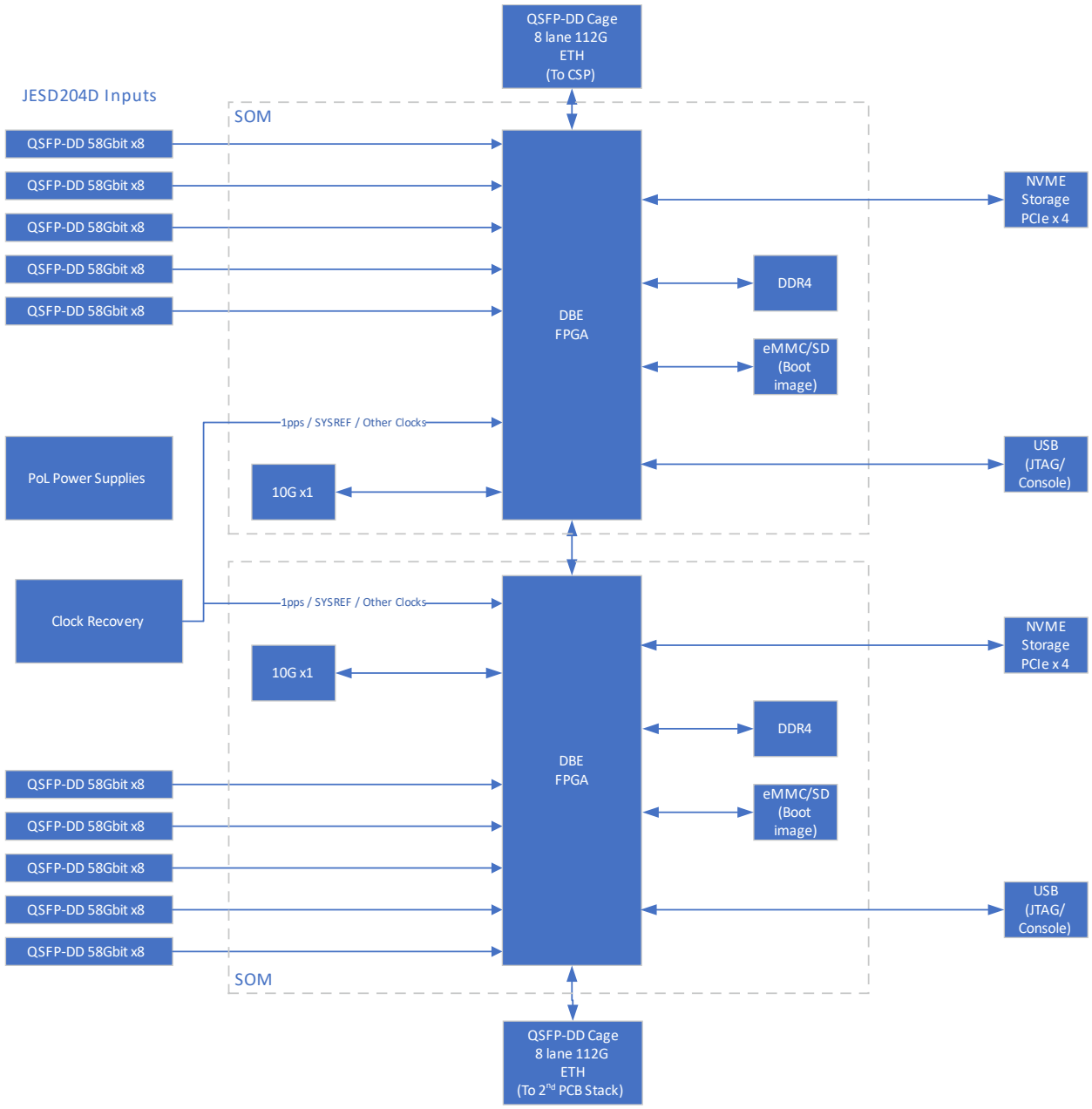

Figure 1: DBE PCB Stack

The design detailed in [2], supports up-to 10 IRDs and 4 simultaneous IRDs each supporting dual-polarization complex sampling. Output bandwidth could be as high as 2x400Gbit/sec from a single PCB stack as the link between stacks can be used as another output path. Firmware support for 100G mode is also feasible during the prototype if the data recorders can-not support 400G ethernet. However, to allow full band coverage and compatibility with ngVLA, the production DBE for the ngVLBA should use 2x PCB stack and be the same DBE components as ngVLA. From an FPGA perspective the FPGA processing would largely be identical:

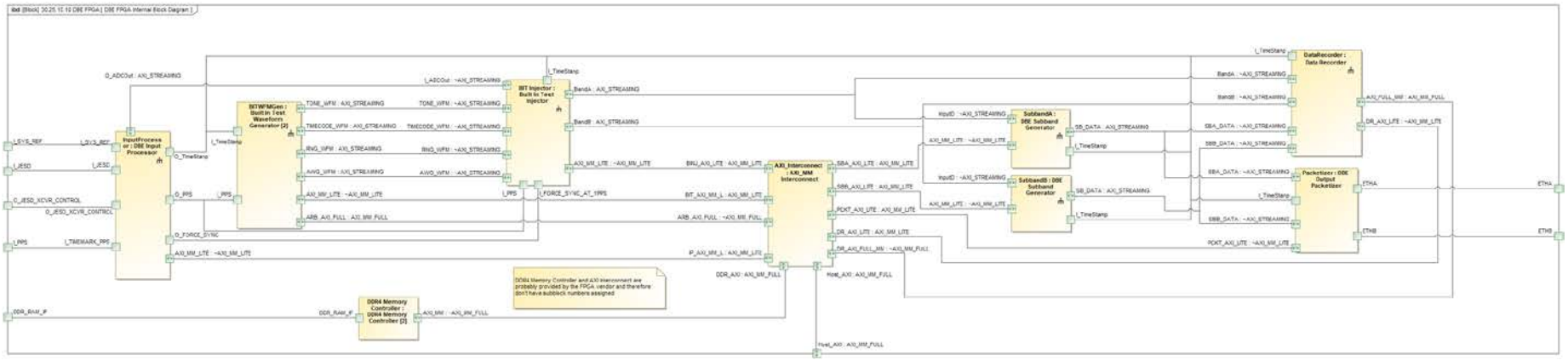

Figure 2: DBE FPGA Top level Block Diagram

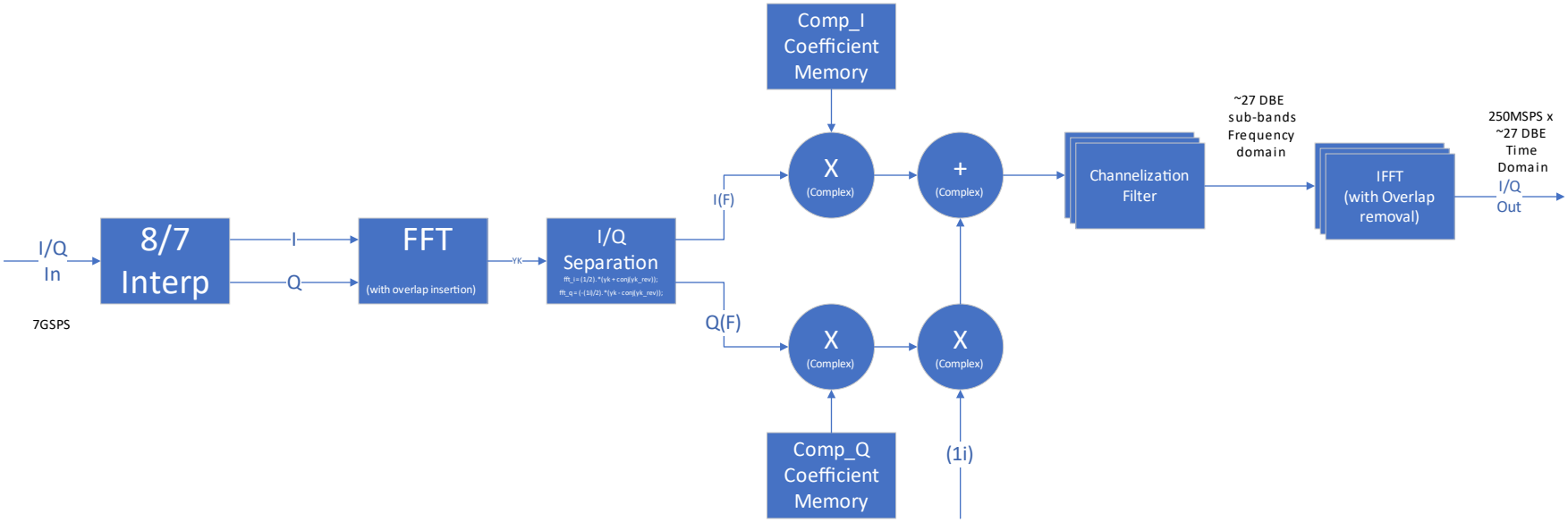

Figure 3: Simplified DSP Block Diagram

The top-level FPGA design would still be largely the same as shown in Figure 2 and Figure 3, however the packetizer block would be implemented initially to support VDIF mode on the antenna qualification prototype. Later, the ngVLA project would add support for VITA49.2 making the packetizer operate in a programmable output format supporting additional quantization modes and more flexible time-stamping. The prototype design would also likely skip implementation of the BIT Waveform Generator, BIT Injector blocks and allow the ngVLA to complete those blocks in time for production.

From a signal processing perspective, the largest changes are additional FFT and IFFT sizes and support for programmable IFFT/FFT sizes at run-time. This adds complexity to the signal processing as additional processing modes are now required, and those modes must be individually tested.

5 Schedule Implications

As laid out in [4], the DBE ngVLA development is currently planned as a 4-year effort beginning in FY2024.

As discussed above, several blocks would need modifications to meet prototype and eventual ngVLBA production requirements:

Table 5: Cost Delta from ngVLA to implement ngVLBA DBE

	ngVLA Labor estimate as of 12/2023	**Prototype Design**	**Delta**	**Notes**
FFT/IFFT Block	160 Hours	400 Hours	240 Hours	Covers implementation of Size changes
Packetizer Block	120 Hours	300 Hours	160 Hours – Likely split into two separate developments for differing schedule.	Covers implementation of VDIF
FW: Unit Testing	480 Hours	720 Hours	240 hours to cover additional test cases	Covers testing for ngVLBA-related requirements
Requirement Dry run Compliance testing	482 Hours	962 Hours	480 Hours to cover additional test cases	Covers testing for ngVLBA-related requirements
Documentation – various PDR	600 Hours	900 Hours	300 Hours	Documentation and meeting prep for separate PDRs
Documentation – various FDR	660 Hours	960 Hours	300 hours	Documentation and meeting prep for separate FDRs
Total Additional Labor			**1720**	**~ 1 Person Year**

It should be noted, that the prototype and eventual ngVLBA development is still reliant on the ngVLA development as laid out in [4]. Many of the ngVLA development tasks must still be completed on the antenna prototype timeline.

In addition, under the assumption that the Antenna qualification will require 2 prototype units (one for the antenna + 1 as a spare/lab unit) we'll need additional M&S for the DBE:

Table 6: Additional DBE M&S (Direct costs only w/o contingency)

M&S Line Item	**Prototype Design /Prototype M&S**
Additional Development needs - FPGA Development Board + Test Equipment	$25,000
Prototype Antenna IRD Transceivers	$400*8 = $3,200
Baseboard Purchase	$3000 * 2 = $6,000
400G Eth Transceivers	$7000 * 2 = $14,000
DBE Chassis	$3000 * 2 = $6,000
DBE SoM	10,000 * 4 = $40,000
DBE Internal Cables	$2,000 * 4 = $8000
Total:	**= $102,400**

An appropriate sharing of labor across the ngVLA and prototype/production LBA contracts should be negotiated with program management, but due to the additional work required and the increased criticality of the development schedule for first light on the qualification prototype antenna, the DBE team should accelerate its schedule by 6-12 months and consider hiring additional staff as soon as possible.

If the ngVLA funding is delayed, this becomes a significant schedule risk for the prototype antenna qualification electronics.

Also to note: A more aggressive schedule will also result in increased needs to travel to CDL or Socorro for testing and team meetings. An additional travel budget of about $15K in each year between FY2024 to FY2027 is probably wise, as with a larger team more frequent travel may be necessary depending on where we can recruit staff.

As laid out in [4], the DBE team expected to complete design over a 3-year period, FY2025, FY2026, FY2027, with most design work not starting until mid FY2025 due to staffing limitations. [FY 2024 largely consisted of risk reduction work by a single engineer], however that schedule is no longer feasible in light of the delivery of the prototype antenna at the end of FY2026 or early FY2027, roughly 9 months sooner than the ngVLA schedule would've delivered a full functional requirement compliant DBE to the larger system. In addition, up-to another year of labor is required to complete the design as compared to the

ngVLA system due to additional requirements. However, it should be noted that the FY2026 delivery can be a scaled back version of the eventual delivery for production, thus it's likely to be necessary to postpone some level of DBE unit testing, automated testing as well built-in-test features from the prototype release antenna qualification and push those tasks to after the prototype is completed.

Table 7: Tasks that can be pushed to after Antenna Qualification prototype release

Block/Task	**Postponable hours to FY2027 or beyond**
FW: Waveform Generator	240 Hours
SYS: System Testing	600 Hours* * Minimal testing for prototype
SW: Requirements Compliance Testing Software	480 Hours* * Minimal compliance testing for prototype
FW: Requirements Compliance testing	240 Hours* * Minimal Compliance testing for prototype
Test: Test Deficiencies	500 Hours * Assumes minimal compliance testing = minimal bugs found
Conduct Compliance Testing	600 hours
Production Test Development	1000 Hours
NCO LO Offset block	160 Hours
SW: Bit Application	320 Hours
SW Monitoring Drivers/Application	480 Hours* * Scaled back Monitor and Control
Total	**4,620 Hours = 2.6 Person years**

5.1 Milestone Comparison

Table 8: Major Milestone Comparison

Milestone	ngVLA	Long Baseline Prototype Antenna Qualification
CoDR	Complete	N/A
First prototype IRD available with Integrated Digitizer	Q4 FY2025?	Q2 FY2025, we should consider building with an existing digitizer such as TI ADC12DJ5200RF at 4.096 GSPS to ensure we have a solution for the prototype
PDR	Q2 FY2026	Q3 FY2025
Kick off of DBE Subcontract for Form/Fit/Function Boards	Q1 FY2025	No later than Q3 FY2025 Even if ngVLA is delayed we must kick this contract off immediately after ngVLBA PDR or the DBE prototype will not be constructed on-time
Delivery of first Form/Fit/Function DBE	Q4 FY2025	Q1 FY2026. Earlier is better, this is a worst case date, if ngVLA funding is delayed
First Antenna with DBE "First Light"	Q4 FY2027	Q1 FY2027
DBE FDR	Q4 FY2027	Q1 FY2027

In general, the long baseline antenna qualification effort slides the DBE schedule 6-9 months to the left, the one exception is that the DBE subcontract was scheduled for Q1 FY2025 on ngVLA to allow as much time as possible to get form/fit/function hardware in house and verify design requirements on real form/fit/function hardware. That is a luxury the prototype project may not have if a $130K subcontract cannot be awarded until after PDR, as indicated here. Especially with the rest of the schedule moving to the left, it increases risk that the initial Form/Fit/Function prototype must work to allow a form/fit/function hardware to be used on the LB prototype antenna. [An alternative is to build a prototype around an FPGA development board, but that is less ideal, due to RFI shielding and limitations on the number of IRDs that can be connected to a development board as compared with a custom "baseboard"].

5.2 Labor Ramp up Comparison

The schedule laid out in [4] would've completed major design work in mid FY2027 on ngVLA. The DBE would've used approximately 22,031 Hours of labor to complete the work over a time period of ~3.5 years requiring an average team size of 3.6 FTEs. ngVLBA requires about 19,111 hours of work to be completed in 2.5 years which requires an average team size of 4.4 FTEs. However, because of the shortened time period involved, and the likely slow process to hire stuff, a larger team of 6 is proposed.

Table 9: Labor Ramp Up Comparison

Fiscal Year	***Position***	***ngVLA Budget from [4]***	***Request for Combined ngVLA/ngVLBA Design team***
	Employees on DBE Task	Hours completed in FY	Hours completed in FY
FY2024	EE, Sr. FPGA/Sys engineer (DBE Lead)	1734	1734
	EE, III. FPGA Engineer	0	900* * Immediate advertisement recommended
FY2025	EE, SR (DBE Lead)	1734	1734
	EE, III. FPGA Engineer	0	1734
	EE, III. FPGA Engineer	400	1000
	Software Engineer IV	800	1400
	Software Engineer III	400	1000
	Software Engineer III	0	400
	Mechanical Engineer IV	440	440
FY2026	EE, SR (DBE Lead)	1734	1734
	EE, III. FPGA Engineer	0	1734
	EE, III. FPGA Engineer	1734	1734
	Software Engineer IV	1734	1734
	Software Engineer III	1734	1734
	Software Engineer III	1734	1734
	Mechanical Engineer IV	194	446
	System Engineer IV	200	200
FY2027	EE, SR (DBE Lead)	1730	1730
	EE, III. FPGA Engineer	1730	400
	EE, III. FPGA Engineer	0	0
	Software Engineer IV	1730	1730
	Software Engineer III	1730	400
	Software Engineer III	0	0
	Mechanical Engineer IV	250	0
	System Engineer IV	120	120

	Technical Specialist	300	300
Peak FTEs		**4.2**	**6.3**

Assumptions: Delivery of a long baseline antenna prototype with functional DBE in September 2026. Qualification Electronics DBE prototype will not include fully functional Built-In-Test or automated production testing. (old schedule planned delivery of first functional feature complete DBE in ~June 2027)

Recommendations: Hire an FPGA engineer as soon as possible for long baseline prototype effort in FY2024. Hire a software engineer lead as soon as economically feasible but no later than December 2024. Increase DBE engineering staff to 6 during FY2025/2026, but can scale back to two engineers in FY2027. This 18-24 month tasking may require contract engineers or a long term career path within NRAO. One possibility is to transfer DBE staff to the ngVLA correlator after DBE completes.

6 Conclusions

The Long Baseline Antenna Qualification design is both an opportunity and a challenge for the DBE. It allows another funding source for the DBE which will allow faster development of the DBE and the ability to retire risks more quickly for both the ngVLA and ngVLBA. But with the more aggressive schedule, retiring those risks quickly are more critical.

As pointed out above several things should occur as soon as possible, preferably in FY2024:

- Labor should be assigned to design a form/fit/function ADC board for the IRD as soon as possible Given that we are still waiting for a multi-channel >= 7GSPS ADCs with support for DC operation we may need to design an interim design with a >=4GSPS ADC.
    - Such as:
        - https://www.analog.com/en/products/ad9209.html
        - https://www.ti.com/product/ADC12DJ5200RF
            - Demo boards are in house for this ADC.
- Or accept a large "hole" at DC with: https://www.analog.com/en/products/AD9084.html
- The DBE Work package should hire an FPGA engineer as soon as possible to accelerate DBE design.
- The DBE team should probably expand to 6 FTEs in FY2025/FY2026 to ensure completion of the Form/Fit/Function prototype in FY2026.
- The Subcontract for the DBE Baseboard should be funded as soon as feasible, but no later than Q3 FY2025.

6.1 Risks

Moving the schedule to the left increases the risk involved in pre-existing ngVLA risks:

- The IRD's ADC board has not been started yet and currently available multi-ADC packages have large 10+MHz holes at DC that limit their usefulness.
- The ability to run JESD204C over fiber optic cables has not been proven by NRAO (it has been demonstrated by vendors however).
    - A Form/Fit/Function ADC board is needed to prove this interface.
    - Alternatively, a custom designed adapter board could be used to adapt the TI ADCs demo board for transmission over fiber.
- The I/Q calibration scheme has not been proven in real hardware.
- Hiring plan is aggressive, and may take long periods to attract suitable candidates.

If the schedule is moving to the left, it would be wise to accelerate ADC board design on the IRD work package, as it helps to address DBE risks. We also need to staff DBE design staff as soon as possible.

7 References

[1] R. Selina, et al. "Long Baseline Antenna Prototype: Antenna Electronics Concept" ngVLA Antenna Memo #15

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