RADIOASTRON DOWNLINK DECODER SPECIFICATION FOR USSR EARTH STATIONS

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April, 1991
(revised December, 1991)

1. DESIGN FOUNDATION.

1.1. Radioastron down link data decoder is contained in ground Radioastron down link station equipment.

2. DESIGN GOALS.

2.1. The Decoder provides the transformation of the down link receiver output on-board formatted data to unformatted data to require the usual digital inputs of a Recorder Terminal Formatter.

2.2. Decoder will be installed at each ground Radioastron down link station.

2.3. Decoder provides the following functions:

- decoding data from two down link receiver outputs: "POLARIZATION I" & "POLARIZATION II" and giving these data with clock signal to recording terminal;

- picking out and processing the auxiliary information from down link data and transmitting the data to Recording terminal Control Computer;

- detecting from down link data the on-board 1 sec tick (s-1 sec) and transmitting it to Recording terminal;

- measuring the time interval between s-1 sec pulse and ground station 1 sec UTC pulse with 10 ns accuracy and transmitting the result of the measurement ("NAVIGATION DELAY"-code) to Recording terminal Control Computer as auxiliary information;

- generating satellite time code based on down link clock and s-1 sec pulse and transmitting the"S-TIME"-code) to Recording terminal Control Computer as auxiliary information;

- checking down link data, accumulating errors and transmitting the result of the calculation to Recording terminal Control Computer as auxiliary information.

3. DECODER EQUIPMENT REQUIRED FOR RADIOASTRON TRACKING STATION.

The final version of Decoder construction will be determined at design step.

3.1. Decoder contains five modules inserted in a common crate:
- "POLARIZATION I"-line decoding module
- "POLARIZATION II"-line decoding module
- synchronization and time measurement module
- local and distance control module
- power supply module.

3.2. Total Decoder Radioastron equipment.
It is needed to produce:
- four Decoder devices with cables to connect Recorder terminal, Down-link Receiver, Recorder Control Computer RS-232 interface, H-maser and Station Clock;
- four transport Decoder boxes; and
- four sets of Technical documentation.

3.3. Decoder test facility must be built into Decoder modules.

3.4. Manufacturer must deliver the engineering Decoder device and four production Decoder devices with external cables for each device.

4. TECHNICAL REQUIREMENTS.

4.1. Common technical requirements.

4.1.1. Designing and testing of Decoder should be make in accordance present document and all changing in designing must be agree with project engineer Novikov A.Yu.

4.2. Mechanical construction requirements.

4.2.1. Mechanical construction of Decoder must be convenience for using in observation, testing and repairing.

4.2.2. All Decoder parts should be marked in accordance Decoder technical documentation.

4.2.3. All electronic components should be marked in accordance principal diagrams of Decoder documentation.

4.2.4. In Decoder designing it should be use universal commercial widespread circuits, components, modules and blocks as much as possible.

4.2.5. The following three options should be considered for the mechanical construction of Decoder:
- Decoder modules placed in Down Link Receiver crate
- Decoder modules placed in Data Acquisition System VME-crate
- Decoder modules placed in Own crate which will be more preferable in turns from cost, availability and other features.

4.3. Common electrical requirements.

Decoder should be produced for using both power supply standards: 220 V/50 Hz and 110 V/60 Hz.

4.4. Decoder special requirements.

4.4.1. Decoder functions.

1. To decode information received from two Down-link Receiver outputs. The down-link data is formatted by on-board spacecraft Formatter before transmission to ground according to Radioastron satellite data format or s-format described in p.4.4.4. From the down-link data the Down-Link Receiver derives a clock and separates the incoming data into two digital data streams, one for each polarization channel and passes the formatted digital data streams to the satellite Decoder by outputs: "POLARIZATION I", "POLARIZATION II", "CLOCK-IN".

The down-link data is transmitted with one of selected down-link data rates: 18, 36 or 72 Mbit/sec. Because of s-frame contains 20000 bytes

independently from various data rates, the frame time duration varies in according data rate and equals 2.5 ms for 72 Mbit/sec; 5 ms for 36 Mbit/sec and 10 ms for 18 Mbit/sec.

Each frame contains three kinds of information: astronomical data, auxiliary information and synchword. All three kinds of the information are transmitted by bytes, synchword transmitting with even bit parity and other ones transmitting with odd bit parity. The astronomical data is the serial on-boarded bits from simultaneously sampled selected numbers of video channels (2 or 4 or 8) by 2-bit ADC with selecting: number of sample bits (1 or 2) for serial data packing to s-frame and sample rate from values 4, 8, or 16 Mbit/sec. Decoder must restore each individual parallel digital output according to selected on-board Radioastron modes describes in p.4.4.3 and Table 1 and to send data to Recorder Terminal through output "ASTRONOMICAL DATA". It should be taken into account that a part of astronomical data isn't packed into the serial s-format; instead, both synchword and auxiliary data replace 30 bytes of astronomical data. The synchword bytes and auxiliary bytes are called the s-frame header. The s-frame begins from the synchword. The first part of auxiliary information follows after the synchword. Then the astronomical data bytes follow and finally the second part of auxiliary information until the synchword of the next s-frame. So s-frames are continuously transmitted without pause. Because part of astronomical data is lost during s-frame header on-board packing, the Decoder must discard the header and replace it with generated pseudo random sequences as pseudo-astronomical data sent to "ASTRONOMICAL DATA" outputs during the header time.

2. At first for correct decoding, Decoder must detect the synchword. This process is called a "primary synchronization" and it will be described at p.4.4.5. Synchword format, length and detection algorithm were used in accordance with a hard recommendation by V.V.Andreyanov. It should be pointed out that to distinguish "POLARIZATION I" data stream from "POLARIZATION II" one, the synchword for "POLARIZATION II" data stream is transmitted two bytes later compared with synchronous transmission for "POLARIZATION I" one; this is provided by difference in format of headers (see Fig. 11).

3. Auxiliary information contains information of various types, such as observation frequency, calibration mode, power level etc. Generally we can say that all kinds of auxiliary information must be processed by Decoder in accordance with mentioned algorithms (see p.4.4.6). The results of this processing should should be formed into serial packets (see packets format in p.4.4.9) and transmitted by serial interface RS-232C to recorder Terminal Control Computer through Decoder output "INTERFACE RS-232C". Auxiliary information processing and transmitting of its results in packets are carried out periodically and synchronously with s-1 sec tick (see next point 4).

4. Decoder must detect s-1 sec tick from data time index transmitted in "POLARIZATION I" header. The detection of s-1 sec tick is based on determining that the data time index is divisible by 400 and gating the first bit of astronomical data from the frame with such data time index. On the other side Decoder must continuously generate the s-1 sec tick independent of failures of s-1 sec detection. This is because Decoder must continuously support the s-1 sec time scale by s-time counter clocked from PLL based on "CLOCK-IN" input signal and started once from s-1 sec detection block (see Fig. 4). The s-time counter output pulses s-1 sec is transmitted to Recorder Terminal through Decoder output "S-1 SEC". In addition s-time counter has to previously setting primary time code, which will be sent by Decoder Terminal Control Computer or by operator from Manual Control front panel. More detail description of Decoder time measurement see in p.4.4.7.

5. Decoder must measure time interval between as-1 sec tick and 1 sec pulse supplied from station clock through Decoder input "1 SEC". This time interval is conditionally called the "navigation delay". The "navigation delay" should be measured with 10 ns accuracy using signal from Decoder input "5 MHz" as a reference signal from Decoder input "5 MHz" as a reference signal for PLL to generate 100 MHz measure clock signal (see Fig 4). The "navigation delay" code should be packed to Decoder auxiliary information packet to sent it to Recorder Control Computer through RS-232C interface line.

6. Decoder must generate data clock signal and send it to Recorder terminal through Decoder output "CLOCK-OUT". The frequency of this signal is selected according to the Recorder Terminal being used: 32 MHz for Canadian and VLBA one, 72 MHz for MkIII one and 32/n MHz for future implementations (K-4 for example). Because the clock-out frequency must be constant independent of Radioastron modes, the clock-out signal should be generated by a PLL with variable divider factor based on clock-in signal as reference.

7. Decoder must have remote control and monitoring of its work by RS-232C interface line through Decoder output "INTERFACE RS-232C". Format of all control commands and monitor messages are described in p.4.4.9. In addition to remote Decoder control and monitoring, Decoder must provide the same functions by means the front panel buttons and indicators.

8. Decoder must test the parity bits of received bytes from "POLARIZATION I" and "POLARIZATION II" lines. Detected parity errors should be accumulated during s-1 sec for each frame, compared with error threshold previously set by Control Computer and the result (1, if parity frame error rate exceeds the threshold; 0, otherwise) should be written to ERROR BIT MAP for further generating information packet SES to Control Computer through RS-232C line.

In addition for each data block (one frame consists of 10 data blocks per 1997 bytes) and for frame header, the Decoder must calculate the Longitude Control Byte (LCB) and correct the single bit errors using byte parity bit. If bit error correcting circuit will require considerable design and cost expenditures, it is allowed to implement a simplified algorithm: add two errors to the block parity error counter in case no parity errors are detected and calculated LCB is not equal the received LCB; this accounts for the expected appearance of a double bit error inside one byte, which is not detected by the parity bit. Otherwise, the block parity error counter is not changed.

9. Decoder must provide complete self testing (Decoder mode AUTOTEST) after power on and in error case interrupts the AUTOTEST procedure and sets the error code in Decoder Status Register read by Control Computer or Front Panel.

10. Decoder must operate in the following modes:
a) Radioastron observation modes - "OBS"
b) Decoder testing by test input signals generated inside the Decoder - "DECT"
c) Formatter testing by test input signals generated inside the on board Formatter - "FORDIGT"
d) continuously generating the synchword - "SYNCHTST"
c) output cable test - "TDG"
Each Decoder mode is described in detail in p.4.4.9.1.5.

4.4.2. Outer devices connected to Decoder and interface signal specification.

4.4.2.1. Decoder input signals received from Down Link Receiver (number of signals = 3):
1) data stream line "POLARIZATION I";

2) data stream line "POLARIZATION II";
3) input data bit rate clock signal "CLOCK-IN", with selected frequency which smoothly varies in reference range less than 10.

- input data bit rates are selected from following values: 72, 36, 18 Mbit/sec with byte parity transmission.

- signal levels ECL biphase: "0"= -1.61 : -1.81 V
"1"= -0.88 : -1.025 V.

- Down Link Receiver output resistance: 50+-20 ohm

- Down Link Receiver output cable (Soviet RK-50): less than 5m+-5.0mm [?]

- RF - connector types: (Soviet) CP-50-73F or (US) BNC.

- input data stream format: see p.4.4.4.

- input clock signal form is in meander form.

- data and clock signal edges - less than 1 ns.

- time difference between clock signal edge and data signal edge: less than 1 ns.

- bit error rate in down link channel - less than 10^-??.

- input clock and data time diagram is shown in Fig. 2.

4.4.2.2. Recorder terminal.

Decoder and Recorder Terminal are connected by plate [ribbon] cable for ECL data and clock transmission. Decoder can be connected to two types of Recorder terminal, S2 and VLBA.

4.4.2.2.1. Cable C2.

4.4.2.2.1.1. Cable C2 signal specification.

Decoder transmits to Recorder Terminal through C2 cable the following signals:

* "ASTRONOMICAL DATA" outputs - 16 biphase data lines:

Spec.	Signal full name	S2	VLBA
1US		03	04
___	sign bit data from upper side band of channel 1		
1US		04	03
1UA		05	06
___	amplitude bit data from upper side band of channel 1		
1UA		06	05
1LS		07	08
___	sign bit data from lower side band of channel 1		
1LS		08	07
1LA		09	10
___	amplitude bit data from lower side band of channel 1		
1LA		10	09
2US		13	14
___	sign bit data from upper side band of channel 2		
2US		14	13

2UA		15	16
___	amplitude bit data from upper side band of channel 2		
2UA		16	15
2LS		17	18
___	sign bit data from lower side band of channel 2		
2LS		18	17
2LA		19	20
___	amplitude bit data from lower side band of channel 2		
2LA		20	19
3US		23	24
___	sign bit data from upper side band of channel 3		
3US		24	23
3UA		25	26
___	amplitude bit data from upper side band of channel 3		
3UA		26	25
3LS		27	28
___	sign bit data from lower side band of channel 3		
3LS		28	27
3LA		29	30
___	amplitude bit data from lower side band of channel 3		
3LA		30	29
4US		33	34
___	sign bit data from upper side band of channel 4		
4US		34	33
4UA		35	36
___	amplitude bit data from upper side band of channel 4		
4UA		36	35
4LS		37	38
___	sign bit data from lower side band of channel 4		
4LS		38	37
4LA		39	40
___	amplitude bit data from lower side band of channel 4		
4LA		40	39

* "CLOCK-OUT"
Clock signal of fixed frequency in all Decoder modess is generated from CLOCK-IN signal. Clock-out signal frequency can be selected by control computer from following values:
32 (default) or 72 or 32/n MHz (n = 2,4,8).

Spec.	Signal full name	S2	VLBA
S-CLK		43	44
_____	Recorder terminal sampler clock		
S-CLK		44	43

* "S-1 SEC" output
Satellite second tick: pulse with duration 31.3 ns and with edges less than 5 ns. S-1 SEC tick time relation to "CLOCK-OUT" signal is shown in Fig. 3.

S-1		47	48
___	satellite 1 sec tick		

S-1 48 47

* "S-FRAME" output
Satellite frame tick: pulse with duration 31.3 ns and with edges less than 5 ns.

S-FRAME 49 50
_____ satellite frame tick
S-FRAME 50 49

C2 cable contacts C2:1, 26, 6, 31, 11, 36, 16, 41, 21, 46, 23, 48, are grounded near signal sources.

4.4.2.2.1.2. C2 cable signal electrical specifications.

All output signals are transmitted by terminated ECL drivers in both true and inverted polarity along twisted pairs. Each twisted pair is terminated differentially in 100 ohms, as shown in Fig. 16.

4.4.2.2.1.3. C2 cable physical characteristics.

Cable is to be SCOTCH type 1700-50 50 conductor twisted pair cable or equivalent and connector is to be Scotch header part number 3443-5302; socket part number 3425-6600 with strain relief clips part number 3448-3050 or equivalent. The length of the cable should not exceed 10 meters.

4.4.2.2.2. S2 cable.

The serial link between the data source and the Recorder Terminal is to be standard RS232. The S2 cable is to be equipped with DB-25 connectors.

Preliminary RS232 serial line parameters:
Serial data rate: 9 600 Baud.
Asynchronous transmission.
Odd parity.
One stop bit.

4.4.2.3. Hydrogen maser.

H-maser (Soviet Ch1-70) provides for Decoder:
- sine form clock reference signal 5 MHz with level 100-200 mV sqr.
- output resistance 50+-20 ohm.
- connector type (Soviet) - CP-50-73F or (US) BNC.

4.4.2.4. Station time service receiver.

Time service receiver (Soviet Ch7-15) provides For Decoder "1 SEC" tick (mark pulse output) with following parameters:
- time scale 1 Hz signal in TTL form with duration 3-5 us, and with edges less than 100 ns.
- output resistance 300+-20 Ohm, 300 pf.
- connector type: CH-50-73A or (US) BNC.

4.4.3. Data packing principle in serial down link lines and decoding algorithm.

4.4.3.1. Radioastron observation mode translation to decoding mode.

Radioastron observation mode specification is a convenience for the astronomical users. In order to make easier understanding of decoding process for Decoder designers we will describe formal rules to translate Radioastron observation mode specification to decoding modes because the Control Computer sends the Radioastron observation mode code to Decoder.

Radioastron observation modes are specified in accordance with the following rules:

First position - Rome digit means number of video channel pairs (upper & lower side band) used for each serial lines ("POLARIZATION I","POLARIZATION II"). It can be selected from 1 or 2 or 3.

Second position - letter means down link transmission rate. It can be selected from L - 18, M - 36, F - 72 Mbit/sec.

Third position - Arabian digit means number of bits in channel data sample. It can be selected from 1 or 2.

All Radioastron modes with data bit rate, number of packed channels and number of sampled bits are shown in Table 1.

Using Radioastron mode specifications, we can obtain decoding parameters in accordance with following rules:

A. Number of packed channels equals double the value of first element of Radioastron mode specification.

I-X-X - channel 1U and 1L are packed for "POLARIZATION I" line,
channel 3U and 3L are packed for "POLARIZATION II" line

II-X-X - channel 1U, 1L, 2U, 2L are packed for "POLARIZATION I" line,
channel 3U, 3L, 4U, are packed for "POLARIZATION II" line

IV-X-X - channel 1U, 1L, 2U, 2L are packed for "POLARIZATION I" line,
channel 3U, 3L, 4U, are packed for "POLARIZATION II" line

B. Number of bits in one channel sample equals third element in Radioastron observation specification.

X-X-1 - each channel sample is represented by one bit called sign bit in Decoder output signal specification: XXS.

X-X-2 - each channel sample is represented by two bits called sign and amplitude bits in Decoder output signal specification: XXS and XXA.

C. The data rate obtained from second element of Radioastron observation mode specification is not required for decoding process, but it is used for Decoder CLOCK-OUT signal generation.

4.4.3.2. Decoding Table.

The left colon of Decoding Table (Table 2) represents the number of bits in serial sample code for "POLARIZATION I" and "POLARIZATION II" lines. In this column the bit numeration begins from 1 for "POLARIZATION I" and from 9 for "POLARIZATION II". Decoder output numbers are shown in table lines for different observation mode groups marked in upper line.

4.4.3.3. Decoding functional diagram.

The common decoding functional diagram is shown in Fig. 6A. It contains a shift register for each lines "POLARIZATION I" and "POLARIZATION II", demultiplexor and output resynchronization triggers. Both shift registers are clocked by CLOCK-IN signal (72 or 36 or 18 Mbit/sec). "POLARIZATION I" data, after changing header to pseudo-noise sequences, is sent to the shift register RG1 serial input DATA1. The similar signal obtained from "POLARIZATION II" data is sent to the shift register RG2 serial input DATA2.

Since data is loaded to shift register with one sample length for all

used channel in given mode (sample length can be selected from 2, 4 or 8 bits for each register), the data are read from parallel outputs of both registers to demultiplexor.

Demultiplexor (Fig. 6B) consists of ten logic switches (Fig. 6C). Each switch connects one input data line to one from two output lines in accordance to control lines C1, C2, C3. All switches are divided by 3 groups. Each group is controlled by single line C1 or C2 or C3. Dependence between C1-C3 control signals and observation modes is shown in Table 3. Demultiplexor supplies the data to output triggers clocked by channel sample pulses with frequency 16 or 8 or 4 MHz.

It should be pointed out that pseudo noise sequences must not repeated during data decoding interval more than s-1 sec (30 bytes * 400 = 12000 bytes for 72 Mbit/sec).

4.4.4. Down link data format for "POLARIZATION I" and "POLARIZATION II" Decoder inputs.

4.4.4.1. The general comments.

1 frame = 20 000 bytes.
Data rates can be selected from 72, 36, 18 Mbit/sec.
Frame header length equals 30 bytes.
One frame consists from header and data zone.
Data zone consists from 10 data blocks.
One data block consists from 1997 bytes.

4.4.4.2. Data byte structure.

Data byte structure depends from Radioastron observation modes and is shown in Fig. 5. Ninth data byte bit is inverted minor bit of sum obtained from all 8 byte bits (odd parity bit).

4.4.4.3. Header structure.

Header contains 30 bytes.

4.4.4.3.1. Longitude Control Byte

The longitude control byte (LRC [or LCB]) is calculated as for each data blocks as for header. Each bit of LRC is inverted minor bit of sum calculated for one bits for all bytes in the block. For example third bit of LRC is sum of third bits of all block bytes (see example in Fig. 13, where 3-bytes data block is illustrated for simplicity). The LRC for all blocks are loaded in 10 bytes of the header of the next frame (header bytes 1-20).

NOTE: The LRC is not implemented in the present on-board formatter designed by the Hungarian group.

4.4.4.3.2. Power level.

One header contains power level information in 4 bytes. The on board power level measurement system produced two pairs power level values per channel.

First pair of values is generated during the power level calibration-off and are loaded in frame with odd data time index for 72 Mbit/sec or with non divisible by 4 data time index for 36 Mbit/sec or with non divisible by 8 data time index for 18 Mbit/sec. Second pair is generated during the power level calibration-on and are loaded in frame with even data time index for 72 Mbit/sec or with divisible by 4 data time index for 36 Mbit/sec or with divisible by 8 data time index for 18 Mbit/sec. The first part of each pairs is 12-bit power level ADC output code called POFF in calibration-off case and PON in

calibration-on case (11-12 header byte).Each power level code consists from 4-bit channel number and 12-bit power level.The second part of each pairs is channel attenuator value in dB called LDBF for calibration-on and LDBF for calibration-off (13-15 header byte). So each packed video channel are accompanied by four values: PON, POFF, LDBN, LDBF loaded in two neibour frames. Because of 2 or 4 video channels are used in different Radioastron modes per "POLARIZATION I" or "POLARIZATION II" lines, power level information for all channels requires 4 or 8 neibour frames.

Channel numbers loaded in 4 bit of header are numerated in accordance to Table in Fig. 12A. The additional numbers 9 and 10 are referred to common power level measured on IF output (this measurement is under considering by Hungarian Formatter designers). Channel #9 is referred to common power level for "POLARIZATION I", and channel #10 - for "POLARIZATION II".

4.4.4.3.4. Radioastron observation modes.

Radioastron observation mode is loaded to 15th byte of header.

1-st bit: bit sampling

0 - 1 bit sampling
1 - 2 bit sampling

2-3-d bits: LPF band

01 - 2 MHz (4 Mbit/sec)
10 - 4 MHz (8 Mbit/sec)
11 - 8 MHz (16 Mbit/sec)

4-8th bits: IF frequency selected configuration and number of video channels. In other words, it is modified first element of Radioastron observation mode designation. I is modified to letter that means one selected IF local oscillator frequency: A, B, C, D. II is modified to two letters that mean two selected IF local oscillator frequencies: AB, AC, AD, BC, BD, CD. IV is modified to letter that means one of selected sky polarization R or L observed in total Radioastron band using all IF local oscillator frequencies A, B, C, D. So binary codes are:

00000 - R-X-X
00001 - L-X-X
10000 - A-X-X
01000 - B-X-X
00100 - C-X-X
00010 - D-X-X
11000 - AB-X-X
10100 - AC-X-X
10010 - AD-X-X
01100 - BC-X-X
01010 - BD-X-X
00110 - CD-X-X

4.4.4.3.4. Synchword.

Synchword is loaded to 7 bytes and it is a beginner of frame. All information replaced before is referred to previous frame. To distinguish "POLARIZATION I" line from "POLARIZATION II" line synchword is loaded to 16th byte of "POLARIZATION I" header and to 17th byte of "POLARIZATION II" header. Synchword format is shown in Fig. 13B.

4.4.4.3.5. Radioastron receivers mode.

Radioastron receivers mode is loaded to 24-25th bytes of header in accordance to following binary codes:

24-th byte:
1-st bit - sky polarization
0 - right polarization
1 - left polarization
2-3-rd bits - receiver band in given observation
00 - P-band receiver is used
01 - L-band receiver is used
10 - S-band receiver is used
00 - K-band receiver is used
4-8-th bits - receiver attenuator value

25-th byte:
1-st bit - means noise calibration
0 - noise calibration on
1 - noise calibration off
2-nd bit - means noise calibration amplitude
0 - calibration amplitude is 10% of antenna noise temperature
1 - calibration amplitude is 100% of antenna noise temperature
3-rd bit - means phase calibration
0 - phase calibration off
1 - phase calibration on
4-th bit - means Formatter mode
0 Formatter generates test signal
1 Formatter observation mode

4.4.4.3.6. Data frame index.

Data frame index is loaded to 26-29th bytes in binary code.

4.4.4.3.7. Header LCB.

Header LCB is loaded to 30-th header byte.

4.4.4.3.8. On-board equipment status.

On-board equipment status is loaded to 23-th POLARIZATION I header byte and to 16-th POLARIZATION II header byte. The bit assignment is following:

0 bit [TBD](awaiting information from Andreanov)
1 bit [TBD]
2 bit [TBD]
3 bit [TBD]
4 bit [TBD]
6 bit [TBD]
7 bit [TBD]

4.4.5. Synchword detection algorithm.

4.4.5.1. Primary synchronization.

Version 1: main Fig. 7.

Digital data stream is supplied to serial input of shift register. Length of shift register equals to synchword length 63 bit. The register shift clock equals data rate. Parallel outputs of the shift register are connected to 63 XORs. Other input of XORs is connected to synchword mask register with written expected synchword code. XOR output signals are supplied to 63-input adder. When the whole synchword is loaded to shift register the adder output will be equal to synchword auto correlation function with zero delay. The adder output is compared with threshold loaded by control computer.

Version 2: option

Parallel outputs of the same shift register are connected to 7 parity checkers to check even parity. Because of synchword bytes have even parity bit in difference data bytes with odd parity bit, outputs of parity checkers summed in 7 input adder will produced the maximum value at the adder output. Comparing the adder output with threshold in comparator provides the synchword detection signal.

It is desirable in designing to consider version 1 and version 2 in terms of synchword detection probability vs. circuit complexity.

We suggest the following primary synchword detection block signals:

inputs:
- DATA 72,36 or 18 Mbit/sec
- DSNW shift register enable
- TACF set threshold by control computer
- switch to synchword mask

outputs:
SYN synchword detection signal

4.4.5.2. Secondary synchronization.

Secondary synchronization uses the primary synchronization circuits and additionally generates control strobe signal based on previously primary synchronization to enable shift register in expected synchword time arrival interval. In addition secondary synchronization circuit must be able to test expected time index and in case a great distortion in synchword with good result of time index testing it must not lose synchword synchronization. It should be planned error indication of "WRONG TIME INDEX" in Decoder status register.

4.4.6. Auxiliary information processing algorithm.

4.4.6.1. Power level processing.

Because of power level measurement time constant more than 1 sec Decoder will use power level value transmitted in the beginner and tail of s-1 sec interval. Decoder control microprocessor will be able to calculate power level in accordance with following algorithm:

1. Skip about 10 frames from the beginner of s-1 sec interval.
2. Read and store POFF1, PON1, LDBN1, LDBF1.
3. Skip some frames until about 10 frames before tail of s-1 sec interval.
4. Read and store POFF2, PON2, LDBN2, LDBF2.
5. Calculate means of its values:

$$PON = (PON1 + PON2) / 2$$
$$POFF = (POFF1 + POFF2) / 2$$
$$LDBN = (LDBN1 + LDBN2) / 2$$
$$LDBF = (LDBF1 + LDBF2) / 2$$

6. Using LDBN find in calibration dependence the calibration step CAL versus LDBN.

7. Calculate the reference gain diverge factor COG:

$$COG = (PON - POFF) / CAL$$

8. If LDBN <> LDBF, then to correct COG:

$$COG = COG + (P1(LDBN) - P2(LDBF)) / CAL$$

where, P1 and P2 are power levels obtained from calibration table of

dependence the power level versus attenuator value.

9. Calculate the common power level for transmission to Control computer.

4.4.6.2. Radioastron mode code processing.

Radioastron mode code is moved to SMF packet to transmit it to Control Computer.

4.4.6.3. Data time frame index processing.

For beginning make more clear meaning of data time index. The functional block diagram of data time index forming in on board Formatter is shown in Fig. A3 [this figure is missing]. The data time index code is read to data time index register from data time counter. The data time counter is clocked by "fixed" rate 400 Hz pulses generated from up link reference frequency. This rate is independent from the different down link rate 18,36,72 Mbit/sec. Each current frame tick (2.5 ms, 5 ms and 10 ms) the data time index counter value is rewritten to frame index register to insert this value to frame header. So the relation between down link rate, frame duration and frame index increment is followed to:

Down link rate Mbit/sec	Frame duration msec	Frame index increment
72	2.5	1
36	5.0	2
18	10.0	4

The primary data time frame index value is set by another, similar "rubidium time frame index" counter clocked by continuously working on-board Rb-standard. This setting procedure is carried out each new connection with changing of ground down link station or by special command from Control Space Center.

Decoder packs frame index to SMF message (See p.4.4.9.3) each as-1 sec.

In addition, Decoder marks the continuous time interval which doesn't contain any sync-errors, by the beginning frame index and trailing frame index of this interval. These frame indexes are packed to SES message (See p.4.4.9.3).

4.4.6.4. Longitude Control Sum Code processing.

To correct errors inside the data block of frame Decoder uses Longitude Control Sum Code from Header of next frame and byte parity bit. To provide the error correction the 180000 kBit RAM is required. The final decision to use or to discard block error correction should be get in designing step.

4.4.7. Time measurements in Decoder.

The common block diagram of Decoder time measurements is shown in Fig. 4.

S-time counter counts clock pulses with "fixed" frequency 32 MHz provided by divider with variable divisor factor. The divider is supplied by down link synchro clock 18, 36, 72 MHz.

The primary value of this counter is set by command "TIME" from Decoder Control Computer with accuracy 1 msec or is cleared by Decoder. The counter is started by frame clock pulse strobed from Decoder or Control Computer signal. S-time code from parallel outputs

of this counter is packed to SMF message each as-1 sec tick. Output pulse from s-time counter is called "as-1 sec" to distinguish it from Header detector s-1 sec pulse.

It is desirable to form s-time error flag bit in decoder status register when the time interval between s-1 sec pulse and as-1 sec pulse will change more than one pulse of clock frequency 32 MHz.

Decoder navigation delay time counter must count 100 MHz pulses formed by PLL-oscillator supplied 5 MHz reference signal from "5MHz" input. The navigation delay counter is started by station 1 sec pulse from "1 sec" input and is stopped by as-1 sec pulse. The navigation delay code from parallel output of the counter is packed to SMF message. More detail description of tie setting procedure see in 4.4.9.1.

4.4.8. Data quality estimation.

Transmitted data quality is determed by the quantity of sync errors and the quantity of byte parity errors. Decoder must mark the sync errors and count the quantity of parity errors for each frame.

Each s-1 sec Decoder sent to Control computer the start time when the reliable header synchronization will be achieve by writing the frame index aligned with this time to SES message. Then Decoder counts the quantity of byte parity errors for each frame and Longitude Control sum for each frame data block. In case when Decoder doesn't detect byte parity errors for a data block and the counted Longitude Control Sum (LCS) doesn't equal to written LCS in frame header, the frame data error counter is incremented by 2 (if designer doesn't use the correction of data in data block). After data error analyzing for whole frame Decoder compares the value of data error counter with frame error threshold previously set by Control Computer. Decoder has Error Bit Map memory to generate SES message for s-1 sec interval. Each bit of this Map is a result of above mentioned comparing.

In addition Error Bit Map reflects the beginner of sync error inside of s-1 sec interval by writing the frame index of last process able data frame. In principle Decoder can mark the end of sync error inside of s-1 sec interval by similar technique. But for sync reliability Decoder always begins decoding of data exactly with s-1 sec tick. (It would be interesting to consider the flexible control of Decoder header detector mode to realize the short burst (less than s-1 sec) data interval marks in SES message that may be useful in trouble error rate situations.) Anyway, each Error Bit Map begins from frame index code.

4.4.9. Decoder Control and Monitoring

The Satellite Decoder will operate in two control modes: the LOCAL and REMOTE control modes. In the LOCAL control mode, The Satellite Decoder operations are controlled by the Satellite Decoder front panel functions, in addition to the control commands from the remote Control Computer (CC). In the REMOTE control mode, the Satellite Decoder receives control commands only from the CC and all of the front panel functions are disabled. The communication between the Satellite Decoder Controller is standard RS232.

In addition to receiving control commands from the CC, the Satellite Decoder sends status information to the CC as well as message information destined for logging onto a status floppy.

The general message protocol for communication over the RS232 link between the Satellite Decoder Controller (DC) and CC will now be described (see Fig. 14a,b). Each transmission packet consists of an SOT (ASCII control character for Start of Transmission, 01 Hex), a

byte count (indicating the total number of bytes sent, excluding the SOT and EOT), a 1-byte binary code (representing the various command and status message packets), message packet of variable length, a checksum byte (representing the 8-bit sum of the byte count, code and the message packet) and an EOT (ASCII control character for End of Transmission, 04 Hex).

The message packet itself is "free format", that is it may contain up to 252 bytes of either binary data or ASCII characters or both. For this reason, an extra SOT must be appended to any packet byte (after the first SOT & including the checksum) containing the ASCII value of SOT (01 Hex) in order for the recipient of the packet to distinguish it from the true framing SOT character. The CC will always discard the current packet and assume the start of a new transmission whenever a single SOT character is received. When a transmission error occurs (ie. when the checksum does not agree or an EOT is not found after the checksum byte) the CC will request a resend.

There are three types of message packet:

* Instruction packets: These are the various control commands sent to the DC such as initialization, setting of time, setting the Decoder modes, etc.

* Status packets: These contain status information requested by CC such as synchronization ok, time set ok, etc.

* Information packet: These are information packets such as Satellite Decoder Header message packet, Satellite Decoder Error message packet, etc. sent to CC synchronously to s-1 sec Hz.

4.4.9.1. Decoder instruction packets.

Fig. 14a shows the instruction message packets with the binary codes, their mnemonics, and their corresponding code descriptions. The instruction packet code start from hex 10 and end to 2F hex.

4.4.9.1.1. Initialization - INIT.

INIT instruction has code 10 hex. This command resets Decoder registers, counters, latches etc. and prepares the Decoder for synchronization. INIT does not reset Status Register. After INIT, Decoder enters WAIT state until the next instruction.

4.4.9.1.2. Set the Decoder time - TIME.

TIME instruction has code 11 hex. After the CC sends an OBS (or DECT, or SFORMT) instruction to set the observation mode, the Decoder carries out the frame synchronization sequence and initializes the as-1 Hz output tick. The Decoder then sends the SMF message to CC, where the time index counter contents are extracted. The CC must calculate the time for transmission of TIME instruction using the received time index counter contents and difference between own clock and s-clock concerned with Doppler effect. This transmission time provides the receiving the TIME instruction before desirable frame tick but after preceding desirable frame tick. In Novikov's case the desirable frame tick is frame with frame index divisible by 400. And in D'Addario's case the desirable frame tick is nearest to ground station 1 sec tick. The CC must calculate too s-time in DHMS form using or the receiver time index and other information (such as Rb-start time, etc), and then sends the TIME instruction to the Decoder in calculated time. The Decoder receives the TIME instruction, presets the s-time counter and halts it; the nearest next frame tick enables the counter. Following this procedure, the Decoder will transmit the 'correct' s-time in SMF packet. Note: the s-time setting

procedure cannot be initiated while the Decoder is in WAIT condition.

4.4.9.1.3. Send Decoder Status Register to CC instruction - SRS.

SRS instruction has code 12 hex.

4.4.9.1.4. Resend previous message instruction - RSN.

RSN instruction has code 13 hex. If the checksum does not agree, such as in the case of transmission error, the recipient of the message will request a resend.

4.4.9.1.5. Set Decoder mode instruction group DECMOD.

If the new Decoder mode results in a change in the down link data clock frequency, an internal INIT instruction is executed to begin primary s-frame synchronization, and the new data demultiplexing is set in. If the down link frequency is unchanged, s-frame synchronization is not lost and only the data demultiplexing needs to be set in. Down link frequencies are encoded as L = 18 Mb/s, M = 36 Mb/s, H = 72 Mb/s. There are 4 possible Decoder modes: DECT, SFORMT, SYNCHT, OBS.

4.4.9.1.5.1. Decoder test mode instruction - DECT.

DECT instruction has code 14 hex. This instruction sets Decoder to test mode according to the observing mode prescribed in message packet. In test mode, the Decoder produces internal down link receiver clock. The input data streams POL. I and POL.II are read from the input ROM. The output ASTRONOMICAL DATA is then compared with the expected data read from output ROM. ROM address is determined by the decoding mode. Any errors occurring during the test will set the Status Register Error Bit. The SMF and SES messages are formed and can be sent to CC to be analyzed. In addition, DECT will inform The Decoder to commence transferring, at the next s-1 Hz tick, the prescribed test vector sequence to the recording system over the RadioAstron Record Interface (C1 cable) for the purpose of checking the consistency of the Decoder to recorder data link. Test vector data is to be replaced by true (astronomical) data when the Decoder leaves this test mode.

4.4.9.1.5.2. Formatter test mode instruction - SFORMT.

SFORMT instruction has code 15 hex. This instruction sets Satellite Formatter test mode; this instruction is similar to DECT except the down link receiver clock and the input data streams are not generated internally by the Decoder, instead these inputs are taken from the external satellite source. (Presumably, this instruction is used in conjunction with a instruction to the satellite to enter a satellite formatter check mode as well.)

4.4.9.1.5.3. Down link synchronization test mode instruction - SYNCHT.

SYNCHT instruction has code 16 hex. This instruction sets Decoder to synchronization test mode. In this mode, a series of synchro words (without the formatted data) is sent to the Decoder inputs POL.I and POL.II. The Decoder then performs the primary frame synchronization. Synchronization failures is accumulated for every s-1 Hz interval and then sent to the CC in BER packet.

4.4.9.1.5.4. Observation mode instruction OBS.

OBS instruction has code 17 hex. This instruction sets the Decoder to the observation mode as prescribed in the message packet. The Decoder then synchronizes to the beginning of s-frame, starts transmitting the

SMF and SES packets synchronous with s-1 Hz. This instruction is used to commence a normal observing period.

4.4.9.1.6. Decoder output clock frequency set instruction - SCLK.

SCLK instruction has code 18 hex. This instruction selects one of the Decoder output frequencies: S-32 (for S2 and VLBA DAS), S-72 (for MkIII DAS), S-16, S-8, S-4 MHz (for future implementation).

4.4.9.1.7. Threshold value set instruction - SETTRESH.

SETTRESH instruction has code 19 hex. This instruction sets the threshold value for qualifying the frame error count to set the Frame Error Bit Map. The SETTRESH message packet contain two bytes of binary coded threshold value: the first being the most significant threshold byte and the second being the least significant threshold byte.

4.4.9.2. Decoder status message packets.

Fig. 14b shows the status message packets with the binary codes, their mnemonics, and their corresponding code descriptions. The instruction packet code start from hex 30 and end to 3F hex.

4.4.9.2.1. Status message INITST.

Status message INITST has code 30 hex. The INITST is sent after the power-up, autotest procedure or initialization requested by INIT instruction has been completed. The status of the Decoder initialization is ASCII 1 = OK, 0 = not OK. OK is INIT successful. i.e. power on and AUTOTEST procedure successful, not OK is INIT failure, i.e. power on and AUTOTEST procedure was completed with error and status register error bit set.

4.4.9.2.2. Status message SYNCHST.

Status message SYNCHTST has code 31 hex. The SYNCHST indicates the status of the Decoder s-frame synchronization after the DECMOD instruction is performed. If the synchronization is successful, the Decoder will respond with the SYNCHTST packet with ASCII 1.

4.4.9.2.3. Status message TIMEST.

Status message TIMEST has code 32 hex. Time status used to indicate whether time in Decoder has been received from CC and updated on the next frame tick. ASCII 1 = OK, 0 = not OK.

4.4.9.2.4. Status message ALARM.

Status message ALARM has code 33 hex. The ALARM status message is the logical sum of all external signals and some signals of the error conditions in Decoder sub-blocks.

4.4.9.2.5. Status message LOCALST.

Status message LOCALST has code 34 hex. The current status of the Local/Remote control mode of the Decoder; ASCII 1 = local ON, ASCII 0 = local OFF.

4.4.9.2.6. Status message TRST.

Status message TRST has code 36 hex. The status of whether the error threshold set successfully following the SETTRESH instruction. ASCII 1 = OK, 0 = not OK.

4.4.9.2.7. Status message CLKST.

Status message CLKST has code 35 hex. The status of whether the output s-clock frequency was set successfully following the SCLK instruction. ASCII 1 = OK, 0 = not OK.

4.4.9.3. Decoder information message packets.

Fig. 14c-d shows the information message packets with the binary codes, their mnemonics, and their corresponding code descriptions.The instruction packet code start from hex 40 and end to 4F hex.

4.4.9.3.1. Information message STREG.

Information message STREG has code 40 hex. Format of STREG message is shown in Fig. 14b,c. Status register information is sent out in response to the SRS command.

4.4.9.3.2. Information message SMF.

Information message SMF has code 41 hex. Format of SMF message is shown in Fig. 14b,e, Satellite Information Message to Formatter. This information is sent during the decoding process synchronously with S-1 Hz tick. The first SMF is sent after response SYNC-OK.

4.4.9.3.3. Information message SES.

Information message SES has code 42 hex. Format of SES message is shown in Fig. 14b,d. Synchronization error status information to CC. This information is sent out during the decoding process synchronously with S-1 Hz tick.

4.4.9.3.4. Information message BER.

Information message BER has code 43 hex. Format of BER message is shown in Fig. 14b,c. Bit error rate determined from synchrotest mode SYNCHT. This information is sent out during primary synchronization process synchronously with S-1 Hz tick. The first BER is sent after status message SYNCHST-OK.

4.4.9.4. Standard Decoder Control Procedure

The standard message exchange between Decoder and Control Computer (CC) can consider as serial steps as it described below and shown in Fig. 8.

Step 0:

When power on the Decoder initializes own counters, triggers and register to status for primary synchronization. Then AUTO TEST procedure automatically carries out. In AUTO TEST the Decoder controller generates the instruction pairs from ROM: INIT - DECT for all decoding modes during 10 sec for each ones. In AUTOTEST the all Decoder outputs has a logical zero of ECL-level. (Decoder is not alive yet for CC). If Decoder will complete AUTOTEST without any errors, the last INIT status packet (INITST-OK) is sent to CC by RS232C link . The first sent to CC INITST means that Decoder is ready to work (Decoder says: I am alive and ready!). Otherwise if any error occurs during decoding in some mode the AUTOTEST procedure stops and Decoder sends the INITST-DOWN to CC. Error code is contained at status register and it can be read by SRS-instruction.

Step 1.

It is recommended that CC sends SRS-instruction to test Decoder status register before each mode switching.

Step 2.

CC sends the SCLK-instruction in order to set required s-clock-out frequency 72, 32, 16, 8 or 4 MHz (32-MHz is default value).

Step 3.

CC sends the DECT-instruction for expected observation mode. After receiving the DECT-instruction the Decoder connects "POLARIZATION I" and "POLARIZATION II" inputs to internal data and synchro test generator. Then it begins the primary synchronization process in Header detector. The S-TIME counter is started in arbitrary moment and counts s-clock pulses and generates the invalid as-1-sec signal to Decoder output "S-1-SEC". Until Header detector can't synchronize to synchword, the Decoder will be send SYNCHST-DOWN at each invalid as-1-sec time. When synchword will be reliable detected (more than for ten frames continuously), using frame tick next events are initialized:

- SYNCHST-OK is sent to CC

- the SMF/SES packets forming are begun

- restart of S-TIME counter to produce as-1 sec tick synchronously with beginner of any frame (soon we don't tag s-time scale or to s-1 sec or to ground 1 sec tick)

In the next as-1-sec Decoder sends the SMF/SES packets to CC. CC analyzes the received data time index and calculate the nearest data time index divided to 400, named S-IND, and calculate s-time code in form hh-mm-ss-ms-us in according to S-IND with additional part, which can be input by operator. When CC receives the data time index (S-IND - 2), it sends the TIME-instruction to Decoder. (it is supposed that speed of RS232 is sufficient to provide the receiving of TIME command by Decoder with one frame accuracy and that CC can calculate the moment for TIME command transmission with the same accuracy taking into account difference between CC-clock and s-clock because of Doppler effect) Then Decoder resets and stops the s-time counter, writes the time code formed by CC to the counter and starts the counter from nearest frame tick. (In VLBA case CC sends TIME command at ground station 1-sec tick with station time code).
After this time setting procedure the SMF packet will be content the valid s-time code. CC receives the TIMEST-OK packet and analyzes the testing SMF/SES packets for some time. Simultaneously Decoder compares all own outputs with content of output ROM. Results of the analysis is written to Decoder status register. The Decoder outputs "ASTRODATA" supplies the test data for recording system.

Please pay attention that SMF/SES packet sending has more high priority than TIMEST packet.

Step 4.

Radioastron observation time schedule determines time when CC sends the SYNCHT-instruction. It is pointed that Decoder always send the last SMF/SES packet completely because of information of its packet refers to previous s-1-sec interval.

In SYNCHT mode Decoder begins a primary synchronization process as above described (some SYNCHTST-DOWN packets and SYNCHST-OK).

When synchword will be detected Decoder begins to send BER packet contained the synch error rate. All packets are sent synchronously with s-1-sec with arbitrary phase.

CC analyzes the BER-packet and calculates the threshold level which is

sent at the end of SYNCHT mode in SETTRESH instruction.

Step 5.

Radioastron observation time schedule determines time when CC sends the SFORMT-instruction. Following control actions are similar to actions in DECT instruction.

Step 6.

Radioastron observation time schedule determines time when CC sends the OBS-instruction. Following control actions are similar to actions in DECT instruction.

Table of Contents

OPERATING MODE #LO-BW-smpl	BASEBAND BANDWIDTH [MHZ]	# BASEBAND CHN. PER POLARIZATION	SAMPLING RATE [MHZ]	DIGITIZING MODE bits/sample	DATA RATE PER BASEBAND [Mb/s]	# of VCRs PER BASEBAND	DATA RATE PER POL. [Mb/s]	# of VCRs PER POL.	UNATTENDED RECORD TIM [hours]
I - 8 - 2	8	2	16	2	32	2	64	4	3.75
I - 8 - 1	8	2	16	1	16	1	32	2	7.50
I - 4 - 2	4	2	8	2	16	1	32	2	7.50
I - 4 - 1	4	2	8	1	8	1/2	16	1	15.0
I - 2 - 2	2	2	4	2	8	1/2	16	1	15.0
II - 8 - 1	8	4	16	1	16	1	64	4	3.75
II - 4 - 2	4	4	8	2	16	1	64	4	3.75
II - 4 - 1	4	4	8	1	8	1/2	32	2	7.50
II - 2 - 2	2	4	4	2	8	1/2	32	2	7.50
II - 2 - 1	2	4	4	1	4	1/4	16	1	15.0
IV - 4 - 1*	4	8	8	1	8	1/2	64	4	7.50
IV - 2 - 2*	2	8	4	2	8	1/2	64	4	7.50
IV - 2 - 1*	2	8	4	1	4	1/4	32	2	15.0

* In Mode IV operation, only one polarization is brought down at a time.

Table 1. Radioastron Modes

Astro Space Centre
Academy of Sciences of the USSR
Fast Processing Laboratory: A.Novikov

Title: RADIOASTRON MODES

Size	Document Number	REV
A	FILE: MODTAB.SCH	1
Date: March 15, 1990	Sheet 1 of 1	

modtab.sch

T1

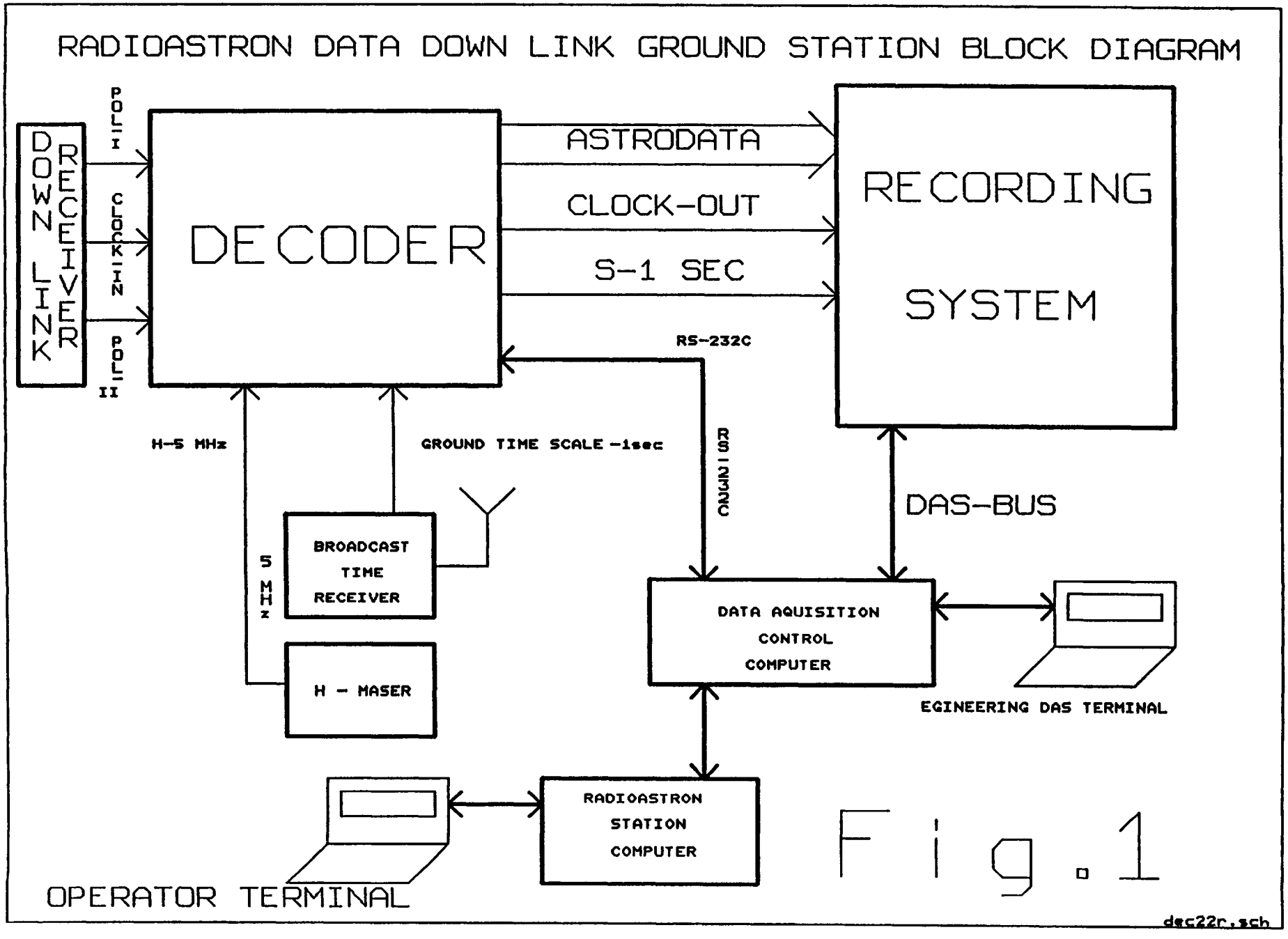

RADIOASTRON DATA DOWN LINK GROUND STATION BLOCK DIAGRAM
DOWN LINK RECEIVER
POL I
CLOCK IN
POL II
DECODER
ASTRODATA
CLOCK-OUT
S-1 SEC
RECORDING SYSTEM
RS-232C
RS-232C
H-5 MHz
GROUND TIME SCALE -1sec
DAS-BUS
5 MHz
BROADCAST TIME RECEIVER
H - MASER
DATA AQUISITION CONTROL COMPUTER
EGINEERING DAS TERMINAL
RADIOASTRON STATION COMPUTER
OPERATOR TERMINAL
dec22r.sch

Fig. 1

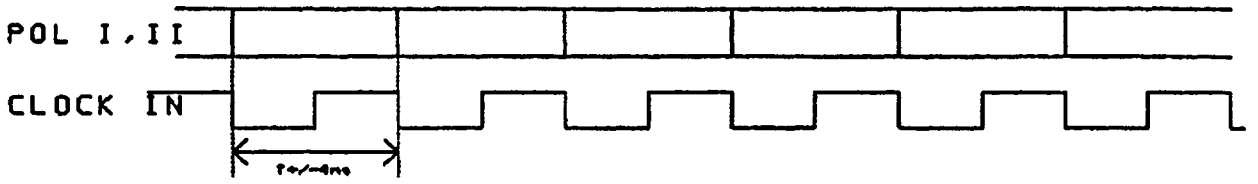


Fig.2. TIMING DIAGRAM OF DECODER INPUT SIGNALS

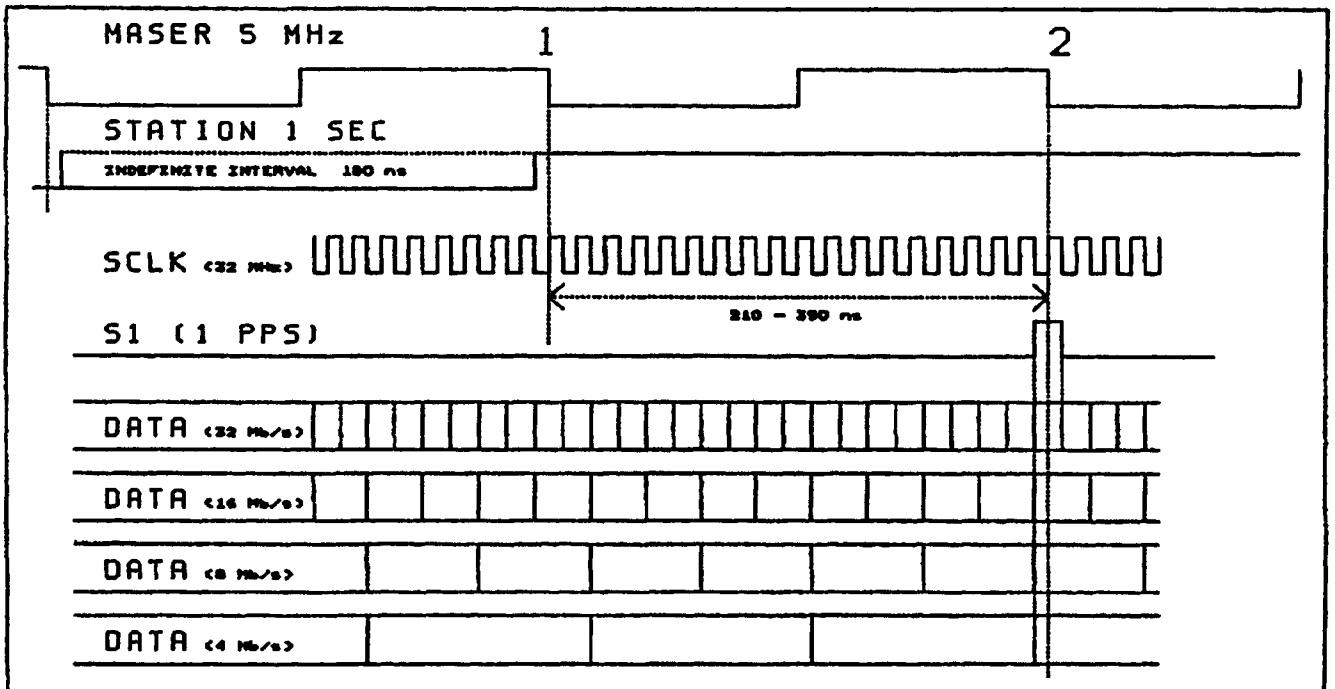


Fig.3. TIMING DIAGRAM OF DECODER OUTPUT SIGNALS

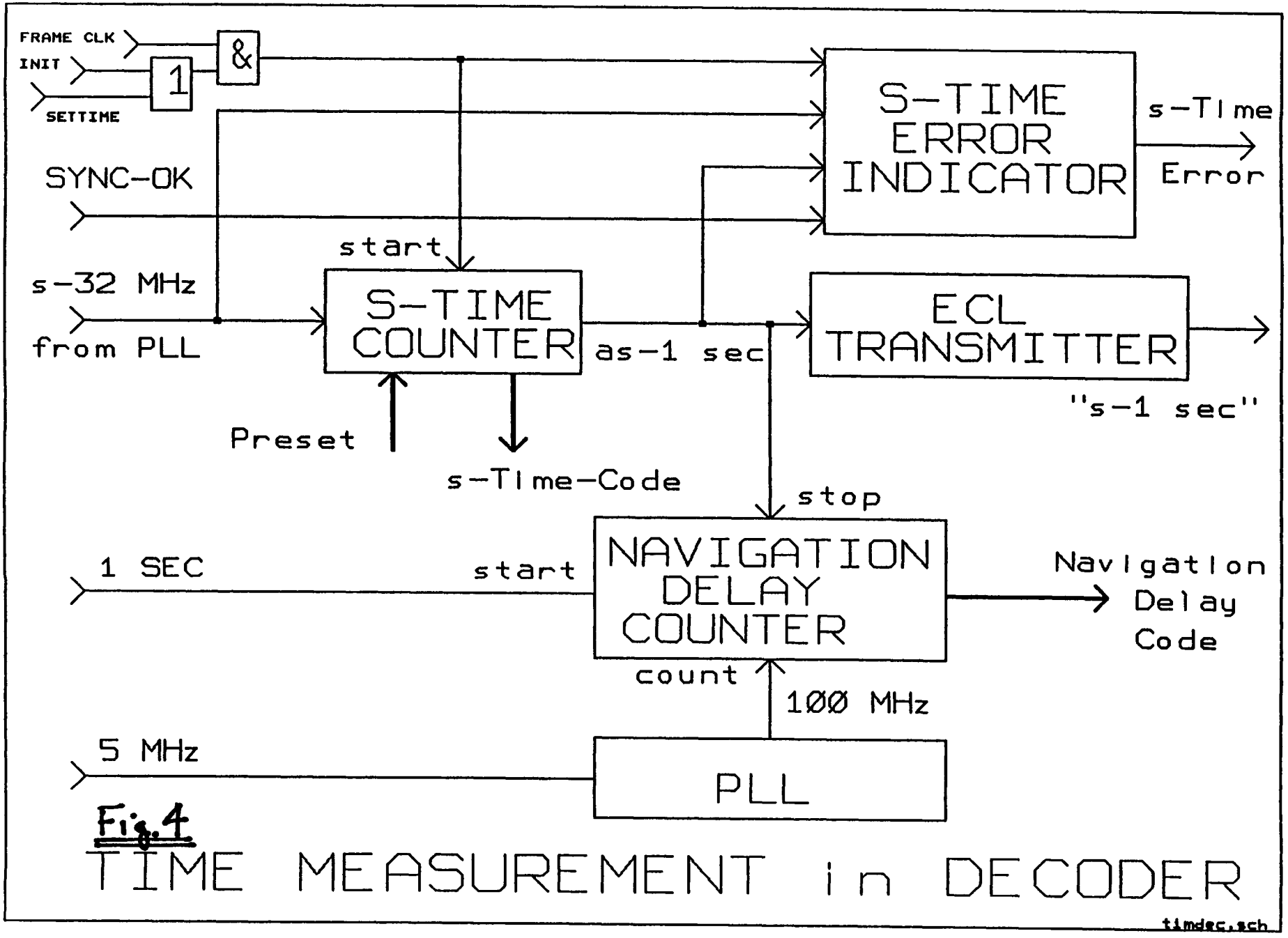


Fig.4

TIME MEASUREMENT in DECODER

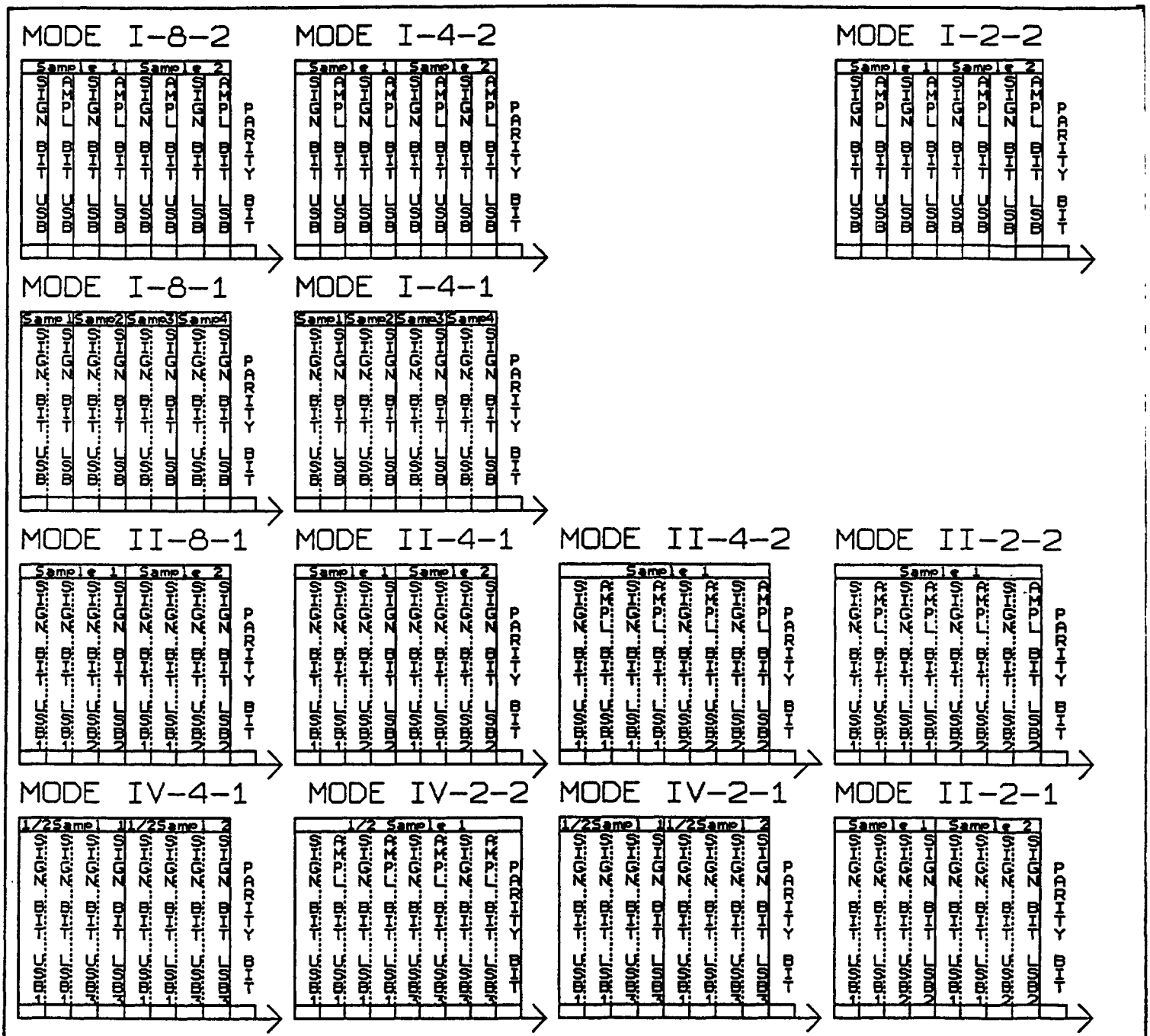


Fig. 5. BYTE STRUCTURE FOR RADIOASTRON MODES

FIGURE 6

TABLES 2 AND 3

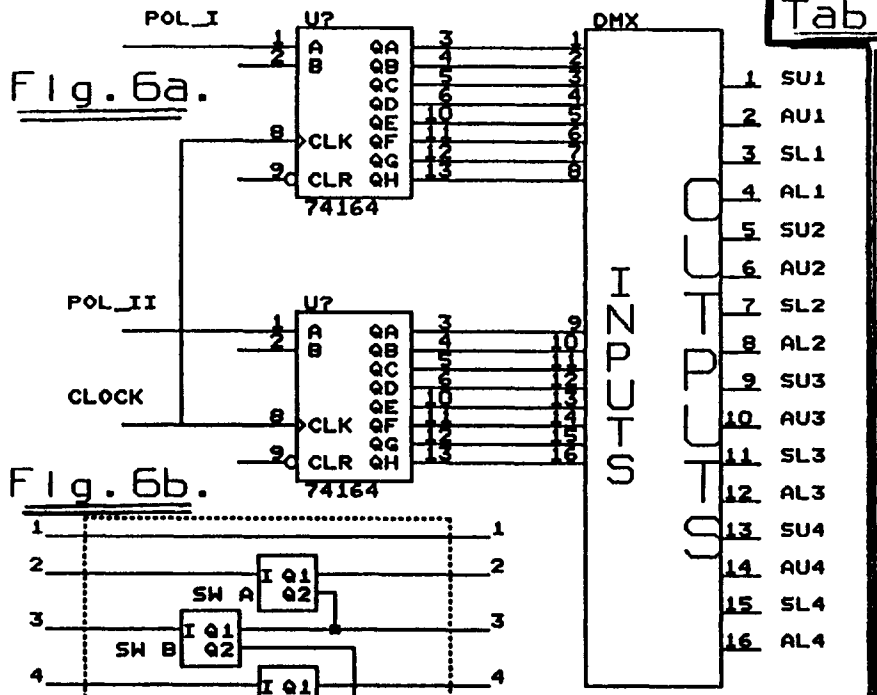


Fig.6a.

Fig.6b.

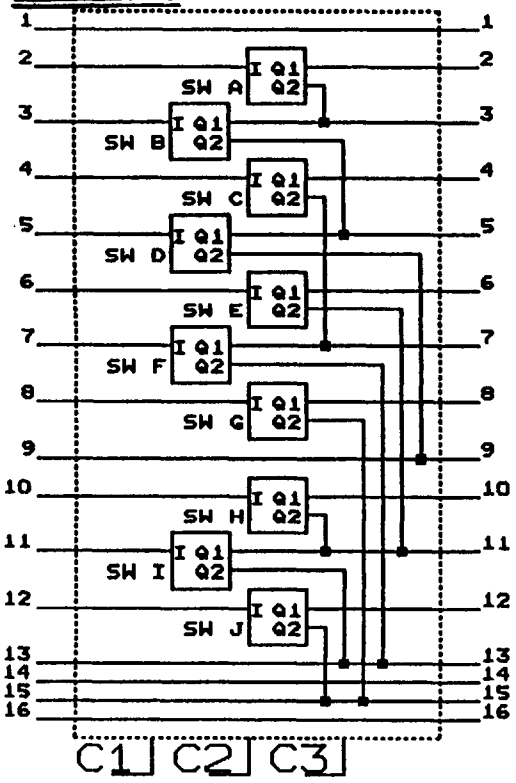
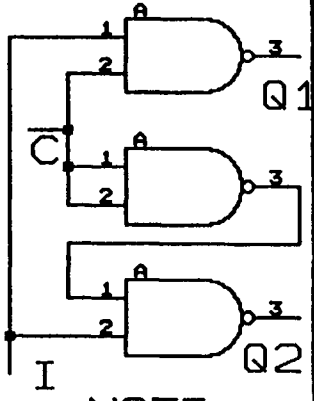


Fig.6c.



NOTE:

C1 controls SW A-C

C2 controls SW D-J

C3 controls SW H-J

Tabl.2. Demultiplexor In-Out Table

# Enable Outputs / Mode / In number	16	8		4		2
	IV-X-2	II-X-2	IY-X-1	I-X-2	II-X-1	I-X-1
1	1	1	1	1	1	1
2	2	2	2	2	3	3
3	3	3	3	3	5	
4	4	4	4	4	7	
5	5	5	5			
6	6	6	6			
7	7	7	7			
8	8	8	8			
9	9	9	9	9	9	9
10	10	10	10	10	11	11
11	11	11	11	11	13	
12	12	12	12	12	15	
13	13	13	13			
14	14	14	14			
15	15	15	15			
16	16	16	16			

Tabl.3.

Mode	C1	C2	C3
X-X-2	1	1	1
X-X-1	0	1	0

Space Research Institute
Academy of Sciences of the USSR
Fast Processing Laboratory: A.Novikov

Title: RADIOASTRON Satellite DECODER

Size: A | Document Number: SYNCHROGENERATOR-1 | REV:

Date: October 24, 1990 | Sheet 1 of 1

dmx.sch

F6;T2,3

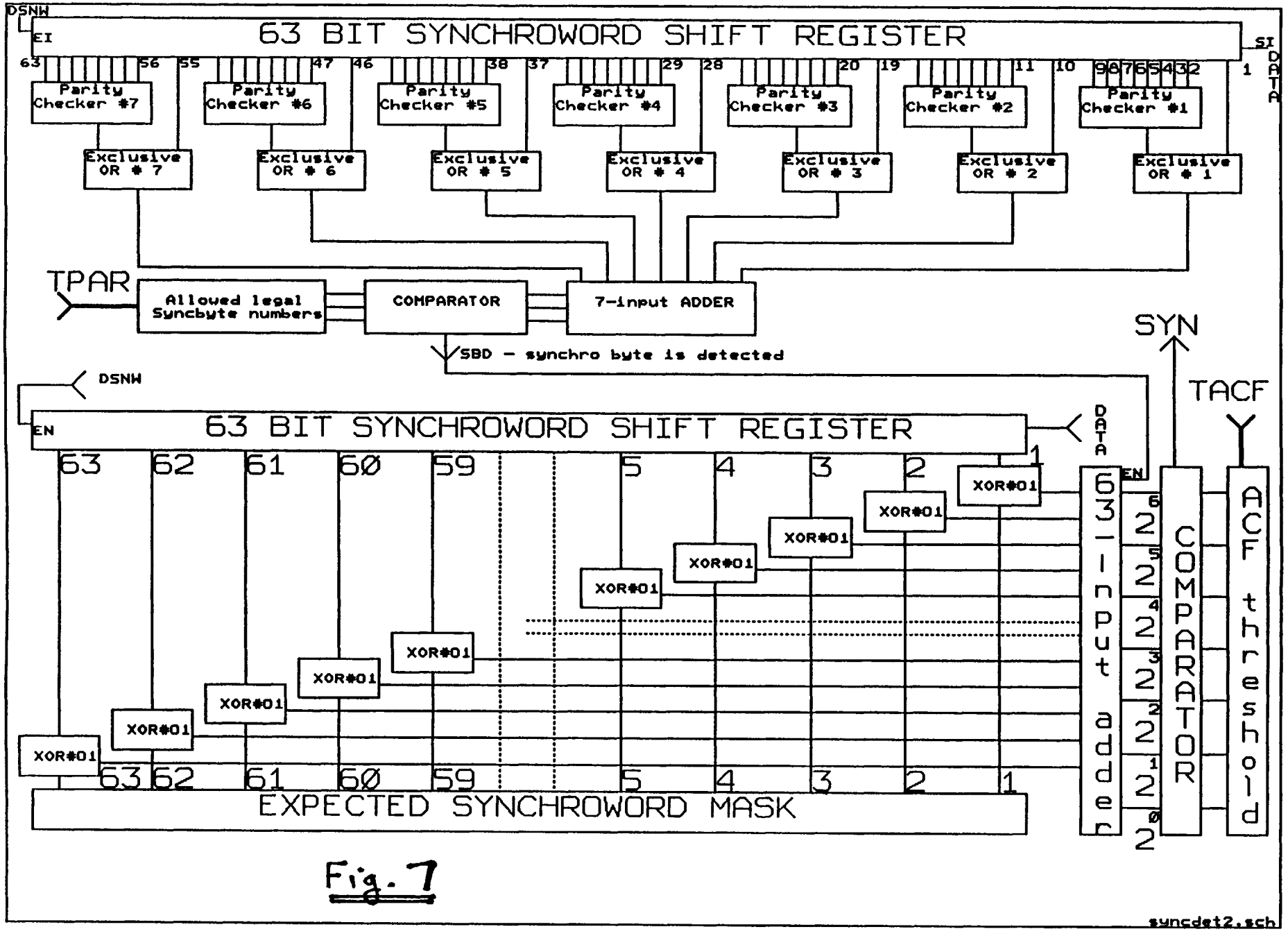
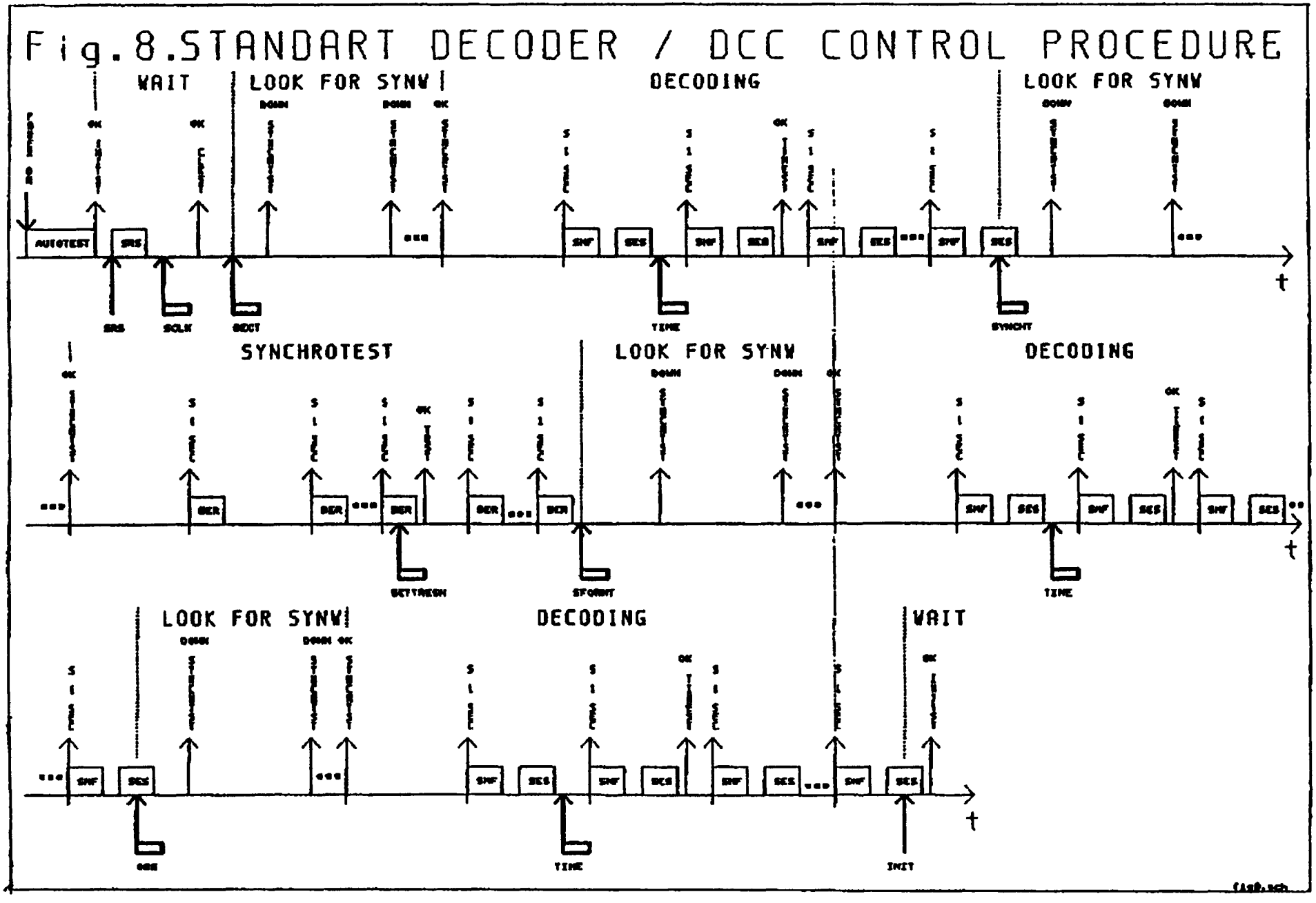

DSNW
63 BIT SYNCHROWORD SHIFT REGISTER
EI
SI
DATA
63
56
55
47
46
38
37
29
28
20
19
11
10
9 8 7 6 5 4 3 2
1
Parity Checker #7
Parity Checker #6
Parity Checker #5
Parity Checker #4
Parity Checker #3
Parity Checker #2
Parity Checker #1
Exclusive OR # 7
Exclusive OR # 6
Exclusive OR # 5
Exclusive OR # 4
Exclusive OR # 3
Exclusive OR # 2
Exclusive OR # 1
TPAR
Allowed legal Syncbyte numbers
COMPARATOR
7-input ADDER
SBD - synchro byte is detected
SYN
DSNW
TACF
EN
63 BIT SYNCHROWORD SHIFT REGISTER
DATA
63 62 61 60 59 5 4 3 2 1
XOR#01
63-input adder
EN
2^6
2^5
2^4
2^3
2^2
2^1
2^0
COMPARATOR
ACF threshold
63 62 61 60 59 5 4 3 2 1
EXPECTED SYNCHROWORD MASK
syncdet2.sch

Fig. 7

F7

Fig.8.STANDART DECODER / DCC CONTROL PROCEDURE



F8

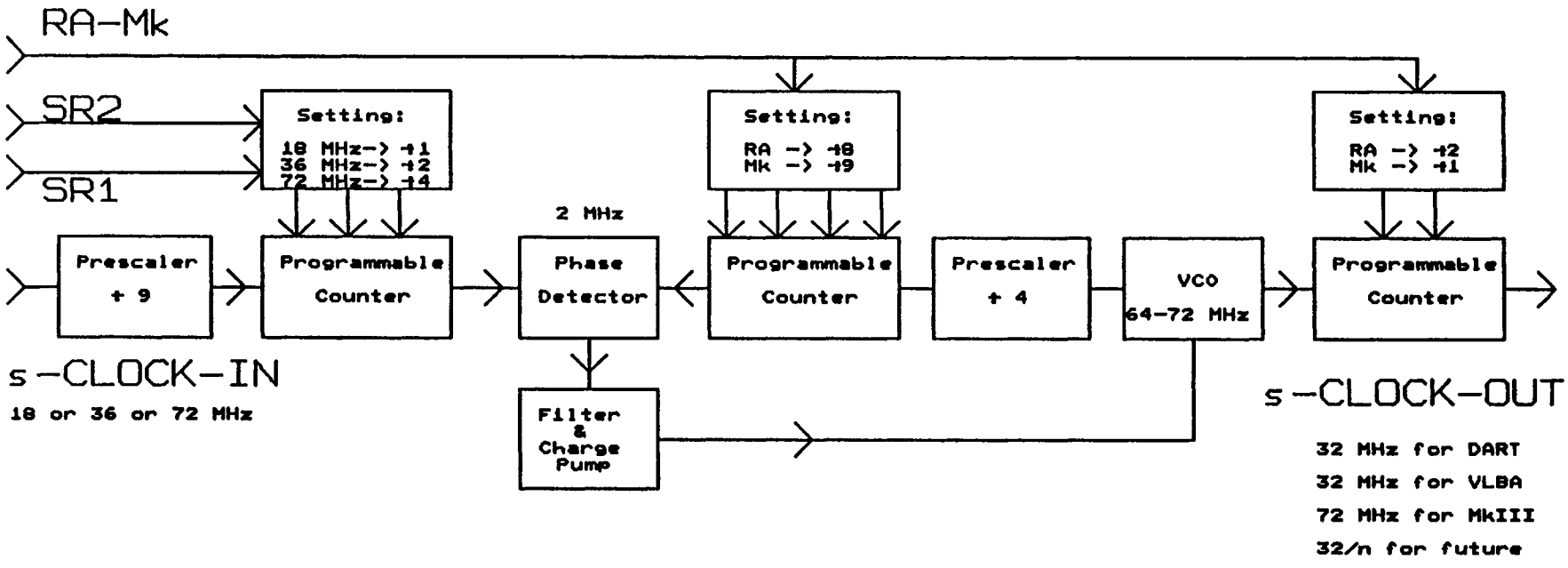


Fig. 10. DECODER s-DIVIDER

Astro Space Centre Academy of Sciences of the USSR Fast Processing Laboratory: A.Novikov		
Title: RADIOASTRON DECODER		
Size: A	Document Number: FILE: S-DIV.SCH	REV
Date: October 24, 1990	Sheet 1 of 3	

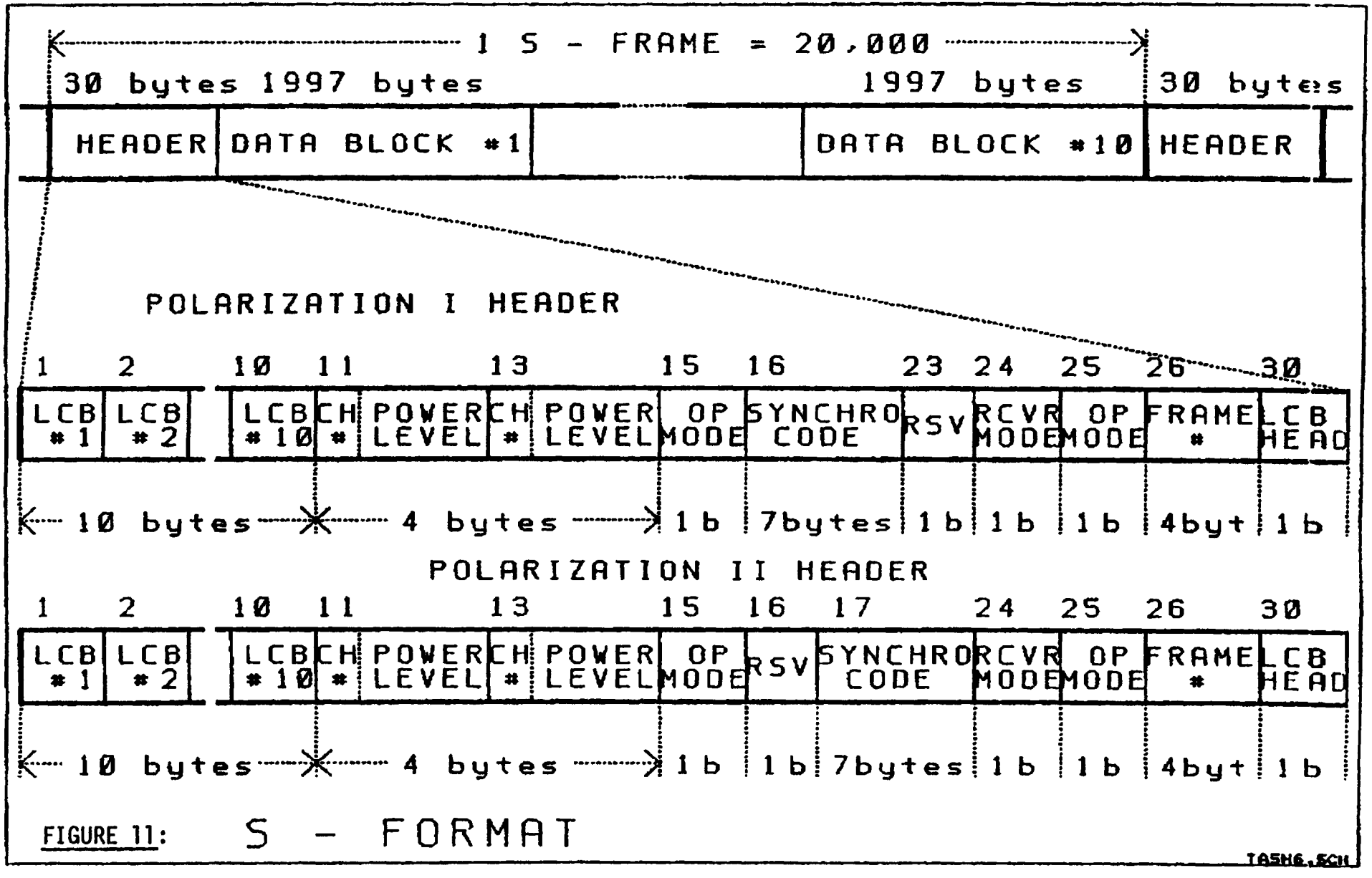


FIGURE 11: S - FORMAT

IA5H6.SCH

OUT CH #	POW CH #
1US 1UA	1
1LS 1LA	2
2US 2UA	3
2LS 2LA	4
3US 3UA	5
3LS 3LA	6
4US 4UA	7
4LS 4LA	8
PI	9
PII	10

4 BITS	12 BITS
CHANNEL NUMBER	POWER LEVEL

Fig.12a. POWER LEVEL CHANNEL NUMBER AND ASTRO DATA CHANNEL IDENTIFICATION

EVEN FRAME

11	12	13	14
Nchan	Power ON	Nchan	Att LDBN
4 bits	12 bits	4 bits	12 bits

ODD FRAME

11	12	13	14
Nchan	Power OFF	Nchan	Att LDBN
4 bits	12 bits	4 bits	12 bits

Fig.12b. Power level format coding.

FIG12.SCH

Fig.13a LONGITUDE CONTROL SUM CALCULATION ALGORITM FOR THREE BYTES.

	P	8	7	6	5	4	3	2	1	P	8	7	6	5	4	3	2	1	P	8	7	6	5	4	3	2	1
1	0	0	1	0	0	1	1	1	1	1	0	1	0	1	1	1	0	0	0	1	0	1	0	1	1	1	0
	BYTE 3									BYTE 2									BYTE 1								

	0	0	1	0	0	1	1	1	1	BYTE 3
+	1	0	1	0	1	1	1	0	0	BYTE 2
+	0	1	0	1	0	1	1	1	0	BYTE 1
	1	1	0	1	1	1	1	0	1	LCB

Fig.13b.SYNCHROWORD

POLARIZATIONI

BYTE 16	111011001	BYTE 17	
BYTE 17	101010111	BYTE 18	
BYTE 18	111000001	BYTE 19	
BYTE 19	000011000	BYTE 20	
BYTE 20	101001111	BYTE 21	
BYTE 21	010001110	BYTE 22	
BYTE 22	010010110	BYTE 23	

POLARIZATIONII

F13

DECODER & DART PROTOCOL
Message Format

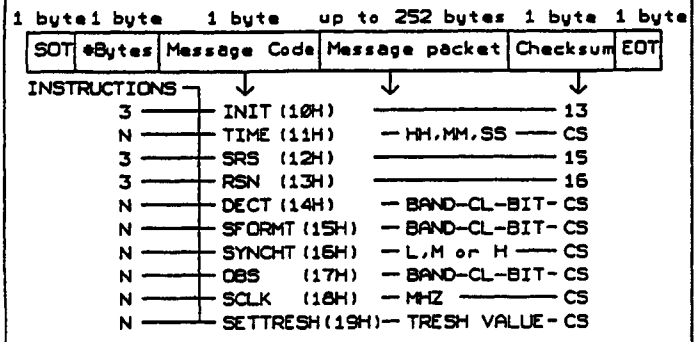


Figure 14a.
Instruction Message Format

DECODER & DART PROTOCOL

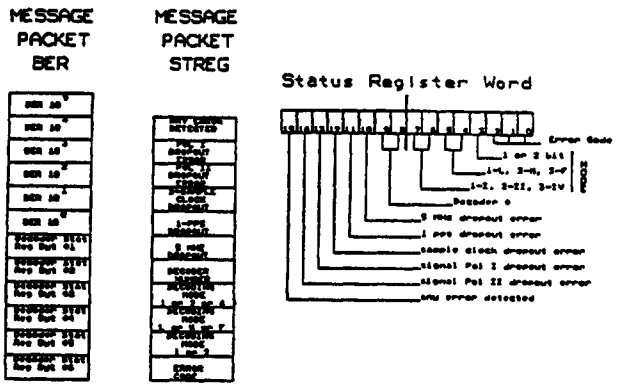


Figure 14c
Satellite Information Message

DECODER & DART PROTOCOL
Message Format

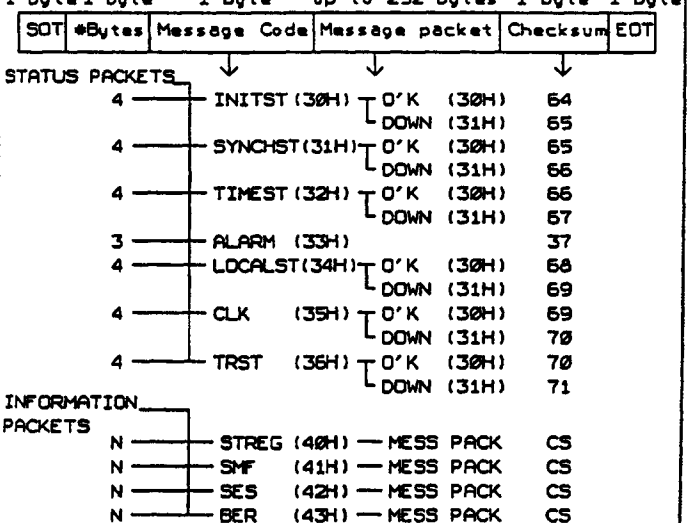


Figure 14b
Status & Information Packet
Message Format

DECODER & DART PROTOCOL

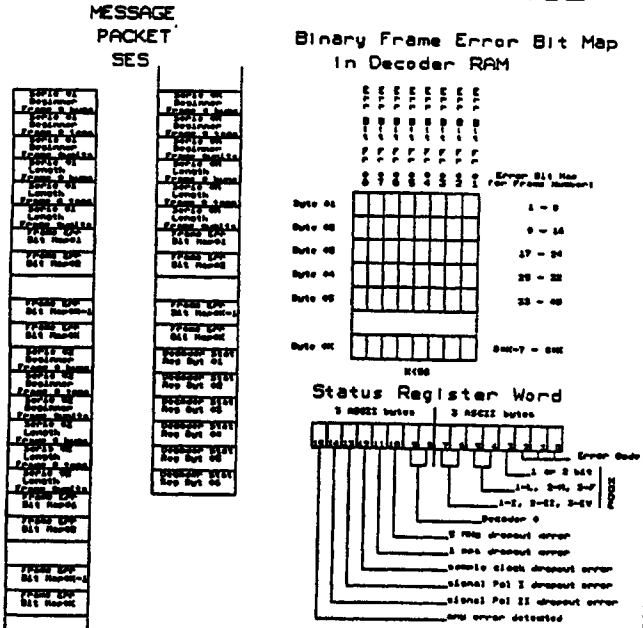


Figure 14d
Satellite Error Message

DECODER & DART PROTOCOL

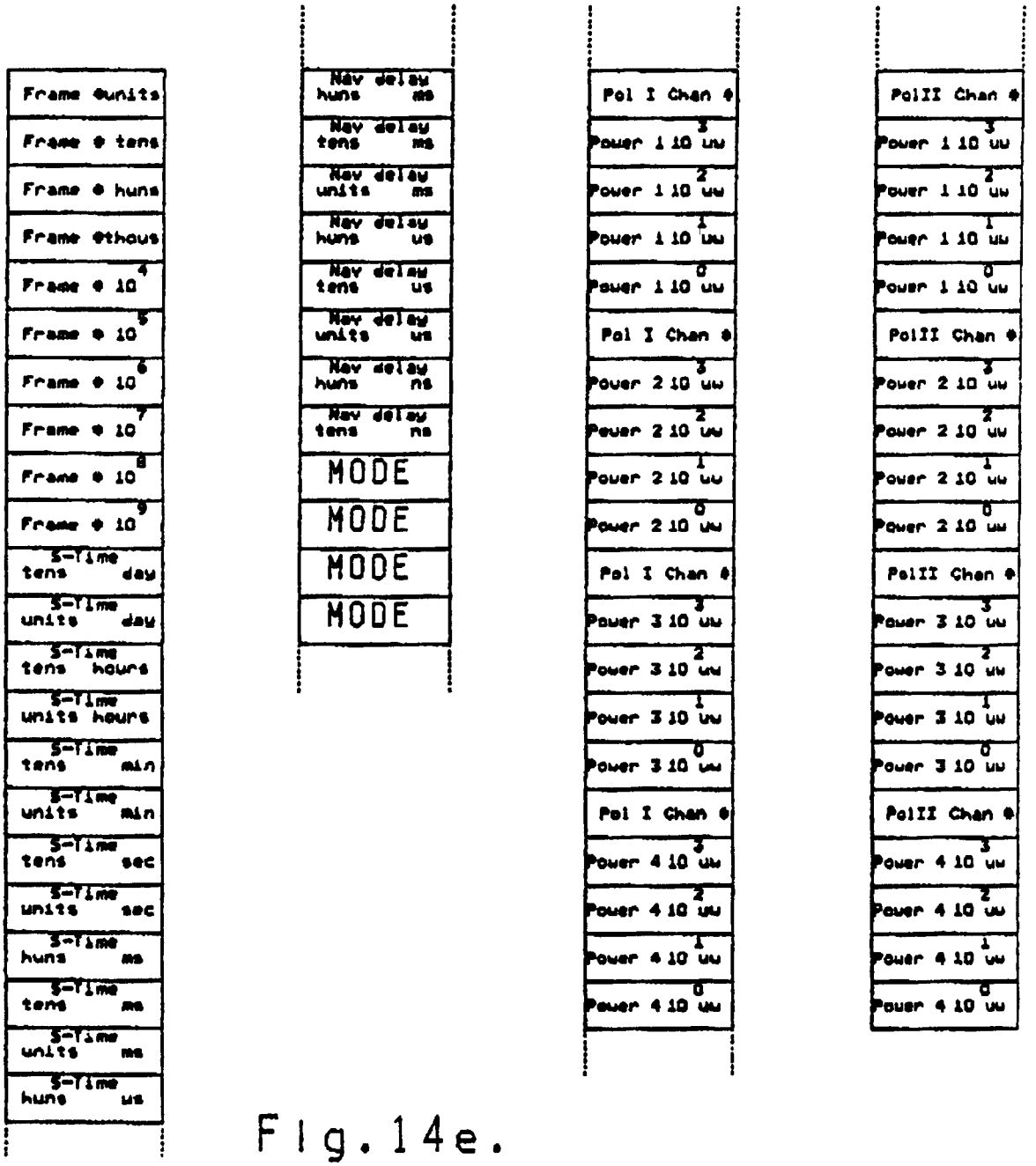


Fig. 14e.

Satellite Message to Formatter

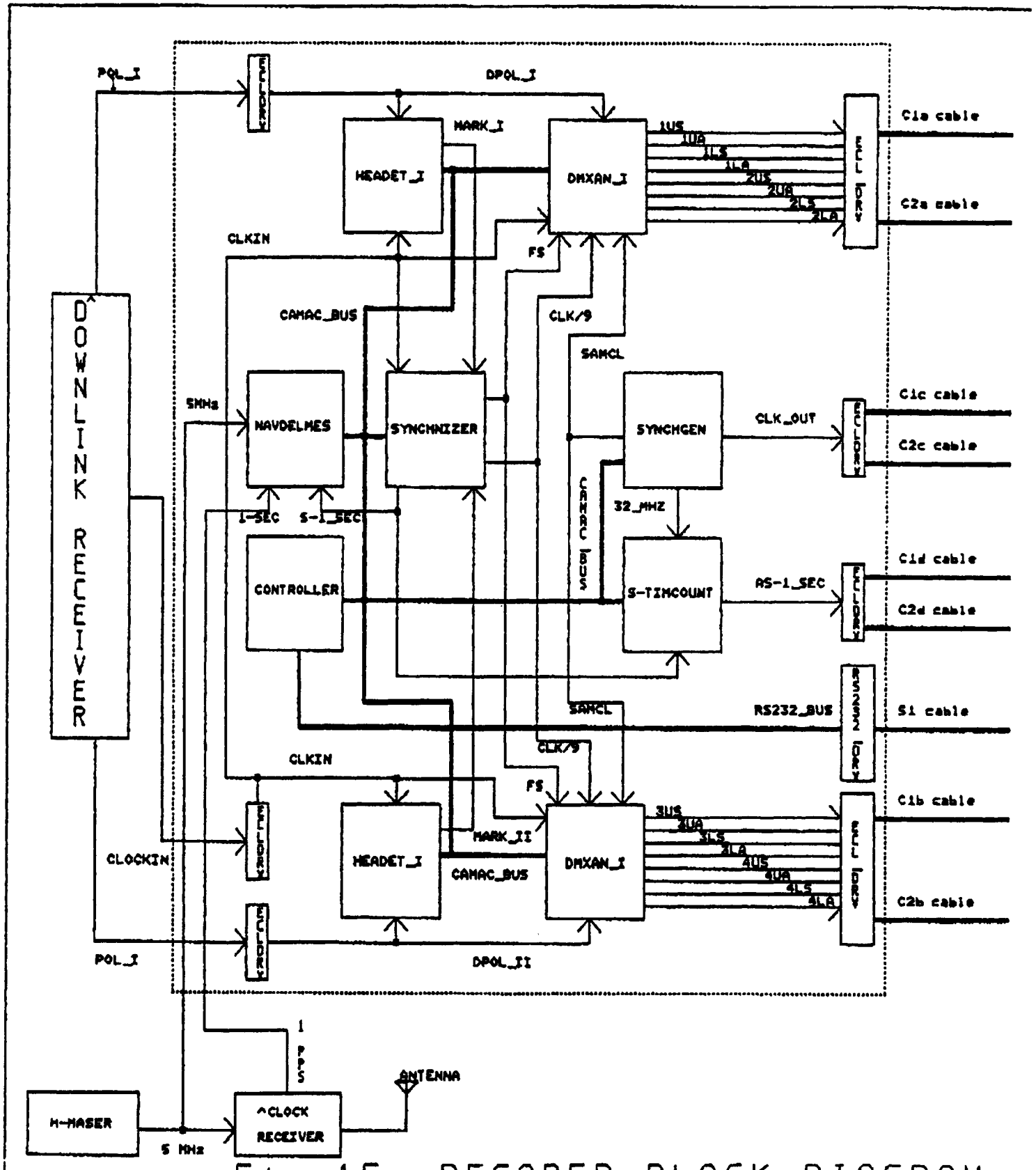


Fig.15. DECODER BLOCK DIAGRAM

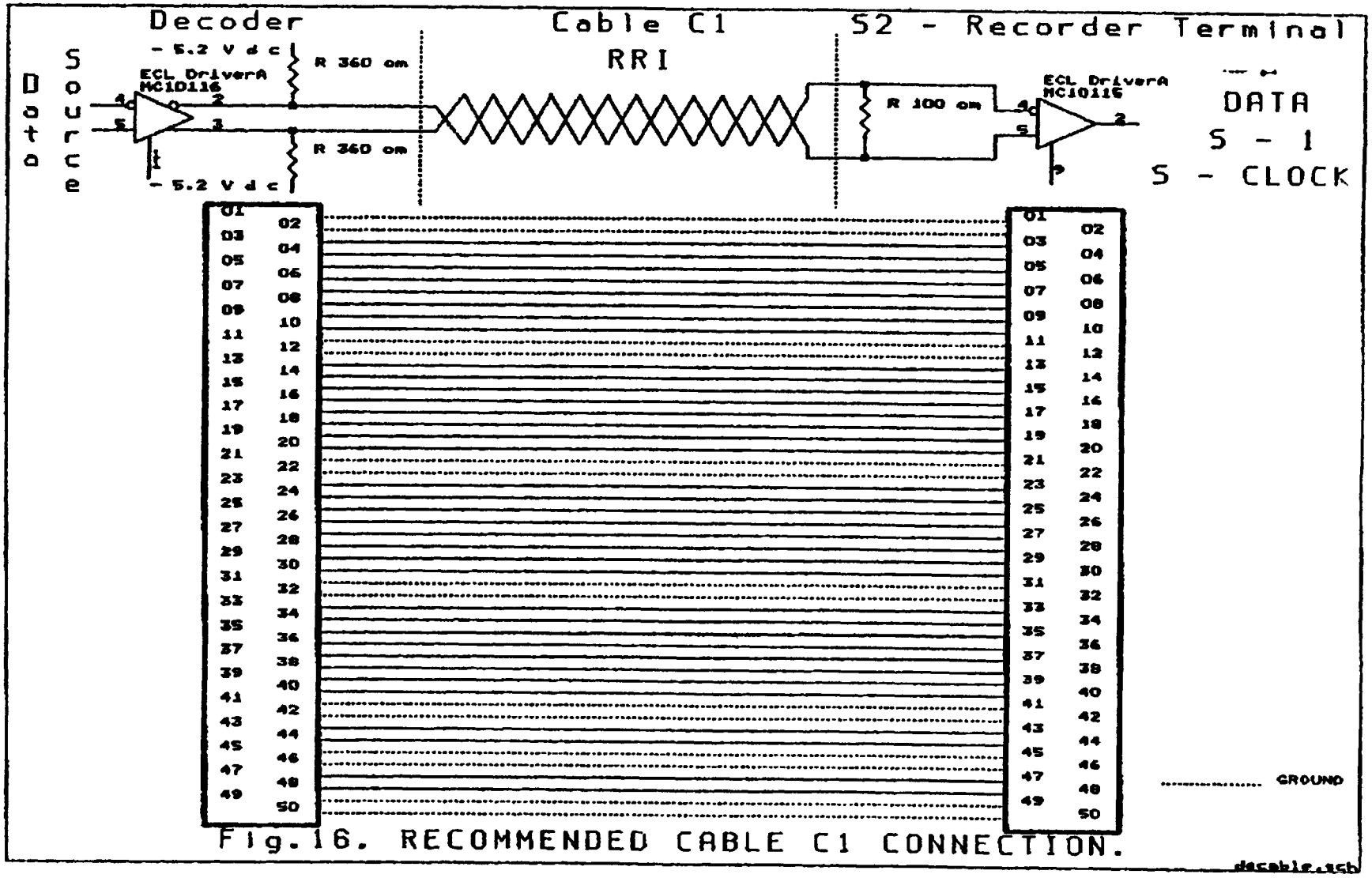


Fig.16. RECOMMENDED CABLE C1 CONNECTION.