11-17-98

Subject: update
Date: Tue, 17 Nov 1998 16:51:28 -0500 (EST)
From: "Arthur W. Lichtenberger" <awl1l@unix.mail.virginia.edu>
To: Tony Kerr <AKerr@NRAO.EDU>
CC: art lichtenberger <awl1l@virginia.edu>

Dear Tony:

Here is a short progress report to date for our SIS work. ...I wrote this on a unix machine ..which is a pain to get to Netscape etc... I will email the figs from Netscape under separate cover.

Present work continues to be primarily focused on two objectives:

(1) fix the trend of increasingly softer I-V curves we have been seeing, and (2) improve our technology for smaller junctions so that we can extend our work for NRAO to ~700 GHz.

  (1) We believe that the reason behind the increased subgap current and rounded I-Vs for our junctions is due to both a deterioration of our trilayer sputter guns from magnet damage and to contamination of the chamber from the silver paste of the guns. These problems occurred when the "house" (closed cycle) water was switched temporarily to another source which, unfortunately, had a very low resistivity. Some of the gun current arced from the target through the backing plate, magnets and water to ground. When all of the guns were inspected it was found that the conductive silver paste had been heated so much that it had mostly vaporized into the chamber. Parts of the guns had fused together from the heat and the magnets were also physically damaged.

  We cleaned/wiped all chamber and fixture surfaces with freon/meth, fixed the guns/replaced parts and targets ($9K), and purchased a dedicated floor standing water chiller to run the guns. Initial fabrication of junctions, both with a new etching process described below for (2) and our conventional process, yielded very poor (point contacts) electrical characteristics. Subsequent anodization profile tests indicated that the Al films were too thin (in situ trilayer thickness monitor crystal was out of calibration). A subsequent trilayer run with thicker Al films did give SIS characteristics but they were rather leaky. Five subsequent runs have given improved characteristics, yet the quality is still rather fair. We have just processed test devices using our old "NRAO-3" anodization process (a very reliable process, but not suited for the more recent NRAO mask designs) and have obtained the same quality I-V's. This supports our belief that the problem is still in the trilayer. We are presently taking the trilayer machine down again and completely removing/cleaning all internal fixturing, cleaning out the cryopump (replacing the charcoal beds) and loadlock pump, replacing all the gas lines etc. This is a big undertaking (for example- the deposition shield and substrate fixturing is composed of numerous parts/small-bolts which must be taken apart and reassembled in the chamber).

  We will hopefully have it reassembled by the end of the week.

  (2) Improving our technology for smaller junctions has involved finding and alternative RIE process for the junction step. Since the NRAO mixer geometry will not permit the use of

a junction anodization (our NRAO-3 process) we have had to resort to a Au overlayer process where a 'button' of Au is left on top of the junction electrode. This additional Au layer results in an electro-chemical effect in the RIE such that the junction Nb is no longer etched anisotropically in our SF6 based RIE process. This detrimental effect is also more pronounced for smaller junction sizes making it increasingly difficult to insulate the junction. The alternative process we have developed (see figures) uses a different RIE chemistry and as can be see uses a very anisotropic etch for the Nb junction. We anticipate using this etch for all of our process in the future. This should permit us to obtain the smaller area junctions needed for the higher frequencies. It should also result in better control/uniformity of the junction area (resistance) since the etch more accurately follows the mask.

Figure Explanation:

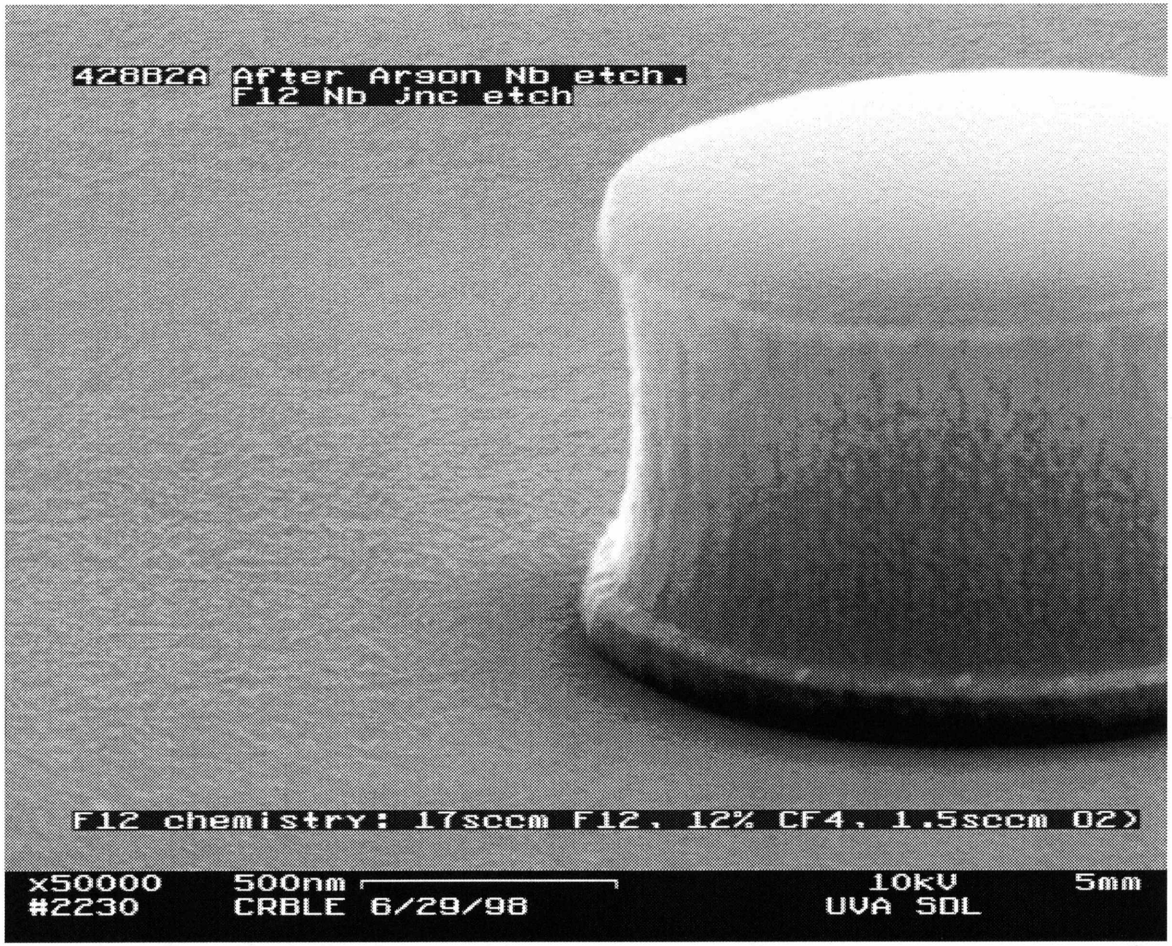
428B(2A) Here we have used our trilevel resist, Ar RIE the overlayer Au, new Nb etched the junction. Nb etch follows the Au mask (which followed the upper trielvel resist feature) anisotropically (no undercutting of the Nb junction wrt the Au)

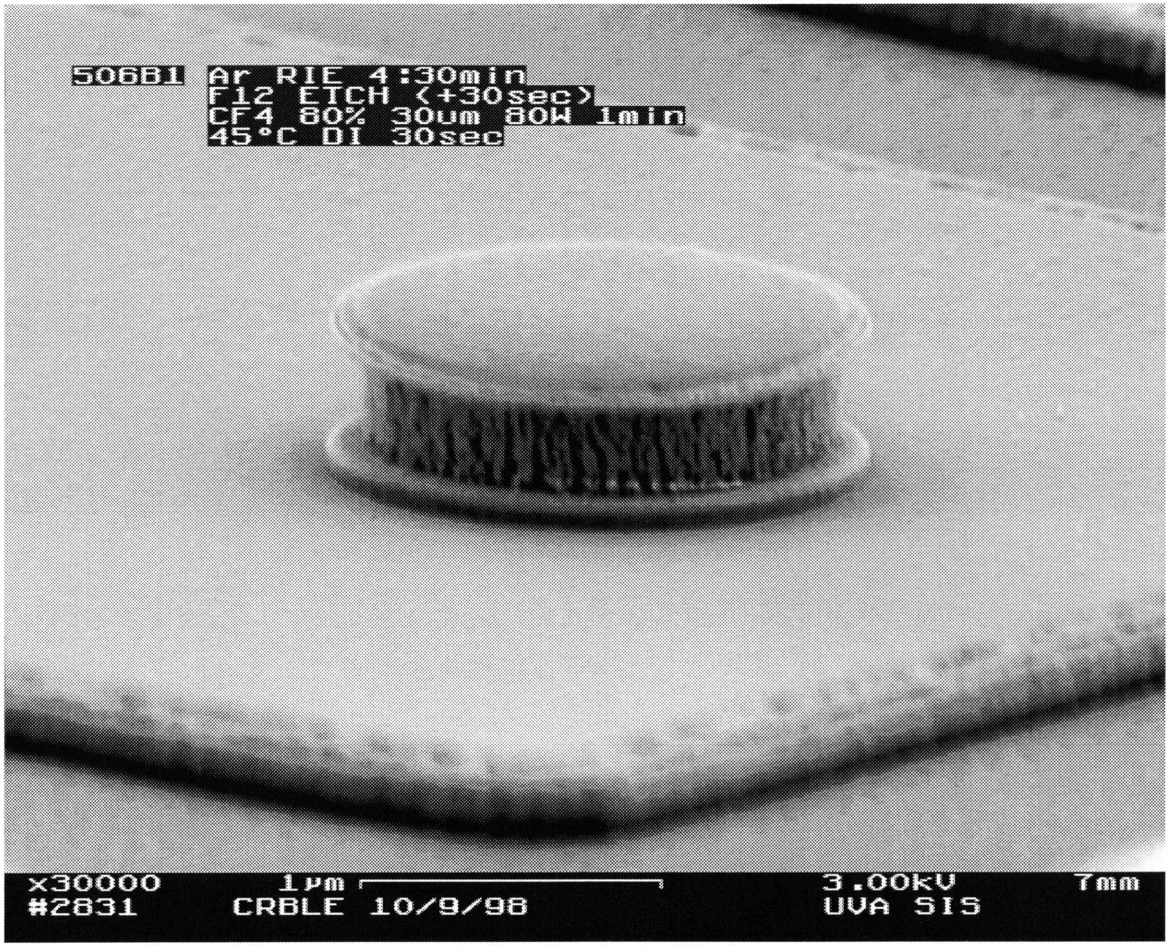
506B Here we again have used the trilevel resist but we have shrunk the polyimide after the Au etch. The new Nb etch follows the previous Au definition such that the Nb junction perimeter is "ready" for a good insulation coverage.

529A Here we have deposited 200nm of SiO insulation and performed liftoff for a nominal 1um size junction. The small junction looks well insulated, the Au surface looks clean.

ps I have also included a view of one of Aaron Datesman's recent HEB devices to show you the smallest thing we have done in the SDL to date.

- Art


428B2A
After Argon Nb etch,
F12 Nb jnc etch
F12 chemistry: 17sccm F12, 12% CF4, 1.5sccm O2)
x50000
500nm
10kV
5mm
#2230
CRBLE 6/29/98
UVA SDL


506B1
Ar RIE 4:30min
F12 ETCH (+30sec)
CF4 80% 30um 80W 1min
45°C DI 30sec
x30000
1µm
3.00kV
7mm
#2831
CRBLE 10/9/98
UVA SIS


529A AFTER SiO LIFT OFF
Tgal 30+20min
120°C NMP+P.GLYCOL(3:1) 60min
REAL JUNCTION
1.03 μm
GAL
x30000
1μm
3.00kV
8mm
#3018
JZZ 11/10/98
UVA SDL/SIS


DEV #3 AFTER 22.5 MIN RIE
65 DEG VIEW
x100000 200nm
10kV 12mm
#3061 469C TOP 11/17
UVA SDL/SIS