11-19-98

Development of SIS Mixers for MMA Receivers

a proposal to NRAO

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1 Introduction

This proposal is for the support of work at Stony Brook in a collaborative effort with NRAO to develop and fabricate SIS mixer chips for the millimeter wave array telescope (MMA). In this collaboration NRAO will have the primary responsibility for the mixer design and testing, while Stony Brook will have the responsibility for the fabrication of mixer chips along with the development of any needed refinement to existing niobium trilayer fabrication technology. The groups will work together to develop design and technology modifications required to optimize the mixer performance.

During the first two years, covered by this proposal, work will focus on the 200-300 GHz and 600–720 GHz bands. By the end of this period our goal is to demonstrate mixer designs and fabrication technology adequate for the production of about 100 SIS mixers in each of these bands. In addition, we hope to have an adequate characterization of the process parameters and reproducibility to define the final frequency bands for the MMA receivers. If successful, it is envisioned that this work would then be extended and expanded to include the fabrication of the roughly 1000 SIS Nb mixer chips required for the MMA.

2 Present status of the Stony Brook process

Stony Brook presently has a fabrication laboratory for niobium trilayer circuits that has unique capabilities for the fabrication of high quality, high uniformity niobium trilayer junctions with very small dimensions i.e., areas down to 0.01 μm^2. The fabrication technology is based on the PARTS process developed at IBM in which the entire wafer is coated with quartz and planarized after junction definition to expose the counter electrode. This process makes it possible to contact extremely small junctions in addition to providing excellent junction isolation without the need for additional steps, e.g. anodization. The resulting junctions have areas very close to the design values down to the $0.01\,\mu m^2$ dimension quoted above. Junctions having critical current densities in the range of $J_c = 100\,A/cm^2 \longrightarrow 200\,kA/cm^2$ are routinely fabricated using this technology. Our present process can use either photolithographic patterning or electron beam lithography (EBL), or a combination of the two, in any layer over a 2" Si wafer. This gives the advantages of the fast throughput of photo-lithography combined with the deep submicron resolution and excellent dimensional control of EBL where required. To our knowledge, ours is the only laboratory in the world having this range of capabilities for the fabrication of niobium trilayer Josephson junctions.

Our present process is detailed in Appendix A, which give the design rules, process parameters and process flow charts. In addition, data are presented (Fig.1) showing a typical I – V characteristic of junctions similar to those which would be fabricated as part of this project, having a $J_c = 6\,kA/cm^2$ and an area of $1\,\mu m^2$. Figure 2, shows

data for the scatter in critical current of similar junctions, both on a chip and from chip to chip across the wafer.

2.1 Facilities of fabrication laboratory

MAJOR EQUIPMENT: The major items of equipment available in the laboratories for this project are:

1. A circuit fabrication laboratory focused on the fabrication of superconducting circuits using niobium trilayer technology. A complete eight level process has been developed on 2" wafers using combined electron beam lithography (EBL) and DUV photo-lithography. This process is presently being used for the fabrication of array oscillators, SQUID magnetometers and digital RSFQ circuits. The major equipment in this fabrication laboratory are:

    - 2 EBL systems for writing patterns with dimensions down to 30 nm on 2" wafers. One system has a laser stage to permit field stitching and software and hardware to permit registration of multilayer circuits. The second system, based on a Leo field emission SEM, is capable (with some addition equipment) of automatic registration to permit rapidly registering multiple patterns over the 2" wafer.
    - DUV contact mask aligner which can print features down to 500 nm on 3" wafers.
    - 400 sq. ft class 100 clean room space with precise temperature and humidity control (below 40%) for resist processing.
    - 1000 sq. ft of class 1000 clean room space for other deposition systems.
    - Strasbaugh polisher for use in dielectric planarization as part of the PARTS process.
    - RIE system with optical end point detector.
    - 4 hearth E-gun deposition system.
    - UHV deposition system.
    - Two niobium trilayer deposition systems with oil free pumping systems (cry- and turbo-), one with a load lock.
    - Sputtering system for quartz dielectric deposition.
    - Three diffusion pumped thermal evaporators.
    - Misc. equipment such as profiler, ellipsometer, dicing saw, Leitz optical microscopes, DI water system (20 MΩ), plasma asher, clean benches, lead bonder, etc.

2. A large collection of cryostats and test equipment exists in the lab:

   - SHE dilution refrigerator, 7 mK base temperature. This system is fully shielded against EM radiation and is vibration isolated. Further, it has magnetic shielding to reduce the ambient field on the sample to 10^{-5} G.
   - ^{3}He cryostat (MRC) with over two day hold time below 0.3 K.
   - Multiple pumped ^{4}He cryostats as well a dip probes suitable for testing chips.
   - An extensive set of microwave test equipment.

3 Statement of work

During each year of this two year project, we will supply to NRAO quartz wafers for testing from 3 different mask designs. During the first year, when process development will be more of an issue, we will supply 1 wafer of each design. During the second year, as we focus on establishing high yield, 2 wafers of each design will be supplied to NRAO. Chips from these wafers will first be tested at Stony Brook to ensure conformity with process goals discussed below.

3.1 Process goals

The initial work will utilize trilayers with a critical current density J_c of about 6 kA/cm^2 and a junction area of about 1.5 μm^2, for which high quality junctions are routinely obtained on Si substrates. For these wafers, the process goals are:

- Junction area: ± 10 % of specification.
- J_c : $\pm 10\%$ of specification.
- Subgap resistance R_{sg} (measured at 2 mV): $> 20R_n$, where R_n is the resistance measured at 4 mV.
- Conductor widths: ± 0.5 μm of design values.
- Resistors: $\pm 10\%$ of design values.
- Resonant frequency of 1/4 wave stubs: $\pm 5\%$ of design value. To accomplish this it is important to control
  - Oxide dielectric constant: $\pm 5\%$ of standard value.
  - Oxide thickness: $\pm 10\%$ of design value.
  - London penetration depth: $\pm 10\%$ of standard value.

In the initial stages of the work, the masks will incorporate designs with a range of parameters (e.g. 1/4 wave stub length) to accommodate process variations. Once process scatter for key parameter is determined, we will work to reduce it so that design variations can be reduced or eliminated in order to increase the yield of useful mixer chips on each wafer.

3.2 Testing

In addition to standard process test chips which Stony Brook will add to the mask sets, chips from the wafers to be sent to NRAO will be first tested at Stony Brook to determine junction quality, uniformity, and J_c and resonator frequency. It may also be useful to measure the low frequency junction noise, if this correlates well with mixer performance.

3.3 Process development

During this project, we see four areas in which process development is required.

1. Optimization of our process for the production of high quality junctions on quartz substrates.

2. Development of high quality, i.e. low leakage, trilayers with high J_c to permit the use of submicron junctions for the higher frequency bands.

3. Characterization of, and improvements in, the uniformity of process parameters over the 2" wafer, so that a high yield can be obtained when the work enters the production phase.

4. An additional quartz layer will be added to the process to permit two dielectric thicknesses between the base electrodes and the wiring layer on each wafer.

3.4 Details

3.4.1 Masks

Stony Brook will purchase the photolithographic mask sets required for this work. AutoCad files, with the mixer designs will be supplied by NRAO. Stony Brook will then make needed modifications (e.g. the addition of EBL registration marks) and add the designs for the process test sites before submitting the final mask design to the supplier.

3.4.2 Substrates

The chips will be fabricated on 2" quartz wafers. It will be Stony Brook's responsibility to obtain the wafers required for this work. The initial work will be done on 10 mil fused quartz, Dynasil 1000 or 4000 or the equivalent. Other types and/or thicknesses of quartz which are compatible with mixer operation may be tested to optimize the processing.

3.4.3 Publication

Since this is a collaborative project, it is expected that publications resulting from this work will include authors involved in the design, fabrication and testing aspects of the work.

3.4.4 Deliverables

The main deliverables under this contract will be the nine wafers for NRAO described above. We will make out best effort to ensure compliance with the initial parameter specifications listed in Sec. 3.2 or refined specification that may be jointly developed by NRAO and Stony Brook during the project. Additional deliverables may include reports on process parameters as required to develop mixer designs. In addition, quarterly reports will be provided to NRAO summarizing each quarter's work.

4 Budget

Item	Year 1	Year 2	Cumulative
Dr. Sergey Tolpygo, 25% time	$17,000	$18,000	$35,500
Dr. Wei Chen, 25% time	14,000	15,000	29,000
Technical staff, 50% time	17,000	18,000	35,000
Prof. James Lukens, 25% time: summer	6,900	6,900	13,800
Grad. Res. Assist.	18,000	19,500	37,500
Total salaries	**72,900**	**77,400**	**150,300**
Fringe benefits	15,839	17,442	33,281
Sample fabrication, 800 hrs @ $50/hr	40,000	40,000	80,000
Supplies	7,000	7,000	14,000
Travel	2,000	2,000	4,000
Publication charges	1,000	1,000	2,000
Equipment	80,000	80,000	160,000
Total direct cost	**218,739**	**224,841**	**443,581**
Indirect costs: 47.5% of MTDC	65,901	68,800	134,701
Total	**$284,640**	**293,641**	**578,281**

Our budget: 125 + 250 + 62.5 + ~~15~~ + ~~30~~

~~$521,000~~ $482,500

160 − 96 = 64K

requires extra ~~$160K~~ ~ $96K

4.1 Justification.

- Fringe benefit rates:

Rate	year 1	year 2
Regular Benefits	29.25%	29.75%
Grad. Student Benefits	3%	5%
Summer Salary	18.25%	18.75%

- Sample fabrication charge is for the proportionate share of lab maintenance and supplies which are not directly attributable to a specific project, e.g. the SEM service contract.

- Supplies:

quartz substrates, 50 @ \$70	\$3,500
machine and electronics shop time 200 hrs. @ \$20/hr	4,000
liquid helium, 1000 l @ \$2/l	2,000
misc. vacuum and electronic components	4,500

- Travel will be for trips to Virginia to confer on SIS mixer fabrication as well a one trip per year to an appropriate conference to report on the results of this work.

- Equipment items, required for mixer fabrication and testing, will be taken for the list below depending on needs to be prioritized as the project progresses. Where appropriate, costs will be shared with other projects.

auto registration system for Leo SEM	\$27,000
ellipsometer for dielectric measurement	\$32,000
4" magnetron sputter heads, 3@ \$5,000	\$15,000
Photo-lithographic mask sets 6 @ \$10,000	\$60,000
MKS pressure and gas flow regulation system	\$5,000
Leica optical inspection microscope	\$15,000
Wafer probe station	\$10,000
HP network analyzer	\$37,000
turbo pumping system	\$15,000
	\$216,000

4.2 Cost sharing

The university will provide 10% of Prof. Lukens academic year time and 15% of Mr. Arthur Davis' time to this project as cost sharing.

Appendix A
Stony Brook PARTS Process for Niobium Trilayer Circuits

REVISION -- 008

1. Layer Sequence and General Design Information

Layer number	Layer Name	Description	Thickness (Å)	Snap (μm)	Color (ACAD #)	GDSII #
0	Text	Designer's Comments	none	0.25	White (7)	12
1	M3	All Junctions, Nb	1500 ± 150	0.25	Yellow (2)	1
2	M2	Base Electrode, Nb	1500 ± 150	0.25	Red (2)	2
3	I2	Insulator – Quartz User defines holes	1350 ± 150 over M2, 2850 ± 150 over field	0.25	Green (3)	3
4	R1	Resistors, Ti/PdAu	800 ± 75	0.25	Cyan (4)	4
5	M4	Wiring layer, Nb	2000 ± 200	0.25	Blue (5)	5
6	I3	Insulator Quartz User defines holes	3000 ± 300	0.50	Grey (9)	6
7	M5	Ground plane, Nb User defines holes	4500 ± 400	0.50	Light Brown (11)	7
8	AU	Contact pads, Ti/Au	500	0.50	Magenta (6)	8

2. Physical parameters of layers

Junction critical current density	$J_c = 6 \pm 0.6$ kA/cm^2 = 60 ± 6 μA/μm^2
Junction specific capacitance	$C_0 = 60$ fF / μm^2
Minimum junction size	0.5 μm x 0.5 μm
Nominal I_C	60 μA (for 1.0 μm junctions)
Nb penetration depth	
Nb film current density - no steps	30 mA/μm
Nb film current density - over steps	6 mA/μm
Quartz dielectric constant	4.2
R1 sheet resistance (Ti/AuPd)	$R_S = 5 \pm 1$ Ω/sq.,
or using (Ti/Au)	Rs=0.5Ω/sq.
R1-M4 Contact resistance	< 0.1 Ω

2.1 General notes

1. The layer sequence is fixed.

2. Layers M2, M3, I2 and M4 are required to make a Josephson junction. Contact to M2 is made directly via I2.

3. Contact between M2 and M5 is made through I2 and I3. A patch of M4 must be added to improve the quality of contact.

4. Ti is used as an underlayer for Au and PdAu to improve adhesion. Ti is a superconductor with T_C of 0.4 K. For circuit operation in mK range, Ti can be replaced by Cr. Please specify if Cr is needed.

5. Minimize M4-M5 overlap area - specially over long wires.

3. SUNY PARTS Design Rules

3.1 Definitions

Spacing is the minimal distance between two objects in the same or different layers that must not overlap or have electrical contact with each other.

Width is the minimal size of an object. It can be specified for an object in some layer or for a structure built in a different layer. (e.g. R1/M4 contact)

Overlap is the minimal distance between the edges of two objects when one of two must be completely covered by the other.

3.2 Minimum Features and Tolerances

1.0 M3 & M3_OPT & EBL

1.1	Min. Spacing	1.0 μm
1.2	Min. Width	0.5 μm

2.0 M2

2.1	Min. Spacing	1.0 μm (1.0 μm for coils, see note)
2.2	Min. Width	1.0 μm (1.0 μm for coils, see note 1)
2.3	Overlap outside M3	0.25 μm
2.4	Max. Width	200.0 μm

3.0 I2

3.1	Min. Spacing	3.0 μm
3.2	Min. hole size	1.0 μm x 2 μm
3.3	Overlap with M2.....	1.0 μm
3.4	Spacing with M3	1.0 μm

4.0 R1

4.1	Min. Spacing	1.0 μm
4.2	Min. Width	0.25 μm
4.3	Minimum width of contact with M4	1.0 μm
4.4	Spacing with I2	1.0 μm
4.5	Spacing with M3	1.0 μm

5.0 M4

5.1	Min. Spacing	1.0 μm
5.2	Min. Width	0.5 μm
5.3	Overlap with M3	0.5 μm
5.4	Overlap with I2	0.5 μm

6.0 I3

6.1	Min. Width	1.0 μm
6.2	Min. Spacing	1.0 μm
6.3	Overlap with M4	0.5 μm
6.4	Spacing with or overlap outside M2	0.5 μm

7.0 M5

7.1	Min. Spacing	1.0 μm
7.2	Min. Width	1.0 μm
7.3	Overlap outside I3	1.0 μm

8.0 Au

8.1	Min. Spacing	1.0 μm
8.2	Min. Width	1.0 μm
8.3	Overlap outside M5	1.0 μm

3.3 . Junction Shapes

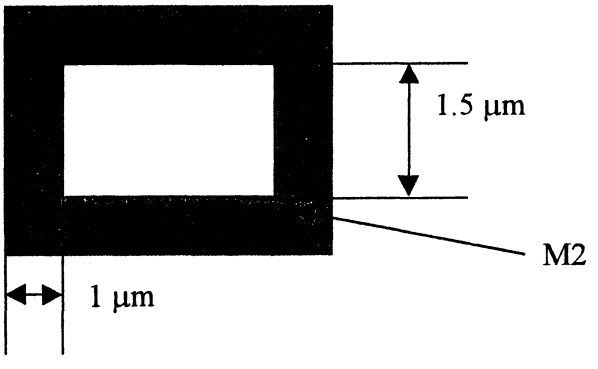
Josephson junctions may have the following shapes:

Square - 0.5 μm x 0.5 μm, I_c = 1 unit

Increment junction size by 0.1 μm

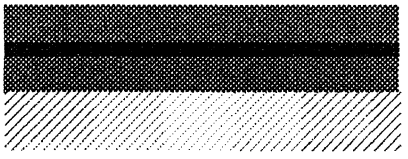
0.6 μm x 0.6 μm, Ic = 1.44
0.7 μm x 0.7 μm, Ic = 1.96
0.8 μm x 0.8 μm, I_c = 2.56
0.9 μm x 0.9 μm, I_c = 3.24
1 μm x 1 μm, I_c = 4

Note:

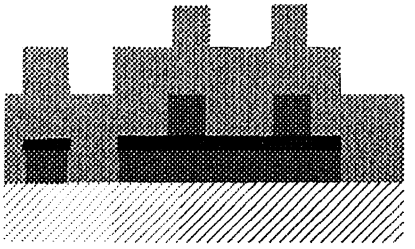


4. Process Flow Chart.

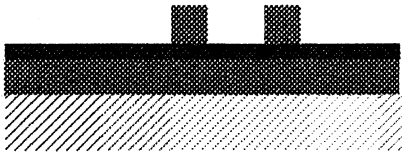
PLANARIZED ALL REFRACTORY TECHNOLOGY
FOR LOW Tc SUPERCONDUCTIVITY (PARTS) PROCESS



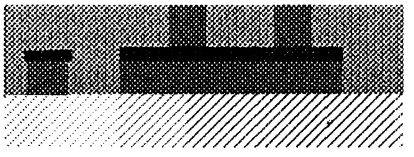
1. Nb/AlOx/Nb trilayer



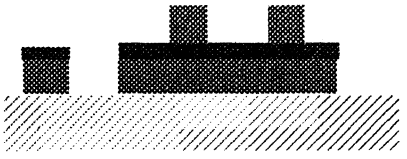
3. SiO2 deposition



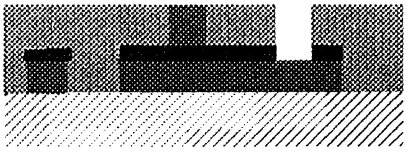
2. Counter electrode definition



4. Planarization



3. Base electrode definition



5. Contact hole definition

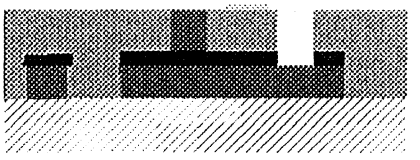
Nb

AlOx

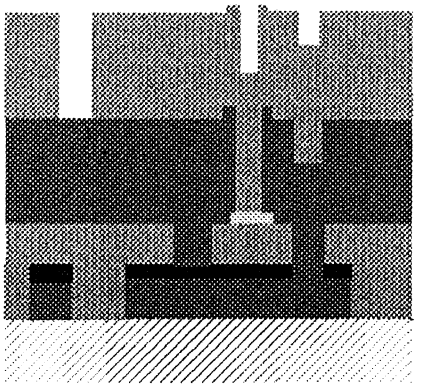
SiO2

Au/AuPd

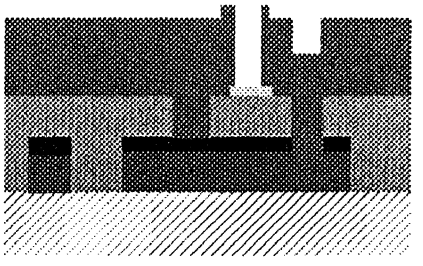
Substrate



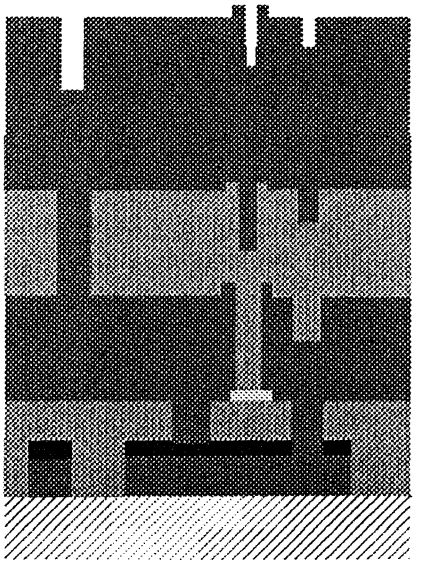
7. Resistor lift-off



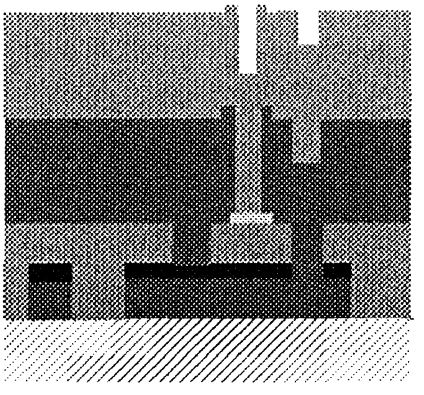
10. Contact hole



8. Wiring layer



11. Ground plane



9. SiO2 deposition

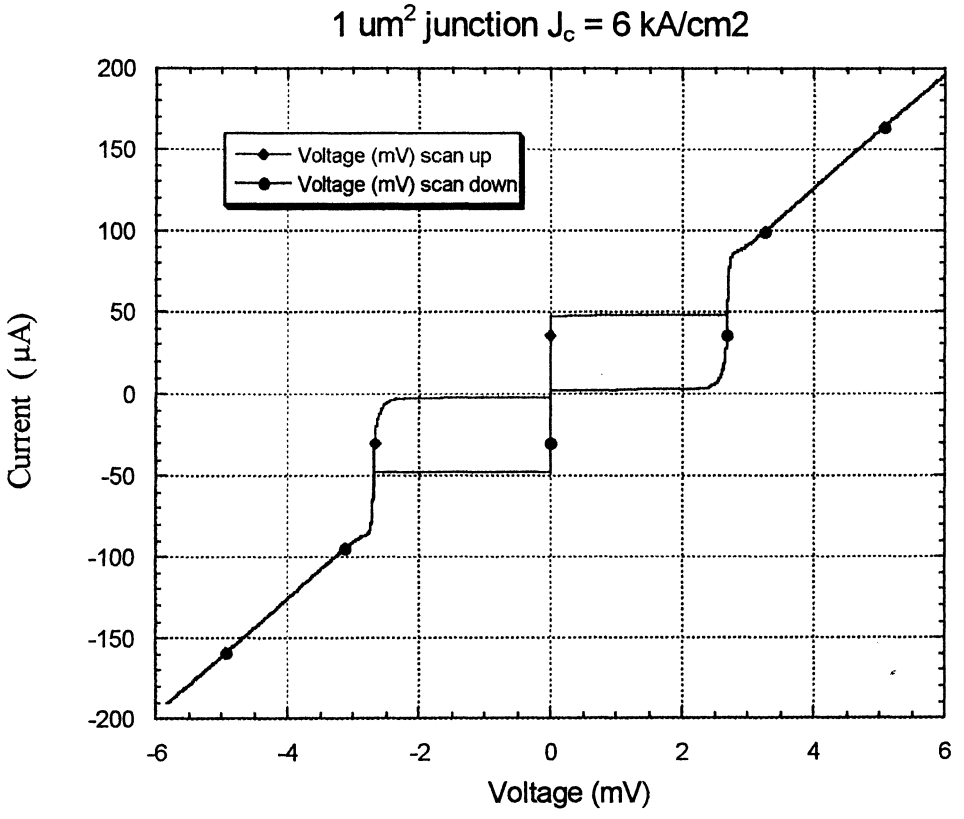


Figure 1. Current – Voltage characteristic of $1\mu m^2$ junction measured at 4 K.

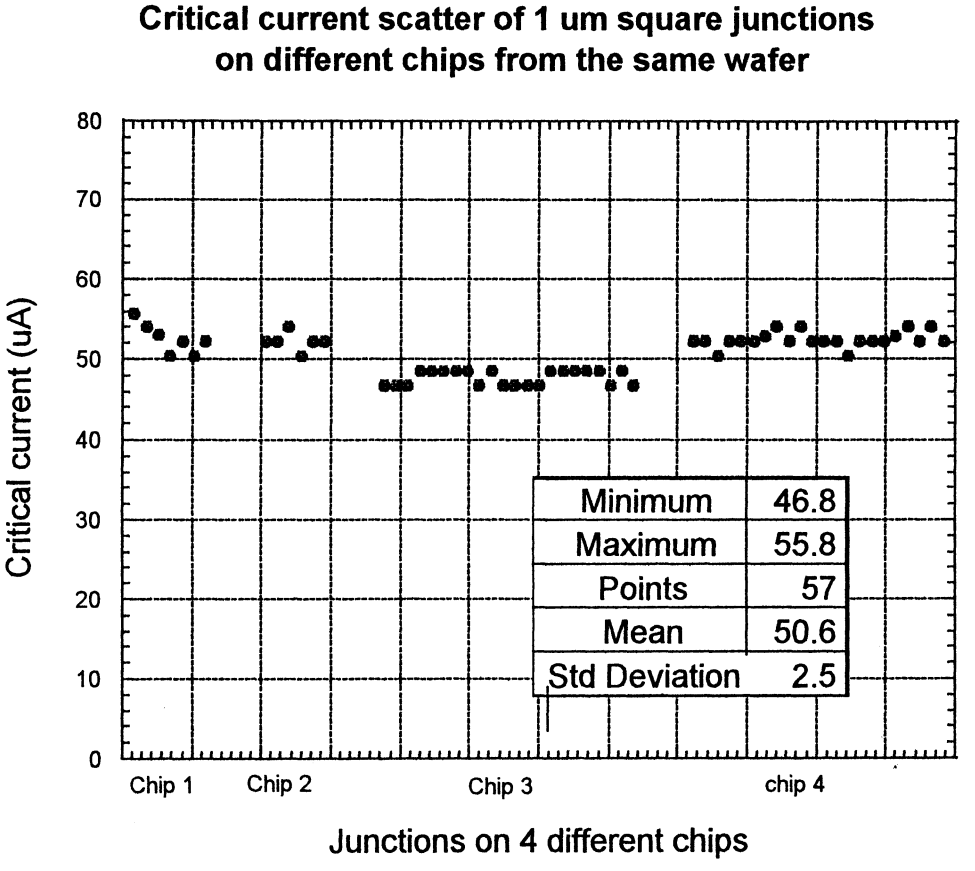


Figure 2. Scatter in the critical currents of 1μm^2 junctions across a 2" wafer. Data are from 4 different chips.

STONY BROOK

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November 12, 1998

James L. Desmond
Assoc. Director for Administration
National Radio Astronomy Observatory
520 Edgemont Road
Charlottesville, VA 22903-2475

Dear Dr. Desmond:

15% of the time of Mr. Arthur Davis of the Department of Physics & Astronomy's technical staff will be provided to the project for the "Development of SIS mixers for MMA receivers" if funded by the NRAO. Mr. Davis will provide support for the maintenance of fabrication systems and the production of liquid helium to be used on this project.

This represents a commitment to cost sharing by the University in the amount of $29,902 (15% of 2 years' salary, plus fringe benefits at 25.67%+Indirect Costs at 47.5%).

Sincerely,

Janos Kirz

Janos Kirz
Professor of Physics
Department Chair