

**Subject: Vasquez second draft****Date:** Fri, 20 Nov 1998 08:43:52 -0500 (EST)**From:** John Webber <jwebber@NRAO.EDU>**To:** akerr@polaris.cv.nrao.edu, rbrown@polaris.cv.nrao.edu, span2@polaris.cv.nrao.edu

Here's the second draft of the letter to Vasquez. I have incorporated all comments. Bob, upon reflection Kerr & Pan have decided it might generate bad feelings to dwell upon what we have paid for but did not get, so the previous management point #4 has been omitted entirely.

John

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SECOND DRAFT of letter to Rick Vasquez 11-20-98

Dear Rick,

We have carefully considered your draft proposal of 10-19-98 to have CalTech, SAO, and NRAO join forces to get SIS mixers fabricated by JPL. We have a number of concerns about this proposal which are discussed here. After your staff have had a chance to consider these items, we wish to have a teleconference to discuss them.



Purely technical issues:

1. Silicon substrates are not suitable for our mixer designs. We require fused quartz in order to benefit from its low dielectric constant. Is this a problem?
2. We believe that e-beam lithography is required for the higher frequency mixers, and it is highly desirable for junction definition at all frequencies, as it greatly reduces one of the major process uncertainties. Improved definition of the junctions must, of course, not result in degraded junction quality. If we specify e-beam lithography for junctions, is process development needed, and if so, is it possible to estimate how long it will take?
3. The proposed alignment tolerance of  $\pm 1.5$  microns is too large; we need this parameter to be  $\pm 1$  micron. Is process development needed in order to achieve this tolerance?
4. The tolerance on  $J_c$  of  $\pm 20\%$  is high. We would prefer  $\pm 10\%$  tolerance in order to land closer to the design. Is process development needed in order to achieve this tolerance?
5. The proposed ratio of subgap to normal resistance of  $>8$  is not acceptable. We require that this parameter be  $>20$ . Is process development needed in order to achieve this?
6. The assumption that the "...NRAO, SAO, CSO, and OVRO designs are sufficiently similar...so that common device processing is possible" is incorrect. We require additional resistor and insulator layers not used by other current designs, and, almost certainly, different  $J_c$  values. What is the impact of this fact on the proposed program?

Management issues:

1. The proposal is contingent upon SAO's continuing participation for 3 years beyond the end of their present contract. Furthermore, it is likely that much of the final 3 years of SAO work will not be in Nb--possibly NbTiN. Is SAO's position on these matters clear?
2. The proposal is contingent upon obtaining a loan from JPL administration for purchase of a new Nb system. We are unable

to evaluate the likelihood of this and would appreciate clarification.

3. We believe that 10% of Rick LeDuc's time is insufficient to ensure high quality mixers. Our past experience strongly indicates that intensive participation of a highly experienced fabricator is needed in order to obtain consistent high quality.
4. Based on our past experience, we believe that two technicians on maintenance and fabrication are unlikely to provide sufficient labor to meet the combined needs of the NRAO, SAO, CSO, and OVRO.

Schedule issues:

1. It is important that we obtain new, good wafers as soon as possible. We are in the design and development phase of the Millimeter Array, and have a short timetable to meet. However, we believe the time required to acquire a new Nb system, commission it, and calibrate it for SIS junction fabrication will be at least six months. Is our evaluation incorrect?
2. According to your proposal, a new hire for Nb fabrication would not even start until mid 1999. Even for an experienced fabricator, there will be a considerable period of training before high quality SIS mixers can be expected. Please address training and its impact on the schedule.
3. Scheduling problems are almost inevitable if "common device processing" is required.

For all these reasons, we are afraid that it will be early 2000 before we get anything useful under the proposed plan--and this is too late to do us any good.

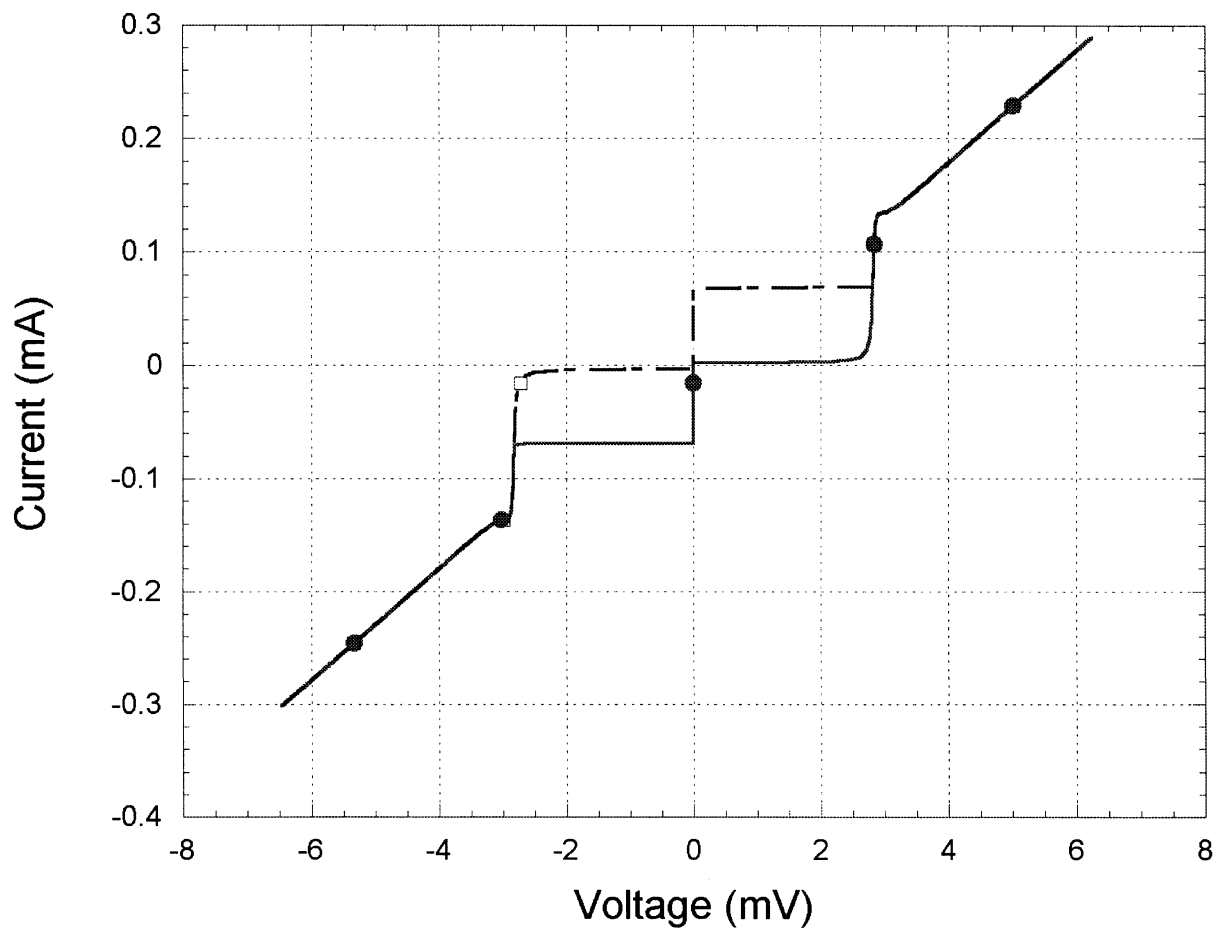
Cost issues:

1. We are concerned that development will be required in at least some of the areas listed as technical concerns, and that this will involve additional delays and consequent expenditure of funds by the NRAO.
2. Two wafers from each of two mask sets per year is not sufficient. We require at least two wafers from at least 3 mask sets per year, which will be an additional cost.
3. Under the proposal, the NRAO is responsible for the masks (mask designs and mask fabrication) separately from the JPL contract. This also affects the budget.
4. The total amount of funds requested from the NRAO even in the context of a joint program with CalTech and SAO already exceeds the amount available for SIS mixer fabrication by a large amount. The additions required to the proposed program in order to address the concerns listed above, we believe, will drive these costs even higher.
5. The NRAO's budget contribution increases with time, whereas that of other participants does not. However, there is no corresponding increase in what we get for our money.

Sincerely, etc.

SUNY 18 Nov 98

1  $\mu\text{m}$  junction on 8  $\text{kA}/\text{cm}^2$  trilayer on quartz substrate



From SONY - 10 Nov 98

1  $\mu\text{m}$  junction on a 8 kA/cm<sup>2</sup> trilayer on Quartz substrate

