9-1-99

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September 1, 1999

Dr. John Webber
National Radio Astronomy Observatory
2015 Ivy Rd., Suite 219
Charlottesville, VA 22903-1733

Re: Purchase Order No. 55162
"Development of SIS Mixers for MMA Receivers"

Dear Dr. Webber:

Enclosed please find the Quarterly Report for the above referenced project.

If I can be of further assistance to you in this matter, please contact me at (516) 632-9024.

Sincerely,

Ivar Strand

Ivar Strand
Associate Director of Sponsored Programs

IS:rs

xc: Dr. J. Lukens
File 431-6238A

State University of New York at Stony Brook
Department of Physics and Astronomy

Development of SIS Mixers for MMA Receivers

Principal Investigator: Prof. James Lukens

Sponsoring Organization: National Radio Astronomy Observatory

Quarterly Report

Prepared for: Dr. Anthony Kerr

Report Period: April 15, 1999 - July 15, 1999

Prepared by: Dr. Sergey K. Tolpygo

August 15, 1999

During the second quarter of the contract, we were working on the fabrication of the first design of NRAO mixers and electric testing of the fabricated devices and test resonators. Wafer NRAO1 was fabricated using our planarized process. The wafer was diced, inspected, and good chips were electrically tested. The critical current density was 6.3 - 6.4 kA/cm^2, and the dielectric (I2) thickness was 125 nm. The junctions in mixers have a gap voltage of 2.6 mV and the R_{sg}/R_n ratio of more than 20. This ratio gets yet larger on suppressing the Josephson current with a magnetic field or cooling the mixers below 4.2 K. From testing the resonators, we estimated the values of the high frequency penetration depths and the junction specific capacitance. Two chips containing the total of 12 electrically good mixers were transferred to NRAO for further microwave testing.

Several problems were encountered during the fabrication:

1. Firstly, there was a quartz problem at the first step of the fabrication process, on the stage of junctions definition. After the lift-off there was a great number of tiny quartz particles left on top of the M3 layer. These particles then served as an etch mask during the M3 etch, and eventually resulted in the presence of unwanted metal junk on the wafer, which shorted in many cases some of the devices. The source of the quartz problem was identified as possibly due to overheating of the wafer during the quartz deposition and a new (thicker) quartz target recently installed in the deposition chamber. The problem went away in the subsequent fabrication runs (wafers NRAO2 and NRAO3).
2. There was a major mistake made during comprising a macrofile for the EBL. As you know, the top part of each chip in the design presents an inverted (180° rotated about the chip center) image of the bottom part. However, all top parts were written without this inversion, limiting immediately the yield of useful devices by 50%.
3. A visual inspection also showed that each chip had a couple of devices with somewhat misalign layers. This could be due to an error at automated registration.
4. On some of the chips, areas of incomplete M2 etch were found. This seems a simple problem which can be eliminated by increasing the etching time.
5. There was a problem with RIE of contact holes. For some unclear reason M3 does not etch completely after planarization and the etch rate is much lower than during the M3 layer etch. This problem has never been encountered before with Si wafers. One possible cause could be charging. We are currently working to eliminate the problem.
6. And finally, the gold metalization layer did not stick as well on top of M4 as it was in the test runs. We are working on this problem also.

We are currently working on eliminating all of these problems, which would allow us to increase the yield in future fabrication runs.