11-23-99

Memorandum

To: A. R. Kerr
S. K. Pan
G. Lauria
W. K. Crady
R. Groves

Cc: J. C. Webber

From: J. Effland

Date: 1999-11-23

Subject: Dewar, Mixer Bias, and IF Amplifier Interconnections

The attached schematics show interconnections between the Mixer Bias Controller, Bias Pod (which encloses the low-level bias boards), and the Dewar. The schematics are based on comments received from the last memo[1] on this subject. The list below contains important issues and questions about the design. Following that are a few design details.

1. If each IF preamp requires three FET stages, and there are two preamps per Dewar, then ***two*** preamp bias supplies are required for each Dewar, because each bias supply has only 5 outputs. We are building only three preamp bias supplies: One for each mixer rack and the third for Gene Lauria's preamp design work.
2. Is there any need to shield the bias wires between the bias card and the inside of Dewar?
3. Is independent control of the bias state (output ground, output zero, open loop, closed loop) required for each bias board? Independent control increases the number of wires between the Mixer Bias Controller and the bias boards. Each of the four bias boards in the bias pod will have a cable from the mixer bias controller chassis with 22 wires in it, and there will be four cables. Other functions that might be shared include output shorting states, ±20V, and grounds.
4. Can a single differential voltage input be used on each bias board for both open-loop and closed-loop operation, or is there an advantage to using separate bias command inputs?
5. Independent magnet supplies are planned for each balanced mixer assembly. This means that both mixers in a balanced mixer assembly will use the same magnet supply. Both mixer racks already have an HP E3631 programmable power supply, which is sufficient to power two electromagnets assuming they are wired to use a common return. This power supply can also

[1] "Preliminary DC Interface Specifications for Dewar," Internal Memo from J. Effland, 1999-11-03.

measure the magnet currents and includes a GPIB interface for the computer to read the currents. Specified accuracy for current measurements is 0.15%+4 mA over 25±5C temperature range, although we usually observe less than a 2-mA discrepancy between this supply and the HP 34401 DVM.

The HP E3631 power supply also has a 5V output that is independent and programmable output for future use.

6. Are two oscilloscopes sufficient to monitor all four junctions? If so, then switching is required to select which of the junctions to monitor.
7. Computer monitoring of bias voltage and current for all four junctions requires using the multiplexer that Kirk Crady designed into the IO Controller to provide enough inputs for the computer's analog card. This may slow down, by an unknown amount, acquisition of I-V curves for each junction because voltage and current will be measured sequentially, rather than simultaneously as with the present system. However, data acquisition speed with the new system may actually increase from a reduction in noise on the signal lines. The present system must average 40 measurements for each data point to achieve an acceptably low variance in the data.

A simplified AutoCAD sketch of the Dewar interfaces is shown in Attachment 1, which has been revised based on the meeting of 1999-11-05. This AutoCAD sketch is the basis for the detailed design, which is drawn in OrCAD, because OrCAD readily accommodates hierarchical designs, and because it provides error-checking routines to confirm the consistency of interconnections. OrCAD uses bus nomenclature to represent multiple signals on a single connector and cable. Bus signals are denoted with brackets, such as V_MON[1..8], which means that this connection actually carries 8 signal lines.

Attachment 2 shows the overall measurement system from OrCAD in block diagram form. The "Bias Pod" contains the bias boards with amplifiers for the low-level junction voltages. The Bias Pod has four mixer bias boards, and the pod will be attached to the side of the Dewar. Two IF amp bias supplies are required to power the 6 junctions in the balanced IF amplifiers, even though the drawing shows only a single box for this subsystem. The number of "Preamp Bias Supplies" may also need to increase as discussed below.

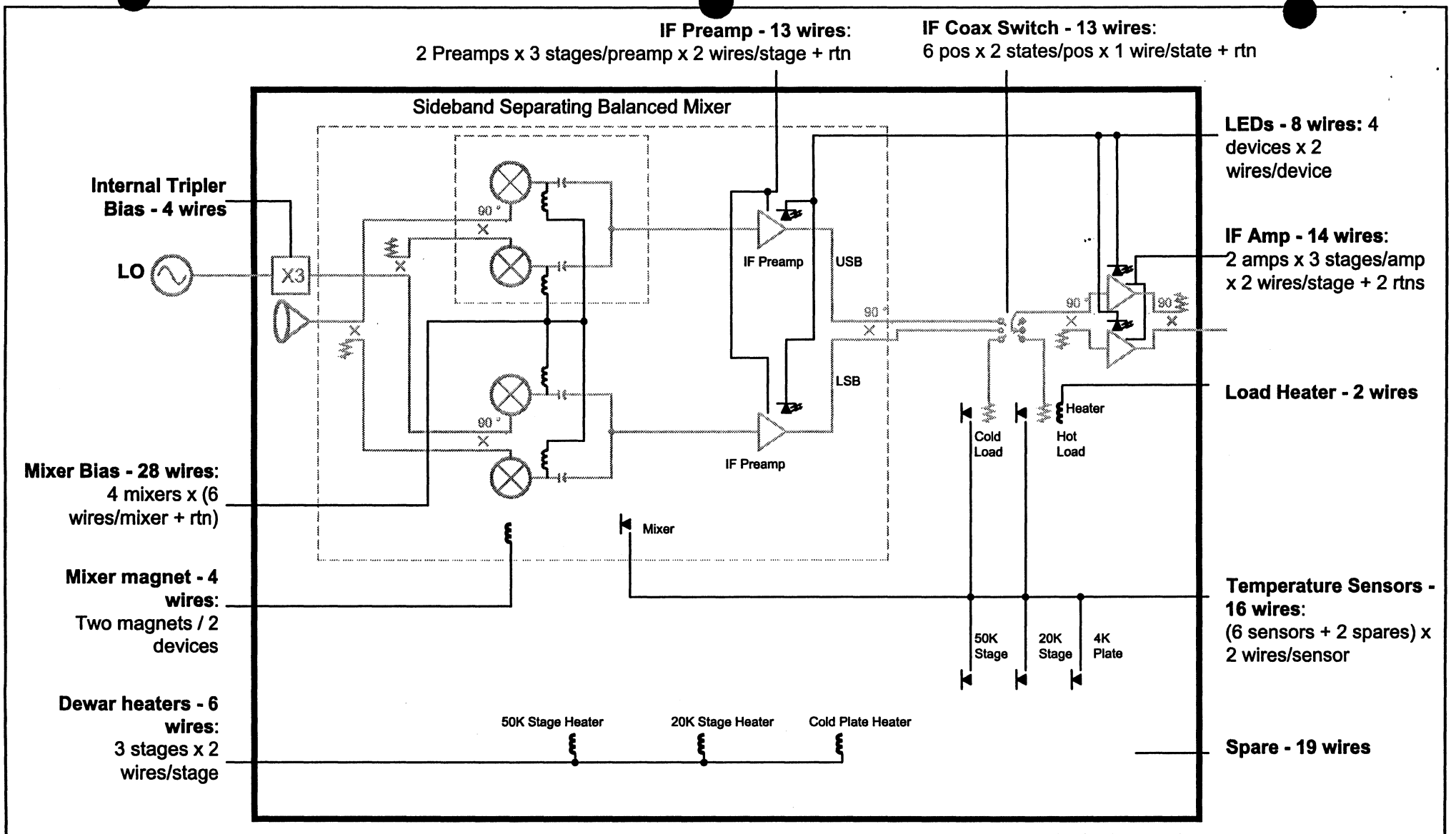
Attachment 3 shows the subsystems inside the Dewar, consisting of two balanced mixer assemblies, the coaxial IF switch, and the balanced IF amplifier. Attachment 4 is a drawing of the balanced mixer assembly. It is assumed that a single electromagnet will provide the magnetic field required for both junctions. The box with reference "AMP1" is the integrated IF preamp, which is represented by the simplified schematic in Attachment 5. All IF preamps use the same simplified schematic that shows only enough details to define interface line functions.

Attachment 6 shows the four bias cards in the Bias Pod. The vacuum interface will be located at the feed-through line filters, so the low level bias boards can operate at atmospheric pressure. Important signal names are defined in Table 1 below.

Table 1 : Bias Pod Signal Lines used in OrCAD		
Name	**Direction**	**Function**
BIAS_OLOOP	From controller	Differential control voltage for open-loop bias mode
BIAS_CLOOP	From controller	Differential control voltage for closed-loop bias mode
VMON	To controller	Junction voltage monitor
IMON	To controller	Junction current monitor
State	From controller	State of bias card: 1. Output grounded 2. Output shorted 3. Open/Closed loop operation
BIAS_OUT	To junction	Bias command voltage
VL_MON+	From Junction	Junction voltage monitor
IL_MON+	From Junction	Junction current monitor

Attachment 7 shows the bias card schematic. This schematic is Wes Grammer's implementation of Tony Kerr's original bias circuit with the addition of shorting relays and input/output signal lines. The design remains unfinished and will be completed after some of the interface issues raised in the memo are resolved.

Please review and forward your comments to me.



ATTACH 1

REV	WHO	DATE	DESCRIPTION
A	JEE	1999-11-05	REVISED FROM MEETING WITH ARK & SKP

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22903

TITLE: DEWAR INTERFACES: POWER, CONTROL, & MONITORING

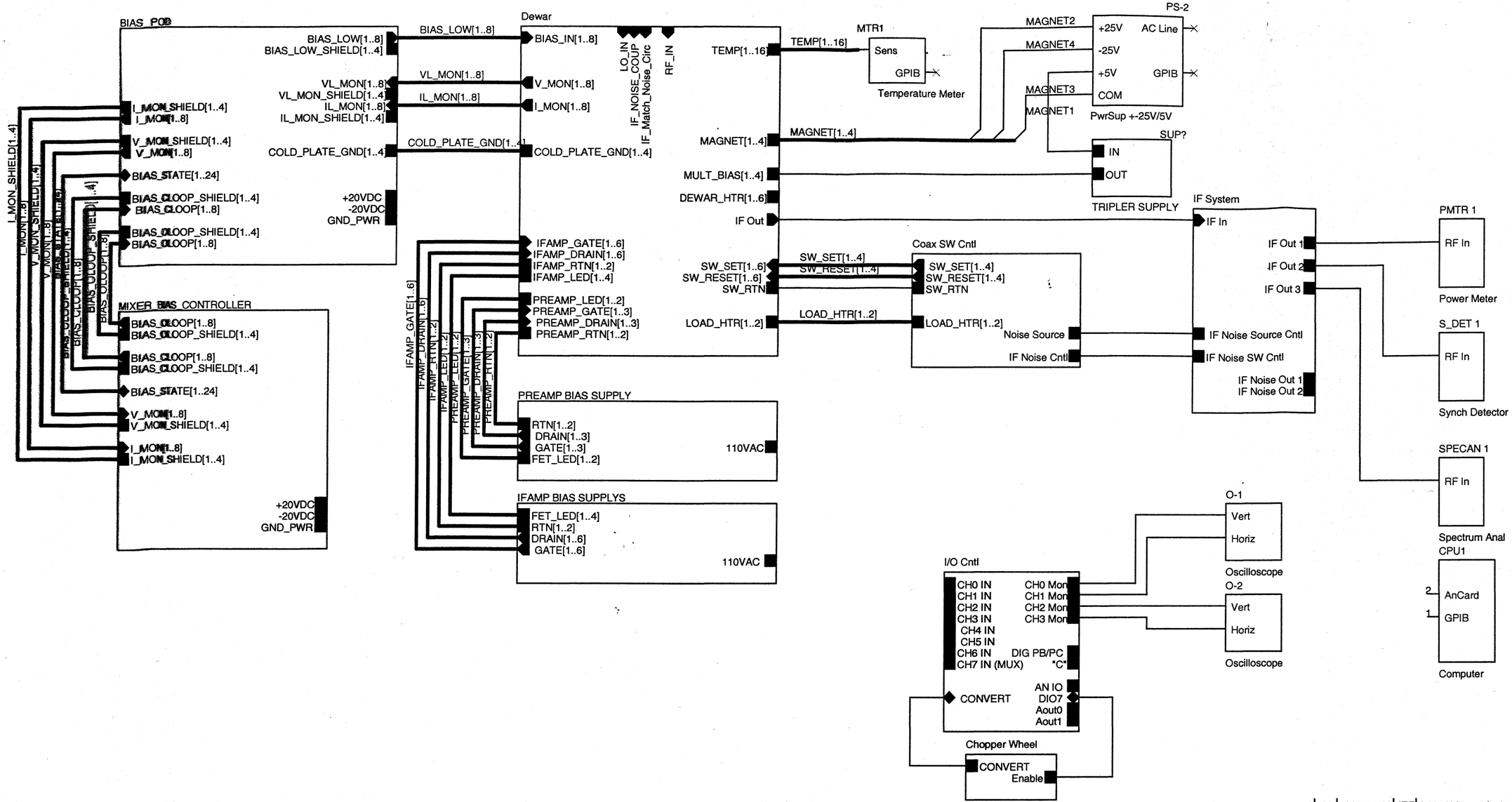
PROJECT: SIS MIXER MEASUREMENT SYSTEM

DESIGN	JEE	1999-11-03		
DRAWN	JEE	1999-11-03	MATERIAL	
SHEET			FINISH	

COMPUTER DRAWING: \\Eagle\cv-cdl-sis\docs\rack\Dewar\interfaces.dwg

SCALE: None | DWG. NO. | REVISION: A

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES± .1°
2 PLACE DEC ±.01
3 PLACE DEC ±.005
4 PLACE DEC ±.001



Rev	Date	By	Description
09	1999-11-19	JEE	Added bias pod, etc.
08	1999-09-02	JEE	Moved Chopper Trigger Cable to chopper sheet
07	1999-08-19	JEE	Added Chopper Trigger Cable
06	1999-08-10	JEE	Updated to OrCad V9.0
05	1999-07-14	JEE	Added chopper wheel
04	1999-05-03	JEE	Added IF Noise Source Control
03	1998-12-25	JEE	Corrected power input pinouts, DGND on con B
02	1998-11-05	JEE	New Versions on Comp. I/O and SW Cnt.
01	1998-11-02	JEE	Bias Monitor and added CPU

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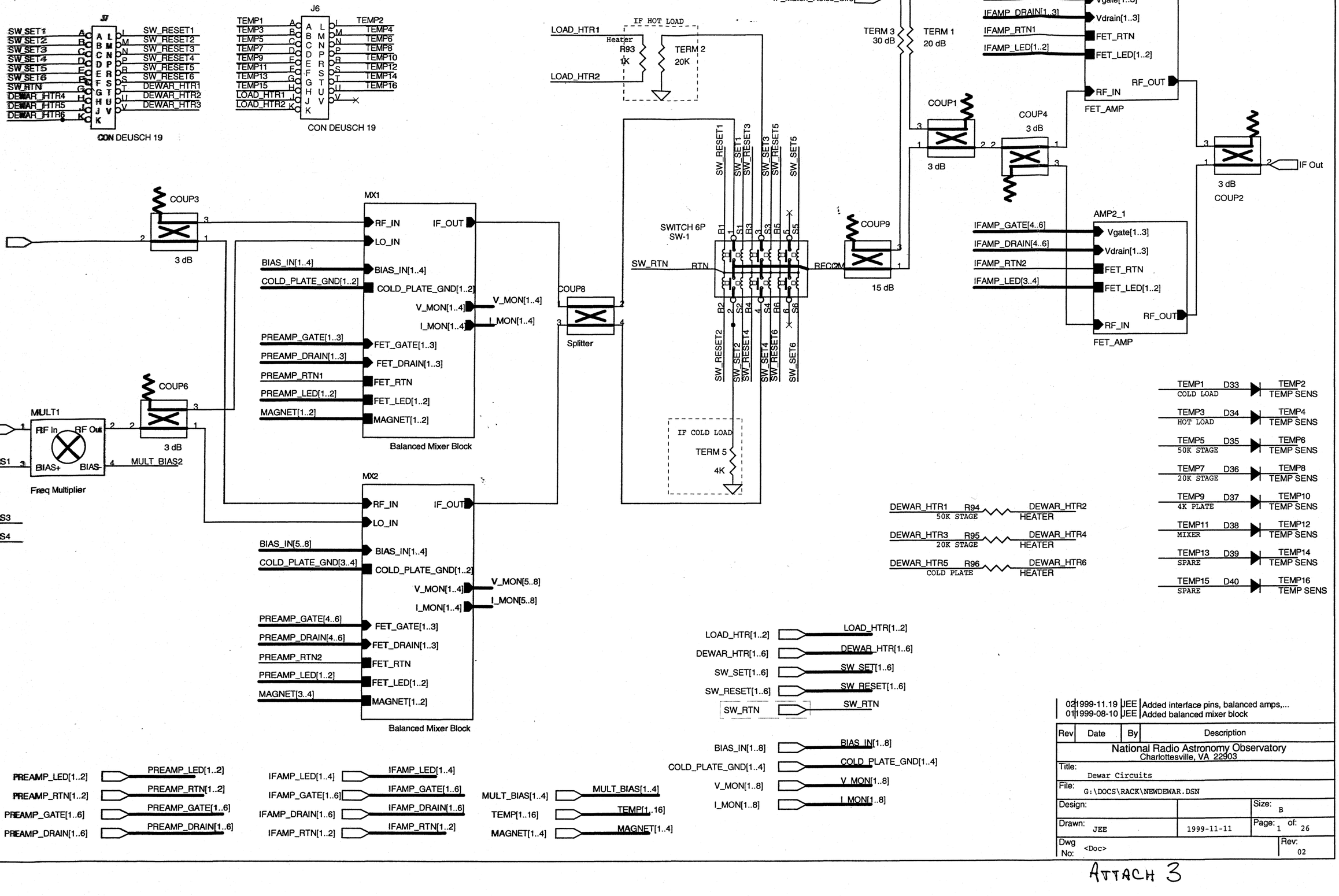
Charlottesville, VA 22903

Title: SIS Mixer Measurement System - JT-2		
File: G:\DOCS\RACK\NEWDEWAR.DSN		
Design: SIS Group		Size: B
Drawn: JEE	1998-Aug-07	Page: 1 of: 23
Dwg No: Doc		Rev: 09

ATTACH 2



Rev	Date	By	Description
02	1999-11.19	JEE	Added interface pins, balanced amps,...
01	1999-08-10	JEE	Added balanced mixer block

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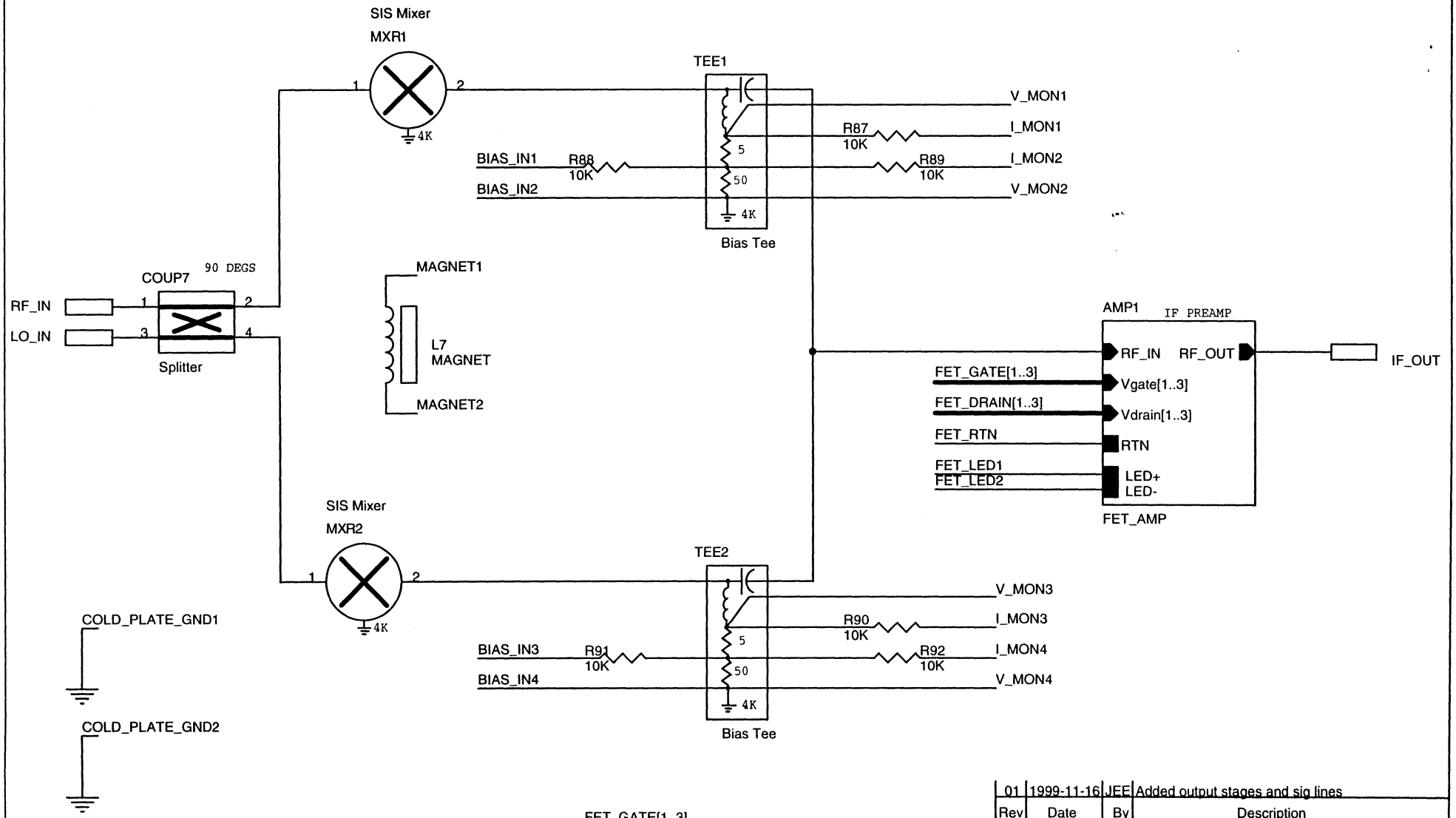
Charlottesville, VA 22903

Title: Dewar Circuits		
File: G:\DOCS\RACK\NEWDEWAR.DSN		
Design:		Size: B
Drawn: JEE	1999-11-11	Page: 1 of: 26
Dwg No: <Doc>		Rev: 02

ATTACH 3



Rev	Date	By	Description
01	1999-11-16	JEE	Added output stages and sig lines

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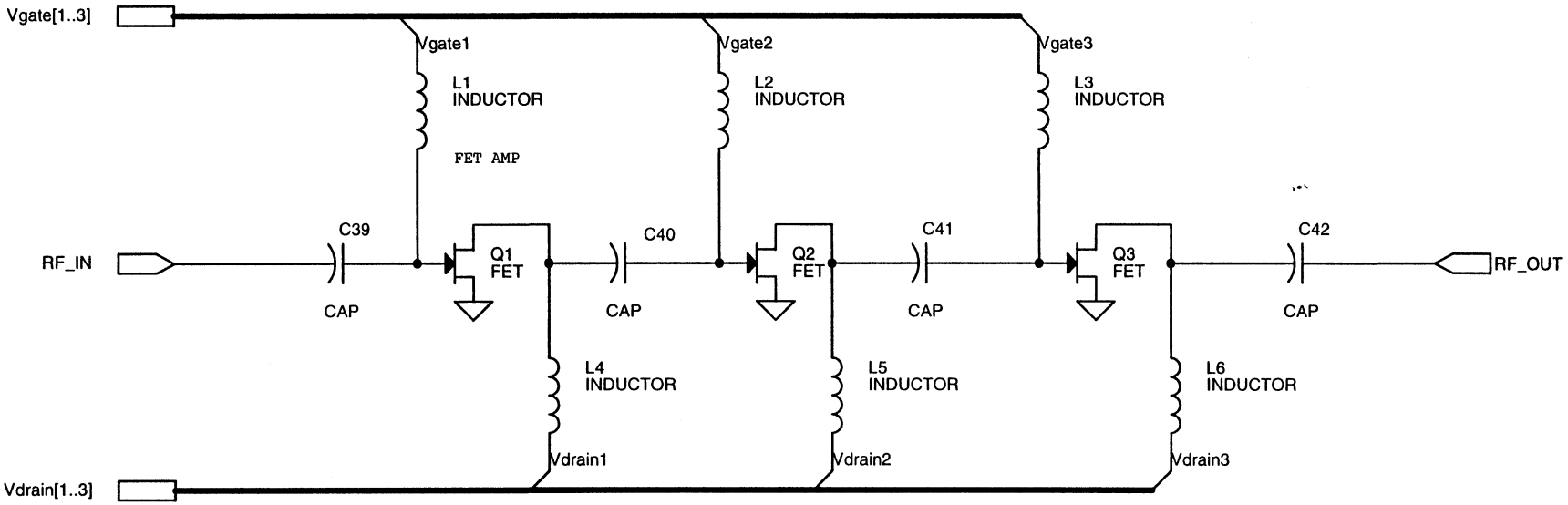
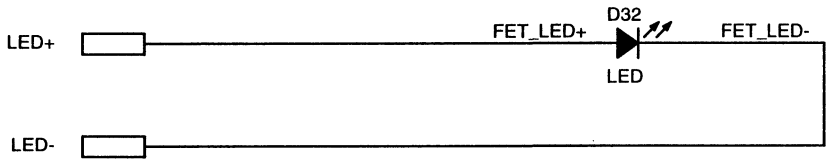
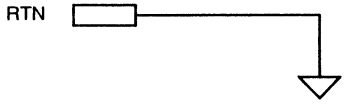
Charlottesville, VA 22903

Title: Balanced Mixer Block		
File: G:\DOCS\RACK\NEWDEWAR.DSN		
Design: ARK & SKP	Date Designed	Size: A
Drawn: JEE	1999-08-10	Page: 1 of: 26
Dwg No: <Doc>		Rev: 01

ATTACH 4

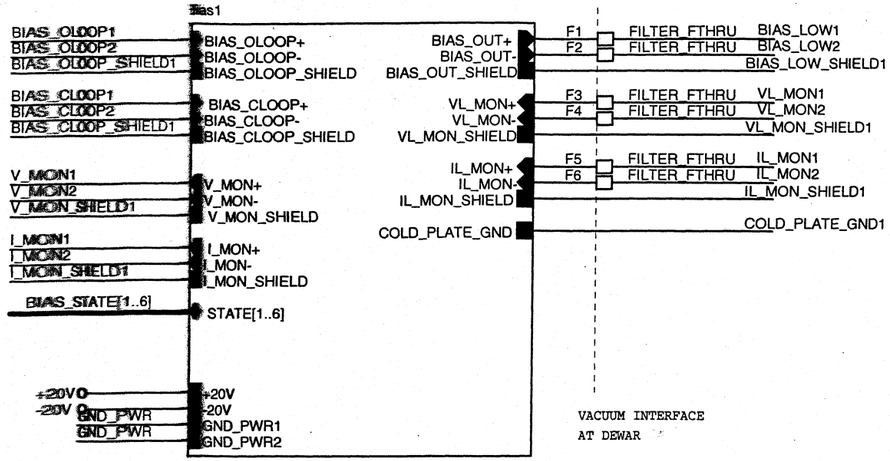


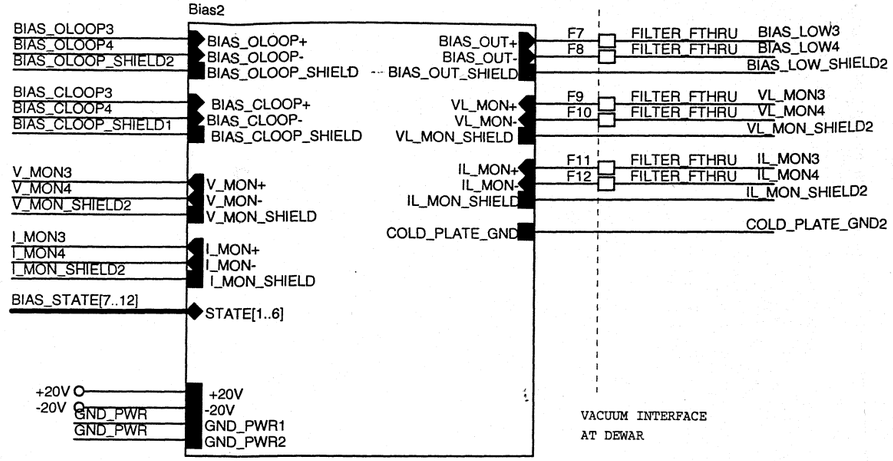


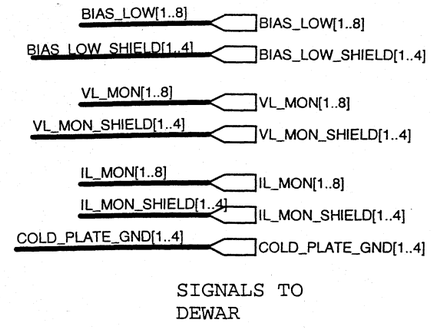


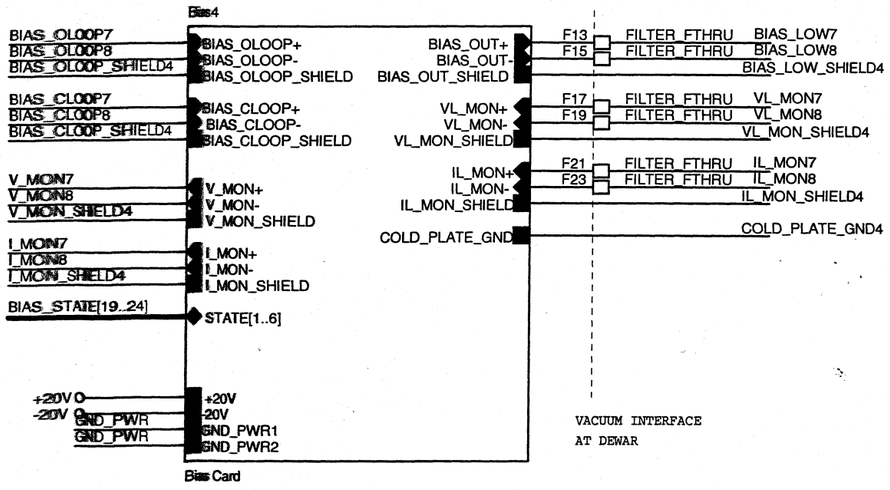
Rev	Date	By	Description
National Radio Astronomy Observatory Charlottesville, VA 22903			
Title: FET AMP			
File: G:\DOCS\RACK\NEWDEWAR.DSN			
Design:			Size: A
Drawn: JEE	1999-11-09		Page: 1 of: 26
Dwg No: <Doc>			Rev: 00

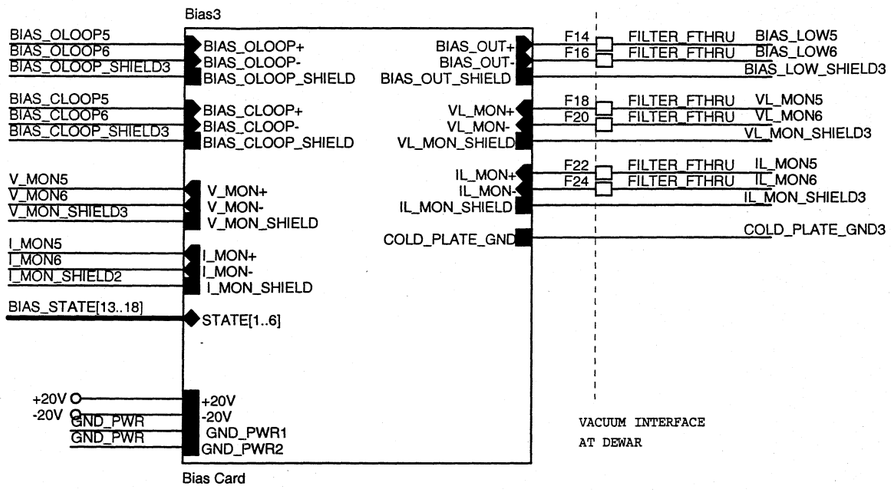
ATTACH 5











BIAS POD
CONNECTOR FOR
EACH MIXER
JP1

BIAS_OLOOP1	1	2	
BIAS_OLOOP2	3	4	I_MON1
BIAS_OLOOP_SHIELD1	5	6	I_MON2
BIAS_CLOOP1	7	8	I_MON_SHIELD1
BIAS_CLOOP2	9	10	+20V
BIAS_CLOOP_SHIELD1	11	12	-20V
V_MON1	13	14	GND_PWR
V_MON2	15	16	GND_PWR
V_MON_SHIELD1	17	18	BUS_STATE2
BUS_STATE1	19	20	BUS_STATE4
BUS_STATE3	21	22	BUS_STATE6
BUS_STATE5	23	24	

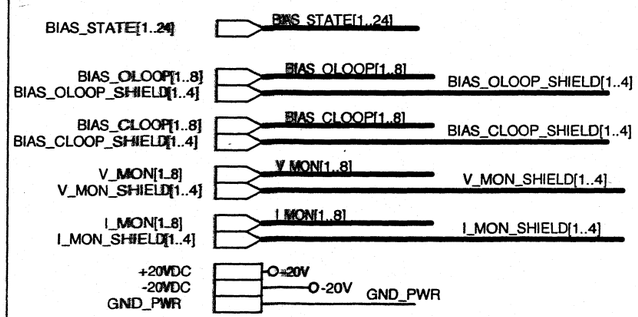
CON 24e

JP2

BIAS_OLOOP3	1	2	
BIAS_OLOOP4	3	4	I_MON3
BIAS_OLOOP_SHIELD2	5	6	I_MON4
BIAS_CLOOP3	7	8	I_MON_SHIELD2
BIAS_CLOOP4	9	10	+20V
BIAS_CLOOP_SHIELD2	11	12	-20V
V_MON3	13	14	GND_PWR
V_MON4	15	16	GND_PWR
V_MON_SHIELD2	17	18	BUS_STATE8
BUS_STATE7	19	20	BUS_STATE10
BUS_STATE9	21	22	BUS_STATE12
BUS_STATE11	23	24	

CON 24e

SIGNALS FROM BIAS CONTROLLER



OPEN LOOP BIAS
COMMAND

CLOSED LOOP BIAS
COMMAND

BIAS POD
CONNECTOR FOR
EACH MIXER
JP4

BIAS_OLOOP7	1	2	
BIAS_OLOOP8	3	4	I_MON7
BIAS_OLOOP_SHIELD4	5	6	I_MON8
BIAS_CLOOP7	7	8	I_MON_SHIELD4
BIAS_CLOOP8	9	10	+20V
BIAS_CLOOP_SHIELD4	11	12	-20V
V_MON7	13	14	GND_PWR
V_MON8	15	16	GND_PWR
V_MON_SHIELD4	17	18	BUS_STATE20
BUS_STATE19	19	20	BUS_STATE22
BUS_STATE21	21	22	BUS_STATE24
BUS_STATE23	23	24	

CON 24e

BIAS POD
CONNECTOR FOR
EACH MIXER
JP3

BIAS_OLOOP5	1	2	
BIAS_OLOOP6	3	4	I_MON5
BIAS_OLOOP_SHIELD3	5	6	I_MON6
BIAS_CLOOP5	7	8	I_MON_SHIELD3
BIAS_CLOOP6	9	10	+20V
BIAS_CLOOP_SHIELD3	11	12	-20V
V_MON5	13	14	GND_PWR
V_MON6	15	16	GND_PWR
V_MON_SHIELD3	17	18	BUS_STATE14
BUS_STATE13	19	20	BUS_STATE16
BUS_STATE15	21	22	BUS_STATE18
BUS_STATE17	23	24	

CON 24e

Send 15V or 20v to this board?
Shield outputs to filter bulkhead?
Can't we keep OL/CL switching
in bias board?

Rev	Date	By	Description

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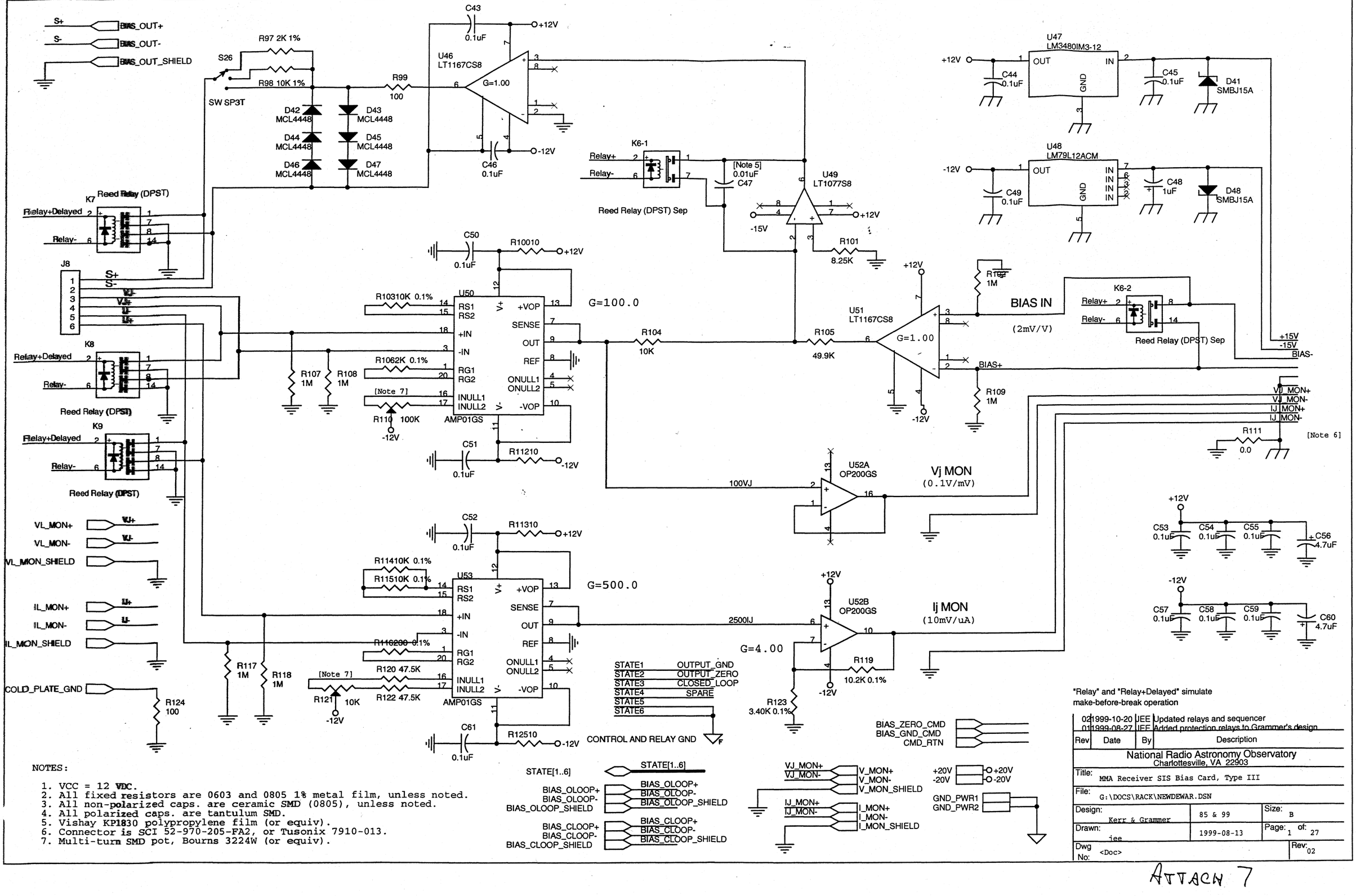
Title: BIAS POD			
File: G:\DOCS\RACK\NEWDEWAR.DSN			
Design:		Size: B	
Drawn: JEE	1999-11-19	Page: 1 of: 27	
Dwg No: Doc		Rev: 00	

ATTACH 6



NOTES:

1. VCC = 12 VDC.
2. All fixed resistors are 0603 and 0805 1% metal film, unless noted.
3. All non-polarized caps. are ceramic SMD (0805), unless noted.
4. All polarized caps. are tantulum SMD.
5. Vishay KP1830 polypropylene film (or equiv).
6. Connector is SCI 52-970-205-FA2, or Tusonix 7910-013.
7. Multi-turn SMD pot, Bourns 3224W (or equiv).

"Relay" and "Relay+Delayed" simulate make-before-break operation

Rev	Date	By	Description
02	1999-10-20	JEE	Updated relays and sequencer
01	1999-08-27	JEE	Added protection relays to Grammer's design

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Charlottesville, VA 22903

Title: MMA Receiver SIS Bias Card, Type III			
File: G:\DOCS\RACK\NEWDEWAR.DSN			
Design: Kerr & Grammer	85 & 99	Size: B	
Drawn: jee	1999-08-13	Page: 1 of: 27	
Dwg No: <Doc>		Rev: 02	

ATTACH 7