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January 12, 2000

Dr. John Webber
National Radio Astronomy Observatory
2015 Ivy Road, Suite 219
Charlottesville, VA 22903-1733

RE: Purchase Order No. 55162
"Development of SIS Mixers for MMA Receivers "

Dear Dr. Webber:

Enclosed is the July 1999 to October 1999 Quarterly Report for the above referenced award.

Please contact me at (516) 632-4402 if you should have any questions concerning this submission.

Sincerely,

Ivar Strand
Director of Sponsored Programs

IS:sb
Enc.

xc: Dr. James Lukens
File 431-6238A

State University of New York at Stony Brook
Department of Physics and Astronomy

Development of SIS Mixers for MMA Receivers

Principal Investigator: Prof. James Lukens

Sponsoring Organization: National Radio Astronomy Observatory

Quarterly Report

Prepared for: Dr. Anthony Kerr

Report Period: July 16, 1999 - October 15, 1999

Prepared by: Dr. Sergey K. Tolpygo

November 15, 1999

During the third quarter of the contract, we worked on the fabrication of more wafers with the first design of NRAO mixers and on electric testing of the fabricated devices and test resonators. Wafer NRAO3 was fabricated, diced, inspected, and several chips were electrically tested. Although the overall look of this wafer was much better than the previous one, optical inspection showed that the base electrode in the contact holes was etched away so the bridges of the input CWG did not make electrical contact with the ground. In the contact holes of tuning structures, however, the wiring layer did make a contact. This was confirmed by dc electric testing of the mixers, which showed good I-V characteristics in about 50 % of the tested devices. Since there were little chances that these mixers would perform adequately in rf testing (due to the mentioned problem with the bridges) it was decided not to transfer this wafer to NRAO. From the data on test structures and resonators we extracted the junction specific capacitance, insulator dielectric constant, and magnetic field penetration depth in our Nb films. These parameters were reported to NRAO for the use in future designs.

We also worked to build an understanding of the contact hole etch problem, since it was never encountered before in fabrication on Si wafers. To be specific, the problem is that Nb counter electrode (M3 layer) in the contact holes etches much slower than the same M3 layer on the stage on junction definition or than the base electrode, or any freshly deposited Nb layer. Because of this much smaller etch rate, the PMMA mask and quartz around the contact holes get also etched away. As a result, M2 layer around the contact holes gets exposed and eventually etched away. By comparing the observed etch rates with the results of tests on clean and contaminated Nb surfaces, I came to think that the M3 surface in contact holes gets much stronger contaminated (or oxidized) during the processing than it usually does in our standard PARTS process on Si wafers. This difference could be due to a higher wafer temperature during quartz depositions because of a low thermal conductivity of quartz than Si. We are working on testing different cleaning procedures and other ways to eliminate encountered fabrication problems. However, it is more or less clear at the moment that it would be nice to upgrade our quartz deposition system to achieve a better thickness uniformity and better control over plasma, substrate temperature, and other deposition parameters.