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C: Kerr
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June 13, 2000

Dr. John Webber
National Radio Astronomy Observatory
2015 Ivy Road, Suite 219
Charlottesville, VA 22903-1733

RE: "Purchase Order No. 55162"
"Development of SIS Mixers for MMA Receivers"

Dear Dr. Webber:

Please find enclosed the Progress Report covering the period from October 1999 to June 2000 for the above referenced project.

If you should have any questions concerning this submission, you can reach me at 631-632-4402.

Sincerely,

Ivar Strand

Ivar Strand
Director of Sponsored Programs

IS:rs
Enc.

xc: Dr. J. Lukens
File 431-6238A

State University of New York at Stony Brook
Department of Physics and Astronomy

Development of SIS Mixers for MMA Receivers

Principal Investigator: Prof. James Lukens

Sponsoring Organization: National Radio Astronomy Observatory

Progress Report

Prepared for: Dr. Anthony Kerr

Report Period: October 16, 1999 - June 1, 2000

Prepared by: Dr. Sergey K. Tolpygo

June 5, 2000

During the fourth and the fifth quarters of the contract, we worked on the fabrication and testing of additional wafers with the 200-300 GHz mixer design. Two wafers, NRAO5 and NRAO6 had been fabricated, diced, inspected, and about 30% of all chips had been electrically tested. Several chips from NRAO5 wafer had been sent to NRAO for a high frequency testing. Electric testing of mixers showed a yield of mixers with good dc IV curves of about 40%. However, the normal state resistance of the devices on NRAO5 wafer was about 30% higher than the design value, 90-100 Ohms instead of the required 63 Ohm. The critical current was correspondingly ~ 30% lower. It was thought initially that this deference was due to a lower critical current density of the trilayer used. However, a further inspection of the devices in the electron microscope had shown the size of the junctions to be ~ 1 um instead of the design value of 1.2 um. This difference can fully explain the observed deviation of the dc properties from the design values. The junction size problem was corrected in the next fabrication run, wafer NRAO6. However, the yield of electrically good devices was found to be basically the same.

A considerable effort was made to determine the factors which limit the yield. One of the main ones was found to be layer misalignment caused by errors in write-field alignment at automatic mark recognition routing of electron beam lithography. Layer misalignment causes shorting of one (or both) of the junction islands to the ground and/or misalignment of contact holes and thus poor contact of the devices and CWG bridges with the ground. Devices with these defects can be relatively easily found at optical inspection and, hence, be excluded from further testing. Another frequent problem is an incomplete quartz lift-off between the junction islands on the stage of M2 layer definition. This problem is mainly caused by an excess resist heating at quartz deposition because of a lower thermal conductivity of quartz wafers and, in principal, can be solved by modifying our quartz deposition system. Partially, the problem is also a design-related one (cause by an unfavorable ratio of the distance between the islands to their width) and thus could be eased by a slight modification of the design. And finally, an almost complete etch through of the base electrode on one side of the contact holes was often found. This problem is design-related and is due to the equal sizes of the junctions to be etched and etch windows on the mask. Though visually unpleasant, this defect should not cause any degradation in device performance.

After excluding all the devices with optically visible defects, the most frequent type of defects found in electric characterization was a parasitic resistance (100 - 200 Ohms) in parallel with some or all four of the junctions. A possible cause could be an incomplete sealing of junctions by quartz. A hint to this comes from profilometer scans which show a considerable dip in the quartz thickness near edges of the junctions. If quartz does not seal the junctions and leaves a part of the base electrode around the edges exposed, a thin metal shorts between the base and counter electrodes can be formed during the wiring layer deposition. This problem is disturbing because I do not have a good explanation for its cause and because no such problem was found in junctions on a Si wafer processed in parallel with NRAO6 wafer.

A considerable amount of time was spent on designing a new set of optical masks for the new 600-700 GHz mixer design. The idea was to take into account and try to eliminate all the problems encountered during the work on 200-300 GHz design and also

to minimize the number of ebl steps. Only two ebl steps were left (there were four in the previous design), junction definition and definition of small features on M2 layer (CWG bridges). There is a hope that the modified process is more robust and reliable, and thus capable of a higher yield.

EBL software on our electron microscope has been upgraded, and the new version so far seems more stable than the previous one. Main problems with the beam blanker on the microscope have also been solved. A wafer with the new design, NRAO7, is being processed now and is expected to be completed in two weeks if God permits.