

SPECTRAL PROCESSOR NO. 26

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To: Spectral Processor Group

From: R. Fisher

Subj: WINDOW MULTIPLIER ADDRESSING SEQUENCES

Below are two short notes on addressing and storage requirements for the input buffers and coefficient tables associated with the four 16-bit window multipliers. The notation used is defined in Memo No. 24.

Window INPUT BUFFER  
Read Addresses

The address generator is a 9-bit counter with the following output word:

**msb**

	8		7		6		5		4		3		2		1		0		<b>lsb</b>
--	---	--	---	--	---	--	---	--	---	--	---	--	---	--	---	--	---	--	------------

These bits are rearranged to form a common address for reading the WXYZ buffers into the window multipliers. A different rearrangement is necessary for the 1, 2, 4 or 8 input channel configuration. The counter bit notation above is used to compose the following addresses:

```
1 channel
   | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
```

```

2 channels
  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
                                }
                                Channel
                                Select

```

```
2 chan x 256
would use
only bits 0-7
with 7 being
the lsb.
```

```

4 channels
  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 8 | 7 |
                                Channel
                                Select

```

8 channels

Buffer memory writing order (4 channels)

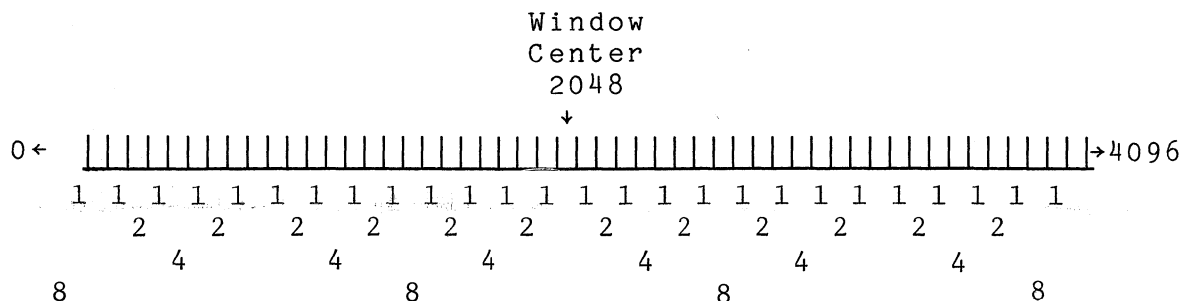
Notation: Ch 2 (0) = channel 2 real data point number 0

Common Address	W	X	Y	Z
0	Ch 1 (0)	CH 1 (1)	Ch 1 (256)	Ch 1 (257)
1	Ch 2 (0)	Ch 2 (1)	Ch 2 (256)	Ch 2 (257)
2	Ch 3 (0)	Ch 3 (1)	Ch 3 (256)	Ch 3 (257)
3	Ch 4 (0)	Ch 4 (1)	Ch 4 (256)	Ch 4 (257)
4	Ch 1 (2)	Ch 1 (3)	Ch 1 (258)	Ch 1 (259)
5	Ch 2 (2)	Ch 2 (3)	.	.
6	Ch 3 (2)	Ch 3 (3)	.	.
7	Ch 4 (2)	Ch 4 (3)	.	.
8	Ch 1 (4)	Ch 1 (5)	.	.
	.	.	.	.
	.	.	.	.
	.	.	.	.

## Window Function Storage and Recall Sequences

A window function is normally symmetric and should be centered on the array of sampled real data. If there are 2048 real samples (numbered 0-2047) put into a 1024 channel transform the window function should be centered between samples 1023 and 1024.

Assume that we have an array of 4097 ( $2^{12} + 1$ ) 16-bit coefficients which represent the window amplitude at each point. These coefficients are numbered 0-4096 and the center is 2048. The central portion of this array is represented by the bins in the diagram below, and underneath each bin is a number which tells in which spectrometer configuration (1, 2, 4 or 8 channels) that coefficient is used.



Notice that none of the coefficients are used twice and that all of the subarrays are centered on the window. The coefficient sequence to be used in each case is given in the following table and equations.

1 chan	1,3,5 ...2041,2043,2045,2047, 2049,2051...4093,4095
2 chan	2,6,10 ...2034,2038,2042,2046, 2050,2054...4090,4094
4 chan	4,12,20...2020,2028,2036,2044, 2052,2060...4084,4092
8 chan	8,24,40...1992,2008,2024,2040, 2056,2072...4072,4088

Let N be the number of the real window coefficient starting with zero and M be the coefficient number in the array above.

1 chan	$M = 1 + 2N$	(2048 coefficients)
2 chan	$M = 2 + 4N$	(1024 coefficients)
4 chan	$M = 4 + 8N$	( 512 coefficients)
8 chan	$M = 8 + 16N$	( 256 coefficients)

The first half of the coefficients apply to the W and X buffer values, and the second half apply to the Y and Z values. The even numbered coefficients  $N = 0,2 \dots$  go with W and Y and the odd numbered ones  $N = 1,3 \dots$  go with X and Z. Hence, the coefficient table for each multiplier needs to contain only one quarter of the coefficients.

Since the data values appear at the window multipliers in bit-reversed order the coefficients must be accessed in bit-reversed order. One way to do this would be to store the coefficients in bit reversed order to be accessed with normal sequential addressing. A 1024-word ROM could be used for each window multiplier with the 1-channel coefficients in the first 512 words, the 2-channel coefficients in the next 256, the 4-channel coefficients in the next 128, and the 8-channel coefficients in the next 64 words. Which table is accessed could be controlled by the high order address bits.

The address word used in the bit reversal is 10 bits wide in the 1-channel case with the two low order bits before reversal ignored.

JRF/cjd