

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VIRGINIA
VERY LARGE ARRAY PROJECT

VLA ELECTRONICS MEMORANDA #134

COMPUTER CONTROL AND PROCESSOR FOR
VLA DIGITAL DELAY-MULTIPLIER SYSTEM

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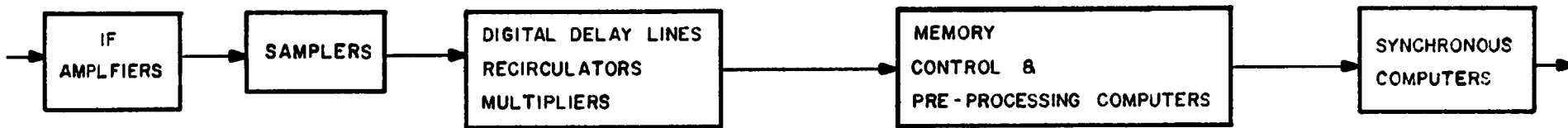
I. INTRODUCTION

The VLA continuum and spectral line system from the IF amplifiers to the synchronous computers is shown in Figure 1. The responsibilities of design are divided among four groups into the following four section:

1. IF amplifiers and samplers.
2. Delay lines, recirculators and multipliers.
3. Multiplier memories, controller, and pre-processor.
4. Synchronous computers.

This memo covers section 3 and is a preliminary report based on presently available data of the delay-recirculator-multiplier design and tentative correction equations which are to be applied to the data.

Although the systems will be built in modular sections to somewhat match antenna construction, this memo will mainly deal with the complete, final system.



VLA CONTINUUM AND SPECTRAL LINE SYSTEM

FIGURE 1

II. SPECIFICATIONS

A. Modes of Operation.

See Table 1.

Continuum as produced with two of the multiplier modules is described in VLA Technical Report #16.

B. Integration Times (Dump Period)

See Table 2 on page 15.

MODE	DESCRIPTION	— MULTIPLIER MODULE —				MAX. NO. OF CHANNELS	NOTES AND ADDITIONAL PRE-PROCESSING
		1	2	3	4		
— CONTINUUM —							
1	2EA. 50 MHz B.W.	SxS & SxC		SxS & SxC			NOTE: EACH MULTIPLICATION e.g. SxS REPRESENTS 4 MULTIPLICATIONS; RSxRS; LSxLS RSxLS; LSxRS
2	2EA. 50 MHz B.W.		CxC & CxS		CxC & CxS		
3	DITTO - GREATER SENSITIVITY	SxS & SxC	CxC & CxS	SxS & SxC	CxC & CxS	NOTE: OVER-SAMPLED	
4	2EA. 100 MHz B.W.	SxS & SxC	CxC & CxS	SxS & SxC	CxC & CxS		
— SPECTRAL LINE —							
5	SINGLE SPECTRA } MAXIMUM RESOLUTION }	A x A	A x A	A x A	A x A	512	NOTE: ABCD REFER TO FRONT END BANDS: A & B - LEFT C & D - RIGHT
6		B x B	B x B	B x B	B x B	512	
7		C x C	C x C	C x C	C x C	512	
8		D x D	D x D	D x D	D x D	512	
9	DUAL SPECTRA } 2 INDEPENDENT BANDS }	A x A	A x A	C x C	C x C	} 2 EA. } 256	} ADD 1+3 } & 2+4
10		B x B	B x B	D x D	D x D		
11	SINGLE SPECTRA } MAX. SENSITIVITY }	A x A	A x A	C x C	C x C	256	
12		B x B	B x B	D x D	D x D	256	
13	DUAL SPECTRA }	A x A	A x A	B x B	B x B	} 2 EA. } 256	
14		C x C	C x C	D x D	D x D		
15		A x A	A x A	D x D	D x D		
16		B x B	B x B	C x C	C x C		
17	POLARIZATION } SPECTRA } QUADRUPLE SPECTRA }	A x A	A x C	C x A	C x C	} 4 EA } 128	
18		B x B	B x D	D x B	D x D		
19		A x A	C x C	B x B	D x D		

BW NO.	B.W.	MAX. F CH ₂	BW NO.	B.W.	MAX. F CH ₂	B.W. NO.	B.W.	MAX. F CH ₂	OVERSAMPLE FACTOR
1	50 MHz	16	5	3.125 MHz	256	8	390.625 KHz	512	2
2	25 "	32	6	1.5625 "	512	9	195.3125 "	512	2
3	12.5 "	64	7	.78125 "	512	10	97.65625 "	512	2
4	6.25 "	128							

MODES OF OPERATION - BANDWIDTHS

TABLE 1

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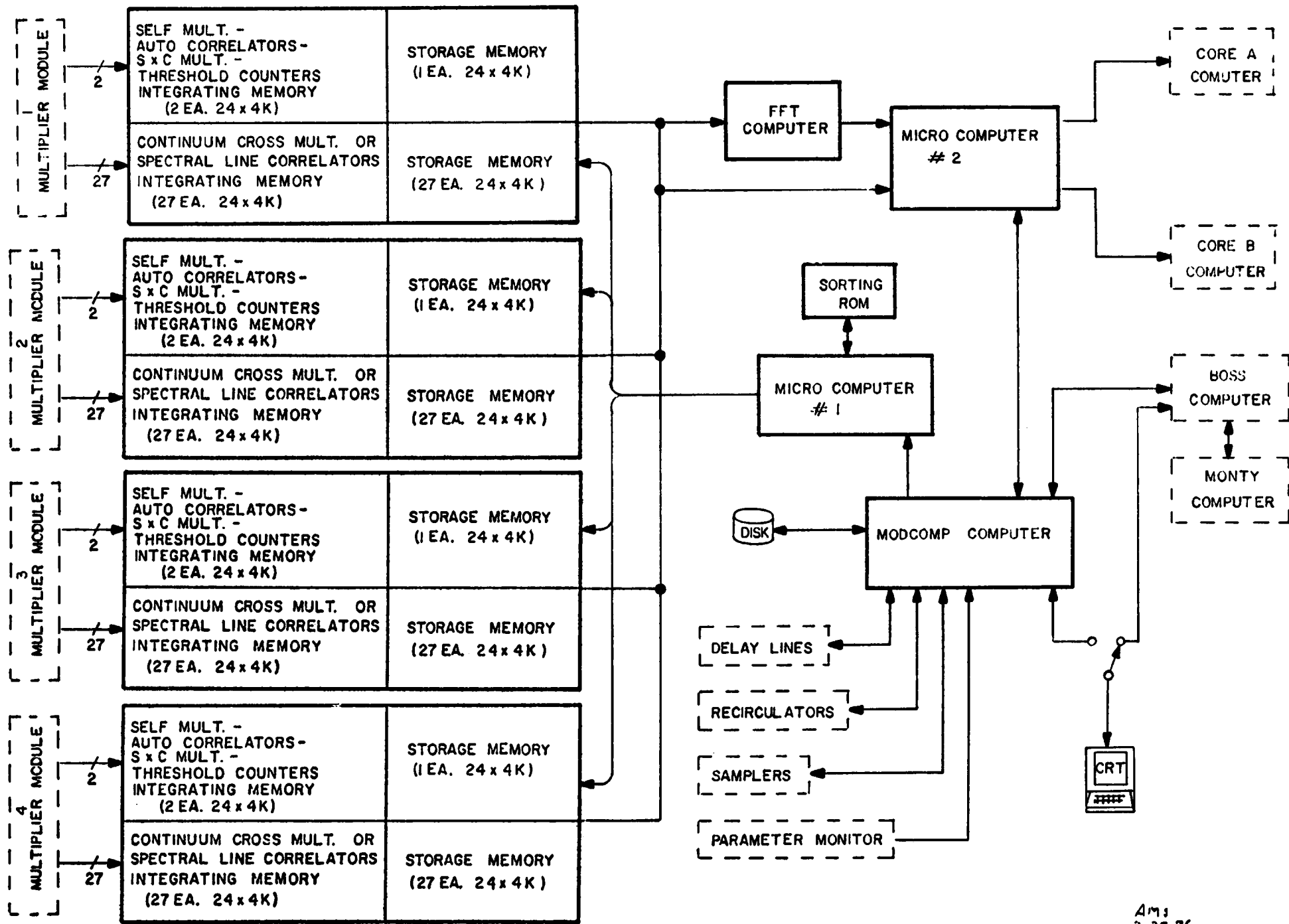
III. DESCRIPTION

Figure 2 is a block diagram of the computer control and processor. Many fine details have not been resolved yet; therefore, the following descriptions of the various blocks are not complete.

A. Modcomp Computer

Figure 3 illustrates a tentative configuration for the Modcomp computer. The computer will be the overall control center and also provide a convenient input-output via the CRT and its keyboard for complete testing of the Delay-Multiplier. Listed below are the computer's tasks as associated with other blocks in the system:

1. Boss synchronous computer
 - a. Every 50 msec receive 108 delay words and disable (standby) flags. Each word consists of 14 bit delay line-delay, 4 bit sampler-delay and 1 bit enable flag.
 - b. At beginning of each observation, receive mode of operation, bandwidth(s), baselines desired.
 - c. Every 50 msec receive miscellaneous data, such as time to end of observation, whether observation is a test or an actual observation, etc.
 - d. Receive coded test messages, to put system through prearranged tests.
 - e. Every 50 msec transmit to Boss computer the data received in a, b and c above as a check.
 - f. Every 50 msec transmit to Boss computer any errors detected and any corrective action taken, such as replacing a defective delay line with a test delay line.
2. Microcomputer 1
 - a. At beginning of observation send coded words to microcomputer indicating mode of operation, integration time and number of recirculations (derived from bandwidth and mode).
 - b. At beginning of observation send baselines desired by synchronous computers.



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VLA DELAY-MULTIPLIER CONTROL SYSTEM
FIGURE 2

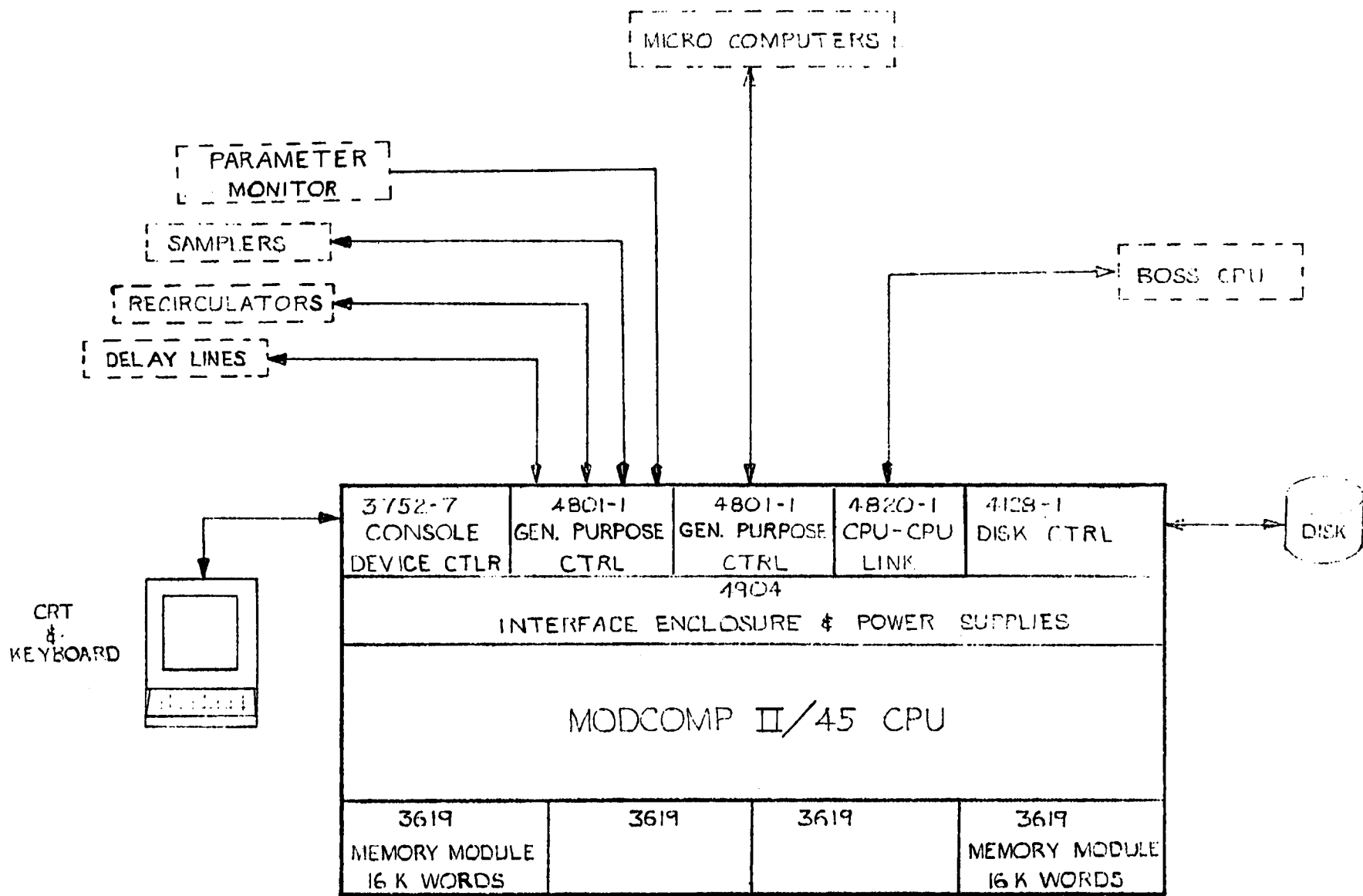


FIGURE 3 MODCOMP COMPUTER

III. (continued)

3. Microcomputer 2

- a. Same data as in 2.a above.
- b. Modcomp is capable of monitoring from micro-computer the raw data and the corrected and FFT'ed data for test purposes and display on CRT screen as desired by operator.

NOTE: After further investigation it may be deemed desirable to have the Modcomp communicate with only microcomputer 2 and allow microcomputer 2 to relay the data to 1.

4. Delay Lines

- a. Modcomp-to-delay lines, every 50 msec, 108 ea. 20 bit words containing delays, multiplexer controls and enable (standby) data.
- b. Delay lines-to-Modcomp, every 50 msec, Go-No Go data indicating results of test delay lines operations. Data words listed in 4.a from previous 50 msec for checking purposes.

5. Recirculators

- a. Modcomp-to-recirculators, at beginning of observation, mode of operation and number of recirculations required (based on bandwidth and mode).

6. Samplers

- a. Modcomp-to-samplers, every 50 msec, 108 ea. 8 bit words containing 4 bits of sampler delay, one bit for "invert" control and two bits for test control.

7. Parameter Monitor

- a. Parameter monitor-to-Modcomp, every 50 msec, 128 (or if needed 256) data words of monitor information. This is a monitor of voltages, currents, clocks, temperatures and air flow.

The original purpose of incorporating a mini-computer in the delay-multiplier system was to have a unit that could completely control the delay lines, recirculators and multipliers and yet be software programmable. However, there is a tendency to put "hardwired" control on the delay-recirculator-multiplier section because of the desire to be

able to check the equipment out prior to the arrival of the computer system. A decision should be made soon as to whether these hardwired components should be a permanent part of the equipment or should be removable test fixtures. One might also consider the possibility of making interface simulators so that the Modcomps of the synchronous computer system could be used for preliminary checkouts prior to the arrival of this computer control system.

B. Memory

The memory accepts the data from the short 14 bit counters of the multipliers. It acts, in combination with adders, as an integrator for the data and as a storage medium until the data can be pre-processed and passed on to the synchronous computers. Figure 4 shows some of the logic detail. Multiplier counter data is dumped every 81.92 μ sec.

The memory input, see Figure 2, is divided into four ports, corresponding to the four multiplier modules. The outputs all tie together to feed one FFT computer. One-half of the memory is an integrator and its data is dumped every dump time into the storage half of the memory.

Input timing for the integrator portion of the memory is as follows, as applied to one module:

Number of cross correlator input lines - 27

Number of bits per word - 12 (multiplier discards the two
LSB's by truncation)

Number of words per line - 104

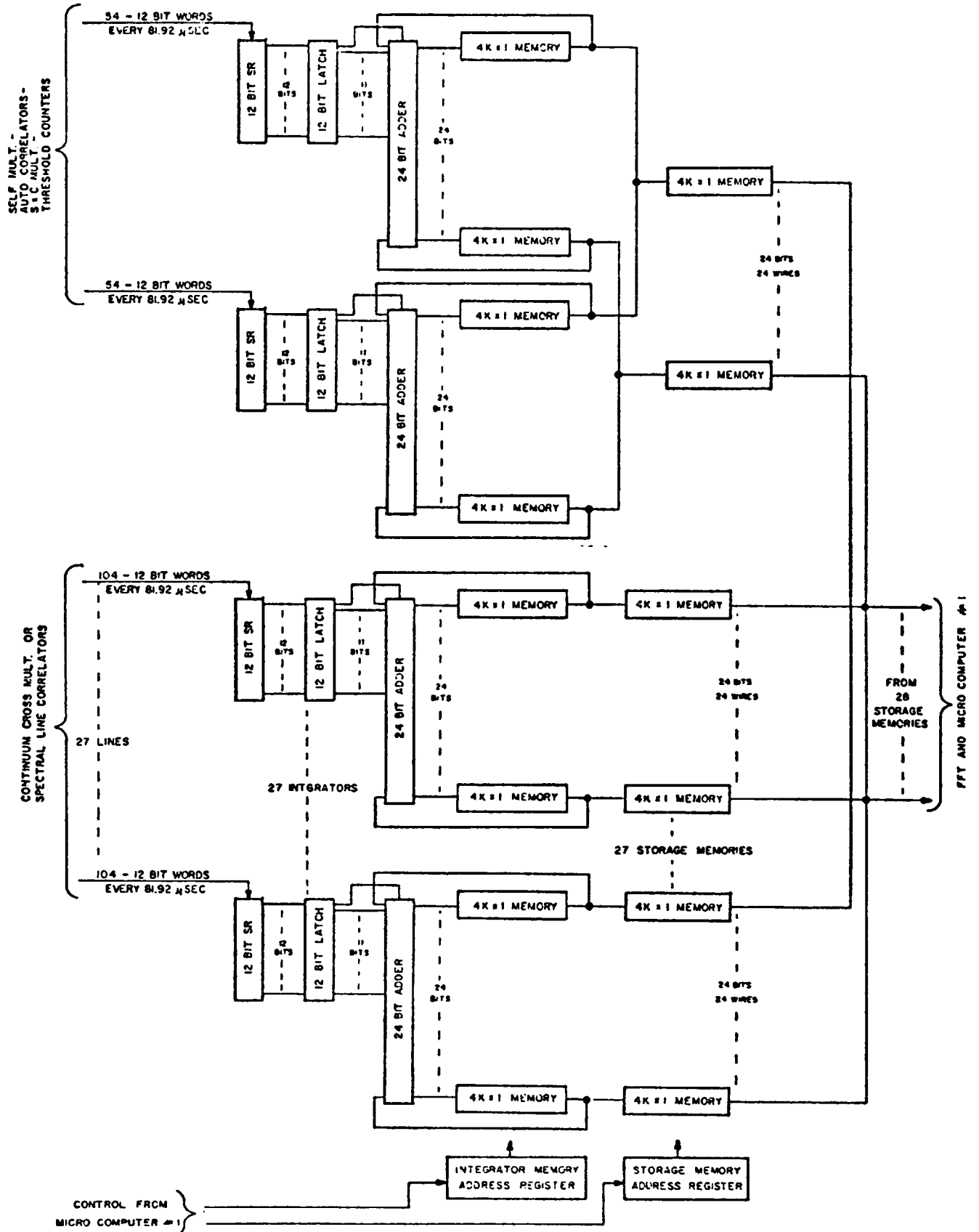
Clock rate - 16.66 ... MHz Period - 60 nsec (clock supplied
by memory system)

Data transfer time per line:

per word - 780 nsec (one clock pulse skipped out of every 13)

per 104 words - 81.12 μ sec (This provides a safety of 80 nsec
time)

In the maximum case there will be 32 recirculations to produce 512 frequency channels. A look at Figure 4, the memory logic diagram, will show that we thus can store $(32)(104) = 3328$ bits per 4Kx1 chip. The remaining 768 storage places in each chip are wasted. This is the best that can be done - allowing a reasonable safety factor - with such small



ONE MODULE OF INTEGRATING AND STORAGE MEMORY
FIGURE 4

recirculations requiring the absorption of so much data in such a short time.

At dump time, the data in the integration portion of memory is transferred to the storage portion of memory. The minimum dump time available is "data invalid time" plus "time to load a recirculator (10,240) once" = $1.603 \dots + .1024 = 1.7057 \dots$ msec. This minimum applies to a sample rate of 100 MHz and increases as the sample rate decreases. At 100 MHz only one circulation is performed, so that each memory chip only contains 104 bits and 1.7057 \dots msec allows plenty of time for transfer from integration to storage memory. As the sample rate decreases, the dump time increases and there is always sufficient time for the transfer.

The words are removed from the storage memory in groups of complete cross correlators and transferred to the FFT computer and if required into microcomputer 2.

There is a similarly operating smaller portion of the memory which handles an additional 108 multipliers per module. These are either self multipliers, autocorrelators, or sine times cosine multipliers depending on the mode. The threshold counters may also be included in this group.

Physically, the memories will be located all in one rack. It will consist of one chassis per memory module plus one chassis for control and output circuitry.

C. Microcomputer 1

Because of the speed requirements, both microcomputers will be bipolar types. Selection has been narrowed down to either the Intel 3000 series (second sourced by Signetics) or the Advanced Micro Devices 2900 series (to be second sourced by Motorola and Raytheon).

Microcomputer 1 with an associated ROM to store sorting information, will control the input, output and operation of the memory unit.

D. FFT Computer

Although a couple of other models are still being considered, the Floating Point Systems Model AP-120B Array Transform Processor is the present leading contender for an FFT computer. In addition to performing the FFT, it will be programmed to subtract V_s , normalize and perform the corrections required on the correlated channels. If still more capability is available - that is, timewise - Barry Clark has indicated he may request that this computer perform still more functions presently left to the synchronous computers.

Physically the FFT and the two microcomputers will occupy one rack.

E. Microcomputer 2

This computer will handle the data transfer from the FFT to the synchronous computers (core A & B). It will also send raw data and FFT processed data to the Modcomp, when requested, for display or testing.

F. Rack Arrangement

Figure 5 illustrates a possible configuration of the equipment. It is felt that this equipment would best be located in the delay-multiplier screen room. However, it is probably possible to locate the FFT computer, microcomputer 2 and Modcomp computer in the computer room. Unless there is a push for the computer room location, it will not be planned that way.

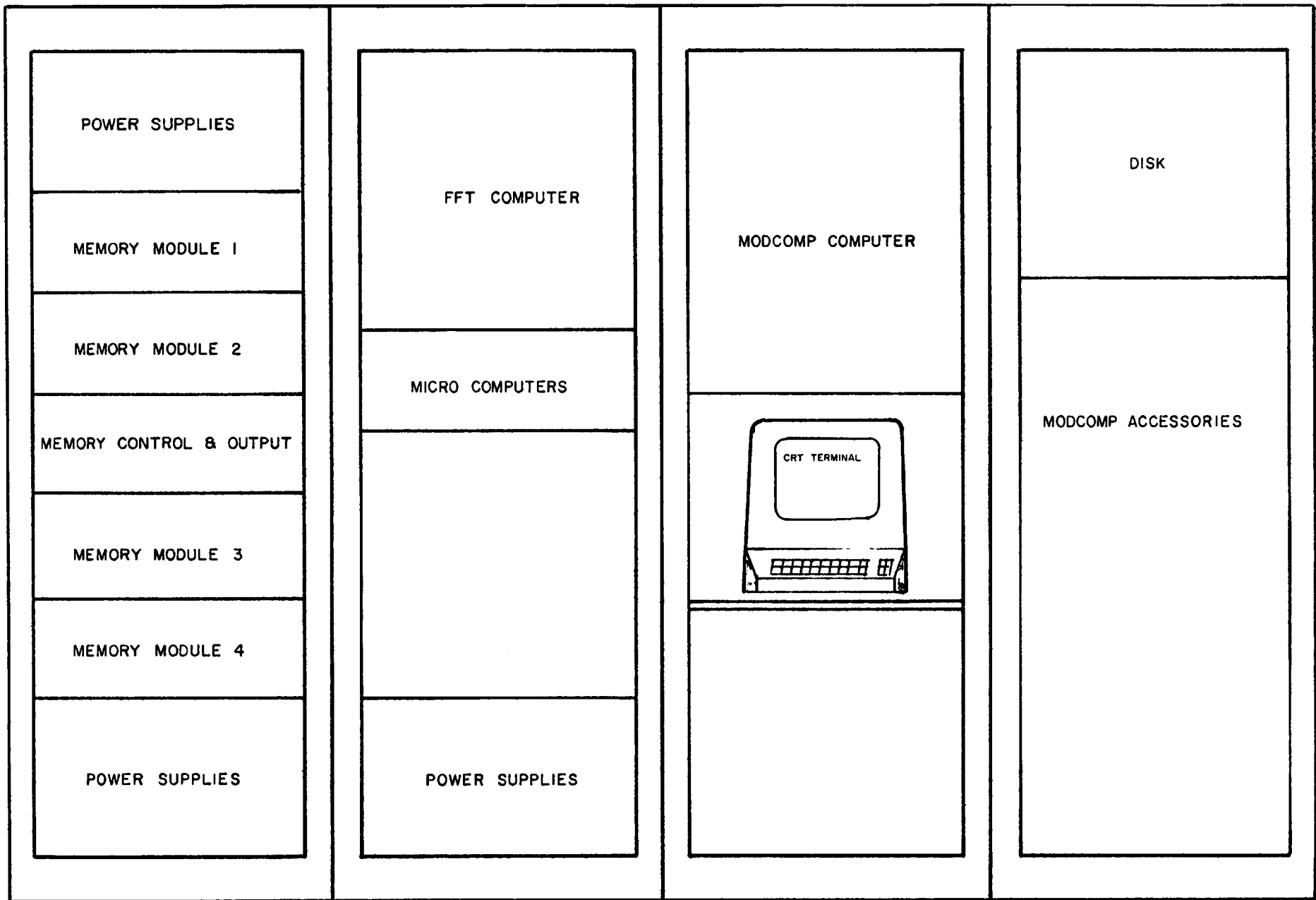
G. Bits & Equations

In a memo, in the process of being written by Larry D'Addario, it is shown that in transferring the data from the multiplier 14 bit counters to the integrator memory, we can discard k of the least significant bits if the data is rounded - where k is:

$$k \leq \frac{1}{2} \log_2 R - 2.42$$

R is the number of multiplications performed to produce the data.

The multipliers will normally produce 8192 multiplications before the counters are dumped. This gives a value of $k = 4.08$. In certain



RACK SPECIFICATIONS :
 4 RACKS REQUIRED
 24" PANEL WIDTH
 70" PANEL HEIGHT
 29" DEPTH

AMS
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MEMORY & COMPUTER CONTROL & PROCESSOR RACK LAYOUT
 FIGURE 5

-13-

narrow band modes, the number R will be reduced to 2048 part of the time to increase efficiency. This (2048) gives a value of $k = 3.08$. Thus a maximum of three bits of the 14 bit multiplier counter can and will be discarded. Two of the bits will be truncated when the data is transmitted to the integrator memory. When the data is added to the previously integrated data from memory, one more bit will be discarded and the result will be rounded at this point.

The memory will be capable of holding a 24 bit word. The two extreme cases will be used to determine the integration time possible and the number of bits to be discarded prior to manipulating the data in the FFT computer - bandwidths of 50 MHz and 1.5625. Also the equation derived in a previous memo by L. D'Addario will be used:

$$\sigma_d = .5407 \sqrt{V_s}$$

where σ_d is the standard deviation of the count obtained from a three level multiplier. V_s = number of samples (or multiplications) to produce the data.

BW = 50 MHz

Max. number of bits required = $(100 \times 10^6 \text{ Hz})(.6 \text{ sec}) = 60 \times 10^6$ counts which requires 27 bits if we assume that the average number coming out of the multiplier is between 1 and 2.

Max. number of bits which may be discarded = $.5407 \sqrt{60 \times 10^6} = 4188$ this requires 12 bits. If we use the standard rule of thumb of saving 3 bits for safety we can discard 9 bits.

From the above we would require $27 - 3$ (bits discarded between counters and memory) = 24 bits per memory word. And, we would require $27 - 9 =$ 18 bits per word to be transferred (after rounding) to the FFT computer. Max. integration time = 600 msec.

BW = 1.5625 MHz:

Max. number of bits required = $(3.125 \times 10^6 \text{ Hz})(19.2 \text{ sec.}) = 60 \times 10^6$ which, as would be expected from the integration time chosen, agrees with the 100 MHz case.

Max. number of bits which may be discarded also will agree with the 100 MHz case.

There is a small difference between the two cases taken above, because their efficiencies are not exactly the same; however, it is lost in the safety factors. An integration time of double the figures given above may be obtained by allowing the memory adders to overflow by one bit. It is believed that this can be done without introducing an error. The FFT computer will process the data in floating point and with sufficient bits in the mantissa so as not to introduce an appreciable error. The resultant transform will then be rounded off to 18 bits or whatever number is desired by B. Clark and transferred to the synchronous computer system.

The following table shows the minimum and maximum integration time available in integers of the 52.083 ... msec VLA cycle time. The actual integration times are approximately 90 to 96% of the times shown. As stated above, the maximum times can be doubled if we allow overflow. The minimum times are due to the speed of the FFT computer. The minimum times can be decreased if we reduce the number of channels per baseline.

TABLE 2

BANDWIDTH	INTEGRATION TIME		MAXIMUM NO. OF FREQ. CH. IN SINGLE SPECTRA MODE
	MIN.	MAX.	
50 MHz	312.5 msec	625 MHz	16
25 MHz	625 msec	1.25 sec	32
12.5 MHz	1.25 sec	2.5 sec	64
6.25 MHz	2.5 sec	5 sec	128
3.125 MHz	5 sec	10 sec	256
1.5625 MHz	10 sec	20 sec	512
.78125 MHz	10 sec	40 sec	512
.390625 MHz	10 sec	20 sec	512 Oversample Factor = 2
.1953125 MHz	10 sec	40 sec	512 "
.09765625 MHz	10 sec	80 sec	512 "

Prior to performing the FFT or, in the case of continuum, passing the data on to the synchronous computers, the FFT computer will perform the following functions on each multiplier data output.

1. Subtract V_s (the number of sampler-multiplications- associated with the integration).
2. Divide by V_s to normalize the data.
3. Perform a three level correction equivalent to the Van Vleck two level correction. This will be a function of the type:

$$\hat{\rho}_{ij} = (\alpha C_{ij}'' + \beta C_{ij}''^3) [1 + \gamma(C_{ii}'' + C_{jj}'') + \delta(C_{ii}''^2 + C_{jj}''^2)]$$

See D'Addario's memo to appear shortly. The exact form and constants are to be worked out by John Granlund.

If there is arithmetic capability (that is, timewise) and B. Clark or others decide it, the FFT computer may be programmed to do additional corrections or calibrations or testing; although, where possible, the testing will be left to the Modcomp computer.

IV. PRICING, SCHEDULING & MANPOWER

Because this portion of the delay multiplier system was the last to be studied, the pricing and scheduling are fairly rough approximations:

A. Block Pricing

	<u>Price</u>	<u>Order Date</u>
1. Modcomp Computer	\$65,000	June 1, 1976
2. FFT Computer Floating Point Systems	45,000	June 1, 1976
3. Computer Interfaces NRAO Built	10,000	July 1976 thru November 1976
4. Microcomputer 1 with Sorting ROM	9,000	August 1976 thru October 1976
5. Microcomputer 2	8,000	August 1976 thru October 1976
6. Memory	106,500	April 1976 thru September 1976* See note below
7. Misc. - Racks, displays power supplies, cables, spares, non-recurring charges, etc.	30,000	April 1976 thru January 1977
	<hr/>	
	TOTAL	\$273,500

This figure should be reasonably accurate unless considerably more memory is required for the FFT computer.

*NOTE: Item 6 will be built with only one-quarter of the memory boards installed. Thus we will spend approximately \$50,000 less in 1976.

B. Test Equipment Pricing

This test equipment, of course, would also be useful for future projects:

	<u>Price</u>	<u>Order Date</u>
1. Microcomputer Assembler & Checkout Equipment	\$9,500	August 1976 thru September 1976
2. ROM Programming and Simulating Equipment	2,500	September 1976
3. Oscilloscope 100 MHz	1,995	May 1976
4. Logic State Analyzer	6,800	May 1976
5. Miscellaneous Accessories, Probes, etc.	1,000	June 1976
	<hr/>	
TOTAL	\$21,795	

C. Detail Pricing (see IV.A.)

1. Modcomp Computer
See Page 19.

<u>ITEM</u>	<u>QTY</u>	<u>MODEL</u>	<u>PRE-REQ.</u>	<u>DESCRIPTION</u>	<u>UNIT PRICE</u>	<u>SUBTOTAL</u>	<u>REF. P.</u>
1	1	C001	(375	Std. 19" Cabinet	\$ 950	\$ 950	27
2	1	0210-x	(3752-x)	30' Cable for CRT	50	50	27
3	1	II/45	(0001)	CPU, 4-port Memory, W/16K wd Memory & 375x cons. dev. ctr.	16,500	16,500	5
4	3	3619	(II/45)	Memory Modules, 4-port; 16K wds each	6,500	19,500	8
5	1	3752-7	(4904)	Console device ctr.; (-7 = 9600 baud)	400	400	5,8
6	1	4128-1	(490x or 3708)	Disk controller & one disk drive, moving- head, 5 M-byte capac.	14,000	14,000	13
7	1	4610	(3752-x)	Console CRT & keyboard	2,500	2,500	12
8	2	4801-1	(490x)	General purpose ctr.	600	1,200	11
9	1	4820	(490x or 3708)	CPU-CPU Link	4,000	4,000	24
10	1	4904	(II/xx & 3752-x)	Interface (= enclosure with power supply) for 4 device controllers & console device controller	1,200	1,200	11
11				Miscellaneous items	4,200	<u>4,200</u>	
TOTAL						\$65,000	

Explanations:

Ref. p. denotes page where item is discussed in 1 July 1975 ModComp price list booklet.

Item 5 probably can be deleted, since a 375x type controller is supposed to come with the CPU.

Item 7 (console CRT) is assumed to be ADDS or Beehive make.

Item 9 is rated at 100K words/sec. No speed limitation is cited for the interface in item 10. We assume item 10 implies an internal Direct Memory Processor (DMP) either within item 10 or within item 3. If necessary to add a DMP to the list, the following are available (ref. p.8).

Model 3704, DMP for automatic block transfers to/from 8 peripheral devices concurrently; transfer rate 330K wd/sec; \$1,500

Model 3708, External DMP for automatic block transfers to/from 4 peripheral devices concurrently; transfer rates 833K wd/sec (input), 625K wd/sec (output); includes enclosure and power supply, locations for 6 std. ctrs.; \$4,000.

2. FFT Computer

Floating Point Systems Model-120B
with power supply, 8K memory and
interface \$ 40,000
Allow for additional memory 5,000
TOTAL...\$ 45,000

3. Computer Interfaces NRAO built.

Interfaces: Modcomp-to-delay lines,
recirculators, samplers, parameter
monitor, microcomputer.

FFT computer-to-microcomputers
and Core A & B synchronous
computers.

Ballpark Guess\$ 10,000

4. Microcomputer 1

Microcomputer \$ 4,000
RAM Memory 3,000
ROM Memory 2,000
TOTAL...\$ 9,000

5. Microcomputer 2

Microcomputer \$ 4,000
RAM Memory 3,000
ROM Memory 1,000
TOTAL...\$ 8,000

6. Memory and associated logic	
5500 ea. 4Kx1 memory chips	
@ \$16.00 each	\$88,000
Chassis, connectors, bus bars, etc.	2,000
Logic with wirewrap boards -	
648 adders, etc.	6,500
Rack hardware, cables, bus bars,	
etc.	2,000
Printed circuit boards, assembly,	
test	<u>8,000</u>
TOTAL....	\$106,500

7. Miscellaneous

Racks, displays, power supplies,	
cables, spares, non-recurring	
charges, etc.	
Ballpark Guess	\$ 30,000

D. Scheduling

No detail scheduling has been done yet. One will be put into the Pert Chart System within a month or two. An attempt will be made to complete the system by September 1977, at which time it will be shipped to the VLA site to be checked out with the delay-multiplier, sampler and synchronous computer systems so that the whole system can be operating by January 1978.

If January 1978 is not a realistic date for the IF section, samplers, synchronous and asynchronous computers, etc. to be ready to do spectral line observations, we should consider whether the date should be relaxed.

E. Personnel

- 1 Engineer - full-time - Arthur Shalloway
- 1 Technical Specialist - full-time - Gene Runion
- 1 Programmer - one-half time - George Conant
- 1 Technician - part-time construction - -----
- 1 Student - part-time

F. Support

It is assumed the project will receive full support from purchasing and a draftsman one-half to three-quarter time throughout the project.