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SUBJECT: Monthly Report for November 1976  
VLA Optical Processor  
Contract: VLA-215

#### 1.0 SUMMARY

November activity consisted of a consolidation of Task 2 efforts wherein a system configuration recommendation was formulated, a limited performance experimental breadboard processor was used to demonstrate the VLA data processing concept, and system modeling and performance analysis was continued.

Based upon performance estimates, and the need to limit developmental costs, a VLA optical processor system consisting of a pre-filter, CRT/film optical recorder, beyond-the-lens-input optical processing channel, and a dual output which allows immediate direct viewing of the sky map as well as a rapid conversion to an electronic signal using a linear push-broom detector array is recommended. A detailed review of the recommended design configuration will be made to NRAO representatives in early December [1]. Data on a lens system [2] suited to the before-the-lens-input configuration (rather than after) of potentially excellent quality, but comparatively high cost was received from one of several optics manufacturers queried on Fourier lenses.

Our breadboard processing experiments were successfully completed and examples of results have been formulated [3]. The

breadboard processing experiment consisted of using computer compatible tapes of complex visibility data simulating a single star as seen by the VLA. This data was then pre-filtered for conversion to a real signal on a carrier frequency, recorded on film with a line scan CRT recorder, optically processed using a beyond-the-lens processor configuration with a reference wave which is switched between the 0 and  $\pi$  relative phase states, detected with a Reticon detector array and then post-filtered to give the desired sky map consisting of a single star. Results were consistent with the quality of the experimental facility being used and served to demonstrate the feasibility of the processing concept.

A system model was formulated which included noise and phase error sources [1], and input signal encoding was further analyzed [4].

Task 2 efforts are now completed. The remaining effort in the program consists of preparing a detailed review of the proposed design and its operating features, performance estimates, design parameter specification and error budget, and system cost estimates. This remaining effort will comprise the remaining Task 3 of the program.

		PROCESSOR			2000
		OF DATA			1900
		PRINT			1800
	AT N/A/O				1700
	RM 158			AT N/A/O	1600

