23 June 1976

MEMORANDUM TO: I. Cindrich

FROM: R. Dallaire

SUBJECT: Recommendation for the Purchase of the Fairchild CCD as an Image Sensor

After a brief review of several image sensor technologies, the Fairchild CCD is recommended for the image sensor for the VLA Optical Processor Program. The selection was primarily based on the superior sevsitivity of the device without sacrificing any other critical parameters.

Three families of image sensing devices were surveyed: CCD, photo-diode, and vidicon. The vidicon was rejected early due to its limited dynamic range. A comparison of the Fairchild CCD's and Reticon's photo-diode array is shown in Table 1. The comparisons were made more difficult by either typical (rather than min/max) specs or non-existent data. The Reticon device is very poorly specified and such things as crosstalk and MTF have not been tested.

The need for cooling was a concern prior to the survey but on examination of the specs and discussions with the technical aides at Fairchild and Reticon has shown that cooling may not be required. Cooling does not significantly reduce the thermal noise of the devices (the limiting factor for a wide dynamic range). Cooling does reduce the dark current but this affect is not noticed until long integration times are required (on the order of 10 ms). The integration time should be less than 1 ms for the Fairchild device (the integration time would be 80 times longer for the Reticon device).

Table 1 CCD/Photodiode Comparison

Item	Fairchild CCD	Reticon Photodiode
Dynamic Range		
Full Scale/fixed pattern ratio	50/1	200/1
Full Scale/RMS noise ratio	1730/1	2000/1*
Minimum Sensitivity @ 620nm	2.14μJ/M^2	170μJ/M^2
MTF (at full resolution)	36%	10%*
Crosstalk (nearest neighbor)	6%	2%**
Reliability	Typical IC	Typical IC
Cooling	Not needed	Not needed$^+$
Readout Electronics	Avail.	Avail.
Cell Spacing	13μ	15μ
Cell/Cell Gain Variation	±6%	±12%
Cost^{++}(Incl. readout elec.)	$1450	$3800
Availability	2-4 weeks	On shelf

* Dissimilar tests, comparisons not accurate.

** For 64 element array

$^+$ Not needed for usual integration times but due to lower sensitivity Reticon device will need a longer integration time.

$^{++}$ For Reticon RL-1872, Fairchild CCD121

Another factor influencing the decision was the readout method. The Reticon devices shift one cell at a time to an output bus while the CCD devices shift all cells at one time. to a parallel analog shift register. The integration takes place at all other times. If the image is scanned in a broom fashion, the Reticon device will have a phase shift (or time lag) between the top cell and the bottom cell. The phase shift also increases the complexity of timing when several devices are placed in series for scanning out a larger image.

Fairchild has a suggested method of serializing the image sensors. The method is sketched in Figure 1. A beam splitter is used to send the image to staggered CCD arrays. This method sacrifices half of the light intensity but avoids the high cost of custom hybrid circuits. Another method would allow staggered sensors without the beam splitter and require the computer to re-arrange the digitized output records.

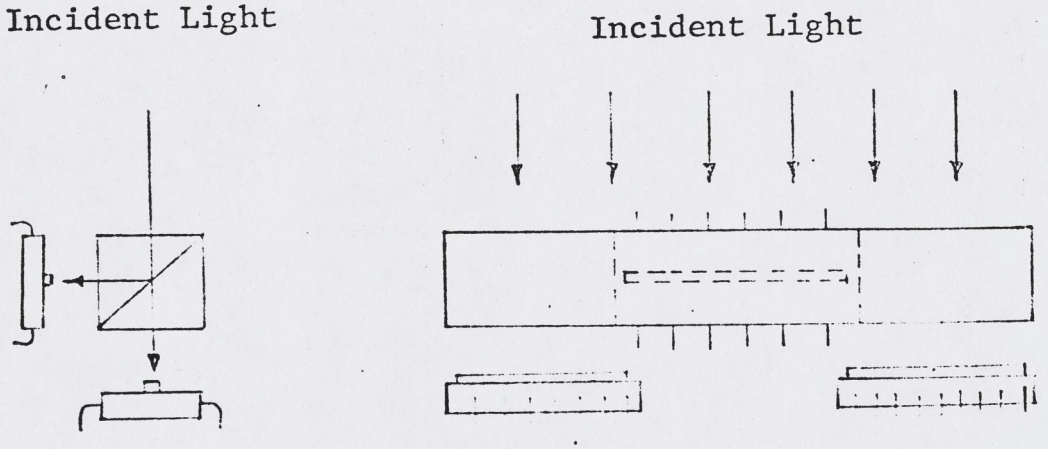

Figure 1. Using a beam splitter to serialize image sensor arrays (two views)

Since both CCD's and photo-diode arrays have large fixed patterns and element-to-element variations, computer processing will be required to achieve the full potential of the sensors. Although not mandatory for the VLA study, computer processing of scanned patterns will simplify the measurements and provide an impressive image display on the Ramtek. The most economical method for sending the data to the computer would require a 12 bit A/D (4096 quantization levels), some buffer and timing circuitry, and cabling to the PDP-11/10 computer. The computer has the hardware for interfacing with the rotary platform and DP/OC. Modified DP/OC software would be used for the data acquisition. The hardware cost would be about $300, the design and fabrication about 2 weeks and the programming (for acquisition, fixed pattern correction, and display) about 2 additional weeks. The computer processing will save many weeks of data reduction and the elimination of the sample and hold plus clocking circuitry that would be required to make the analog measurements on a DVM.

There are two feasible CCD sensors available: a 1024 element (CC0131) and a 1728 element (CCD121). The trade off is sensitivity for resolution. The CCD131 has only half of the sensitivity as the CCD121 but has a square aperature (13μ × 13μ) rather than a rectangular aperature (17μ × 13μ). The enlongated dimention is in the direction of the mechanical scan and will reduce the resolution in a direction which already suffers heavily due to the motion through the cells during the integration. Better resolution could be obtained through a step and integrate approach but would require a longer scan time while waiting for each step to be completed.

Since the sensitivity of the Fairchild devices is good, thought should be given to purchasing the CCD 121 (1024 elements).

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