Correlator Discussion Topics (Aug. 27-28, 2001)

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1. Interference

-L-band: looks like 8-bit sampling required…still getting data.

-other bands: 3-bits ok…still getting more data.

-sensitivity loss: need 2 bits for noise…other bits for dynamic range (ATA PDR).

2. Architecture

-poly-phase FIR/FFT with sample rate conversion for sub-band overlap sensitivity loss elimination with even more anti-aliasing: include at no extra cost, no schedule impact, no flexibility impact by "combining" the radar-mode filter and "clear sub-band" filter into one big chip (~$600) c/w data highways. Worry about implementation later. Concern: speed of multipliers in Virtex-2 chip may require ping-pong multiplication to get 250 MHz clock. Do NOT want to change to 125 MHz system speed/design just to support this.

-sample rate rate coversion: impacts on sampler/demultiplexer design and sample rates? 1:15 demux, 256 may be required?…or 15 x 250 → 16 x 250 to not impact FOTS frequencies results in 1.875 GHz bandwidth or 15 GHz total; thus, 1 GHz total bandwidth is lost. With 15 x 256, total BW is 15.36 GHz or 640 MHz lost.

3. Other performance/functional refinements?

4. Sub-band multi-beaming (and phased-sub-band sub-sample delay tracking)

-3 methods: **#1** +/-0.5 sample with phase tracking; **#2** +/-0.5 sample with FIR tap changes to track delay; **#3** +/-0.5 sample at high rate with phase tracking (same as done already but only need to do sub-band beam offset from baseband beam). #3 method: no cost now, needs 36 k deep (x64) buffer for 10,000 km baseline with 0.25 degree beam offset at 30° elevation angle (i.e. ~70 μsec). Use on-chip RAM!

-sub-band phase offsets: can only include in phase model sent to correlator board every 10 msec. Ok if $d(\tau_b-\tau_s)/dt$ small – should be, but need to quantify.

-how important to build into the a) h/w design; b) s/w/system design?

-method #2 required for sub-sample delay tracking with phased-array sub-bands.

5. Pulsar processing

-new refinements/desires?

6. **De-scoping options?**

   -anything to decide now?

7. **Software**

   -process: how/are we involved in architecture development? Is VCI developed as part of overall architecture?

   -correlator config/GUI builder? Demonstration development under way at DRAO as part of in-house "test project". Should this evolve to something more concrete or not?

   -need meeting devoted to software?

   -how much functionality in initial design? New "mode"/observing paradigm required/needed? Involvement?

8. **MCB mezzanine card:**

   -cheap, proprietary board?

   -PPMC/industry standard I/F and FF?

   -home-brew (e.g. USB microcontroller?)

   -same across all array systems?

9. **Transition plan.**

   -problems with simultaneous new/old correlator operation?

   -can LO shift (new), and LO phase rotation (old) be done simultaneously?

   -Fibre-optic receiver config (Jackson).

10. **Design documentation standards**

    -We will have a) func/perf. Spec doc; b) "User Manual"; c) "Design Manual". Document numbering according to WBS. Documentation standards?

11. **Recirculation**

    -understanding side-effects: dump-time skew.

    -correlation "holdoff" signal after each dump. (i.e. clear shift regs, let fill with new data before starting correlation). Should easily fit into current design...needed to eliminate "data valid trickle" systematic effect.

    -2 BBs/sampled data streams limits (memory/cost).

-is scheme for recirculating the correct one? (I think so: robust, simple, DUMPTRIG driven).

-corr. chip data valid counters: 1 at center, 1 at edge of every 128-lag correlator…fits into LTA nicely for 1000 phase/time bins. OK?

12. Coarse Delay Module

-design for 300 km with SDPSRAM? Simple design, but costly (but, within budget).

-design for 10,000 km up front with SDRAM? More complex design but certainly cheaper for >300 km. Probably doable (but, input clock not the same as output so ping-ponging more complicated). Should be able to use on-chip buffers.

13. One LTA controller per correlator chip? (~$900/BB)

-one for every 4 chips is *required* for recirculation.

-one per chip permits dual clock design.

-one per chip: performance for pulsar phase binning.

-FPDP design seem ok?

14. Phasing issues

-design for 40 or 48 station?

-need 8-bit phasing capability? If so, max sub-band bandwidth will be 64 MHz with no increase in current connectivity estimate. *Depends on how the 8-bit data is transported after FIR filtering.*

-look at each Phasing Board to see if we can phase-up a sub-band pair rather than just 1 sub-band? Cost? ½ phasing boards required, or more phased bandwidth for slight increase in cost. Too many input signals?

-useful to have multi-bit output (of PB) before requantization to allow >48-station expansion? (just throw in…no significant cost [one connector]).

-conversion to VLBI standard frequencies (from 250 MHz) **may** be all digital…DSP tricks.

15. Data statistics and w.b. autocorrelation

-**EXACTLY** what statistics are required? Mean, mean-squared, + state counts?

-how many wideband autocorrelation spectral points required? Don't want to drive correlator chip design (i.e. additional interconnects). Do w.b. autocorr in FPGA instead?

16. Correlator installation

-possible parallelization of system integration and test in Penticton with installation at VLA to speed up delivery. Include in project plan/delivery schedule at this point?

-note battery plant is 716 lbs/ft^2.

-cooling, rack power/crate density (too conservative?), procedures? Other issues?

17. FIR filters

-probably ~500 taps (4-bit) or 100 taps (3-bit) is affordable in FPGA. Ok? (loss curves). Using FPGAs enables a lot of versatility, minimum risk etc.

-Ray Escoffier reports excessive power dissipation due to bits flipping rapidly in the adder tree...use DC offset that eventually cancels out to mitigate.

18. Management issues

-would like clear statement of what reporting requirements, dates etc. are. (goals/justification?)

-other?

19. 2 GHz analog passband ripple/ampl slope (conversation with J. Webber)

-sensitivity losses due to uniform distribution of quantization noise. Max sensitivity variation/slope: issue for I/F designers (not correlator issue...except as it affects the FIR design). Specification required.?

20. Walsh switching

-still in antenna design plans (take out just after initial sampler)?

-no effect on correlator/integration time?

21. Noise diode switching synchronization: antenna→correlator

-Identified in chapt. 8, Table 8-5.

22. Ways of speeding up correlator delivery:

-more money, more engineers (parallel development), more cost for corr chip NRE.

23. Straw-man (future) upgrade plan (information only).

-architecture supports future upgrade for more spectral channels, recirculation, phase binning if required.
-keep all infrastructure...just replace Baseline Board.