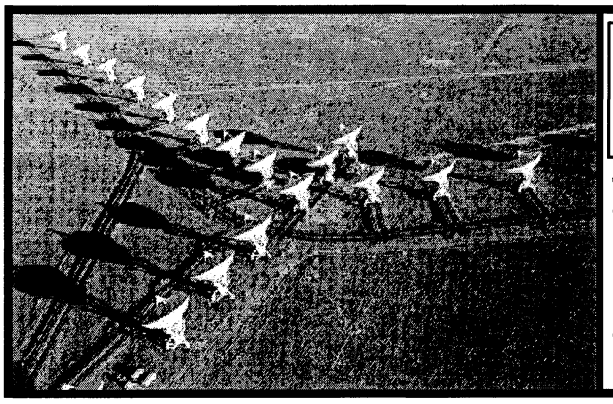

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Expanded Very Large Array

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L352 Round Trip Phase Monitor Module

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Change Record

Revision	Date	Author	Sections Affected	Remarks
1.1	6/08/04	J. Abdullah	5.5	
1.2	8/05/04	J. Abdullah	5.2	Added access information for telnet
1.3	11/22/04	T. Baldwin	5.5.6	Changed output description
			8	Changed GPIO description
1.4	9/23/05	T. Baldwin	1.1	Changed functional description

TABLE OF CONTENTS

1 FUNCTIONAL DESCRIPTION

1.1 Brief Functional Description

The purpose of the Round Trip Phase Monitor (RTPM) is to monitor any phase shift in the 512 MHz signal sent through the optical fiber from the central electronic racks to the antenna. One-half of the round-trip phase change is assumed to equal the phase change from the central electronic racks to the antenna.

General Round-Trip Signal Description:

The L353 LO transmitter module transmits a 512MHz LO optical signal via optical fiber to an antenna. Ninety-five percent of the optical power is returned to the L353 via a second fiber. The return optical power is received and converted to electrical power and used as the RF input to the L352 Round-Trip Phase Measurement System.

General L352 Module Description:

The functional purpose of the L352 is to measure the LO phase change to an antenna. The measurement is accomplished by first comparing the return LO signal from the antenna with a master LO signal that is purposely offset. The offset of the two LO signals is the result of this comparison from a mixer process. The offset is 128Hz and has the same phase attributes as the returned LO signal.

Second, the offset 128Hz signal is multiplied and integrated with a reference 128Hz to generate the sine and cosine coefficients of the Trigonometric Fourier Series.

Third, the L352 MIB calculates relative phase using the coefficients and the C language arctan2 library function.

Detailed L352 Module Description:

The return 512MHz from the L352 is amplified and phase-locked to cleanup noise and to provide a constant-power signal. The output of the PLL is mixed with a 512.00128 MHz reference signal generated in the L351 Master Offset Generator. The resulting 128Hz signal is then passed through a low-pass active filter and converted to a square-wave signal with a comparator. The resulting 128Hz has the same phase shift as the return 512 MHz signal. This 128Hz signal is referred to as the Round-Trip 128Hz, or RT128.

A leading edge of Ref128 starts two counters that are sequenced to produce two triangle staircase functions 90° out of phase (as is sine and cosine). The digital staircase functions are used to recall memory locations in RAM that represent a hexadecimal value for sine. Only a quarter-wave of the sine function is stored in RAM so that time-sharing and multiplexing must be used to convert the staircase functions to sine and cosine functions. The RAM outputs (digital sine and cosine representations of Ref128) are then de-multiplexed and resynchronized.

The sine and cosine functions are multiplied with the RT128 using a one-bit multiplier, implemented with multiplexers with a two-compliment as one input.

The result of the multiplication is accumulated for one second at a clock rate of 512kHz. This is the integration required to produce the sine and cosine coefficients of the Fourier Series. The results are buffered in flip-flops for a one-second period. This gives the MIB ample time to retrieve the data via the GPIO bus.

The circuit board also contains several monitor points such as the VCO tune voltage, Lock indication, voltages, and temperature, all of which is sent to the MIB via the SPI bus.

Trigonometry Description:
The trigonometric Fourier series using Euler's identity:

$$f(t) = a_0 + \sum (a_n \cos(n\omega_0 t) + b_n \sin(n\omega_0 t))$$

where the coefficients of sine and cosine are

$$a_n = \frac{2}{T}\int_{-T/2}^{T/2} f(t)\cos(n\omega_0 t)dt$$

and

$$b_n = \frac{2}{T}\int_{-T/2}^{T/2} f(t)\sin(n\omega_0 t)dt$$

The MIB can then calculate phase:
Phase is the arctangent of the quotient of the two coefficients.

$$\varphi_n = -\tan^{-1}\left(b_n / a_n\right)$$

2 PERFORMANCE SPECIFICATIONS

2.1 RF Specifications
2.2

Item	Specification	Notes
Input Frequency	512,000,000 Hz (512MHz+) 512,000,128 Hz (512MHz LO) 128 Hz (LVDS digital reference) 5.12 MHz (LVDS digital clock)	
Input power level	-3 dBm - 512MHz and 512MHz+	

3 PHYSICAL SPECIFICATIONS

3.1 Temperature

The *L352 Round Trip Phase Monitor* is housed in a RFI sealed module. This module is further housed in an RFI sealed rack. The rack is forced-air cooled from the Central Electronics Room HVAC system. The *L352* module will operate within the range of 18°C to 22°C (64°F – 72°F) and not vary more than ±1°C in any given 24 hour period. The temperature stability of the *L352* is important for maintaining both short-term and long-term phase stability.

Temperature Specifications

Normal Operating temperature range:	20° ±2°C	68° ±4°F
Maximum operating temperature range:	10° to 30°C	50° to 86°F
Maximum variation in 24 hour period:	±1°C	±2°F
Maximum variation in 30 minute period:	±0.25°C	±0.5°F
Maximum critical temperature:	35°C	95°F

3.2 Other Environmental Specifications

The *L352* is designed to meet all specifications at an elevation of 12,000 feet (3,600 meters) above sea level (ASL) and over a humidity range of 0 - 95%. Typically, the converters will be operating at 7,200 feet (2200 meters) ASL in a relatively dry environment of approximately 10-35% humidity.

3.3 Module Physical Specifications

The circuitry shall be contained within an RFI tight module. The RFI requirements are in NRAO ????. Table 3.3 contains the physical specifications for the Offset Generator.

Table 3.3

Item	Requirement	Notes
Weight	15 lbs max	
Module size	NRAO standard 2 wide	see

4 POWER REQUIREMENTS

4.1 Input Power Requirements

The External Power Requirements are shown in Table 4.1.1. The power supply must be battery backed up.

Table 4.1.1

Voltage	Current	Notes
+6.5V		
+16.5V		

The internal power requirements are shown in Table 4.1.2.

Table 4.1.2

Voltage volts	Current amps	Notes
+5		To power the MIB
+5		
3.3		
1.5		

Each input supply shall be filtered with ??? feed thru capacitors.

4.2 Power Dissipation

The power dissipation of the module shall not exceed 10 watts.

4.3 Voltage Monitoring

All internally generated voltages are monitored via the monitor and control system (MIB).

5 INTERFACES (MONITOR & CONTROL)

Interface Control Document (ICD)

5.1 General Monitor/Control Interface

The L352 Round Trip Phase Monitor communicates to the Monitor/Control system through an NRAO supplied Module Interface Board (MIB) that is mounted inside the module housing. The MIB communicates with the Monitor/Control system via a fiber optic Ethernet link, and to the RTPM through a digital I/O bus and synchronous serial (SPI) bus. Basically, the MIB gathers all the RTPM monitor data, calculates the arctan of the results and issues commands to the RTPM. The monitor and command requirements of the RTPM are fairly low.

5.2 Access the MIB control module via telnet.

Within the AOC network access to the MIB control monitor can be achieved by a telnet to the following address: **evla-mib-XX** where XX is the last two digits of the MIB MAC address which can be found on the MIB optical transceiver.

For example:
L352 Module#001 has a MIB with a MAC address of 00-0C-F1-B6-9D-3D so, to access the module you would use the following DOS command: **telnet evla-mib-3d**

5.3 Summary of Monitor and Command data

Commands. The only commands required to the RTPM are the command words to control the ADC to monitor the analog monitor points.

These digital commands are typically changed only during observing source changes, which can be tens of minutes to hours between command changes.

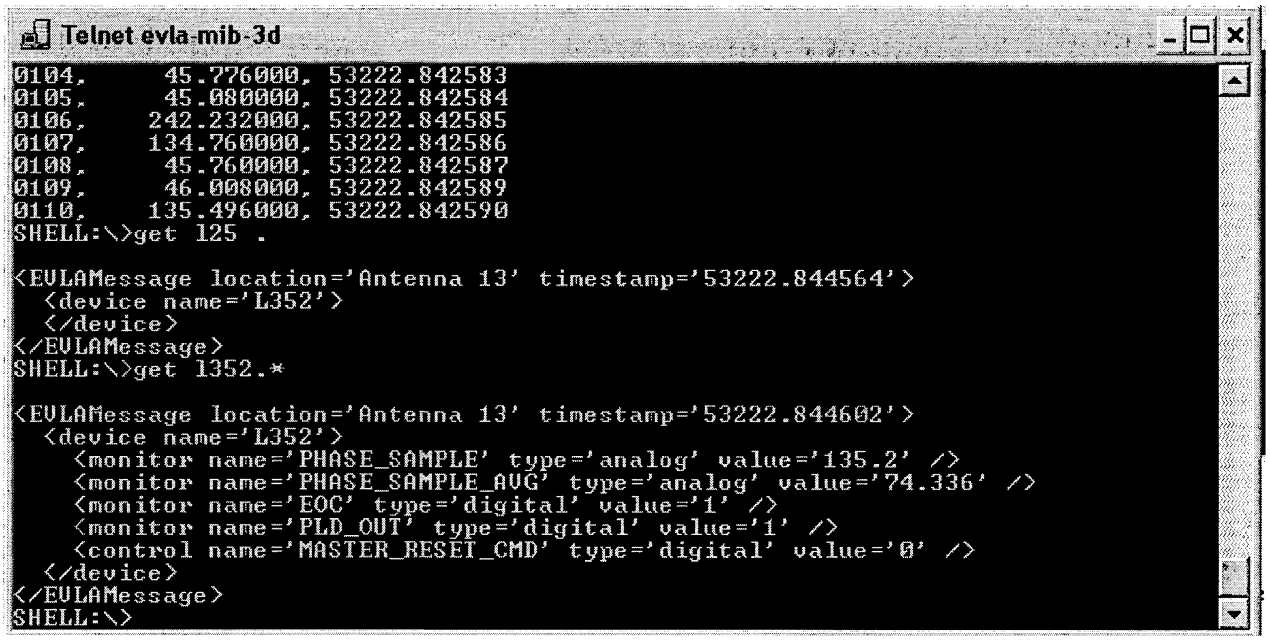
The commands **Set** and **Get** allow user access to the L352 board via the MIB. Current software allows the display of the last 1000 phase points taken by the MIB by using the command **l352_dump**. Other commands will display information about the PLD or temperature data.

For example:
After logging in to the L352 module, the command **l352_dump** will display the following information.

- Point Number
- Instantaneous phase difference
- Timestamp

The command **get l352.*** will display information:

- Reset Status
- Phase Lock Detect
- Phase average
- Antenna #
- Time Stamp



Finally, a soft reset can be performed on the module by using the following command '**set l352.MASTER_RESET_CMD=1**'. Following this, the master reset MR will be momentarily toggled.

Digital Monitor. There are 3 digital monitor points the Phase, PLL Lock and the Temperature. No commands words are required to access these points, they are simply read through the SPI bus and general purpose I/O connector.

Analog Monitor. There are 6 analog monitor points, which are converted to digital and transferred to the MIB via the SPI bus. The analog monitor points in the RTPM are:

1. VCO Tune Voltage.
2. True power

3. DC onboard power supplies voltages, monitoring the +5v(MIB), +5v, +3.3v, and +1.5v internal voltage regulators.

Table 53.1 Monitor Points for the L352 Module

Name:	+5.0_reg(MIB)	+5.0_reg	+3.3_reg	+1.5v_reg
Function Number:				
Control Register Address:	U2 - 0x0B	U1 - 0x0F	U1 - 0x0F	U1 - 0x0F
Chip Select:				
Memory Map:				
Source:	A/D #2 – Vin2	ADC #1 – Vin2	ADC #1 – Vin3	ADC #1 – Vin4
Description:	Regulated board power	Regulated board power	Regulated board power	Regulated board power
Units:	Volts dc	Volts dc	Volts dc	Volts dc
Nominal Scale:				
Number of Bits:	12 bits	12 bits	12 bits	12 bits
A/D Scale:	+/- 10.0 Vdc, 4.88 mV bit	+/- 10.0 Vdc, 4.88 mV bit	+/- 10.0 Vdc, 4.88 mV bit	+/- 10.0 Vdc, 4.88 mV bit
Nominal:	16.5 V	15.0 V	12.0 V	6.5 V
Alarm Range not:	4.5 to 5.5 V	4.5 to 5.5 V	3 to 3.6 V	1 to 2 V
Sample Rate:	200 ms.	200 ms.	200 ms.	200 ms.
Display Rate:	1 s	1 s	1 s	1 s
Archive Rate:	6 Minutes	6 Minutes	6 Minutes	6 Minutes
Alarm Archive Rate:	30 Seconds	30 Seconds	30 Seconds	30 Seconds

5.4 Monitor and Command Data Points

RTPM Assembly – Monitor Points

Relative Address	Monitor Point Name	Source	No. of Bytes	Size of Word	Approximate Scaling
00	0 deg. Phase	Altera	1	16 bits	
01	Temperature monitor		1	16 bits	(X/8*.0625)*1.8+32=°F
02	Voltage Monitor	ADC	1	16 bits	+ 5v/2 (+5v=+2.5v)
03	Reset	MAX6629	1	16 bit	X/8*.0625=°C
04	PLL Lock Detect		1	1 bit	High-Lock, Low-Unlock

Digital Command Words for RA 03(See data sheet for TLC2558)

	Name	Function	Comment

5.5 **Reading the Temperature with the MAX6629**

The MAX6629 gives a 12-bit temperature reading with a range of –55 C to 150 C. The resolution of the device is 0.0625 degrees C per bit.

The MAX6629 is a read-only device. Whenever the CS input to the chip is high, it is takes a temperature reading every 5 seconds. When the SPI bus is not being used, EN should be set high, to insure that temperature readings are being taken.

The device sends out the temperature data in a 16-bit word. Following are the bit assignments for this word:

BIT 15	SIGN BIT
BIT 14 – BIT 3	TEMPERATURE DATA IN TWOS COMPLEMENT FORMAT
BIT 2	ZERO
BIT 1 – BIT 0	DON'T CARE

Since the 12 bit word (BIT 14 – BIT 3) is in twos complement format, BIT 14 is a sign bit, as well as bit 15.

Sample temperature readings for BIT 15 – BIT 3 (BIT 3 is the LSB):

0x1C90	-55 C
0x0	0 C
0x960	150 C

Following is a procedure to read a temperature from the MAX6629:

1. Send 0xFE to the shift register, to select the device.
2. Set CLK REG, then clear it, to latch the select bit.
3. Clear EN, to enable the select bit.
4. Read the 16 bit word out of the MAX6629 using the SPI bus. Data are clocked out of the device on the falling edge of SCLK.
5. Set EN, to disable the select bit and start automatic temperature readings.
6. Wait at least 300 ms before reading the next result.

5.6 Reading the Phase from the ALTERA chip

The ALTERA FPGA produces two 23-bit words. If CS0 (used as Sin/CosN) is asserted high, the sine coefficient is displayed. If CS0 is asserted low, the cosine coefficient is displayed. To calculate relative phase, find the arctan2 of the quotient sin/cos.

The sine and cosine coefficients naturally carry a sign which indicate resulting quadrant. Since the arctan function is only defined between $-\pi/2$ and $\pi/2$, and can not resolve quadrant II or III without quadrature indication, the arctan2 function must be used. Arctan2 is a function in the standard C math library.

Initialization:
The L352 FPGA can be initialized by setting the low true signal MR (J7-29) on the SPI for no less than 5 microseconds. This is the master chip reset and should be used as a last resort.

If only a soft restart of the accumulators is required, as might be desired at the beginning of an observation, restart (J4-44) can be asserted high.

5.6.1 Data Output:

Twenty-three bits of data is displayed on the GPIO bus. Toggling the chip select (CSO) will alternately display sine(H) and cosine(L) on the bus. The data is stored as two's compliment binary accumulated over 1 second, then latched into the output buffer. Therefore the data changes only every 1 second. Absolute phase is calculated in the MIB by dividing the sine result by the cosine result, then calculating the arctangent2 of the quotient.

The MIB should read the GPIO bus every 1 second.

6 FIRMWARE REQUIREMENTS

6. This module has no firmware requirements.

7 DESIGN CRITERIA

7.1 General

8 APPENDIX

8.1 MIB I/O

L301 Name	MIB Name	MIB Jx-n	I/O	Function

SDO	MISO	J7-02	O – M&C	Serial Data Out
SDI	MOSI	J7-04	I – M&C	Serial Data IN
SCLK	SCLK	J7-06	I – M&C	Shift Clock
CS0		J7-08	I – C	Select RT Data(Altera) (sin/cosN)
CS1		J7-09	I – C	Select Temperature
CS2		J7-11	I – C	Select ADC
MR		J7-29	I – C	Master Reset
MISO0+		J7-32		
MISO0-		J7-33		
MISO0_RET		J7-34		
MOSI0+		J7-35		
MOSI0-		J7-36		
MOSI0_RET		J7-37		
SCLK0+		J7-38		
SCLK0-		J7-39		
SCLK0_RET		J7-40		
IPREQ+		J7-41		
IPREQ-		J7-42		
IPREQ_RET		J7-43		
HEARTBEAT+		J7-47		
HEARTBEAT-		J7-48		
HEARTBEAT_RET		J7-49		
Result0 (D0)	126	J6-2	O – M	Result bit 0
Result1 (D1)	104	J6-3	O – M	Result bit 1
Result2 (D2)	103	J6-5	O – M	Result bit 2
Result3 (D3)	127	J6-6	O – M	Result bit 3
Result4 (D4)	128	J6-8	O – M	Result bit 4
Result5 (D5)	100	J6-9	O – M	Result bit 5
Result6 (D6)	99	J6-11	O – M	Result bit 6
Result7 (D7)	129	J6-12	O – M	Result bit 7
Result8 (D8)	130	J4-14	O – M	Result bit 8
Result9 (D9)	98	J4-15	O – M	Result bit 9
Result10 (D10)	97	J4-17	O – M	Result bit 10
Result11 (D11)	131	J4-18	O – M	Result bit 11
Result12 (D12)	132	J4-20	O – M	Result bit 12
Result13 (D13)	96	J4-21	O – M	Result bit 13
Result14 (D14)	94	J4-23	O – M	Result bit 14
Result15 (D15)	133	J4-24	O – M	Result bit 15
Result16 (IO13)	134	J4-26	O – M	Result bit 16
Result17(IO12)	91	J4-27	O – M	Result bit 17
Result18 (IO11)	85	J4-29	O – M	Result bit 18
Result19 (IO10)	139	J4-30	O – M	Result bit 19
Result20 (IO9)	140	J4-32	O – M	Result bit 20
Result21 (IO8)	84	J4-33	O – M	Result bit 21
Result22 (IO7)	83	J4-35	O – M	Result bit 22
IO6	141	J4-36		Spare IO line
IO5	142	J4-38		Spare IO line

Quad0 (IO4)	82	J4-39	O – M	LSB of Quadrature
Quad1 (IO3)	79	J4-41	O – M	MSB of Quadrature
AccOF (IO2)	143	J4-42	O – M	Accumulator Overflow – Indicates invalid data
Restart (IO1)	144	J4-44	I – C	Soft restart of the counters and accumulators.
DataRdy (IO0)	78	J4-45	O – M	Data Ready – Indicates output data is valid. Will be asserted except during the reset clock cycle.
EOC		J4-47	O – M	A/D EOC
PLD_Out		J4-48	O – M	Phase Lock Detect

Table 1 I/O Signal List

8.2 Analog to Digital Converter Channel Assignments

A to D Channel	Name	Signal	Display Factor	Update freq. (s)	Archive
AIN0	TUNEVOLT	Tune Voltage	*1	As req'd	?
AIN1	TRUPWR	PLL Power Out	*1	As req'd	?
AIN2	3.3V	Board Voltage	*1	As req'd	?
AIN3	1.5V	Altera Core Voltage	*1	As req'd	?
AIN4	5V	Board Voltage	*2	As req'd	?
AIN5	VCC	MIB 5V Supply	*2	As req'd	?
AIN6	GND	GND	*1	0	?
AIN7	GND	GND	*1	0	?
AIN8	GND	GND	*1	0	?
AIN9	GND	GND	*1	0	?
AIN10	GND	GND	*1	0	?

Table 3. Analog to Digital Converter channels

TLV2556 (11 Channel, 12 BIT, Analog to Digital Converter) Control Lines

This A to D converter is responsible for monitoring analog voltages. The external 4.096 volt reference is used. Refer to Texas Instruments Data Sheet for detailed Information.

Signal Name	MIB I/O	Function	Remarks
SCLK	SCLK	Shift Clock	Refer to data sheet
SDI	MOSI	Serial Data in	Refer to data sheet
SDO	MISO	Serial Data out	Refer to data sheet
CS	CSADC1	Chip Select	Active Low
EOC	EOC	End of Conversion Flag	Refer to data sheet

8.3 MAX6629 Temperature Sensor Control Lines

This sensors measure the temperature of the module in one location, on the RTPM board. Refer to Maxim Data Sheet for detailed Information

Signal Name	MIB I/O	Function	Remarks
SCLK	SCLK	Shift Clock	Refer to data sheet
SDO	MISO	Serial Data Out	Refer to data sheet
CS	CSTEMPn	Chip Select	Refer to data sheet