Garth Hunt

NATIONAL RADIO ASTRONOMY OBSERVATORY
Charlottesville, Virginia
VERY LARGE ARRAY PROJECT

SPECIFICATION NO.: A13500N3, Rev. B

NAME: Communications Between Digital Delay-Multiplier System and VLA Synchronous Computers

DATE: May 8, 1975

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DESCRIPTION:

All data between the Digital Delay-Multiplier System and the VLA Synchronous Computer (VLAC) will be controlled by a unit referred to as the System Controller (SC), which is the interface into and out of the Delay-Multiplier System. The only exceptions are monitored from the Samplers and, in the two antenna systems, one analog signal which is a combined total power signal. The exceptions will not be covered by this specification.

A block diagram of the communication system is shown in Figure 1. Two System Controllers (SC) are shown -- one for each 50 MHz system. In the prototype -- two antenna system -- there is only one SC, and all delays and multipliers are handled as though they were in the left polarization rack.

The System Controller CRT can be switched between the System Controller and Monty Computer. Thus the CRT can be used to communicate with the computer system in the same manner as other CRT's in the VLA. A CRT output of Monty Computer can also communicate directly with the SC. This connection is made whenever bit 2^2 (C) of the first word sent by Boss Computer to SC is a 1. This mode allows the on-line computer system to control the SC tests in the same manner that the SC's CRT terminal controls tests. The data input to the SC's CRT terminal controls tests. The data input to the SC's CRT input required for each test is listed in Table 6. Table 5 shows how Monty Computer could receive data back through its CRT input; however, this mode is not required by the on-line computer system since the same data is available to Core Computer via its connection to the SC. Table 7 is the format for Table 5.

To operate the SC in test mode, Boss Computer should send two complete sets of data as shown in Tables 2 and 4. In addition to delay data, the two sets should contain the following:

First Set of Data:

Word 0: A=1, B=1, C=1

Words 55 ····: Multiplier Sets Desired During Test

Second Set of Data:

Word 0: A=0, B=0, C=1

DO NOT SEND WORDS 55 THRU 405. (55 thru 60 in case of prototype).

Each of the communication networks to the Core computers and from the Boss computer consists of three signals:

1. Clock - maximum of 5 MHz
2. Data
3. Ready Line

The inputs to Core Computers are double buffered and when one buffer is full and the second begins receiving data the Ready Line changes state to "Not Ready". The sending block continues to send to the end of the present word, then stops and waits for the line to go "Ready" again.

Each of the three lines are twisted pair coaxial cable (RG-22) which is driven and received differentially with ECL logic. The transmission system has been tested with 500 ft. of cable and operation was excellent with considerable safety margin.

Tables 1 through 4 list all data transmitted to and from the System Controller, excluding the CRT, as follows:

Table 1 - Final System	-SC to VLAC
Table 2 - Final System	-VLAC to SC
Table 3 - Two Antenna System	-SC to VLAC
Table 4 - Two Antenna System	-VLAC to SC

The following rules are to be observed:

1. No transmission of data from VLAC to SC is to occur during blanking time. Therefore during blanking time the ready line from SC to VLAC is held "not ready".
2. Data transmission from VLAC to SC can be absorbed at the maximum rate (5 MHz clock rate) by the SC.

3. The block of data (VLAC to SC) shown in Tables 2 and 4 must be sent complete between two adjacent blanking times. This includes the first block sent before an observation is begun.
4. After a dump time, data from SC to VLAC may be taken at any rate and may extend across blanking times, but must be completed at least 2 microseconds prior to the beginning of the next dump time. Dump Time refers to the blanking time following completion of an integration period by the multipliers. Blanking time is referred to in the VLA system as "data invalid time" (1.603 ms).
5. Format of data in both directions:

   $000000,P,D_{23},D_{22} \cdots\cdots\cdots D_1,D_0,1$

   P = parity D_n = data D_o = LSB D_{23} = MSB 1 = start bit

   Transmission is serial, starting at "1". A minimum of one clock time will exist between words. The clock from SC to VLAC will be continuous (5 MHz, 80 ns positive, 120 ns negative - negative going edge centered on data bit at transmitter). The clock from VLAC to SC same as above except discontinuous - 32 clock pulses per 32 bit data word. The data word length and number of clock pulses may be as short as 30, leaving off the last two zeros.
6. For each observation the VLAC will send a block of data between every set of blanking times, the first being before the blanking time which precedes the start of an observation (integration) and the last being before the blanking time which follows the end of the observation (integration).
7. The relationships between when the different sets of data sent to the VLAC are obtained and to what they apply is shown in Figure 2.
8. The delay data should never contain a delay value of less than 70 ns.
9. Data in the tables which indicate errors - such as parity, overflow, etc. - are indicated thus:

   NO ERROR = 0 ERROR = 1

FINAL SYSTEM

SYSTEM CONTROLLER ⟶ VLAC (CORE A & B)

CORE INPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION	SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
0	0 0 0 G H_4 L_4 H_3 L_3 H_2 L_2 H_1 L_1 S_7 S_5 S_4 P_2 P_1 P_0 F E D C B A	A=0 UPDATE DATA-EVERY 50 ms.	0	0
		A=1 INITIATION DATA-AT START OF OBSERVATION		
		B=0 STOP OBSERVATION ON NEXT BT.		
		B=1 START OR CONTINUE OBS. ON NEXT BT.		
		C=1 COMPUTER TEST-CONTROLLED BY MONITY COMPUTER THROUGH CRT TERMINAL. INPUT.		
		D=1 PARITY ERRORS RECEIVED BY VLAC		
		E=1 OBSERVATION STOPPED BECAUSE OF TOO MANY PARITY ERRORS		
		F=1 DELAY-MULTIPLIER SYSTEM LOCAL TEST		
		P_2, P_1, P_0 = DUMP PERIOD - BINARY NUMBER 1=50; 2=100; 3=150; 4=200; 5=250; 6=300 ms.		
		S_4=1 DISABLE NEGATIVE SAMPLER		
		S_5=1 DISABLE POSITIVE SAMPLER		
		S_7 - SPARE SAMPLER BIT - ALWAYS = 0		
	L OR H=0 DENOTES Vs COUNTER IN TOLERANCE. L=1 COUNTER BELOW LOW TOLERANCE H=1 COUNTER ABOVE HIGH TOLERANCE L_1, H_1 REFER TO 1Vs L_2, H_2 " " 2Vs ETC.			
	NOTE: IF Vs IS WITHIN TOLERANCE, G ALTERNATES BETWEEN 0 & 1 BETWEEN OBSERVATIONS.	G=0 SET 1 Vs's USED		
		G=1 SET 2 Vs's USED		
1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	SPARE WORD	1	1
2	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	SPARE WORD	2	2
3	0 0 0 0 0 0 D_{18} D_{17} D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	THEORETICAL VALUE OF Vs.	3	3
4	0 0 P Ø S D_{18} — D_0	SET 1-(LS×LS)Vs SET 2-(LC×RS) Vs	4	4
5	0 0 P Ø S D_{18} — D_0	SET 1-(LC×RC)Vs SET 2-(LS×LC) Vs	5	5
6	0 0 P Ø S D_{18} — D_0	SET 1-(RS×RS)Vs SET 2-(RC×LC) Vs	6	6
7	0 0 P Ø S D_{18} — D_0	SET-1-(RC×LS) Vs SET 2-(RS-RC) Vs	7	7
8	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 A_4 A_3 A_2 A_1 A_0	ANTENNA USED IN S×C MULTIPLICATION - BINARY	10	8
9	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	SPARE WORD	11	9
10	0 0 0 0 0 0 — 0	SPARE WORD	12	10
11	0 0 0 0 0 0 — 0	SPARE WORD	13	11
12	0 0 P Ø S D_{18} D_{17} D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	MULTIPLIER 1 L NLS×NLC	14	12
13	0 0 P Ø S D_{18} — D_0	MULTIPLIER 2 L NLS×NLC	15	13
14	0 0 P Ø S D_{18} — D_0	MULTIPLIER 1 R NRS×NRC	16	14
15	0 0 P Ø S D_{18} — D_0	MULTIPLIER 2 R NRS×NRC	17	15

SIN × COSINE MULTIPLIERS

NOTE ⟶ IN all computer words from 12 through 3039 the D_{18} bit is obtained by using the overflow bit to form a 19 bit Vn word before subtracting Vo. Ø = OVERFLOW P = PARITY (OBTAINED DURING TEMPORARY STORAGE TO SYSTEM CONTROLLER — TRANSMISSION)

S = SIGN

TABLE 1

REV. B 5-7-75 ams A.M. SHALLOWAY

REV. A 11-12-74 ams 6-11-74

FINAL SYSTEM

SYSTEM CONTROLLER → VLAC (CORE A & B)

CORE INPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION	SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
16	0 1 P Φ S D_{18} D_{17} D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	1 RS × 1 RS	20	16
17	0 1 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 RS × 1 RS	21	17
18	0 1 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 LS × 1 LS	22	18
19	0 1 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 LS × 1 LS	23	19
20	0 1 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 RC × 1 RC	24	20
21	0 1 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 RC × 1 RC	25	21
22	0 1 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 LC × 1 LC	26	22
23	0 1 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 LC × 1 LC	27	23
24	0 1 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	2 RS × 2 RS	30	24
⋮	⋮	⋮	⋮	⋮
231	0 1 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	27 LC × 27 LC	347	231
232	1 0 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 RS × 2 RS	400	256
233	1 0 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 RS × 2 RC	401	257
234	1 0 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 LS × 2 LS	402	258
235	1 0 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 LS × 2 LC	403	259
236	1 0 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 RC × 2 LC	404	260
237	1 0 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 RC × 2 LS	405	261
238	1 0 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 LC × 2 RC	406	262
239	1 0 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 LC × 2 RS	407	263
240	1 0 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1 RS × 3 RS	410	264
⋮	⋮	⋮	⋮	⋮
3039	1 0 P Φ S D_{18} — — — — — — — — — — — — — — — — — — D_0	26 LC × 27 RS	5767	3063
3040	1 1 0 0 S_6 A D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 S_3 S_2 S_1 S_0	D_{13}-D_0 = DELAY-10ns RESOLUTION - BINARY	6000	3072
	NOTE: Word No. 3040 = LEFT ANT. 1	S_3-S_0 = DELAY-625ps RESOLUTION - BINARY		
	Word No. 3041 = RIGHT ANT. 1	S_6=0 NON-INVERT } SAMPLER INVERT SIGNAL		
	Word No. 3042 = LEFT ANT. 2	S_6=1 INVERT }		
	Word No. 3043 = RIGHT ANT. 2 & ETC.	A=0 ENABLE DELAY LINE OUTPUT		
3093	1 1 0 0 S_6 A D_{13} — — — — — — — — — — — — — — — — — — D_0 S_3 S_0	A=1 DISABLE DELAY LINE OUTPUT	6065	3125
3094	1 1 0 0 0 A D_{13} — — — — — — — — — — — — — — — — — — D_0 T T T T	D_{13}-D_0 = LEFT TEST DELAY LINE DELAY	6066	3126
3095	1 1 0 0 0 A D_{13} — — — — — — — — — — — — — — — — — — D_0 T T T T	D_{13}-D_0 = RIGHT TEST DELAY LINE DELAY	6067	3127

SELF MULTIPLIERS

CROSS MULTIPLIERS

MULTIPLIER SET 32

MULTIPLIER SETS 33 THRU 382

TABLE 1

REV. B 5/7/75 ams A.M. SHALLOWAY

REV. A 11/12/74 ams 6-11-74

FINAL SYSTEM

SYSTEM CONTROLLER → VLAC (CORE A & B)

CORE INPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION	SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
3096	1 1 0 0 0 0 0 0 0 0 0 0 X_M^{C} X_L^{C} X_M^{S} X_L^{S} 0 0 0 M_4 M_3 M_2 M_1 M_0	M_4-M_0 = LEFT SIN INPUT MULTIPLEXER ADDRESS	6070	3128
	NOTE: IF T (IN WORD NOS. 3094 & 3095) = 1 ALL EXCHANGE DATA BITS = 1. X's ARE EXCHANGE DATA BITS FOR ANTENNA ASSOCIATED WITH INPUT MUX. ADDRESS. X_M^{C} X_L^{C} X_M^{S} X_L^{S} 0 0 0 0 / 0 0 0 0 / 0 0 0 0 / 0 0 0 0 / 0 0 0 0	M_4-M_0 = RIGHT SIN INPUT MULTIPLEXER ADDRESS M_4-M_0 = LEFT COS INPUT MULTIPLEXER ADDRESS M_4-M_0 = RIGHT COS INPUT MULTIPLEXER ADDRESS M_4-M_0 = LEFT SIN OUTPUT MULTIPLEXER ADDRESS M_4-M_0 = RIGHT SIN OUTPUT MULTIPLEXER ADDRESS M_4-M_0 = LEFT COS OUTPUT MULTIPLEXER ADDRESS		
3103	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 M_4 — M_0	M_4-M_0 = RIGHT COS OUTPUT MULTIPLEXER ADDRESS	6077	3135
3104	1 1 0 0 0 0 0 0 G F_1 F_0 E D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	SYSTEM MONITOR DATA	6100	3136
	G=0 POWER ON G=1 POWER OFF (DOWN) } DELAY MULTIPLIER RACK	D = 12 BIT BINARY ABSOLUTE VALUE DATA E=0 WITHIN LIMITS E=1 OUT OF LIMITS		
3167	1 1 0 0 0 0 0 0 G F_1 F_0 E D_{11} — — — — D_0	F_0 F_1 BINARY NUMBER INDICATES WHICH LIMIT HAS BEEN EXCEEDED	6177	3199
3168	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 C_1 C_0 S_1 S_0	GO/NO-GO RESULTS FROM DELAY COMPARATOR	6200	3200
		S = SIN - L & MSB C = COS - L & MSB S OR C = 0 = GO S OR C = 1 = NO-GO EVEN COMPUTER WORDS = LEFT ODD = RIGHT		
3221	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 C_1 C_0 S_1 S_0		6265	3253
3222	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	SPARE WORDS	6266	3254
3231	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		6277	3263
3232	1 1 0 0 0 0 0 0 0 0 0 0 B_2 B_1 B_0 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	A_8-A_0 = COMPUTER WORD NO. (STARTING AT 0) OF WORD(S) VLAC → SC WITH PARITY ERRORS	6300	3264
	NOTE: A MAXIMUM OF 64 ERRORS CAN BE INDICATED.	B_2, B_1, B_0 = BLANKING TIME IN WHICH ERROR OCCURRED - BINARY 1 THRU 6.		
3295	1 1 0 0 0 0 0 0 0 0 0 0 B_2 B_1 B_0 A_8 — — — — A_0		6377	3327
3296	1 1 0 1 0 0 0 0 0 0 0 0 0 0 L C_5 C_7 C_6 C_5 C_4 C_3 C_2 C_1 C_0	C_8-C_0 = MULTIPLIER SETS DESIRED BY VLAC. EACH NUMBER = 8 MULTIPLIERS	6400	3328
MAX ↓		NOTE: 32 = 1×2 33 = 1×3 34 = 1×4 ETC.	MAX ↓	MAX ↓
3646	1 1 0 1 0 0 0 0 0 0 0 0 0 0 L C_8 — — — — — C_0	MAXIMUM OF 351 SETS OF CHANNELS L = 1 IN LAST WORD.	7136	3678
LAST WORD	1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 T_8 T_7 T_6 T_5 T_4 T_3 T_2 T_1 T_0	T_8-T_0 = TIME IN TENS OF SECONDS TO END OF OBSERVATION - BINARY	7137	3679
	NOTE: Four 1's in bit positions 20, 21, 22 & 23 indicate the last word of transmission.			

TABLE 1

REV. B 5/7/75 amc A.M. SHALLOWAY
REV. A 11/12/74 amc 6-11-74

FINAL SYSTEM

VLAC (BOSS) → SYSTEM CONTROLLER

BOSS OUTPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION
0	0 0 0 1 0 0 0 0 0 0 0 0 S_7 S_5 S_4 P_2 P_1 P_0 F E D C B A	A=0 UPDATA DATA — EVERY 50ms. A=1 INITIATION DATA — AT START OF OBSERVATION. B=0 STOP OBSERVATION ON NEXT BT. B=1 START OR CONTINUE OBS. ON NEXT BT. C=1 COMPUTER TEST-CONTROLLED BY MONTY COMPUTER THROUGH CRT TERMINAL INPUT. $P_2 P_1 P_0$ = DUMP PERIOD - BINARY NUMBER 1=50; 2=100; 3=150; 4=200; 5=250; 6=300 ms. S_7 - SPARE SAMPLER BIT - ALWAYS=0 S_5, S_4 = SAMPLER TEST CODE S_4=DISABLE NEGATIVE SAMPLER S_5=DISABLE POSITIVE SAMPLER
1	0 0 1 0 S_6 A D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 S_3 S_2 S_1 S_0	D_{13} - D_0 = DELAY - 10ns RESOLUTION - BINARY S_3 - S_0 = DELAY - 625ps RESOLUTION - BINARY S_6=0 NON-INVERT, S_6=1 INVERT } SAMPLER INVERT SIGNAL A=0 ENABLE DELAY LINE OUTPUT A=1 DISABLE DELAY LINE OUTPUT
	NOTE: WORD NO. 1 = LEFT ANT. 1 WORD NO. 2 = RIGHT ANT. 1 WORD NO. 3 = LEFT ANT. 2 WORD NO. 4 = RIGHT ANT. 2 & ETC.	
54	0 0 1 0 S_6 A D_{13} — — — — — — — — — — — — — — D_0 S_3 — S_0	
55	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 L C_8 C_7 C_6 C_5 C_4 C_3 C_2 C_1 C_0	C_8 - C_0 = MULTIPLIER SETS DESIRED BY VLAC EACH NUMBER = 8 MULTIPLIERS. NOTE: 32=1×2 33=1×3 34=1×4 ETC. MAXIMUM OF 351 SETS OF CHANNELS. L=1 IN LAST WORD
MAX 405	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 L C_8 — — — — — — — — — C_0	
LAST WORD	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 T_8 T_7 T_6 T_5 T_4 T_3 T_2 T_1 T_0	T_8 - T_0 = TIME IN TENS OF SECONDS TO END OF OBSERVATION - BINARY.

NOTE: COMPUTER WORDS 55 THRU 405 WILL BE TRANSMITTED ONLY ON THE FIRST TRANSMISSION BEFORE AN OBSERVATION BEGINS.

TABLE 2

REV. B 5/7/75 amc A.M. SHALLOWAY
REV. A 11/12/74 amc 6-11-74

PROTOTYPE (2 ANTENNA) SYSTEM

SYSTEM CONTROLLER ⟶ VLAC (CORE A)

CORE INPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION	SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
0	0 0 0 G H_4 L_4 H_3 L_3 H_2 L_2 H_1 L_1 S_7 S_5 S_4 P_2 P_1 P_0 F E D C B A	IGNORE G-WILL ALTERNATE UNLESS Vs BAD	0	0
1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	NC- SPARE WORD	1	1
2	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	NC- SPARE WORD	2	2
3	0 0 0 0 0 D_{19} D_{17} D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	NC- THEORETICAL VALUE OF Vs.	3	3
4	0 0 P ϕ S D_{18} D_0	THERE IS ONLY ONE Vs COUNTER IN	4	4
5	0 0 P ϕ S D_{18} D_0	THE SYSTEM. THE OUTPUT OF THE COUNTER	5	5
6	0 0 P ϕ S D_{18} D_0	IS SENT TO 4 INTEGRATORS, ALL OF WHICH	6	6
7	0 0 P ϕ S D_{18} D_0	SHOULD HAVE THE SAME VALUE.	7	7
8	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 A_4 A_3 A_2 A_1 A_0	ANTENNA USED IN S×C MULTIPLICATIONS (BINARY) ACCORDING TO FOLLOWING TABLE:	10	8

NOTE: A_4-A_0 PROGRESSES ONE STEP EVERY DUMP TIME FROM 1 TO 27. HOWEVER, 1 THRU 18 & 27 DO NOT PROVIDE ANY USEABLE DATA.

A_4-A_0	ANT. No.	50MHz. SYSTEM
19	1R	A
20	1R	B
21	2R	A
22	2R	B
23	1L	A
24	1L	B
25	2L	A
26	2L	B

9	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	NC- SPARE WORD	11	9
10	0 0 0 0 0 0	0 NC- SPARE WORD	12	10
11	0 0 0 0 0 0	0 NC- SPARE WORD	13	11
12	0 0 P ϕ S D_{18} D_{17} D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	MULTIPLIER 1 } ACTUAL MULTIPLICATION	14	12
13	0 0 P ϕ S D_{18} D_0	MULTIPLIER 1 } OBTAINED FROM	15	13
14	0 0 P ϕ S D_{18} D_0	MULTIPLIER 2 } TABLE ABOVE.	16	14
15	0 0 P ϕ S D_{18} D_0	MULTIPLIER 2 } SIN X COSINE MULTIPLIERS	17	15

NOTE: NC = NO CHANGE FROM FINAL SYSTEM.
R = RIGHT L = LEFT

REV. B 5/7/75 amc A.M. SHALLOWAY
REV A 11/12/74 6-19-74

PROTOTYPE (2 ANTENNA) SYSTEM

SYSTEM CONTROLLER → VLAC (CORE A)

CORE INPUT

COMPUTER WORD No.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION		SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
16	0 1 P Ø S D_{18} D_{17} D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	1RS × 1RS	A 50 MHz. SYSTEM	20	16
		1LS × 1LS		21	
		1RC × 1RC		22	
		1LC × 1LC		23	
		2RS × 2RS		24	
		2LS × 2LS		25	
		2RC × 2RC		26	
		2LC × 2LC		27	
		1RS × 1RS	B 50 MHz. SYSTEM	30	
		1LS × 1LS		31	
		1RC × 1RC		32	
		1LC × 1LC		33	
		2RS × 2RS		34	
		2LS × 2LS		35	
		2RC × 2RC		36	
31	0 1 P Ø S D_{18} — — — — — — — — — — — — — — — — — D_0	2LC × 2LC		37	31
32	1 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — D_0	1RS × 2RS	A 50 MHz. SYSTEM — MULTIPLIER SET 32	400	256
		1RS × 2RC		401	
		1LS × 2LS		402	
		1LS × 2LC		403	
		1RC × 2LC		404	
		1RC × 2LS		405	
		1LC × 2RC		406	
		1LC × 2RS		407	
		1RS × 2RS	B 50 MHz. SYSTEM — MULTIPLIER SET 33	410	
		1RS × 2RC		411	
		1LS × 2LS		412	
		1LS × 2LC		413	
		1RC × 2LC		414	
		1RC × 2LS		415	
		1LC × 2RC		416	
47	1 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — D_0	1LC × 2RS		417	271

SELF MULTIPLIERS — CROSS MULTIPLIERS

TABLE 3

REV. B 5/7/75 amd
REV. A 11/12/74 amd

A. M. SHALLOWAY
6-19-74

PROTOTYPE (2 ANTENNA) SYSTEM
SYSTEM CONTROLLER → VLAC (CORE A)

CORE INPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION				SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
48	1 OP Ø S D_{18} D_{17} D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	1LS × 1LC	A 50 MHz SYSTEM	MULTIPLIER SET 34	REDUNDANT SIN × COS MULTIPLIERS	420	272
		1LS × 1LC				421	
		2LS × 2LC				422	
		2LS × 2LC				423	
		1RS × 1RC	B 50 MHz SYSTEM			424	
		1RS × 1RC				425	
		1LS × 1LC				426	
		1LS × 1LC				427	
		2RS × 2RC				430	
		2RS × 2RC				431	
		2LS × 2LC				432	
59	1 OP Ø S D_{18} — — — D_0	2LS × 2LC		MULTIPLIER SET 35		433	283
60	1 OP Ø S D_{18} — — — D_0	1LC × 1LC	A 50 MHz SYSTEM	MULTIPLIER SET 36	REDUNDANT SELF MULTIPLIERS	434	284
		2LS × 2LS				435	
		1LS × 1LS	B 50 MHz SYSTEM			436	
		1RC × 1RC				437	
		2LS × 2LS				440	
65	1 OP Ø S D_{18} — — — D_0	2RC × 2RC				441	289
66	1 OP Ø S D_{16} — — — D_0	1RS × 2RC	A 50 MHz SYSTEM	MULTIPLIER SET 37	REDUNDANT CROSS MULTIPLIERS	442	290
		1LS × 2LC				443	
		1RC × 2LS				444	
		1LC × 2RC				445	
		1LC × 2RS				446	
		1LC × 2RS				447	
		1RS × 2RS	B 50 MHz SYSTEM			450	
		1RS × 2RC				451	
		1LS × 2LC				452	
		1RC × 2LS				453	
76	1 OP Ø S D_{18} — — — D_0	1LC × 2RS				454	300
77	1 OP Ø S D_{18} — — — D_0	A1LC × A2LC	ILLEGAL MULTIPLICATIONS	MULTIPLIER SET 38	ILLEGAL MULTIPLIERS	455	301
		A1LC × B2LS				456	
		A1LS × B2LS				457	
80	1 OP Ø S D_{18} — — — D_0	A1LS × B2LC				460	304

MULTIPLICATIONS BEFORE INVERSIONS:
1RC × 2RS
1LC × 2LS
1RS × 2LC
1LS × 2RC
2RC × 1LS
2RS × 1RC
2LS × 1LC
1RS × 2LC
1LS × 2RC

← NOTE: THIS MAY BE A "0" IN WORD 0 BIT 23

REV B 5/7/75 AMS

A.M. SHALLOWAY
6-19-74

PROTOTYPE (2 ANTENNA) SYSTEM

SYSTEM CONTROLLER → VLAC (CORE A)

CORE INPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION	SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
88	1 1 0 0 S_6 A D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 S_3 S_2 S_1 S_0	NC – DELAY LINE DATA	6000	3072
	NOTE: ORDER OF DELAYS IS AS FOLLOWS:			
	WORD NO. | ANT. NO. | 50MHz. SYSTEM			
	124 | 1R | A			
	126 | 1R | B			
	128 | 2R | A			
	130 | 2R | B			
	132 | 1L | A			
	134 | 1L | B			
	136 | 2L | A			
	138 | 2L | B		6016	3086
	NOTE: ALL WORDS NOT LISTED ARE SPARE WORDS.		6017	3087
141	1 1 0 —		6065	3125
142	1 1 0 0 0 A D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 T T T T	TEST DELAY LINE	6066	3126
143	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	SPARE DELAY WORD.	6067	3127
144	1 1 0 0 0 0 0 0 0 0 0 0 X_{CM} X_{CL} X_{SM} X_{SL} 0 0 0 M_4 M_3 M_2 M_1 M_0	M_4-M_0 = SIN INPUT MULTIPLEXER ADDRESS	6070	3128
	NOTE: IF T (IN WORD NO. 281) = 1, ALL EXCHANGE DATA BITS = 1. X's ARE EXCHANGE DATA BITS FOR ANT. ASSOCIATED WITH INPUT MUX. ADDRESS.	0 0 0 0 0 0 0 0 0 0	SRARE MULTIPLEXER WORD		
		0 0 0 0 M_4 — — M_0	M_4-M_0 = COS INPUT MULTIPLEXER ADDRESS		
		0 0 0 0 0 0 0 0 0 0	SPARE MULTIPLEXER WORD		
		0 0 0 0 M_4 — — M_0	M_4-M_0 = SIN OUTPUT MULTIPLEXER ADDRESS		
		0 0 0 0 0 0 0 0 0 0	SPARE MULTIPLEXER WORD		
		0 0 0 0 M_4 — — M_0	M_4-M_0 = COS OUTPUT MULTIPLEXER ADDRESS		
151	1 1 0 — — — — — — — — — — 0 0 0 0 — — 0 0 0 0 0	SPARE MULTIPLEXER WORD	6077	3135
152	1 1 0 0 0 0 0 0 G F_1 F_0 E D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	NC – SYSTEM MONITOR DATA	6100	3136
215	1 1 0 — D_0		6177	3199

NOTE: X = EXCHANGE; C = COS; S = SIN; L = LSB; M = MSB

TABLE 3

REV. B 5/7/75 amk
REV. A 11/12/74 amk

A.M. SHALLOWAY
6-19-74

PROTOTYPE (2 ANTENNA) SYSTEM

SYSTEM CONTROLLER → VLAC (CORE A)

CORE INPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION	SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
216	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	GO/NO-GO RESULTS FROM DELAY COMPARATOR S=SIN-L&MSB C=COS-L&MSB S OR C=0=GO S OR C=1=NO-GO CONSIDER THESE WORDS NUMBERED FROM 1 TO 54. THE GO/NO-GO'S ARE ASSOCIATED WITH ANT. AS FOLLOWS:	6200	3200

COMPUTER WORD NO.	WORD NO.	ANT. NO.	50 MHz SYSTEM
252	37	1R	A
254	39	1R	B
256	41	2R	A
258	43	2R	B
260	45	1L	A
262	47	1L	B
264	49	2L	A
266	51	2L	B

262	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 C_1 C_0 S_1 S_0	ALL OTHER WORDS PROVIDE NO USEFUL DATA, AND NORMALLY ARE ZERO	6265	3253
263	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		6266	3254
279	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		6277	3263
280	1 1 0 0 0 0 0 0 0 0 0 0 B_2 B_1 B_0 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	N.C. – PARITY ERROR ADDRESSES.	6300	3264
343	1 1 0 0 0 0 0 0 0 0 0 0 B_2 B_1 B_0 A_8 — — — — — — — — — A_0		6377	3327
344	1 1 0 1 0 0 0 0 0 0 0 0 0 0 L 0 0 0 C_5 C_4 C_3 C_2 C_1 C_0	C_5–C_0 = MULTIPLIER SET DESIRED BY VLAC. EACH NUMBER = 8 MULTIPLIERS. SEE COMPUTER WORD NOS. 32 THRU 87 FOR SET NUMBERS. L=1 IN LAST WORD.	6400	3328
MAX ↓ 350	1 1 0 1 0 0 0 0 0 0 0 0 0 0 L 0 0 0 C_5 C_4 C_3 C_2 C_1 C_0		MAX ↓ 6406	MAX ↓ 3334
LAST WORD	1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 T_8 T_7 T_6 T_5 T_4 T_3 T_2 T_1 T_0	N.C. – TIME TO END OF OBSERVATION.	7137	3679

NOTE: Four 1's in bit positions 20, 21, 22, & 23 indicate the last word of transmission.

TABLE 2

REV. B 5/7/75 A. M. SHALLOWAY
REV. A 10/12/74 6-19-74

PROTOTYPE (2 ANTENNA) SYSTEM
VLAC (BOSS) → SYSTEM CONTROLLER

BOSS OUTPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION
0	0 0 0 1 D 0 0 0 0 0 0 0 0 S_7 S_5 S_4 P_2 P_1 P_0 F E D C B A	N.C. – CONTROL WORD
1	0 0 1 0 S_6 A D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 S_3 S_2 S_1 S_0	N.C. – DELAY LINE DELAY
	NOTE: ORDER OF DELAYS IS AS FOLLOWS:	
	WORD No. / ANT. No. / 50 MHz SYSTEM: 37 / 1R / A; 39 / 1R / B; 41 / 2R / A; 43 / 2R / B; 45 / 1L / A; 47 / 1L / B; 49 / 2L / A; 51 / 2L / B	
	NOTE: ALL WORDS NOT LISTED ARE SPARE WORDS	
54	0 0 1 0 – –	
55	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 L C_8 C_7 C_6 C_5 C_4 C_3 C_2 C_1 C_0	C_8–C_0 = MULTIPLIER SETS DESIRED BY VLAC. EACH NUMBER = 8 MULTIPLIERS. SEE COMPUTER WORD NOS. 32 THRU 87 IN TABLE 3 FOR SET NUMBERS. L = 1 IN LAST WORD.
MAX ↓ 60	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 L C_8 – – – – – – – – C_0	
LAST WORD	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 T_8 T_7 T_6 T_5 T_4 T_3 T_2 T_1 T_0	N.C. – TIME TO END OF OBSERVATION

NOTE: COMPUTER WORDS 55 THRU 60 WILL BE TRANSMITTED ONLY ON THE FIRST TRANSMISSION BEFORE AN OBSERVATION BEGINS.

TABLE 4

REV. B 5/7/75 amc A.M. SHALLOWAY
REV. A 11/12/74 amc 6-19-74

TABLE 5

INSTRUCTIONS FOR CRT TERMINAL DATA DISPLAY

NOTES:

A. In each instruction below, the first heading (e.g. DB 0000.7137) is used to display the desired information in octal and the second heading (e.g. DC 0000.7137) is used to display the information in decimal. If only one heading is shown, the information is available only in octal.

B. At the end of each display instruction, the ENTER key must be depressed to transfer the instruction from the CRT to the SC. This function will appear on the CRT screen as a backwards letter L (e.g. DB 0000.7137⌟).

C. Spaces within an instruction have no effect and may be used as desired for clarity (e.g. DB0000.7137 or DB 0000.7137).

D. To continually update the data display, prefix the desired instruction by one of the following letters:

LETTER	UPDATE PERIOD
R	0.8 sec
S	1.6 sec
T	3.2 sec
U	6.4 sec
V	12.8 sec
W	25.6 sec
X	51.2 sec
Y	102.4 sec

For faster update periods, some displays will not have time to complete between updates depending on the length of the display and the baud rate.

E. To stop an updating display (necessary before entering new instructions) use the DA instruction.

F. Each instruction for displaying multiplier results (instructions 3 thru 6) contains one or more octal number XXXX which is a starting address for a group of 8 multiplier results. These may be interpreted in two ways:

XXXX = Octal number of starting RAM address

or if the least significant digit is taken as zero:

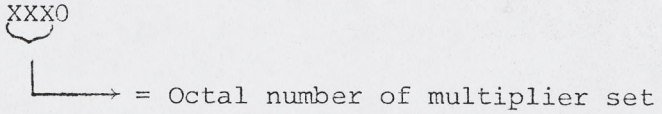


TABLE 5 (continued)

INSTRUCTION	DATA TO BE DISPLAYED
1. DA	STOP UPDATE and RESET DISPLAY LOGIC (No data will be displayed by this instruction)
2. DB DC 0000.7137	CONTROL and TIME WORDS
3. DD DE XXXX ↑—See Note F	MULTIPLIER RESULTS, SEQUENTIAL BEFORE Vs SUBTRACTION (128 sequential multiplier results starting at SC Ram address XXXX)
4. DF DG XXXX. ··· XXXX.1000	MULTIPLIER RESULTS, GROUPS OF 8 BEFORE Vs SUBTRACTION (Maximum of 16 groups, each group consisting of 8 sequential multiplier results starting at SC Ram address XXXX)
5. DH XXXX	MULTIPLIER RESULTS, SEQUENTIAL AFTER Vs SUBTRACTION
6. DI XXXX. ··· XXXX.10000	MULTIPLIER RESULTS, GROUPS OF 8 AFTER Vs SUBTRACTION
7. DL DM 6000	DELAY and DISABLE DATA EXCHANGE DATA AND MUX ADDRESSES (54 delay words; 2 test delay words; left and right exchange data in the order CM, CL, SM, SL; input and output mux addresses)
8. DN DO 6100	SYSTEM MONITOR DATA (64 words)
9. DP 6200	GO/NO GO DATA (Delay Line Self Test Results 54 words = 216 delay lines)
10. DQ XXXX	RAM DATA SET (8 sequential words starting at Ram octal address XXXX, bits 0 thru 21 displayed in octal)
11. DR DS 6300	PARITY ERROR ADDRESSES (64 words, contains computer word number for parity error and the BT in which it occurred BOSS computer to SC)
12. DT DU 6400	ADDRESSES OF MULTIPLIERS REQUESTED (Maximum of 351 words, each representing one multiplier set requested by VLAC)

TABLE 6

INSTRUCTIONS FOR CRT TERMINAL DATA ENTRY

NOTES:

A. All numbers indicated by X are in octal.

B. At the end of each entry instruction, the ENTER key must be depressed to transfer the instruction from the CRT to the SC. This function will appear on the CRT screen as a backwards letter L (e.g. EE XXJ).

C. Spaces within an instruction have no effect and may be used as desired for clarity (e.g. EXX or EE XX).

D. The following table gives the delay word number for each of the eight prototype delay words and the corresponding multiplexer address that tests the associated delay lines:

DELAY WORD NUMBER		DELAY		MULTIPLEXER ADDRESS	
Decimal	Octal	Ant. No.	50 MHz System	Decimal	Octal
37	45	1R	A	19	23
39	47	1R	B	20	24
41	51	2R	A	21	25
43	53	2R	B	22	26
45	55	1L	A	23	27
47	57	1L	B	24	30
49	61	2L	A	25	31
51	63	2L	B	26	32

E. The following table gives the GO/NO GO logic tests for mux addresses 0 and 28-31.

MUX ADR	INPUT MUX DATA	OUTPUT MUX DATA	GO/NO GO RESULTS
0	0	0	GO
28	1	1	GO
29	0	1	NO GO
30	1	0	NO GO
31	Random Data	Random Data	NO GO

TABLE 6 (continued)

1. EA XXXX — CONTROL WORD

- Observation/Test Status: Bits CBA (see Table 2)
- Parity Error Status = Bits FED (see Table 2)
- 1 thru 6 = 50ms thru 300ms Dump Period = Bits P_2 P_1 P_0 (see Table 2)
- 1 = Disable Neg Sampler 2 = Disable Pos Sampler 3 = Both: Bits S_7 S_5 S_4 (see Table 2)

---

2. EB X XXXXX XX — DELAY DATA, SAME TO ALL DELAY CONTROLS

- Sampler delay in 625 picosecond steps
- Delay Line Delay in 10 nanosecond steps
- 0 = Normal 1 = Delay Line Disable 2 = Sampler Invert 3 = Both

---

3. EC X XXXXX XX. ····X XXXXX XX — DELAY DATA DIFFERENT TO EACH DELAY CONTROL

54 delay words each as in EB

---

4. ED XX.X XXXXX XX — DELAY DATA TO ONE DELAY CONTROL

- Same as in EB
- Octal delay word number (In decimal 1 = 1L ···· 53 = 27L, 2 = 1R ···· 54 = 27R) See Note D for prototype)

---

5. EE XX — HOLD MUX ADDRESSES

- Octal mux address to hold (In decimal 1 = Ant 1 27 = Ant 27, 0 and 28-31 = Tests of GO/NO GO Logic) See Note E.

---

6. EF XXXX — EXCHANGE DELAY LINE(S) AT ONE MUX ADR

- Octal mux adr to hold
- Exchange data 1 = SL 2 = SM 3 = Both
- Exchange data 1 = CL 2 = CM 3 = Both

7a. EG 3317 — MULTIPLIER TEST-RANDOM NOISE GENERATOR

(All multiplier terminated inputs receive the same data pattern and all bridging inputs receive the same data pattern but different from the terminated inputs)

7b. EG XXXX7317 — MULTIPLIER TEST-STATIC PATTERN

(As above except the inputs receive static data determined by XXXX.)

- Bridging LSB Input
- Bridging MSB Input
- Terminated LSB Input
- Terminated MSB Input

TABLE 6 (continued)

8.	EH XX ↑— Octal mux address to hold	DELAY LINE TEST-HOLD MUX ADR SHORT PATTERN
9.	EI XX ↑— Octal mux address at which test starts	DELAY LINE TEST-ROTATE MUX ADR SHORT PATTERN (One complete cycle = 20 seconds for DT = 50ms)
10.	EJ XX ↑— Octal mux address to hold	DELAY LINE TEST-HOLD MUX ADR LONG PATTERN
11.	EK XX ↑— Octal mux address at which test starts	DELAY LINE TEST-ROTATE MUX ADR LONG PATTERN (One complete cycle = 5.7 min. for DT = 50ms)
12.	EL	RESET FROM COMPUTER (Left GO/NO GO and Exchange Data)
13.	EM	RESET FROM COMPUTER (Right GO/NO GO and Exchange Data)
14.	EQ	RESET TEST INSTRUCTIONS 5 THRU 11 (Resets storage flip flops F13 thru F17 on L31 but does not reset the TEST indicator)
15.	ER	RESET ALL TESTS (Same as EQ but also resets the TEST indicator)

TABLE 7

CRT DISPLAY FORMATS

NOTES:

1. The following table is intended to aid the user of the System Controller CRT to interpret the displayed information. This table is intended to be used along with Tables 1-6 to provide a complete users description of the display functions available.
2. For each type display instruction an example display or partial display is shown, and where appropriate, the associated 24 bit computer word is shown to indicate which bits of the word are represented by each character displayed on the CRT screen.
3. If certain conditions are present in the displayed information, the associated character is displayed on the CRT screen as a reverse flashing character. In the display examples these characters are shown with an underline. For certain test conditions that are not errors, the associated display character appears on the screen as a reverse character but without flashing.

EXAMPLES: 2 indicates error condition

2* indicates test condition

DISPLAY EXAMPLES

1. CONTROL and TIME WORDS

Octal

DB 0000.7137

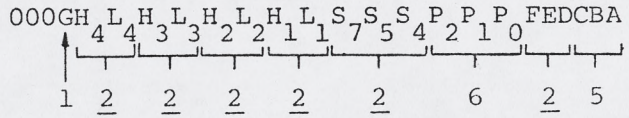
1 2 2 2 2 2* 6 2 5 7777 (tens of seconds)

Decimal

DC 0000.7137

1 2 2 2 2 2* 6 2 5 5110 SEC

Control Word Only



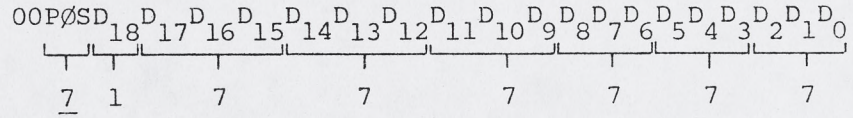
2. MULTIPLIER RESULTS

Octal

DD XXXX (seq. before V_S)
DH XXXX (seq. after V_S)
DF XXXX.10000 (non-seq. before V_S)
DI XXXX.10000 (non seq. after V_S)

7 1777777 ←8 per line→ 7 1777777

Multiplier Result

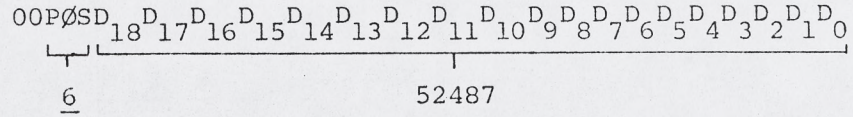


Decimal

DE XXXX (seq. before V_S)
DG XXXX.10000 (non-seq. before V_S)

6 524287 ←8 per line→ 6 524287

Multiplier Result



NOTE: The sign bit should always be 0 before V_S.

3. DELAY VALUES and EXCHANGE DATA

Octal

DL 6000

LEFT - RIGHT

1 1 3 377 3 3 17 ←4 per line→ 1 1 3 377 3 3 17

14 Lines Total: Line 1 = 1 left 1 right 2 left 2 right

Line 14 =27 left 27 right Left Test Delay Right Test Delay

LEFT		RIGHT	
1 1 1 1	37	1 1 1 1	37
	37		37
	37		37
	37		37

Decimal

DM 6000

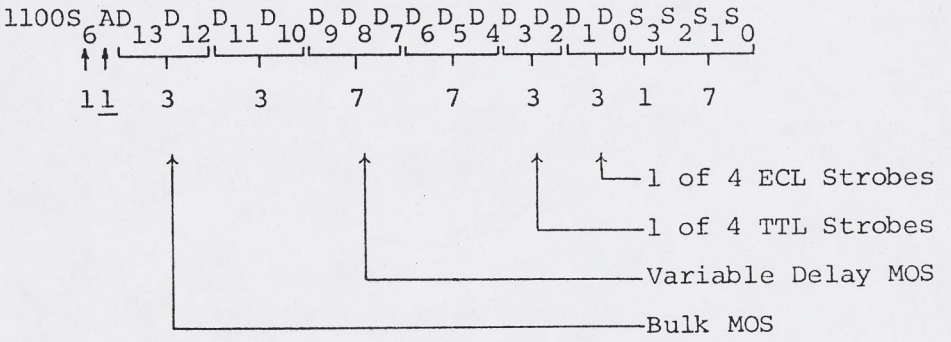
LEFT - RIGHT

1 1 16383 15 ←4 per line→ 1 1 16383 15

14 lines total in same order as above

LEFT		RIGHT	
1 1 1 1	31	1 1 1 1	31
	31		31
	31		31
	31		31

Delay Word

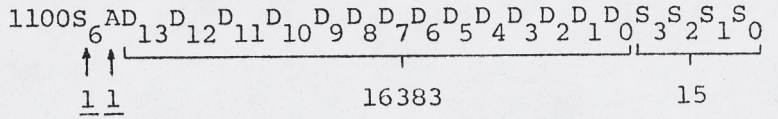


Exchange Data

CM CL SM SL

Sin Input Mux Adr
Cos Input Mux Adr
Sin Output Mux Adr
Cos Output Mux Adr

Delay Word



Exchange Data

Same as for octal

4. SYSTEM MONITOR MEASUREMENTS (2 ANT PROTOTYPE)

DN 6100 (octal)

DO 6100 (decimal)

	1	2	3	4	5	6	7	8	Out of Spec Code:
1.	0 2500* (+5 SC)	0 2500* (+5 D/M)	0 XXXX	0 2600* (-5.2 D/M)	0 2600* (-5.2 SC)	0 1200 (-12 D/M)	0 1200 (-12 SC)	0 2800 (+28 D/M)	0 = In spec 3 = Emergency Low
2.	0 1500 (+15 SC)	0 1500 (-15 SC)	0 900 (-9 SC)	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	5 = High 7 = Low
3.	0 1000* (02V D/M)	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	For an Emergency High condition in either the SC or D/M rack, the D/M rack will be automatically powered down and all error codes will contain either an 8 or 9 or a punctuation character.
4.	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	
5.	0 750* (Mult Clk)	0 750* (Dly Clk)	0 750* (Cont A Clk)	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	
6.	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	
7.	0 1100* (SC Temp)	0 1100* (SC Temp)	0 1100* (D/M Temp)	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	
8.	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	

NOTES:

1. The nominal measurement is shown above in decimal. For octal display, only the measurement is in octal.
2. Measurements marked * must be doubled to obtain the value.
3. The user must enter the decimal point mentally.
4. Clock measurements are of the peak value of the sinewave 100 MHz clock.
5. SC = System Controller Rack D/M = Delay-Multiplier Rack.
6. XXXX = Inputs not used in 2 Ant Prototype and spare inputs. These are not all zero on the display.
7. Full range temperature = 81.90°C.

5. GO/NO GO RESULTS

DP 6200 (octal only)

LEFT - RIGHT

	COS		SIN			COS		SIN	
	M	L	M	L		M	L	M	L
1	1	1	1	1	←4 sets per line→	1	1	1	1

9 Lines Total: Line 1 = 1 left 1 right 2 left 2 right 3 left 3 right

Line 9 = 25 left 25 right 26 left 26 right 27 left 27 right

6. RAM DATA SET

DQ XXXX (octal only)

17777777

↕ Total of 8 words

17777777

Computer Word Bit:

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		1	7			7			7			7			7			7			7		

7. PARITY ERROR ADDRESSES

DR 6300 (octal)

DS 6300 (decimal)

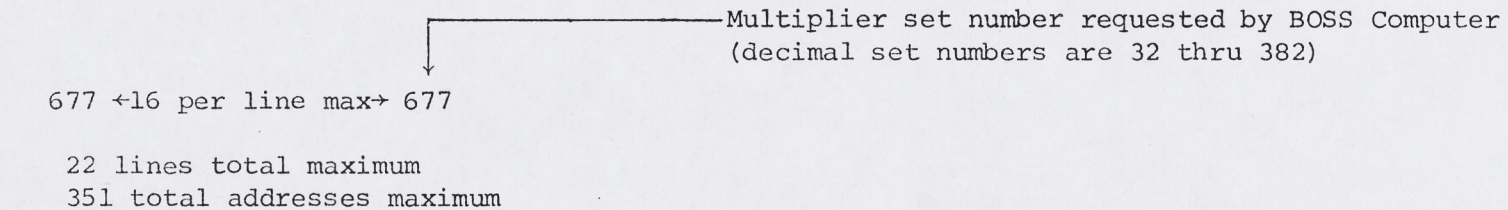
6 677 ←8 per line→ 6 677

↑ ↑ Computer Word No. Boss → SC

↑ Blanking Time in which error occurred (1 thru 6)

8. ADDRESSES OF MULTIPLIERS REQUESTED

DT 6400 (octal)
DU 6400 (decimal)



22 lines total maximum
351 total addresses maximum

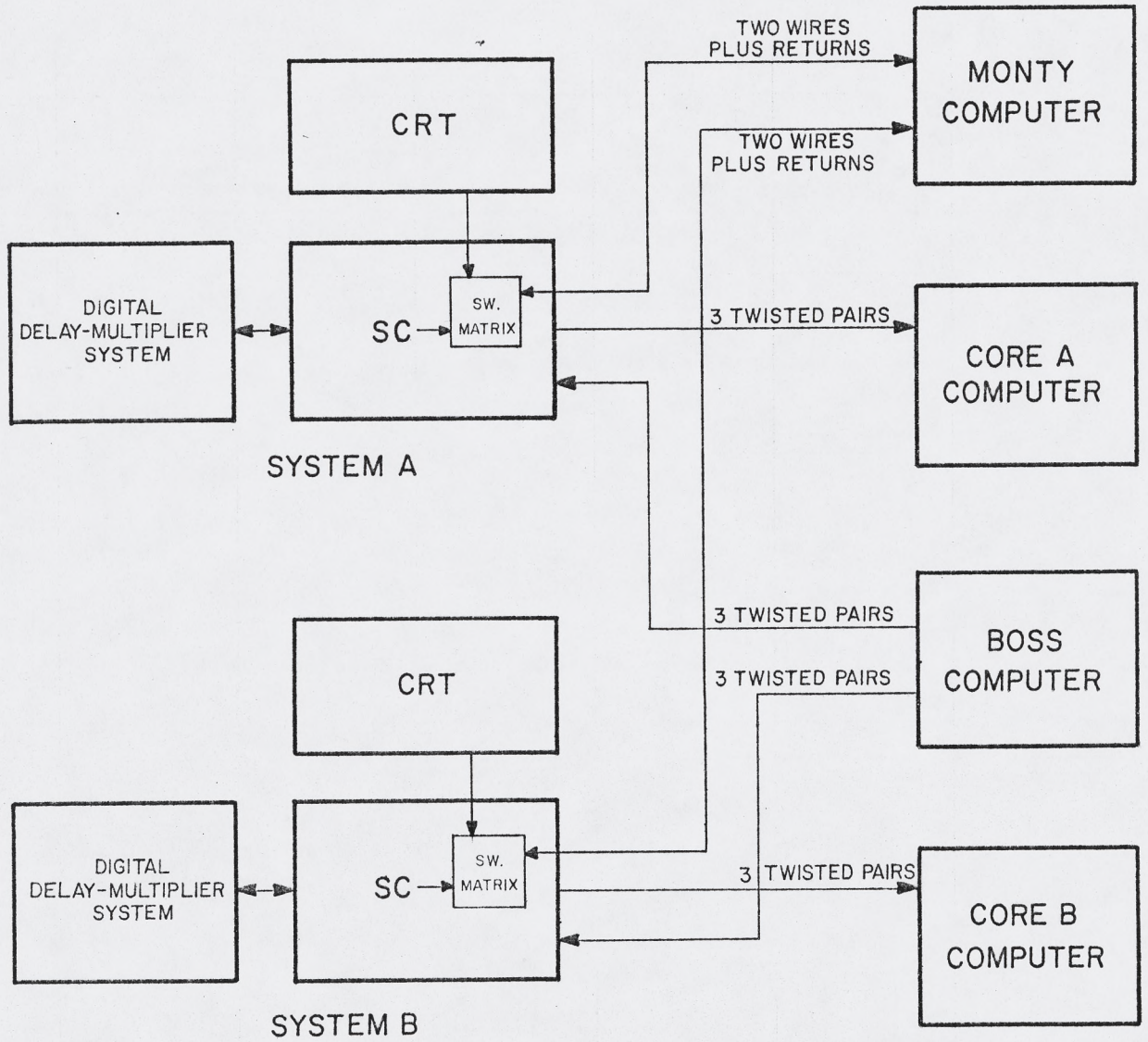
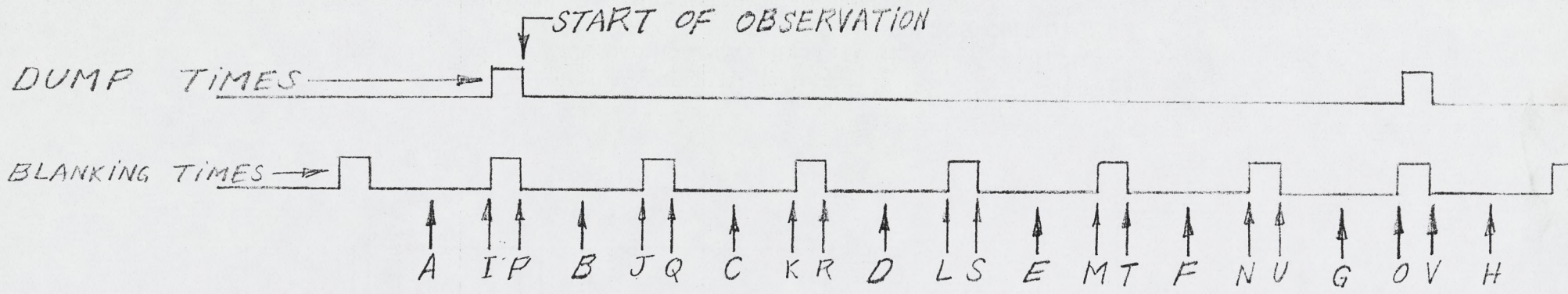


FIGURE I

COMMUNICATIONS SYSTEM BETWEEN SYSTEM CONTROLLER AND VLA SYNCHRONOUS COMPUTERS



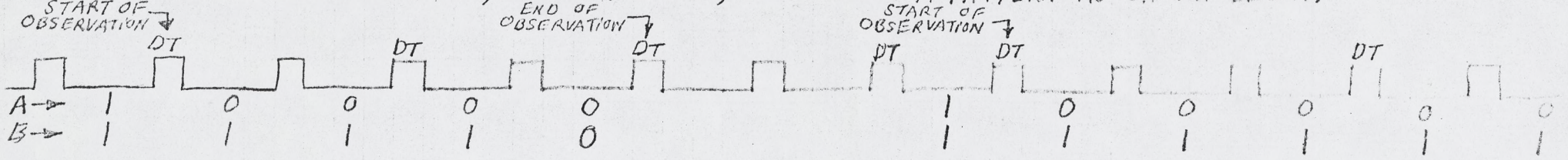
DATA OBTAINED BY SC AT THIS TIME

DATA APPLIES TO THIS TIME

DATA SET SENT TO VLAC AT H	1	2	NOTES
DELAY	G	H	
SYSTEM MONITOR	G	G	IF AN "OUT OF SPEC" CONDITION IS DETECTED AT B, C, D, E OR F THE FIRST ONE DETECTED WILL REPLACE G IN BOTH COLUMNS AT LEFT.
GO/NO-GO	J→O	B→G	ALL GO/NO GO's ARE OR'ED INTO MEMORY UNTIL RESET.
PARITY, VLAC→SC	B→G	B→G	ALL BAD PARITY ADDRESSES (UP TO 64) ARE STORED IN MEMORY & RESET EVERY DT.
MULTIPLIERS DESIRED	A	→	APPLIES TO ALL DATA FROM B TO END OF OBSERVATION
TIME	G	O	
MUX. ADDRESS	O	B→G	
MULTIPLIERS	B→G	O	
EXCHANGE DATA	O	H→	DELAY LINE(S) CONTINUE TO BE EXCHANGED UNTIL RESET.

NOTE: ABOVE COVERS DATA FROM SC TO CORE COMPUTER – SEE TABLES 1&3. COLUMN 1 INDICATES WHEN THE SC's STORAGE RECEIVES THE DATA – FROM EITHER CORE COMPUTER, DELAY MULTIPLIER OR SC's INTERNAL CONTROL. COLUMN 2 INDICATES WHEN THIS DATA WAS USED OR GENERATED.

BITS A&B IN TABLES 2&4, COMPUTER WORD 0, WILL FOLLOW A PATTERN AS SHOWN BELOW:



SC TO VLAC DATA RELATIONSHIPS

A.M. SHALLOWAY
11/13/91
REV 0