VLA TECHNICAL REPORT #3

MODULE T5

IF RECEIVER

A. R. Thompson May 1975

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D13450Z1

D13450Z2

D13450Z3

VII. Data Sheets and Application Notes

MD614

µA733

LH0022

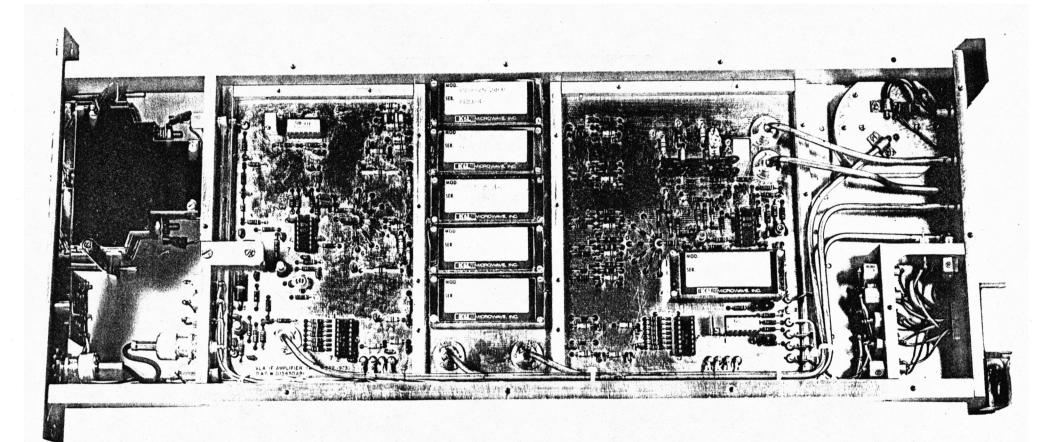
FMA120

5082-3081

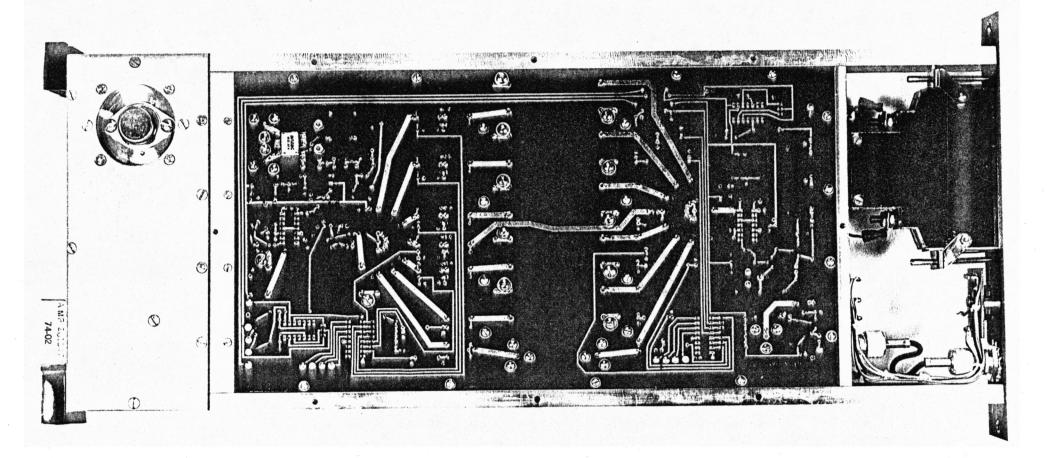
5082-7300

5082-2800

H. P. Application Note 936



IF Receiver, right side with cover plate removed



IF Receiver, left side with cover plate removed

October 18, 1974

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Connector Shield	B13450M1
Mounting Plate for Integrated Circuit	B13450M7
Heat Sink Support	B13450M9
Mounting Frame for Circuit Board	C13450M11
Guides	B13050M4
Machanian Davis for Davis similar Orbits Describing	
Mechanical Parts for Semi-rigid Cable Assembly	
Connector to P.C. Board	B13450M14
Cable Clamp	B13450M15

I. (b) Related Publications and Memoranda

VLA Electronics Memo #115

Bandwidths for the VLA Receiving System

A. R. Thompson July 18, 1973

VLA Electronics Memo #118

The Bandwidth Effect ('Delay Beam') for a Synthesis Array and Related Requirements for the IF Filter Characteristics A. R. Thompson November 13, 1973

VLA Electronics Memo #129

The Response of the VLA to Interfering Signals

A. R. Thompson January 1975

II. General Description

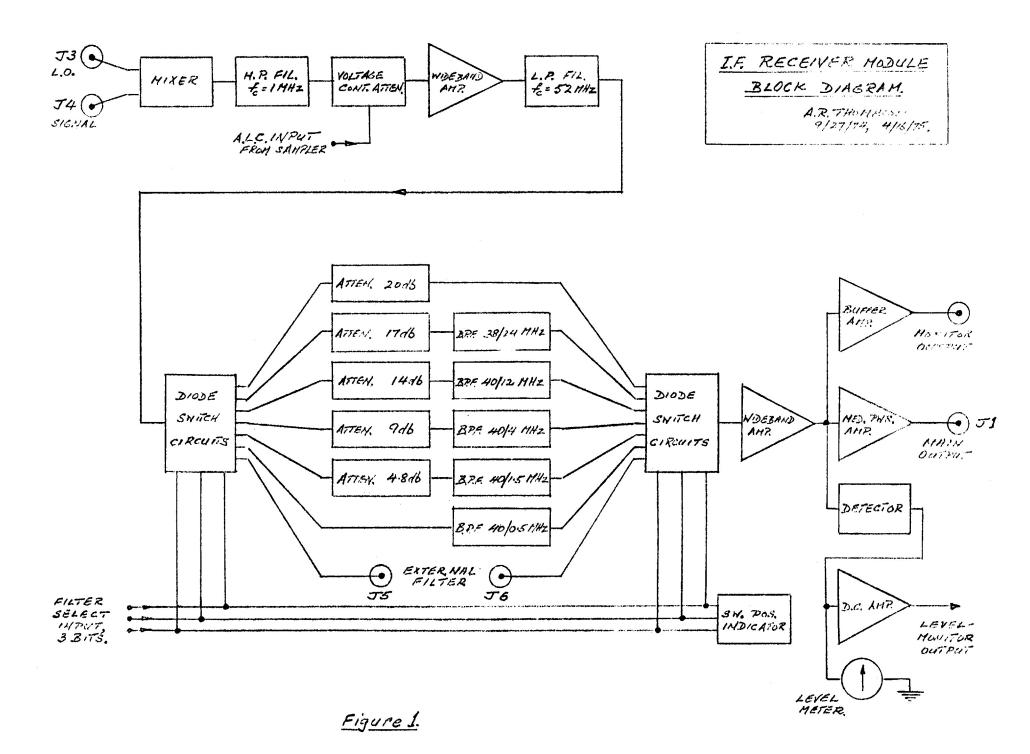
The function of the IF Receiver module is to accept IF signals in any one of the four frequency bands 1300-1350 GHz, 1400-1450 GHz, 1550-1600 GHz and 1650-1700 GHz from the modem, to convert the signals to a frequency band 0-50 MHz, and to amplify them to a level of 45 mw (1.5V rms in 50 ohms). The signals are then passed to the digital sampler. The IF Receiver also allows selection of one of six different signal bandwidths from 0.5 to 50 MHz by means of switched filters, and it provides for automatic level control to hold constant the signal level at the sampler.

A block diagram of the IF Receiver is shown in Figure 1. Input levels to the mixer are -20 dBm in 50 MHz bandwidth for the signal and 8 ± 4 dBm for the local oscillator. The L.O. signal is supplied by the L.O. Offset module and its frequency is variable under computer control so that when a narrow IF bandwidth is used the signal can be selected from any part of the incoming 50 MHz band.

The mixer is followed by a high pass filter with cutoff frequency approximately 1 MHz, a voltage controlled attenuator with a range of 40 dB and a broadband amplifier with gain of approximately 46 dB. The signal next encounters a low pass filter with a cutoff frequency of 52 MHz (-3 dB point). The -1 dB point of the filter is 50 MHz and this together with two earlier filters in the signal path which have -1 dB bandwidths of 50 MHz*results in a signal level of -3 dB at 50 MHz. Diode switch networks then direct the signal through one of seven paths, one of which passes the full signal band of 1-50 MHz, five others contain filters which pass bandwidths of 24, 12, 4, 1.5 and 0.5 MHz each centered on 38 or 40 MHz[†], and the last makes provision for an external filter. Attenuators are incorporated in the signal paths so that the total signal power through each is approximately the same. The filter path desired is selected by setting three TTL levels as indicated in Table 1. These filter select signals come from the IF Control module.

The signal next passes through another broadband amplifier, then to a medium power broadband stage and finally to the output terminal. The frequency response of the amplifiers described here as broadband is essentially flat from 1 to 50 MHz. At the input of the final stage a part of the signal is tapped off to a monitoring detector and also through an isolating stage to a front-panel monitor terminal. The output voltage at the monitor terminal is about 0.06 of that at the main output J1 when both are terminated in 50 ohm loads. The *Later changed to -3 dBm at 50 MHz, see VLA E.M. #129.

[†]25 MHz center frequency was used in the prototype design, but later changed to 40 MHz to obtain better rejection of the image response at the mixer input.



Filter Path Number	Selec MSB	ct S:	ignal LSB	Filter Bandwidth (-3 dB)	Attenuator Network
Ο	0	0	0	49 MHz	20 dB
1	0	0	1	24 MHz	17 dB
2	0	1	0	12 MHz	14 dB
3	0	1	1	4 MHz	9 dB
4	1	0	0	1.5 MHz	4.8 dB
5	1	0	1	0.5 MHz	0 dB
6	1	1	0	External Filter	0 dB

TABLE 1. Characteristics of Switched Filter Paths

detector output drives a front panel meter and an amplifier with a gain of 10 that provides an output monitoring voltage.

On the front panel of the module there are the detector current meter, a BNC jack which provides the monitor signal, and an LED numeric indicator which shows a number in the range 0 to 6 indicating the filter channel chosen.

The high pass filter immediately following the mixer was originally included because in the first version of the VLA electronic system the fringe rotation was introduced at that mixer. A digitally generated signal at approximately 100 kHz was added to the local oscillator, and the effects of unwanted 100 kHz sidebands on the oscillator were eliminated by this filter. The filter is also deemed to be beneficial because the PIN diodes used in switching between the bandpass filters are specified as "useful down to 1 MHz." The degree of distortion that the switching diodes would cause below 1 MHz has not, however, been investigated in detail. Typical values for the frequency response of the high pass filter are as follows:

-3	dB	1.2 MHz	-20 dB	730 kHz
~6	dB	1.0 MHz	-30 dB	590 kHz
-10	dB	920 kHz	-40 dB	480 kHz

Four IF Receiver modules are used for each antenna. They are located in rack N in the control building and occupy slots 4, 6, 8 and 10 of bin S.

III. Circuit Details

All of the electronic components except the final amplifier and the LED filter-channel indicator are mounted on a single printed circuit board of dimensions 12.68x6.45 inches. A circuit diagram of the complete module is shown in Figure 2.

The mixer is an Anzac flatpack model, MD614, with a nominal range of input frequencies of 0.6-2 GHz. An OSM connector on the circuit board, TP1, allows a test signal in the intermediate frequency range to be injected immediately after the mixer. Inductors Ll to L5 and the associated capacitors form a high pass filter of 50 ohms impedance with a cutoff of frequency of approximately 1 MHz. This filter is adapted from a design given on p.150 of Electrical Filters published by White Electromagnetics Inc.

The voltage controlled attenuator which follows the filter contains two 5082-3081 PIN diodes and is taken from a design in Hewlett Packard Application Note No. 936, figure 6 (see section VII). The signal level at C6 is decreased over a range of 40 dB as the voltage at the junction of C12 and R36 goes from zero to about +10 volts. The ALC control voltage coming into the module is buffered by an LH0022 operation amplifier which has a balanced input and a voltage gain of two.

The first broadband amplifier in the signal path is a µA733 with pins 4 and 11 connected to give the highest gain. This amplifier or its equivalent is manufactured by several companies including Fairchild (µA733), Motorola (MC1733), National Semiconductor (LM733), and Signetics (µA733). It is followed by a 2N5197 emitter follower which drives the 52 MHz low pass filter FL1. Resistors R35 and R32 provide matching impedances for the filter.

The signal next passes through one of seven paths selected by the switching PIN diodes^{*}CR4 to CR24. For the path chosen the three diodes that otherwise block the signal are turned on by signals from the SN7445 BCD to decimal decoders which have open collector outputs. In the off condition the SN7445 collectors are returned to ± 15 volts through resistors Rl and Rl4 so that the diodes in the open paths are back biased by $\pm 15V$ on one end of the path and $\pm 1V$ to 6.0V on the other. The latter voltage results largely from the drop across R52 and R48 which carry the current drawn by the diodes in the open path. The SN7445 collector voltage in the on condition should be approximately 0.2V and the currents through the forward biased diodes, which are

*Pin diodes were chosen for the switching since for a given forward current in the on condition they pass much higher signal levels without distortion than other types of diodes. This was verified by tests on other diodes including IN914, IN270 and 5082-2800. Aertech A5S139 is an equivalent replacement for H.P. 5082-3081.

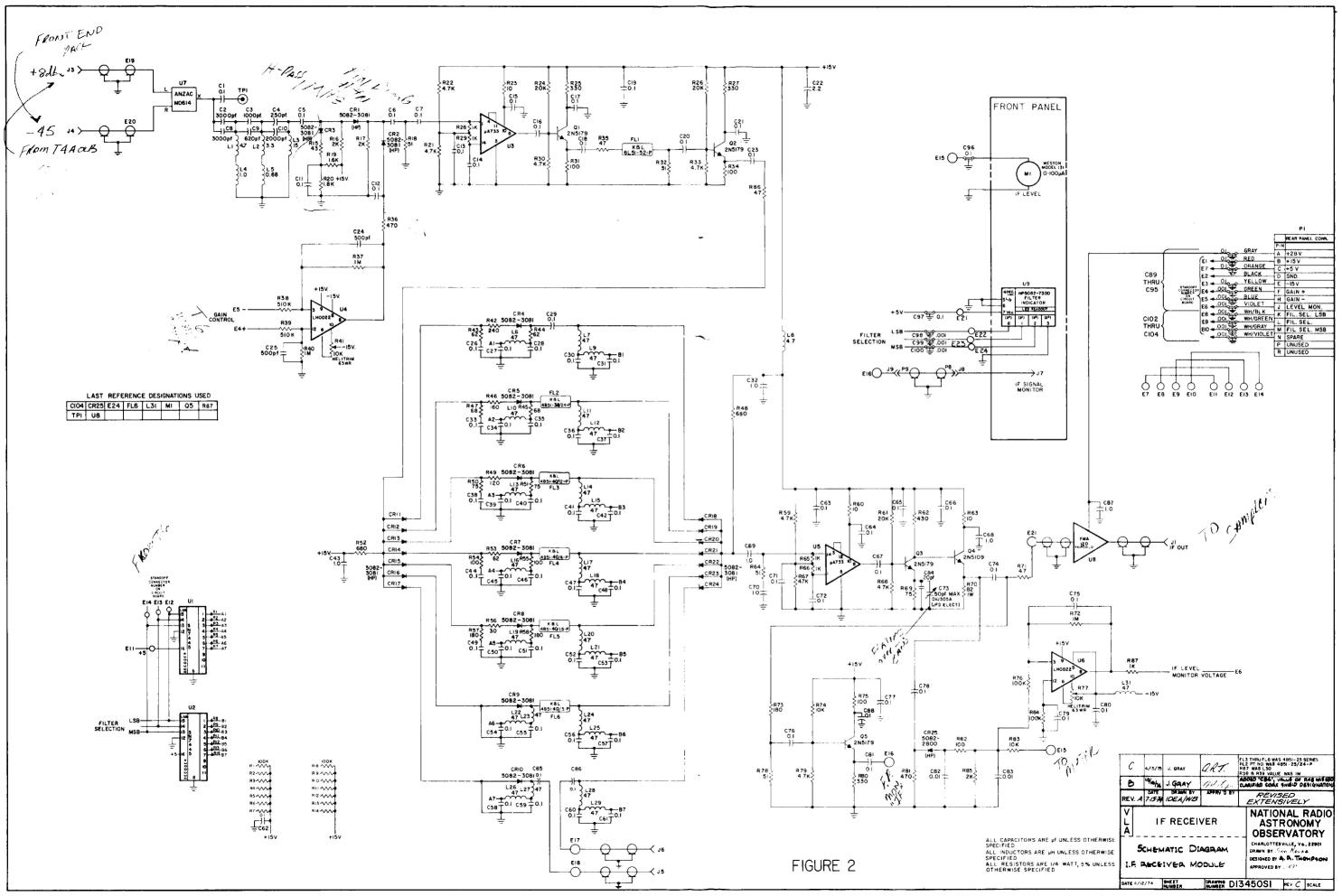
limited by R52 and R48, lie in the range 13 to 20 ma. Resistors R86 and R52 provide matching terminations for the filter-attenuator combinations, and the signal paths on the printed circuit board between the emitter of Q2 and the input to U5 are of width chosen to present 50 ohms impedance to the ground plane on the front side of the board. With the 1/16 inch G10 circuit board the conductor width for 50 ohm impedance is approximately 0.118 inches, depending somewhat upon the dielectric constant of the board material. In the artwork 6.0mm width tape was used for 2:1 reduction in the subsequent photographic process. The filter and switching circuitry occupy a central location on the board. In order to prevent unwanted signal paths between the stages that precede and follow the filters, inductors or resistors are inserted into the power supply, filter selection and monitor level conductors that run between the input and output ends of the board.

Amplification after the filters is provided by U5, a µA733 with pins 3 and 13 connected for the intermediate gain condition. This is followed by Q3 which has a voltage gain of about 4 with a 50 pf variable capacitor to ground on the emitter to allow adjustment of the overall frequency response. The next stage is Q4, a 2N5109 emitter follower, the collector of which has a heat sink to the module. The maximum signal level that can be obtained at the emitter of Q3 is approximately 5V peak-to-peak. Resistor R71 provides matching to the 50 ohm 0.141 coax that takes the signal to the input of the final amplifier, a Fairchild FMA120 which is mounted directly on the module for heat sinking purposes. Note that although the FMA 120 is accessible from the exterior of the module, it cannot be removed without unsoldering connections inside the module.

The emitter of Q4 also drives emitter follower Q5 which provides isolation for the signal monitor output on the front panel. Another signal from Q4 goes to a diode detector, CR25, the output of which drives the front panel meter and operational amplifier U6 which has a voltage gain of 10. The output of U6 is monitored by the computer through the IF Control Module.

Power supply currents drawn are as follows:

+28V	180 ma
+15V	220 ma
+5V	180 ma
-15V	4 ma



IV. Some Assembly Details

Filters

When inserting the filters FLl to FL6 the two hold-down screws should be tightened before the four pins are soldered. This is to ensure a close contact between the board and the filter case. The presence of a gap will allow signals to propogate along the filter case and the full out-of-band rejection of the filter will not be achieved.

OMQ Connectors

When fitting-0.141 inch semi-rigid cable to OMQ connectors it will be found easiest to fit the OMQ to the cable first, then bend to the desired shape and fit the circuit board connector last.

Mixer

The hole in the circuit board into which the mixer fits must be just large enought to allow the mixer to mount with the leads flush with the surface of the conductors to which they are soldered. The RF, LO, and IF conductors should extend not quite up to the edge of the hole so that they cannot short to ground on the mixer case.

Test Connector TP1

The end of the center conductor of the OSM connector which extends on the back side of the board should be cut off after soldering as it may otherwise be long enough to short on the left side plate of the module. If the teflon insulation of the connector protrudes beyond the back of the connector it should be cut off flush with the back surface to that outer part of the connector makes good contact with ground plane of the board.

V. Initial Adjustment and Servicing

For test and adjustment of the IF Receiver module it is convenient to make up a small control box. This should have a potentiometer and three switches mounted in it, a few feet of cable terminating in a connector to mate with the 14 pin module connector, and leads with bananna plugs to connect to the required power supplies (+5V, +15V, -15V, +28V). The switches ground or open the three filter select lines to the module, and the potentiometer provides an adjustable voltage in the range 0 to +10V which is applied to the positivegoing gain input, the negative going one being grounded.

The module contains only three preset adjustments, R41 and R77 which set the offset voltages of the operational amplifiers U4 and U6, and the emitter capacitor of Q3. Test and adjustment procedures are as follows. Before applying power to the module for the first time inspect the board for any short circuits at soldered joints etc. Check that the power supply voltages are precisely adjusted and apply power to the module. Ground the two gain control terminals E4 and E5 on the board and adjust the Helitrim R41 for zero output on pin 8 of the operational amplifier U4. Then for the other operational amplifier, U6, ground the junction of R76 and R83 and adjust R77 for zero output on pin 8.

Next set up the module with the test input, TP1, fed from a sweep signal generator covering the range zero to about 100 MHz; Wavetek Model 2001 is recommend, using band 1. The RF output level of the sweper should be -45 dBm and the sweep output should drive the x scan of an oscillosope with frequency response flat to over 50 MHz; Tektronix 475 is recommended. The IF output of the module, from J1, is then connected by a 50 ohm cable to the y input of the oscilloscope, and the cable should be terminated in 50 ohms at the oscilloscope input terminal. Set the gain control voltage for zero attenuation (zero volts) and the filter select switches to position zero giving the full 1-50 MHz bandwidth. With correct operation the output on the oscilloscope should look like Fig. 3(a). Adjustment of C73 will be required to obtain the optimum response which is flat within +0.5 dB from 1 to 50 MHz.* As the output level of the sweeper is varied the display should show signs of overloading when the output signal level is between 10 and 15V peak-to-peak. If the response is not flat but shows unwanted maxima or minima, check the switching voltages to be sure that all diodes except those in the desired signal path are biased off. If the problem is not associated with the switches and filters check through the

*For final adjustment the gain at 50 MHz should be set 0.5 dB (6% in voltage) above that at the low end to allow for differential attenuation in the cables to the samplers.

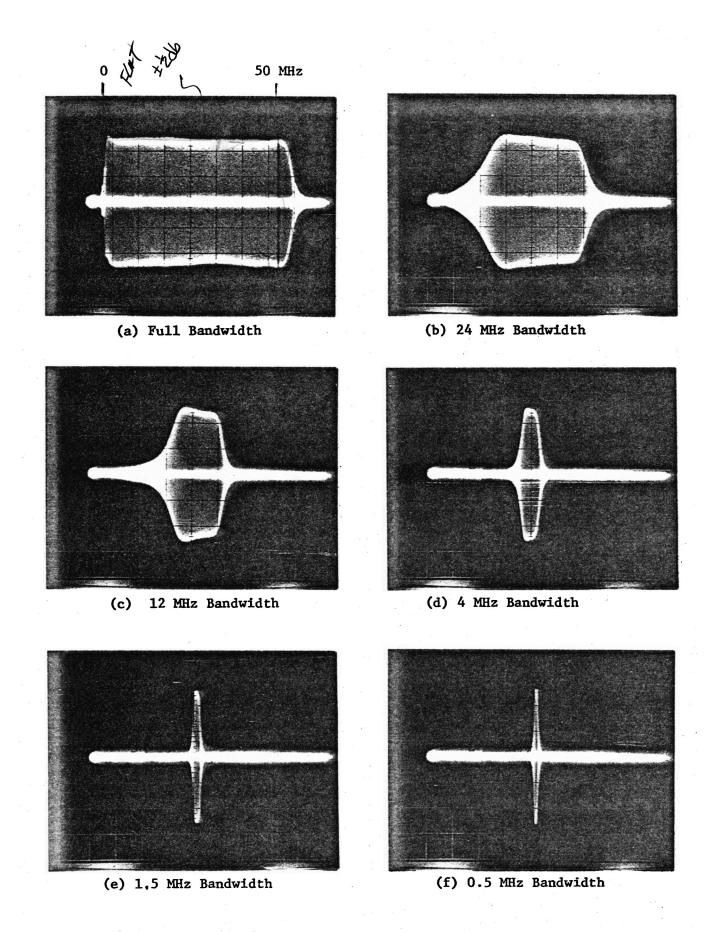


Figure 3 Frequency response with each filter as displayed using Wavetek 2001 sweeper and Tektronix 475 oscilloscope. Vertical scale was 2V per cm and input power levels at TP1were -43, -49, -53, -55 and -58 dBm for cases (a) to (f) respectively. Filters are the prototype units with 25 MHz center frequency.

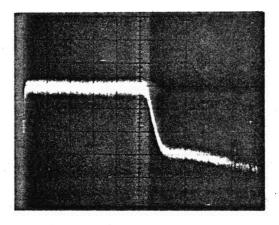
circuit with an oscilloscope probe to attempt to locate the trouble. If the output shows signs of distortion when the level is a little below 10V peak-to-peak, try replacing transistors or μ A733 amplifiers, since the gain and dynamic range of individual units can differ significantly. In particular check Q3 (2N5179). The input signal level at TPl for 10V peak-to-peak output is typically -43 dBm.

Increase the gain control voltage and check that the response remains flat as the signal level decreases. In one module tested insufficient attenuation at low frequencies resulted from a defective capacitor Cl2.

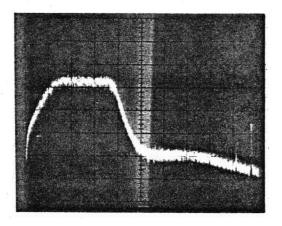
When the unit is operating correctly in the full bandwidth mode examine the response in the other filter positions. Examples of correct operation are shown in Figure 3. In switch position 6, for the external filter, a 20 dB attenuator connected between J5 and J6 should give an output identical to that in the full bandwidth position. The 10V peak-to-peak output without distortion should be obtainable with each filter position, but it will be necessary to reduce the sweeper output in going to narrower filters because of the lower loss in the attenuator network immediately preceding the filter input.

To test for adequate rejection of out-of-band signals in the narrower filter positions a spectrum analyzer is most convenient because of its logarithmic response. A source of noise flat over the required frequency can be used at TP1 instead of the sweeper. A broadband, flat-response amplifier with the input correctly terminated with a resistive load can be used as a noise source; the Hewlett Packard 8447F amplifier with the two sections connected in series is very satisfactory. Examples of the output spectrum displayed on a Hewlett Packard 141T spectrum analyzer with 8553B RF section and the above amplifier used as a noise source are shown in Figure 4. Insufficient out-of-band rejection is most likely to arise from the filters not being mounted close to the board, as mentioned in section IV, or from the switching diodes in other paths not blocking the signal correctly.

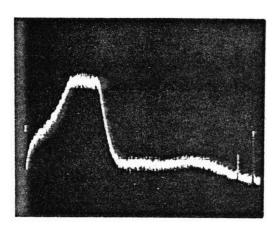
Finally one should test the operation of the mixer which has thus far been omitted from the signal path. A sweeper covering the 1-2 GHz range, or some part of it, should be fed into J4, and a local oscillator signal at some frequency in the same range inserted at J3. The oscillator level should be 8 dBm and IF outputs similar to those shown in Figure 3 should be obtainable. For filter path zero the required signal level for 10V peak-to-peak output should be about -33 dBm.

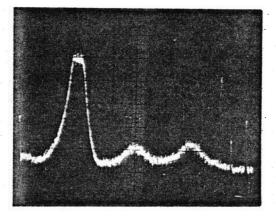


(a)



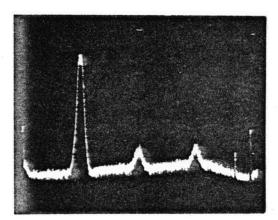
(b)

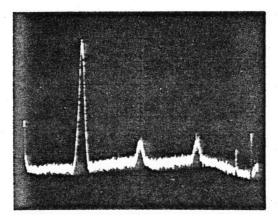




(c)







(e)

(f)

Figure 4 Frequency response with each filter as displayed on HP 141T spectrum analyzer using broadband noise input at TP1. Gain was adjusted to give approximately half scale reading on front panel meter. Frequency range was 0 to 100 MHz. Vertical scale was 10 dB per cm. Low level harmonics of the IF signal are seen in cases (d), (e) and (f). The signals at the extreme right on each trace are FM station pickup. Filters are the prototype units with 25 MHz center frequency.

Following is a list of voltages at various points in the circuit which may be useful for troubleshooting. The figures given were measured from one satisfactorily-operating unit (serial Al) and reasonable tolerances should be borne in mind when comparing them with values for other units.

U3	pin 8	11.OV
U5	pin 8	10.8V
Ql	emitter	1.25V
n	base	2.0V
11	collector	10.9V
Q2	emitter	1.2V
11	base	1.9V
н	collector	11.2V
~ ~	- in the second	1.2V
Q3	emitter	1.20
Q3 "	base	1.2V 1.9V
	0	
п	base	1.9V
17 17	base collector	1.9V 7.2V
" 94	base collector emitter	1.9V 7.2V 6.4V
" " Q4	base collector emitter collector	1.9V 7.2V 6.4V 13.9V

Signal levels through the same unit for the wideband (number zero) filter path were measured using a Wavetek 2001 sweeper and Tektronix 475 oscilloscope with P6201 FET probe. Results were as follows:

Input level at TP1: -43 dBm Pin 8 of U3, 0.8V p-p at low end decreasing to 0.6V p-p at 50 MHz Emitter of Q2, 0.35V p-p at low end decreasing to 0.23V p-p at 50 MHz Pin 8 of U5, 0.8V " " " " " 0.6V " " " " Emitter of Q4, 3.2V · ", flat Across 50-ohm load at J4, 10V p-p, flat

The contribution of the internal noise from the IF Receiver should be less than 1% of the total noise level. In normal system operation this is most easily checked by examining the monitor output at the front panel BNC connector with a spectrum analyzer. Disconnecting the input signals at the 4-way power divider at the back of the rack should cause the output noise level to fall by 20 to 26 dB.

BILL OF MAICHIALS

REV	DESCRIPTION OF CHANGE	DRAWN BY	DATE	APPRV'D BY	DATE
В	PT. NO. 8: CAPACITOR VALUE WAS 212 PT. NO. 9: 8121-050-651-103M ADDED THIS SHEET	J. GRAY	12/11/24		
С	RELEASED FOR MICROFIMING	J. GRAY	12 JAN 1975	CPace	1/13/15
D,	ITEMS 17 & 18; ADDED AERTECH NO. AS ALTERNATE SOURCE OF SUPPLY ITEM 20; PT. NO. WAS 4B51-25/24-P ITEM 21; PT. NO. WAS 4B51-25/12-P ITEM 22; PT NO. WAS 4B51-25/4-P ITEM 23; Pt. NO. WAS 4B51-25/ 1.5-P ITEM 24; PT. NO. WAS 4B51-25/0.5-P ITEM 31; REMOVED L30 FROM REF. DESIGNATIONS AND REDUCED QUANITY TO 24 FROM 25 ITEM 39; QUANTITY WAS 54 ITEM 63; REMOVED R38 AND R39 FROM REFERENCE DESIG AND REDUCED QUANTITY FROM 5 ITEM 70; ADDED	J. GRAY	17 AP 75		4/17/75
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a na manana ang manana Manana ang manana ang ma	MICROFILIES DATE 5/13/25 BEV. LTR. D				
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T5	I.F. RECEIVER DWG.NO.	A1345073			

		BILL OF MATERIAL	MIGROFILMEN
X ELECTRICAL	MECHANICAL	BOM # <u>A13450Z3</u> REV D	DATE DATE PAGE OF
MODULE # T5	NAME I.F. TRANSMISSION	RECEIVER DWG # D13450P3 SUR	ASMB P.C. BOARD ASSY L.F. DWG #3450P4
SCHEMATIC DWG #	D13450S1 LOCATION	QUA/SYSTEM	PREPARED BY IDEA/WWB APPROVED C Former

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA
1		NRAO	D13450P4	P.C. BOARD ASSY I.F. RECEIVER	
2.	-	NRAO	D13450M13	P.C. BOARD	<u> </u>
3		ROB I NSON NUGENT	1CN-143-53	SOCKET 14 PIN	1
4	_	ROB I NSON NUGENT	1CN-163-53	SOCKET 16 PIN	2
5		CINCH	3LPS-3	TRANSISTOR SOCKET	5
6	*	ERIE	8121-050-651-104M	CAPACITOR ,1 UF	69
7	**	ERIE	8131-050-651-105M	CAPACITOR 1.0UF	6
8		ERIE	8141-050-651-225M	CAPACITOR 2.2 UF	1
9	C82&C83	ERIE	8121-050-651-103M	CAPACITOR .01UF	2
10	C73	JFD	DVJ 305A	CAPACITOR 4.5-50 Pf	
11	C2&C8	ARCO	DM19302J	CAPACITOR 3000 Pf	2
12	C10	ARCO	DM19202J	CAPACITOR 2000 Pf	
13	C3	ARCO	DM19102J	CAPACITOR 1000 Pf	1
14	· C9	ARCO	DM19621J	CAPACITOR 620 Pf	1
15	C4	ARCO	DM19251J	CAPACITOR 250 Pf	1

* C1, C5, C6, C7, C11-C21, C23, C26-C31, C33-C42, C44-C67, C71, C72, C74-C81, C85-C86, C88 ** C43 C68 C69, C70, C87, C32

MFG PART #

DM19501J

A5S139 5082-3081

5082-2800

4B51-38/24-P

4B51-40/12-P

4B51-40/4-P

4B51-40/1.5-P

4B51-40/0.5-P

6L51-52-P

1025-36

1025 - 32

1025-48

1025-20

1025-16

1025-60

2307-472

A2S800

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REF

DESIG

C24. C 25

CR1-CR24

CR25

E1-E16

FI 2

FL3

FL 4

FL5

FL G

FL1

LI

12

L3

L4

L5

L6.17

L8

L-L29L31

ARCO

KEYSTONE

AERTECH (OR) HEWLETT-PACKARD

AERTECH (OR) HEWLETT-PACKARD

K AND L MICROWAVE

DEL EVAN

DELEVAN

DELEVAN

DELEVAN

DEL EVAN

DELEVAN

DELEVAN

MECHANICAL BOM # A13450Z3 REV D DATE _____ PAGE ____ OF ____

MANUFACTURER

DESCRIPTION

CAPACITOR 500 Pf

SCHOTTKY DIODE

FILTER 4 POLE BANDPASS

FILTER 6 POLE LOWPASS

INDUCTOR 4.7 Uh

INDUCTOR 3.3 Uh

INDUCTOR 15 Uh

INDUCTOR 1.0 Uh

INDUCTOR .68Uh

INDUCTOR 47 Uh

MICROFILMED

INDUCTOR 4.7 Uh 1/2 W

PIN DIODE

TERMINAL.

TOTAL

OUA

2

24

1

16

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X ELECTRICAL	MECHANICAL BOM	4 # <u>A13450Z3</u>	rev	DATE	PAGE 3	OF <u>6</u>
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ietm #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	total Qua
33	Q1-Q3,Q5	RCA	2N5179	TRANSISTOR	4
34	Q4	RCA	2N5109	TRANSISTOR	1
35	R16, R17			RESISTOR 2.0 Kn, 1W, 5%	3
36	R19			RESISTOR 1.6 K.a. W, 5%	1
37	R20			RESISTOR 1.8 Ku, 4W, 5%	1
38	*			RESISTOR 4.7 Ka, W, 5%	8
39	**			RESISTOR 1.0 Ka, 4W, 5%	5
40	R24, R26,			RESISTOR 20Kr, W, 5%	3
41	R18,R32 R64, B78			RESISTOR 510, W, 5%	4
42	R23, R60, R63			RESISTOR 100, 1W, 5%	3
43	R15			RESISTOR 430, W. 5%	1
44	R25, R27 R80			RESISTOR 330, 7, 78, 5%	3
45	***			RESISTOR 1002, 1W, 5%	6
46	R35, R86 R71			RESISTOR 47Ω, ₩, 5%	3
47	R36,R81			RESISTOR 47012, ☆W, 5%	2
48	R43, R44, R53			RESISTOR 62., 글W, 5%	3
49	R42			RESISTOR 240 α , $\frac{1}{2}$ W, 5%	1

** R65, R66 R28, R29, **R87** *** R31- R34 P54, P55, R82- R75

DATE OF BERRY ITR

X	ELECTRICAL

MECHANICAL BOM # A13450Z3 REV

D

DATE _____ PAGE ____ OF ____6

IETM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	total Qua
50	R46	~~		RESISTOR 160 Ω , $\frac{1}{4}$ W, 5%	1
51	R47, R45			RESISTOR 680, 4W, 5%	2
52	C84	ARCO	DM19200J	CAPACITOR, 20pf	1
53	R48&R52			RESISTOR 680 a, 1W, 5%	2
54	R50, R51, R69			RESISTOR 750, 4W, 5%	3
55	R49			RESISTOR 1202, 1W, 5%	1
56	R56			RESISTOR 300, 4W, 5%	1
57 -	R57, R58 R73			RESISTOR 180 <i>n</i> , 1/W, 5%	3 -
58	R62			RESISTOR 430 a, 1W, 5%	1
59	R83, R74			RESISTOR 10Ka, 4W, 5%	2
60	R1-R14, R76, R84			RESISTOR 100Ka, 4W, 5%	16
61	R70			RESISTOR 82a, W, 5%	1
62	R41,R77	BECKMAN	63WR	TRIMPOT 10Ka 10 TURN	2
63	R37,R40, R72			RESISTOR 1M&,录W 5%	3
64	TP1	OMNI SPECTRA	OSM244-2	CONNECTOR, R.F.	1
65	U3, U5	SIGNETICS	UA733	VIDEO AMPLIFIER	2
66	U4, U6	NATIONAL SEMICONDUCTOR	LH0022	OPERATIONAL AMPLIFIER	2

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X ELECTRICAL MECHANICAL BOM # A1345073 REV DATE PAGE OF	X ELECTRICAL	MECHANICAL	BOM # <u>A1345073</u>	REV	<u>D</u>	DATE	PAGE	5	of <u>6</u>
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IETM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	total Qua	
67	U1, U2	TEXAS INSTRUMENT	SN7445	DECODER/DRIVER	2	
68	U7	ANZAC	MD614	MIXER	1	
69			#22 AWG 1" LG	WIRE BUS	1	
70	R38, P30			RESISTOR, 510K, 1/4W, 5%	?	
						1
				- 1		

MICROFILMED

NATIONAL RADIO ASTRONOMY OBSERVATORY

ELECTRICAL

X MECHANICAL

BOM #A13450Z3

rev D

DATE _____ PAGE ____ OF ____6

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA
11- 0.7		WQLDON	NW875	FLAT WASHER #4 NYLON	4
71 72			#4-40 X .250 lg.	SCREW, PAN HEAD, ST. ST'L.	12
יר 7,2		***	#4 NOM.	WASHER, FLAT, ST.ST'L.	8
יר 7.3		PENNTUBE PLASTICS CO.	0-6591A, 22 AWG 1W NATURAL	TUBING, TEFLON	2 in.
זר 74			∦2-56 x .250 lg.	SCREW, PAN HEAD, ST. ST'L.	.2
7,5 17,			#2-56	NUT, HEX, ST. ST'L.	2
7.6 ר	•		#2 NOM.	WASHER, FLAT, ST. ST'L.	2
7,7					
78		-			
7,9					
80					
81′					
8,2		· · · · · · · · · · · · · · · · · · ·			
83					
84					
85					
8,6					

MIGRUFILMED DATE 5/13/20 DEREV. LTR

REV	DESCRIPTION OF CHANGE	DRAWN	DATE	APPRV'D BY	DATE
LTR	RELEASED FOR MICROFILMING				
A	ADDED THIS SHEET	J. GRAY	1/12/ 75	Parc	17375
	· · · · · · · · · · · · · · · · · · ·		15		
					ļļ
	DATE 5/13/25 STORE REV. LTR				
+ + + + + + + + + + + + + + + + + + +					
MAT	ONAL RADIO ASTRONOMY OBSERVATORY E: I.F. TRANSMISSSION RECEIVER, "T5", P.C. BOARD	PROJ: VL		Y	
1 1 1 2	DWG.NO.	A134 50Z 2		······································	

X ELECTRICAL	MECHANICAL	BOM # A1345022	REV	DATE	PAGE	<u>1</u> OF <u>2</u>
MODULE #	NAME IF TRANSMISSION	RECEIVER DWG # D1345	terrent and a state of the stat	ASMB P.C. BOARD D		
SCHEMATIC DWG #	D13450S1 LOCATION	QUA/S	YSTEM <u>4</u>	PREPARED BY	21/74-	ROVED Ctace

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		NRAO	B13450P2	P. C. BOARD DISPLAY ASSEMBLY		
2		NRAO	B13450M16	P. C. BOARD DISPLAY	1	
3.		ROBINSON NUGGET	INC-236-S1	I.C. SOCKET 28 PIN (MODIFIED TO 8 PIN)	1.	
4	U9	HEWLETT PACKARD	5082-7300	NUMERIC DISPLAY	1	
- 5	E7E10	KEYSTONE	1502-3	TERMINAL	4	
6	-	WALDON	2101-04-00	LOCKING TERMINAL	1	
			<u></u>			
	1					
		· · · · · · · · · · · · · · · · · · ·				

MICROFILMED DATE 5/13/25 BY REV. LTR A

ELECTRICAL BOM # A13450Z2 REV DATE PAGE 2 OF 2		ELECTRICAL		BOM # <u>A1345022</u>	REV	DATE	PAGE	2	OF	2	
--	--	------------	--	-----------------------	-----	------	------	---	----	---	--

IETM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	total Qua	
7		G.E. ELECTRONICS	13-602-C	STANDOFF	2	
8			#4-40x.250 LG.	SCREW, PAN HEAD S.S.	2	
					-	
				m	-	

MICRUFIL ACT

REVISION SHEET WIRE LIST

REV	DESCRIPTION OF CH	ANGE	DRAWN BY	DATE	APPRV'D BY	DA
в	ITEM 37 PART NO. WAS 30 34 75 ADDED THIS SHEET RELEASED FOR MICROFILMING		J. Gray	1/10/75	2 Price	1-7:
		i.				
and the second	MIG. UF LED	<u>E_</u>				
NATIO	DNAL RADIO ASTRONOMY OBSERVA		PROJ: VU	<u> </u>	<u> </u>	<u> </u>
TITL TE	E: I. F. RECEIVER ASSEMBLY	DWG NO	A13450	21		

ELECTRICAL	X MECHANICAL	вом # <u>A13450Z1</u>	rev B	DATE 1/10/75	PAGE 1 OF]
MODULE # T5	NAME I.F. TRANSMISSION	RECEIVERDWG # D13450	P3 SUB	ASMB	DWG #
SCHEMATIC DWG #	D13450S1 LOCATION	QUA/SYS	TEM <u>4</u>	PREPARED BY IDEA/WWB	APPROVED C Pace

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		NRAO	D13450P3	IF TRANSMISSION RECEIVER		
2		NRAO	B13450M2	PANEL, FRONT	1	
3		NRAO	C13450M12	RIGHT SIDE PLATE	1	
4		NRAO	C13450M4	LEFT SIDE PLATE, FRONT	1	
5		NRAO	B13450M5	LEFT SIDE PLATE, REAR	1	
6		NRAO	B13450M10	BAR, SUPPORT, TOP & BOTTOM	2	
.7		NRAO	B1305Qm4	GUIDE	2	
8		NRAO	B13450M3	SHIELD, FRONT	1	
9		NRAO	B13450M1	SHIELD, CONNECTOR	1	
10		NRAO	B13450M6	SUPPORT, LEFT SIDE PLATE	1	
11		NRAO	B13450M9	SUPPORT, HEAT SINK	1 .	
12		NRAO	B13450M7	MOUNTING PLATE, INTEGRATED CIRCUIT	1	
13		NRAO	C13450M11	MOUNTING FRAME, CIRCUIT CARD	1	
14		NRAO	B13450M15	CABLE STRAP .141 DIA	2	
15			4-40 ×.500 LG	SCREW, FLAT HD, S.S.	11	

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ELECTRICAL

Ietm #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	total Qua	
16			6-32 × 1.000 LG	SCREW, PAN HEAD, S.S.	2	
17			6-32 × .500 ⁻ LG	SCREW, HEX SOCKET HD, S.S.	2	
18			4-40 × .375 LG	SCREW, PAN HEAD, S.S.	6	
19		SOUTHCO	47-11-204-10	SCREW, CAPTIVE	2	
20			6-32 x .375 LG	SCREW, FLAT HEAD, S.S.	1	
21			4-40 × .250 LG	SCREW, FLAT HEAD, S.S.	36	
22			2-56 x .250 LG	SCREW, PAN HEAD, S.S.	39	
23			2-56 × .250 LG	SCREW, FLAT HEAD, S.S.	4	
24			6-32 × .250 LG	SCREW, PAN HEAD, S.S.	2	
25			4-40 × .250 LG	SCREW, PAN HEAD, S.S.	1	
26			#2	WASHER, FLAT, S.S.	35	
27		WAKEFIELD	2604th5B	HEAT SINK	1	
28		NRAO	B13450M8	PANEL, REAR	1	
			<u></u>			

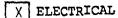
MICROFILMED

X ELECTRICAL

MECHANICAL BOM # A13450Z1 REV B DATE 1/10/75 PAGE 3 OF 7

ietm #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA
29	J7 J8	AMPHENOL	UG-492 B/U	BNC F.T.	1
30	J9	AMPHENOL	UG625 B/U	BNC CONNECTOR	1
31	P1	AMP SPECIAL INDUSTRIES	201355-3	CONNECTOR	1
32		AMP SPECIAL INDUSTRIES	201347-4	SHIELD	1
33		AMP SPECIAL INDUSTRIES	202514-1	GUIDE PINS]
34		AMP SPECIAL INDUSTRIES	202512-1	GUIDE PINS	1
35		AMP SPECIAL INDUSTRIES	202725-1	CRIMP PINS	1
36	Ml	WESTON	MODEL 131	METER 0-100ua	1
37		OMNE SPECTRA	OMO 3043-75	RE CONNECTOR	5
		UNIFORM TUBES	CG-141	CABL E	1
39	C89-C92 C96&C97	SPECTRUM CONTROL	BE001DA104P	CAPACITOR F.T.	6
40	C93-C95 C98-C104	SPECTRUM CONTROL	FB3B10F1289	CAPACITOR F.T.	10
41	U8	FAIRCHILD	FM-A-120	R.F. POWER AMP]
42	-	WAL DON	T2009	RING TONGUE TERMINAL	1
43	1	WAL DON	T2015	CRIMP LUG (SPADE LUG)	2
44		NRAO	B13450P2	P.C. BOARD DISPLAY	I
·45		NRAO	D13450P4	P.C. BOARD ASSY, IF RECEIVER	1





MECHANICAL

BOM # A13450Z1 REV

B DATE 1/10/75 PAGE 4 OF 7

IETM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
46		NRAO	B13450M14	RF CONNECTOR	5	
47		WALDON	2101-04-00	TERMINAL LUG]	
48		ERIE	8131-050-651-105M	CAPACITOR 1.0 uf	1	
49		AMPHENOL	RG174A	COAX CABLE, BLK]	
50		PANDUIT	SST-IN-MP	TYRAPS	3	
51	P8 P9	AMPHENOL	31-315	BNC CONNECTOR	2	
52			#22 AWG 2 LG	WIRE BUS	2	
53			#22 AWG 6 LG	WIRE HOOK-UP PVC 600V 7/30 WHT/BLK	2	
54			#22 AWG 9 LG	WIRE HOOK-UP PVC 600V 7/30 WHT/BLK	1	
55			#22 AWG 3 LG	WIRE HOOK-UP PVC 600V 7/30 WHT/BLK	1	
56			#22 AWG 12 LG	WIRE HOOK-UP PVC 600V 7/30 WHT/BLK	1	
57			#22 AWG 6 LG	WIRE HOOK-UP PVC 600V 7/30 WHT/GRA	2	
58			#22 AWG 12 LG	WIRE HOOK-UP PVC 600V 7/30 WHT/GRA	1	
59			#22 AWG 9 LG	WIRE HOOK-UP PVC 600V 7/30 WHT/GRA	1	
60			#22 AWG 3 LG	WIRE HOOK-UP PVC 600V 7/30 WHT/GRA	1	
61			#22 AWG 9 LG	WIRE HOOK-UP PVC 600V 7/30 WHT/GRN	2	
62			#22 AWG 6 LG	WIRE HOOK-UP PVC 600V 7/30 WHT/GRN	2	

MICROFILMED

total Qua	SCRIPTION	DES	MFG PART #	ł	MANUFACTURER	REF DESIG	IETM #
1	PVC 600V 7/30 ORN	WIRE HOOK UP P	AWG 12 LG	#22			63
3	· ORN	A	6 LG			<u></u>	64
1	ORN		9 LG				65
1	BLK		12 LG				66
1	VIO		3 LG				67
2	VIO		6 LG				68
 1	WHT/V TO		3 LG				69
 1	GRA		3 L.G				70
1	RED.		6 L.G				71
1	RÉD		9 LG				72
1	GRN		3 LG				73
1	GRN		6 LG				74
1	YEL		3 LG				75
1	YEL		6 LG				76
1	BLU		3 LG		· · · · · · · · · · · · · · · · · · ·		77
. 1	BLU		AWG 6 LG	#22			78
1	PVC 600V 7/30 BLK	WIRE HOOK-UP P	AWG 3LG	#16			79

ELECTRICAL

MECHANICAL

BOM # A13450Z1 REV B DATE 1/10/75 PAGE 5 OF 7



MECHANICAL BOM # A13450Z1 REV B DATE 1/10/75 PAGE 6 OF 7

IETM #	REF. DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
80			#22 AWG 6 LG	WIRE HOOK-UP 600V 7/30 GRA	1	
81		AMP SPECIAL INDUSTRIES	#201578-1	PIN, CRIMP	11	
]				

MIGROFILMED DATE 5/13/25 BY SPEY. LTR

NATIONAL RADIO ASTRONOMY OBSERVATORY

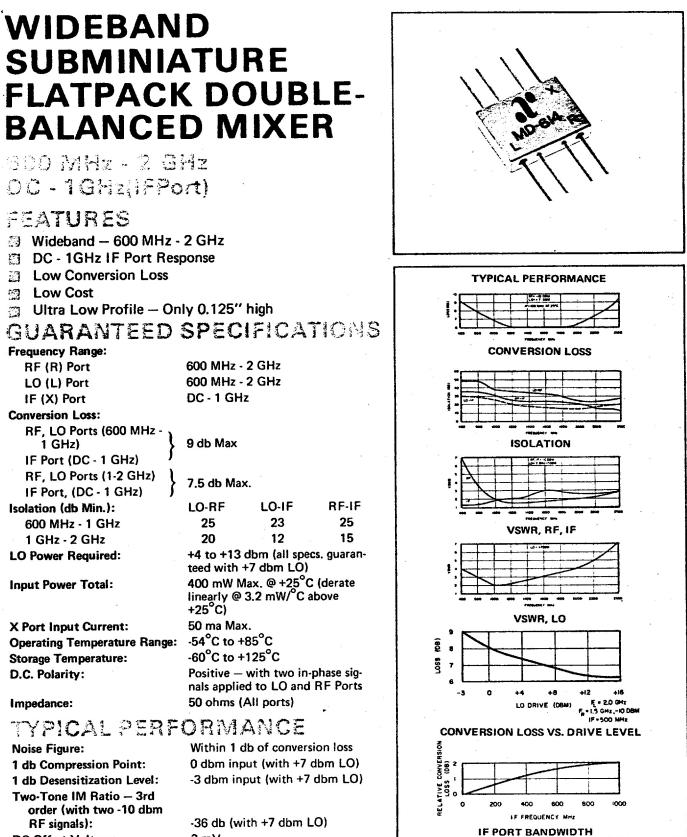
ELECTRICAL

X MECHANICAL BOM # A1345021 REV ____ DATE 1/10/75 PAGE 7 OF 7

TOTAL DESCRIPTION MFG PART # MANUFACTURER ITEM REF QUA Ħ DESIG 2 Pan Head, Slotted, St. St'1. Screw #6-32 X .750 lg. 82h.itin







DC Offset Voltage:

3 mV



DESCRIPTION

The Model MD-614 is a high performance, subminiature double balanced mixer that utilizes well matched, low noise, hot carrier diodes. The L and R ports have a bandwidth of 600 MHz to 2 GHz, while the X port has a bandwidth of DC to 1 GHz. Inputs to any two ports will produce the sum and difference frequencies at the third port with a minimum of undesired modulation products.

Advanced broadband ferrite transformer techniques achieve low conversion loss, a low noise figure, and a LO-RF isolation better than 20 db (up to 2 GHz). Guaranteed performance is achieved with a LO power of +7 dbm, although the mixer may be used with LO inputs ranging from +4 to +13 dbm.

The ultra-low profile flatpack (only 0.125" high) provides improved performance with increased reliability, and very importantly, is ideal for high-density electronic circuit packaging. Metal-package, hermetically sealed, and RFI shielded, the MD-614 is ruggedly constructed to withstand severe environmental conditions, while at the same time lending itself to convenient stripline or microstrip mounting. The leads of this device can be readily soldered or welded.

ENVIRONMENTAL

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This Device Has Been Designed to Meet the Following Environmental and Physical Conditions of MIL-STD-202:

Thermal Shock:	Method 107, Test Condition A -55°C to +85°C, 30 minutes at temperature extremes, 5 cycles
Humidity:	Method 103, Test Condition B (96 hours)
Barometric Pressure:	Method 105, Test Condition D 100,000 feet
Moisture Resistance:	Method 106
Life Test:	Method 108, Test Condition B (260 hours)
Seal Test:	Method 112, Test Condition B (Gross Leak, 10 ⁻⁵ atm cc/sec.)
Vibration:	Method 204, Test Condition B 10-2,000 Hz, 15 G peak
High Impact Shock:	Method 207
Solderability:	Method 208

APPLICATIONS

- As a frequency converter
- As a phase detector
- As a double sideband suppressed carrier modulator
- 🗘 🛛 As a pulse modulator
- As a frequency doubler
- See As a voltage/Current variable attenuator

ORCERING INFORMATION

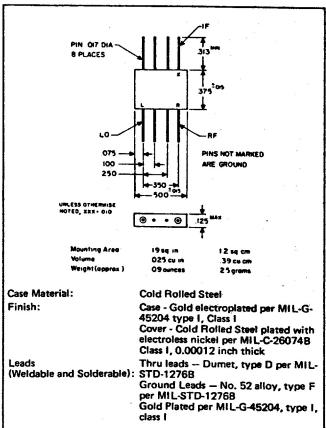
Please specify Model No. when ordering.

Model MD-614:	\$75.00 (1-5 Qty.)
Availability:	Stock
Terms:	Net 30, f.o.b. factory

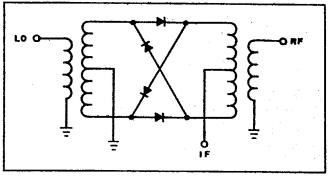
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MECHANICAL DATA



SCHEMATIC



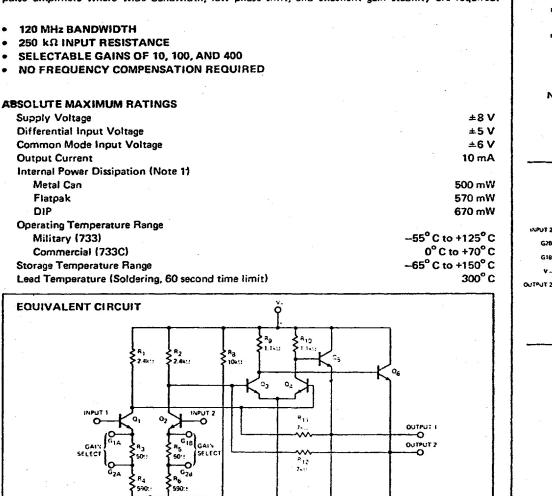
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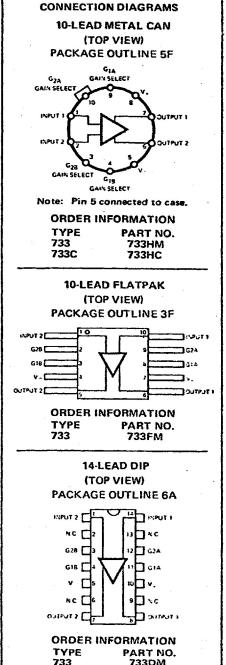
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Division of Adams-Russell

µA733 DIFFERENTIAL VIDEO AMPLIFIER FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μ A733 is a monolithic two-stage Differential Input, Differential Output Video Amplifier constructed using the Fairchild Planar* epitaxial process. Internal series-shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100 or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high speed thin film or plated wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.





*Planar is a patented Fairchild process.

733DC

733C

Notes on following pages.

13

16

320

1 4.12

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μ A733

733

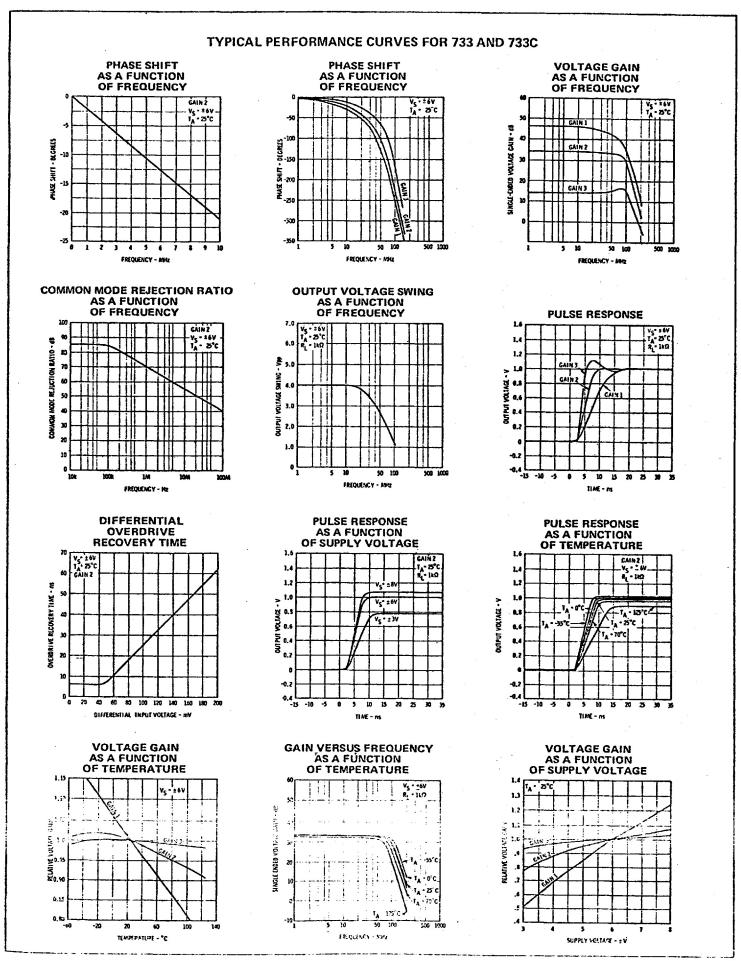
ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$, $V_S = \pm 6.0$ V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		300	400	500	
Gain 2 (Note 3)		90	100	110	
Gain 3 (Note 4)		9.0	10	11	
Bandwidth	R _S = 50Ω				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	$R_S = 50\Omega$, $V_{OUT} = 1 V_{p-p}$				
Gain 1			10.5		ns
Gain 2			4.5	10	កទ
Gain 3			2.5		ns
Propagation Delay	$R_S = 50\Omega$, $V_{OUT} = 1 V_{p-p}$				
Gain 1			7.5		ns
Gain 2		· · ·	6.0	10	ns
Gain 3			3.6		ns
nput Resistance					
Gain 1			4.0		kΩ
Gain 2		20	30		kΩ
Gain 3			250		kΩ
nput Capacitance	Gain 2		2.0		рF
nput Offset Current			0.4	3.0	μA
nput Bias Current			9.0	20	μA
nput Noise Voltage	$R_S = 50\Omega$, BW = 1 kHz to 10 MHz		12		μVrms
nput Voltage Range	1 1	±1.0			V
Common Mode Rejection Ratio				1	
Gain 2	V _{CM} = ±1 V, f≤100 kHz	60	86		dB
Gain 2	$V_{CM} = \pm 1 V$, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio	Cim			++	
Gain 2	$\Delta V_{\rm S}$ = ±0.5 V	50	70		dB
Dutput Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.0	v
Output Common Mode Voltage		2.4	2.9	3.4	v
Output Voltage Swing		3.0	4.0		V _{P-P}
Output Sink Current		2.5	3.6		p mA
Output Resistance		2.3	20		0
Power Supply Current			18	24	mA
The following specifications apply for	$\frac{1}{55^{\circ}C} \leq T_{\star} \leq \pm 125^{\circ}C$		<u>10</u>	24	<u></u>
Differential Voltage Gain			T	· · · · · · · · · · · · · · · · · · ·	
Gain 1 (Note 2)		200		600	
Gain 2 (Note 3)		80			
		8.0	2 ¹⁰ 11	120 12	а
Gain 3 (Note 4)				12	
Input Resistance					10
Gain 2		8.0			kΩ
nput Offset Current			·····	5.0	μA
nout Birs Current				40	μΑ
npu: Vultace Range	<u>_</u>	±1.0			V.
Conversions Priestion Batio		63	İ	·	38
Supply Voltage Rejection Ratio		50		44	с́В
Dutput Offset Voltage					
Gain 1			1	1.5	V
Gain 2 and Gain 3		2.5		1.2	<u> </u>
Dutput Swing		2.5			V _{p-p}
Output Sink Current		2.2	E .	4 . I	mA

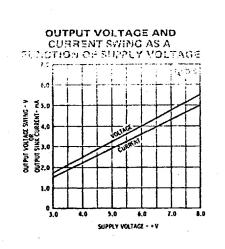
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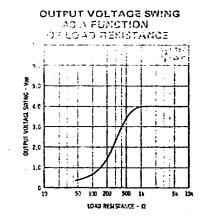
FAIRCHILD LINEAR INTEGRATED CIRCUITS + µA733

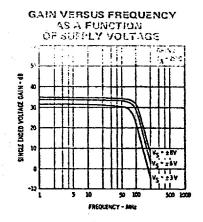
PARAMETER (see definitions)	CONDITIONS	MIN.	TYP,	MAX.	UNITS
Differential Voltage Gain Data + (Plote 2)		· · ·	454		
Gain 2 (Note 3)		250 80	409	600	
Gain 3 (Note 4)		8.0	100 10	120	
Bandwidth	R _S = 50Ω	8.0	10	12	
Gain 1	115 5005		40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	$R_S = 50\Omega$, $V_{OUT} = 1 V_{P-P}$				WITZ
Gain 1			10.5		ns ns
Gain 2	·		4.5	12	ភរ
Gain 3			2.5		ns
Propagation Delay	$R_{S} = 50\Omega, V_{OUT} = 1 V_{p-p}$				
Gain 1			7.5		лs
Gain 2			6.0	- 10	ns
Gain 3			3.6		ns ins
Input Resistance		·			
Gain 1			4.0	1	kΩ
Gain 2		10	30		kΩ
Gain 2 Gain 3	· · ·		250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current		· · · · · ·	0.4	5.0	μΑ
Input Bias Current			9.0	30	μΑ
Input Noise Voltage	$R_S = 50\Omega$, BW = 1 kHz to 10 MHz		12		μV _{rn}
Input Voltage Range	3	±1.0			V
Common Mode Rejection Ratio					·····
Gain 2	V _{CM} = ±1 V, f≤100 kHz	60	86		dB
Gain 2	$V_{CM} = \pm 1 V, f = 5 MHz$		60		dB
Supply Voltage Rejection Ratio					
Gain 2	ΔV _S = ±0.5 V	50	70		dB
Output Offset Voltage			·····		
Gain 1			0.6	1.5	v
Gain 2 and Gain 3			0.35	1.5	v
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	·4.0		V _{p-p}
Output Sink Current		2.5	3.6	[mA
Output Resistance			20		Ω
Power Supply Current			18	24	îmA
The following specifications apply for	0°C≤T _A ≤±70°C				
Differential Voltage Gain				1	
Gain 1 (Note 2)		250		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance-Gain 2	•	8.0			kΩ
Input Offset Current			·······	6.0	μΑ
Input Bias Current				40	μΑ
Input Voltage Range		±1.0		1	V
Common Mode Rejection Ratio					
Gain 2	V _{CM} = ±1 V, f≤100 kHz	`50			dB
Supply Voltage Rejection Ratio			· · · · · · · · · · · · · · · · · · ·	1	
Gain 2	$\Delta V_{S} = \pm 0.5 V$	50			dB
Output Offset Voltage (All Gain)				1.5	v
		2.8		2	V _{p-p}
Output Voltage Swing		[Et	0.0



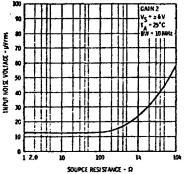
TYPICAL PERFORMANCE CURVES FOR 733 AND 733C







INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE

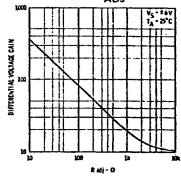


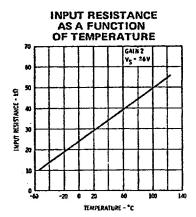
0.2_PF 0 11:2 510 0.24 41 ł IkΩ 512

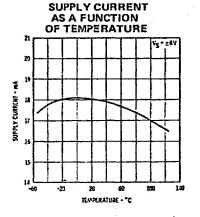
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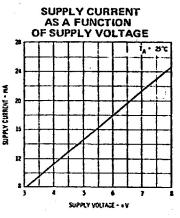
VOLTAGE GAIN ADJUST CIRCUIT

VOLTAGE GAIN AS A FUNCTION OF RADJ



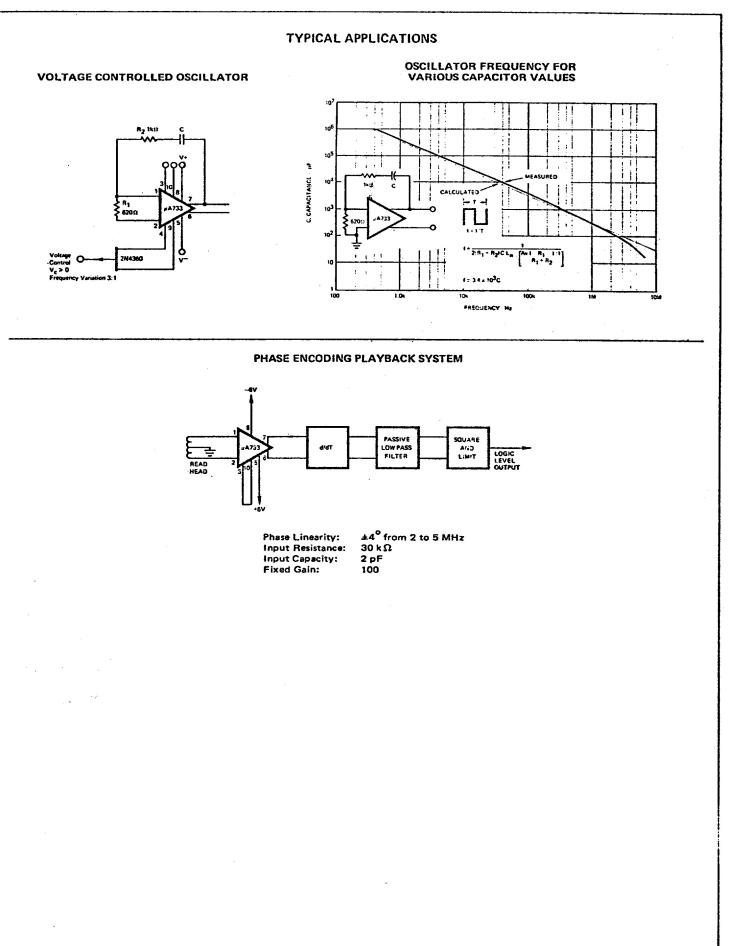






NOTES

- Rating applies to ambiant temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the DIP and 7.1 mW/°C for the Flatpak.
- 2. Gain Select pins G_{1A} and G_{1B} connected together. 3. Gain Select pins G_{2A} and G_{2B} connected together. 4. All Gain Select pins opan.



6-17



Operational Amplifiers

LH0022/LH0022C* high performance FET op amp LH0042/LH0042C low cost FET op amp LH0052/LH0052C precision FET op amp

general description

The LH0022/LH0042/LH0052 are a family of FET input operational amplifiers with very closely matched input characteristics, very high input impedance, and ultra-low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. The internally laser nulled LH0052 offers 200 microvolts maximum offset and $5\mu V/^{\circ}C$ offset drift. Input offset current is less than 100 femtoamps at room temperature and 100 pA maximum at 125°C. The LH0022 and LH0042 are not internally nulled but offer comparable matching characteristics. All devices in the family are internally compensated and are free of latch-up and unusual oscillation problems. The devices may be offset nulled with a single 10k trimpot with neglible effect in offset drift or CMRR.

The LH0022, LH0042 and LH0052 are specified for operation over the -55° C to $+125^{\circ}$ C military temperature range. The LH0022C, LH0042C and LH0052C are specified for operation over the -25° C to $+85^{\circ}$ C temperature range.

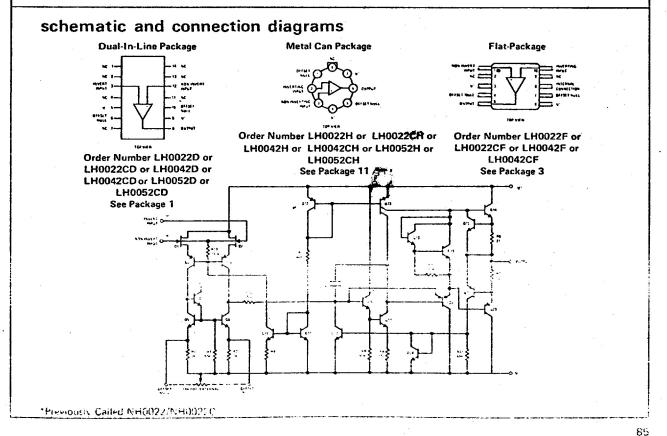
- Low input offset drift—5µV/°C max (LH0052)
- Low input offset voltage 100 microvolts-typ.
- High open loop gain 100 dB typ.
- Excellent slew rate 3.0 V/µs typ.
- Internal 6 dB/octave frequency compensation
- Pin compatible with standard IC op amps (TO-5 package)

The LH0022/LH0042/LH0052 family of IC op amps are intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents and tightly matched input offsets. The LH0052 is particularly suited for long term high accuracy integrators and high accuracy sample and hold buffer amplifiers. The LH0022 and LH0042 provide low cost high performance for such applications as electrometer and photocell amplification, pico-ammeters, and high input impedance buffers.

Special electrical parameter selection and custom built circuits are available on special request.

features

 Low input offset current – 100 femtoamps max. (LH0052) For additional application information and information on other National operational amplifiers, see Available Linear Applications Literature.



absolute maximum ratings

Supply Voltage	±22V
Power Dissipation (see graph)	500 mW
Input Voltage (Note 1)	±15V
Differential Input Voltage (Note 2)	±30V
Voltage Batween Offset Null and VT	±0.5V
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0022, 1.H0042, LH0052	-55°C to +125°C
LH0022C, LH0042C, LH0052C	–25°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

dc electrical characteristics For LH0022/LH0022C (Note 3)

		LIMITS							
PARAMETER	CONDITIONS		LHOOZZ			LH00220		UNITS	
 		MIN	TYP	MAX	MIN	TYP	MAX		
Input Offset Voltage	$R_S \leq 100 \text{ k}\Omega; T_A = 25^{\circ}C$		2.0	4.0		3.5	6.0	۳V	
Ŧ	$R_{s} \leq 100 \ k\Omega$			5.0			10.0	mV	
Temperature Coefficient of Input Offset Voltage	R ₅ ≤ 100 kΩ		5	10		5	15	` C [°] C	
Offset Voltage Drift with Time			3	. 1		4		µV/week	
Input Offset Current	T _A = 25°C		0.2	2.0		1.0	5.0	pА	
				200			200	pА	
Temperature Coefficient of Input Offset Current		Dou	ibles every	20°C	Do.	bles every	20°C		
Offset Current Drift with Time			0.1			0.1		pA/week	
Input Bias Current	T _A = 25°C		5	10		10	25	pА	
				1.0			1.0	nA ·	•
Temperature Coefficient of Input Bias Current		Dou	, ibles every I	20°C	Dou	e ibies every 	20°C		
Differential Input Resistance			1012			1012		Ω	
Common Mode Input Resistance			10'2			1012		Ω	
Input Capacitance			4.0			4.0		ρF	
Input Voltage Range	V ₅ = ±15V	±12	±13.5		±12	±13.5		v	
Common Mode Rejection Ratio	$R_S \le 10 \text{ k}\Omega$, $V_{HN} = \pm 10V$	80	90		70	90		dB	
Supply Voltage Rejection Ratio	$R_S \le 10 \ k\Omega$, $\pm 5V \le V_S \le \pm 15V$	80	90		70	90		dB	
Large Signal Voltage Gain	$R_{L} = 2 k\Omega, V_{OUT} = \pm 10V,$ $T_{A} = 25^{\circ}C, V_{S} = \pm 15V$	100	200		75	160		V/mV	
	R _L = 2 kΩ, V _{OUT} = ±10V, V _S = ±15V	50			50			V/mV	
 Output Voltage Swing	R _L = 1 kΩ, T _A = 25°C, V _S = ±15V	±10	±12.5		±10	±12		v	• •
	$R_{L} = 2 k\Omega$, $V_{S} = \pm 15V$	±10	ļ		±10		ł	v	
Output Current Swing	Vout = ±10V, TA = 25°C	±10	±15		±10	±15		mA	
Output Resistance			75			75		n	
Output Short Circuit Current			25			25		mΑ	
Supply Current	Vs = ±15V		2.0	2.5		2.4	2.8	mA	
Power Consumption	Vs=±15V			75			85	ww	

dc electrical characteristics for LH0042/LH0042C

 $(T_A = 25^{\circ}C, V_S = \pm 15V, unless otherwise specified)$

				LIM	ITS			
PARAMETER	CONDITIONS		LH0042			LH0042C		UNITS
	541	N	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Rs < 1	50 x12, -5V < V5 < 20V		5.0	20		6.0	20	mV
Temperature Coefficient of R _S < 1 Input Offset Voltage	90 K 12		5	20		10	25	µV/°C
Offset Voltage Drift with Time			7			10		µV/week
Input Offset Current			1	5		2	10	рА
Temperature Coefficient of Input Offset Current		Dout I	les every :	20 C	Dou	bles every (20'C	
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current			10	25		15	50	DA
Temperature Coefficient of Input Bias Current		Doub	lles every 2	20 C	Dou	, bles every : I	20°C	
Differential Input Resistance			1012		2.6	10 ¹²		2
Common Mode Input Resistance		- 1	1012			10 ¹²		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	:12	. [:13.5		:12	:13.5		v
Common Mode Rejection Ratio As < 1	3 κΩ, V _{IN} = 110V 70		86		70	60		dB
Supply Voltage Rejection Ratio $R_S \leq 1$	0 kt), -5V ≤ V _S ≤ ±15V 70		86		70	80		dB
Large Signal Voltage Gain RL = 1	\$Ω, V _{CUT} = ±10V 50		150		25	100	-	V/mV
Output Voltage Swing R_ = 1	kt: ±10		:12.5		:10	:12		v
Output Current Swing Vout	±10V ±10		: 15		:10	:15		mA
Output Resistance	- 1	ł	75			75		Ω
Output Short Circuit Current			20			20		mA
Supply Current			2.5	3.5		2.8	4.0	mA
Power Consumption			1	105			120	m₩

dc electrical characteristics For LH0052/LH0052C (Note 3)

		L	··	LIA	TITS			
PARAMETER	CONDITIONS		LH0052			LH0052	-	UNITS
 		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_{S} \le 100 \text{ k}\Omega; V_{S} = 15V,$ $T_{A} = 25 \text{ C}$		0.1	02		0.2	0.5	mV
	R ₅ < 100 kΩ, V ₅ = 115V			0.7			1.0	۳V
Temperature Coefficient of Input Offset Voltage	R ₅ ≤ 100 kΩ		2	5		5	10	μVi^C
Offset Voltage Drift with Time	- -		2			4		µV/week
Input Offset Current	T ₄ = 25 C		0 01	01		0.02	0.2	DA
				100			100	рА
Temperature Coefficient of Input Offset Current		Dou	bles every	20°C	Dou	bles every	20°C	
Offset Current Drift with Time		a - 1	<0.1			<0.1		pA 'week
Input Bias Current	T _a ≈ 25 C		0.5	19		10	5.0	A
				500			500	pΑ
Temperature Coefficient of Input Bias Current		Dou	bles every	20 [°] C	Dou	bles every	20°C	
Differential Input Resistance	а.		10 ¹²	$\mathcal{L}_{\mathcal{T}}^{1,\mathcal{T}} = \mathcal{L}$		10'2		Ω
Common Mode Input Resistance			1012	5 ^{36 100}		10"2		Ω
Input Capacitance	у -		4.0			40		pF
Input Voltage Range	V ₅ = 115V	112	-13.5		:12	:13.5		v
Common Mode Rejection Ratio	R ₅ < 10 k2, V _{IN} = +10V	80	90		76	90		d8
Supply Voltage Rejection Ratio	$R_{S} \le 10 \text{ kC}, 15 \text{V} \le \overline{V}_{S} \le 15 \text{V}$	80	90		76	90		dB
Large Signat Voltage Gain	R _L = 2 kU, V _{OUT} = ±10V, V _S = ±154, T _A = 25 C	100	200		75	160	2	V.'mV
	⊟ = 2 ¥11 M _{CC 1} = *10 V. Ng sintsy	50			50		ч. 	Via,V
A start of the seturated	Second and the Factor	,	1:5		-10	19 7 -		
	θ 2+Ω, Vs = 157	· 10		Ì	: 10			v
Output Current Swing	Vac + = 10V, TA = 25 C	· 10	:15		110	+15		mA
Output Resistance			75			75		12
Output Short Circuit Current	-		25			25		mA
Supply Correct	V _S = *15V		23	25		2.5	30	mA
Power Consumption	Vs - 15V			75			90	m\¥

LH0022/LH0022C,LH0042/LH0042C,LH0052/LH0052C



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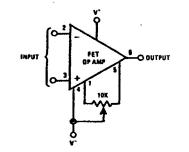
				LIM	115			
PARAMETER	CONDITIONS	U	10022/42	52	LHO	022C/420	/52C	UNITS
		MIC	TYP	MAX	MIN	TYP	MAX	
Steel Rote	Veitare Foilewar	15	3.0		10	30		V (2)
Coner Service Bungersotts	Miktaga Folipulu	<u>!</u>	1		1	:		र स्तर
Serial Septed Prends of the		•	15					11.12
Res Time			23	1		0.3	1.5	l
Overshoot			10	30		15	40	8
Settling Time (0.1%)	∆V _{IN} = 10∨		4.5			4.5		μs
Overload Recovery			4.0			4.0		μs
Input Noise Voltage	$R_{s} = 10 \text{ k}\Omega$, $f_{o} = 10 \text{ Hz}$		150			150		nV/VHz
Input Noise Voltage	$R_{\rm S} = 10 \ {\rm k}\Omega$, $f_{\rm o} = 100 \ {\rm Hz}$		55			55		nV/VHz
Input Noise Voltage	$R_{s} = 10 \text{ k}\Omega, f_{o} = 1 \text{ kH}_{2}$		35			35		nV/VHz
Input Noise Voltage	R _S = 10 kΩ, f _o = 10 kHz		30			30		nV/√Hz
Input Noise Voltage	BW = 10 Hz to 10 kHz, R3 = 10 k??		12			12	4	μVrms
Input Noise Current	BW = 10 Hz to 10 kHz		<.1			<.1		pArms

Note 1: For supply voltages less than ±15V, the absolute maxim Out voltage is equal to the supply voltage

stance of 10 kf2, for source resistances less than 10 kts, maxim

Note 2: Butting applies for minimum source resistance of 1 input voltage is :5V. Note 3: Unless otherwise specified, these specifications a LH0022, LH0042 and LH0052 and -25'C \leq T_A +85'C for T_A > 25'C. pply for +5% the LH20222, \leq Vs \leq +20V and +55 C \leq TA \leq +125 C for the LH0052C Typical values are given for

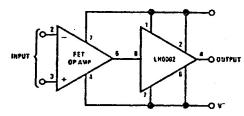
auxiliary circuits (shown for TO-5 pin out)



FET OP AMP INPUT O GUTPUT Note All diades are ultra tan tasi ag-

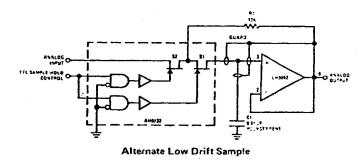
Offset Null

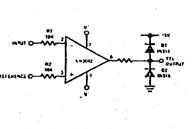




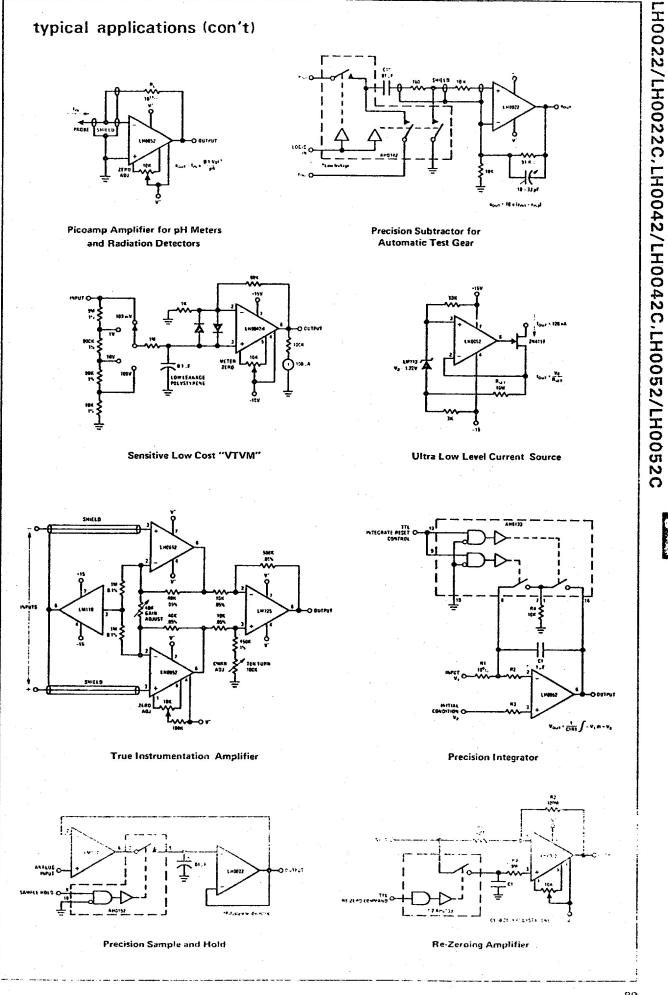
Boosting Output Drive to ±100 mA

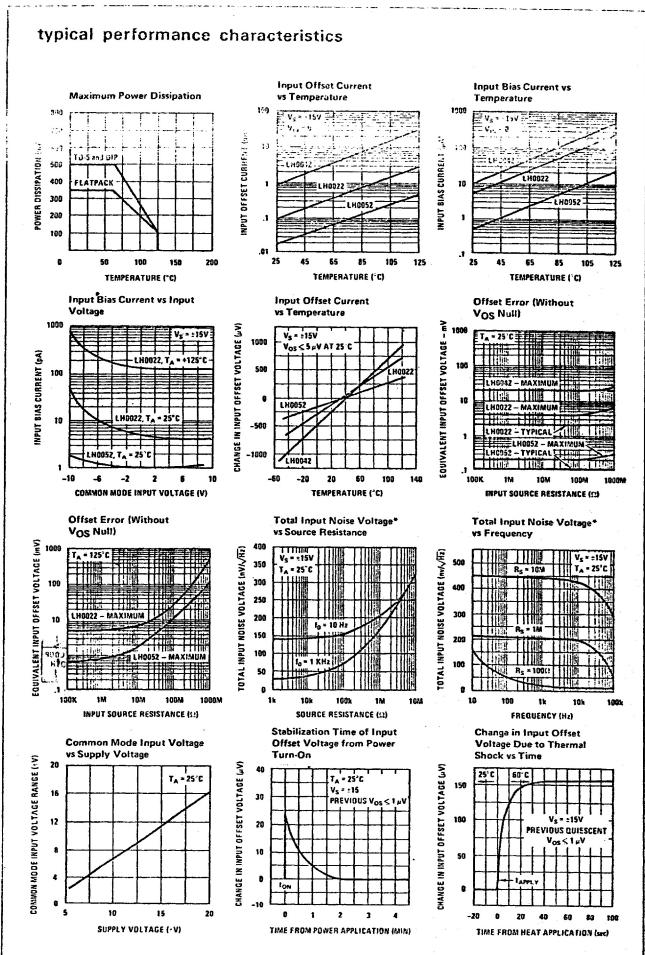
typical applications





Precision Voltage Comparator

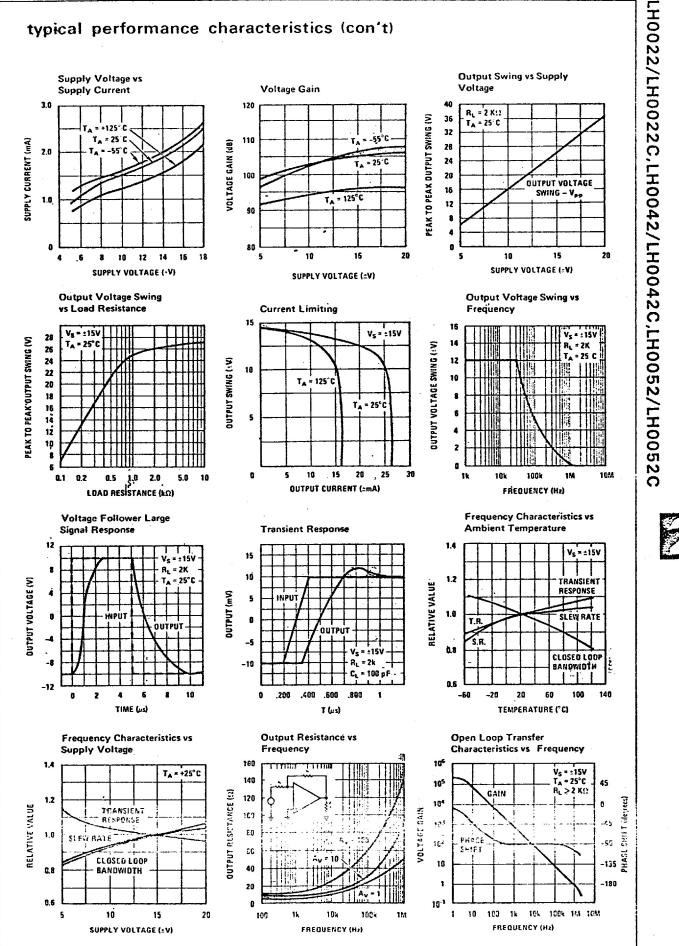




*Noise Vultage Includes Contribution from Source Resistance

LH0022/LH0022C,LH0042/LH0042C,LH0052

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FMA SERIES .5 MHz to 550 MHz THIN FILM VHF/UHF MICROWAVE IC AMPLIFIERS AND ATTENUATORS

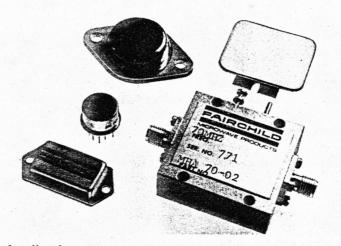
Features

- More than 10-octaves of flat RF bandwidth
- Low-noise, wide dynamic range amplifiers
- Low, tightly-matched VSWR into 50-ohms (1.5:1)
- Up to 40 dB gain per single amplifier
- Up to +27 dBm linear power
- Flat gain cascading
- Absolute stability for cascading
- Low cost-designed to compete with discrete designs in price
- Meets MIL S-883 and MIL S-19500 specs
- Five standard package configurations-DIP, Lo-pack, Metal Can, Chassis Mount, Connector Type
- IC-compatible dual-in-line package with excellent RF ground
- PC-compatible packages
- Custom capability

Note: See page 3 for detailed product description Specifications

Maximum Ratings

P _{IN (max)} without damage	+15 dBm
Operating temperature	-40°C to +85°C
Storage temperature	-40°C to +150°C
DC input bias	add 2 V to rated voltage
DC on RF terminals	±25 Volts



Applications

Applications include portable and mobile communications equipment operating in VHF, UHF and microwave regions, ECM, high frequency laboratory instruments, radar and navigational systems, collision avoidance and beacon sets, telemetry and space communication data links, and high speed digital systems. Devices with flat wideband frequency response are suitable for use in RF and IF stages in receivers, local and master oscillator multiplier chains, pulse counting, RF feedback loops, and isolation and buffer stages.

Model No.	Previous Model No.	Bandwidth (MHz)	Gain Minimum (dB)	Flatness (dB)	P _{out} (dBm) @ 1 dB Compression	3rd Order Intercept Pt. Typ. (dBm)	VSWR Max (50Ω)	N.F. Max (dB)	DC Power In V* @ mA (max)	Package
FMA 114	FCH 114	.2-550	20	=1.0	+16	+30	1.5:1	6	+28 @ 120	TO-3
FMA 111		.2-550	21	±0.75	+9	+22	1.5:1	6	+12 @ 60	DIPT
FMA 115	FCH 115	.2-550	33	=1.0	+9	+22	1.5:1	5	+12 @ 70	DIPT
FMA 10	FCH 10	10-500	-1.5 to	±0.5			2:1		+28 @ 25	то-8
			-11.5***							
FMA 300	MHA 300	100-500	25	=1.5	+5	+17	2:1	4	+12 @ 55	Lo-pack
FMA 301		100-500	25	=1.5	+5	+17	2:1	4	+12 @ 55	Connector
FMA 112	FCH 112	200-400	14	= 1.0	+9	+22	2:1	5	+12 @ 50	TO-8
FMA 105	FCH 105**	375-500	23	=0.5	+6	+22	1.5:1	2.5	+12 @ 50	DIPT
FMA 106	FCH 106	375-500	14	±0.5	+7	+20	1.5:1	3.0	+15 @ 40	TO-8
FMA 100	FCH 100	375-500	20	=0.5	+5	+20	1.5:1	2.5	-12 @ 70	Lo-pack
			(10 dB AGC)							
FMA 125	FCH 125	150-170	27	±0.5	+15	+25	1.5:1	2.5	+15 @ 90	TO-3
FMA 120	RFA 120	1-120	14.5	=0.5	+25	+37	1.5:1	8.5	+28 @ 200	TO-3
FMA 70 ^{††}	MHA 70	50-90	40	±0.5	+5	+17	2:1	2.5	+12 @ 55	Lo-pack
FMA 71	MHA 70-02	50-90	40	±0.5	+5	+17	2:1	2.5	+12 @ 55	Connector

*±1% Regulation **available as FMA 107 with negative power supply ***attenuation range [†]IC compatible dual-in-line package ^{††}available as FMA 72 without ground strap



COPYRIGHT FAIRCHILD SEMICONDUCTOR 1973 ● PRINTED IN U.S.A. 2032-11-0004-023 5M MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U.S. PATENTS: 2981877, 3015048, 3025589, 3064167, 3108359, 3117260; OTHER PATENTS PENDING.

Microwave Integrated Circuits

Fairchild offers a microwave integrated circuit line of VHF/UHF amplifiers in a variety of packages that provide the equipment designer with the ability to employ the same time and cost saving techniques previously available at low frequencies. Impedance matching networks, feedback loops, biasing, stabilization elements, noise figure and intermodulation problems are presolved. Amplifiers are absolutely stable; suitable RF case grounding will guarantee that no oscillation will occur. Units can be cascaded to achieve flat gains as high as 60 - 80 dB with good matching between individual units and no sacrifice in performance.

Hybrid integrated circuit amplifiers utilize a combination of computer-aided design and state-of-the-art transistors to provide unparalleled performance, stability, repeatability and reliability. They are suitable for both military and commercial systems.

In most cases, it is possible to impose performance specifications that are tighter than the sum of performances of comparable discrete components. With component interconnections minimized and only one package, significant size and weight advantages are obtained. Resulting performance of MICs exceeds that possible from a discrete circuit design, and ensures uniformity from circuit to circuit.

Fairchild's MICs Eliminate Problems

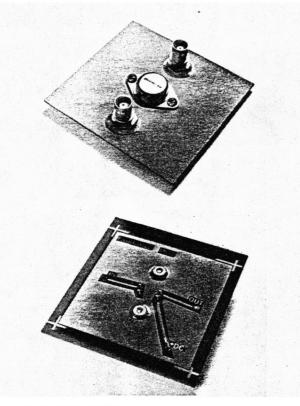
Fairchild uses advanced s-parameter computer programs to speed the design of new and special amplifiers at prices that are more than competitive with the system designer's own internal design and manufacturing costs.

For the user concerned with saving time, reducing costs and efficient systems development, MICs will eliminate such problems as:

- Extensive breadboarding with its costly and time-consuming cut-and-try techniques.
- Overdesign with its higher costs.
- Redesigns or individual matching of components frequently required when prototypes are put into production.
- Space problems caused by the numerous interconnections and individual packages used in discrete component circuits.
- User testing costs caused by the need to perform incoming inspection on a multitude of individual components as well as circuit reworking.

RF Grounding

As circuit designers know, the key to successful amplifier operation at the higher frequencies is effective RF grounding. Poor grounding can result in adverse effects ranging from a decrease in gain to oscillation, depending upon the parameters of the amplifier. Also, one of the principal advantages of MICs-repeatable performance-may be affected if the length of ground leads is allowed to vary, or if they are not kept as short as possible.



RELIABLE RF GROUNDING. Top and bottom views show a technique for assuring a good RF ground. Note that all ground connections are on one side of the circuit board. Never depend upon machine screws to make a good RF connection to the other side.

The various packages supplied by Fairchild MOD require a variety of grounding techniques. The TO-3 package inherently offers good RF grounding as well as good heat dissipation. The Lo-pack has a bottom plate that can be grounded to the PC board ground plane or to the chassis. The TO-8 package, as you will note from the packaging diagram, has all of its unused leads available for grounding. The connector type package is also designed to provide good grounding to the chassis.

From the viewpoint of use in printed circuit boards, most of the packages just mentioned have been somewhat difficult to work with. Now, Fairchild has introduced its hermetically-sealed DIP package, which we believe is the ideal PC package. A 4-pin version of the standard dual-in-line package, the DIP provides direct case-to-ground plane connection for excellent RF operation. Heat is dissipated directly through conduction, rather than depending upon radiation from the case, thereby improving device reliability. At present three amplifiers are available in this package as standard products, and additional circuits will be offered in this package in the future.

Custom Circuits

The product specialists at Fairchild MOD will be pleased to assist you with optimization of circuits or the development of special amplifiers to meet your system requirements. New "standard" MIC amplifiers are constantly being developed which will simplify as well as extend your system design capabilities. Contact us with your performance requirements for a prompt evaluation.

Product Description

FMA 114 Medium Power, General Purpose Broadband Amplifier.

General purpose broadband amplifier covering over three decades of VHF/UHF frequencies. Its 50 mW output for 1 dB gain compression permits it to be used as a driver for power amplifiers. The TO-3 package serves as a good heat sink.

FMA 115 High Gain, General Purpose Broadband Amplifier.

(FMA 111) An ideal pre-driver amplifier for the FMA 114. Has three stages of amplification with high feedback reserve gain. Priced below three single-stage amplifiers. The FMA 115 is produced in the IC-compatible DIP package. The FMA 111 is a lower gain two-stage broadband amplifier.

FMA 300 General Purpose (100 – 500 MHz) With Narrow FMA 301 Band Options.

A general purpose amplifier optimized for low noise figure. Also available on special order are higher gains or lower noise figures for specified narrow frequency range. To order connector package, specify FMA 301.

FMA 112 Low-Cost Octave Band Coverage.

Designed to provide optimum performance in the 200 - 400 MHz band. A popular amplifier, it provides a good compromise between low noise figure and high output power.

FMA 105 Low-Noise 440 MHz IF Amplifier.

Tuned to provide optimum performance in the 350 - 500 MHz band. This two-stage amplifier has a low noise figure and low intermodulation distortion. Also available as the FMA 107 for use with a -12 VDC power supply with a positive ground.

FMA 100 Low-Noise 440 MHz IF Amplifier With AGC. Features built-in AGC capability for the 375 - 500

Bandwidth Selection Guide

MHz range. Has a 10 dB adjustable gain combined with a matched input/output PIN attenuator. This two-stage amplifier, similar to the FMA 105, has a low noise figure and low intermodulation distortion. Operates from a single -12 VDC power supply.

FMA 120 Ultra Low-Distortion Push-Pull Amplifier.

A 1 - 120 MHz 50-ohm impedance complementary push-pull amplifier that offers cancellation of second order distortion in addition to low 3rd order distortion. Features ½ W linear output over the 100 MHz bandwidth.

FMA 70

FMA 71 Low-Noise, High Gain 70 MHz IF Amplifiers.

These high gain, low-noise 70 MHz IF amplifiers differ only in the type of package. The FMA 70 comes in a low profile package; the FMA 71 in a connector type package. Have three stages of amplification. Also available with gain set to center around lower frequencies.

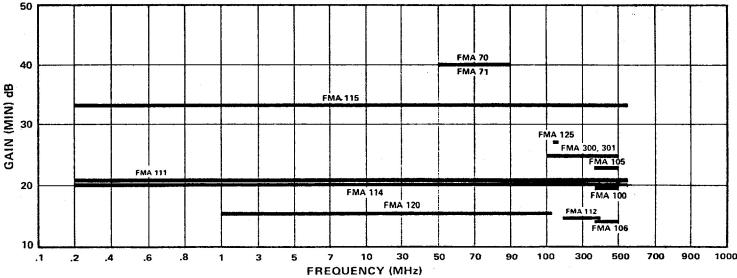
FMA 10 Broadband Low-Cost PIN Attenuator.

A 50 Ω impedance attenuator with matched input/ output from 10 - 500 MHz. Has 10 dB adjustable gain range set by a 20 K Ω external pot (not supplied). Usable up to input power level of +10 dBm.

FMA 125 Low-Noise, Low Distortion 160 MHz IF Amplifier. Has built-in 5-section high-pass filter and features low noise figure. The 3rd order IM products are better than 50 dB down at 0 dBm output. Operates from +15 VDC and out-performs units requiring higher DC input.

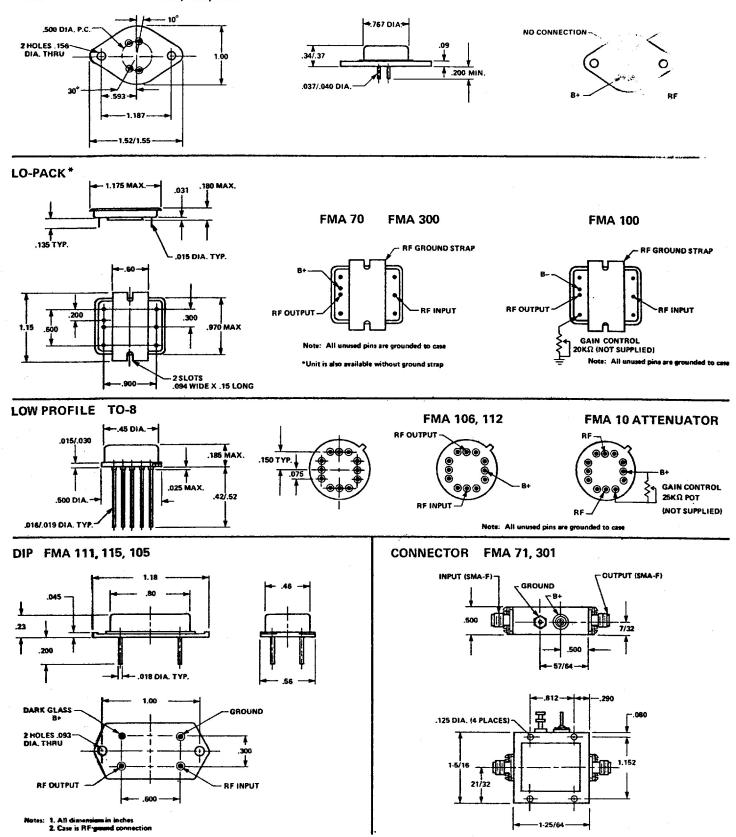
FMA 106 Low-Noise 440 MHz IF Amplifier.

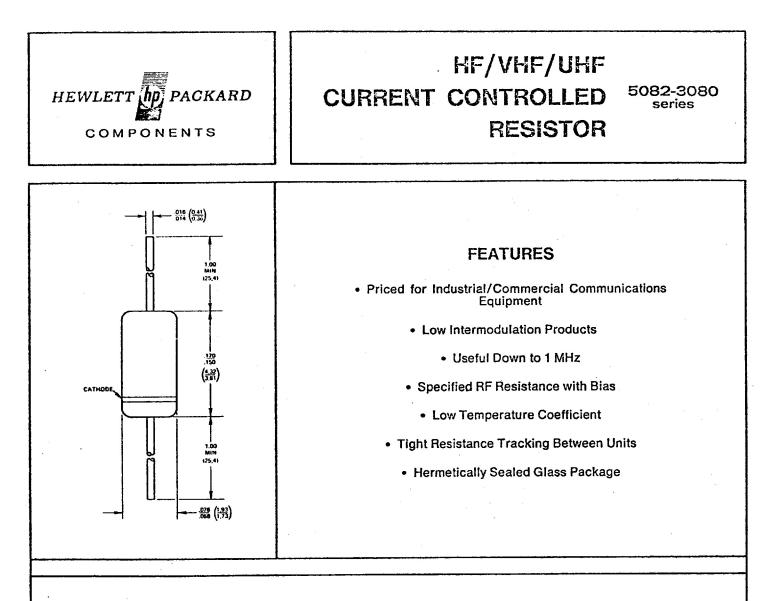
Designed for the 380 – 500 MHz range, it is ideal for 440 MHz IF applications. Has low noise figure combined with high dynamic range and flat gain response.



Dimensional Drawings and Pin Connections

MODIFIED TO-3 FMA 120, 125, 114





DESCRIPTION

The low frequency current controlled resistor consists of a specially processed and tested silicon PIN diode. The long minority carrier lifetime assures usefulness at operating frequencies down to 1 MHz with

APPLICATION

The low frequency current controlled resistor is ideally suited for constant impedance AGC-circuits, leveling circuits and electronically controlled RC and RL circuits operating in the frequency range from 1 MHz to 1 GHz and requiring extremely low signal distortions.

Special care is taken during manufacturing to assure

MECHANICAL SPECIFICATIONS

The HP Outline 15 package has a glass hermetic seal with leads. The leads on the Outline 15 package should be restricted so that the bend starts at least $\frac{1}{16}$ inch (1,6 mm) from the glass body. With this restriction, Outline 15 package will meet MIL-STD-750, Method 2036,

very low distortions. The fabrication process is tightly controlled and units are selected on the basis of similarity of RF resistance variation with bias.

repeatability of the RF resistance from unit to unit, which makes the device ideal for constant impedance attenuators in either pi-, T-, or bridged T-configurations.

The low and high resistance values have been specified to eliminate adjustments in high quantity production.

Conditions A and E [4 lb (1,8 kg)] tension for 30 minutes. The maximum soldering temperature is 235° C for five seconds.

Marking is by digital coding with a cathode band.

ABSOLUTE MAXIMUM RATINGS

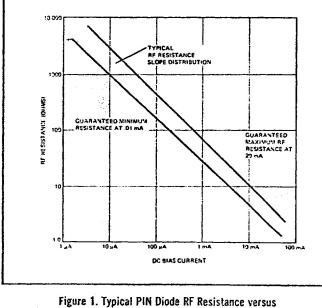
DC ELECTRICAL SPECIFICATIONS $(T_A = 25^{\circ}C)$

		Ses 2-30 ()			5052-3541			·····	
Onaracteristic	Symbol	Mia.	Typ.	flax.	Mia.	Typ.	Niax.	Uaits	Tast Conditions
Breakdown Voltage		100			100			volts	$I_{R} = 10 \ \mu A$
Total Reverse Bias Capacitance	Cvr		0.3	0.4			0.4	pF	$V_{R} = 50 V, f = 1 MHz$
Effective Minority Carrier Lifetime	τ		1.3			2.0		μsec	$I_{F} = 50 \text{ mA}, I_{R} = 250 \text{ mA}$

RF ELECTRICAL SPECIFICATIONS $(T_A = 25^{\circ}C)$

		5082-3080		5082-3081					
Characteristic	Symbol	Min.	Typ.	Max.	Min.	Тур.	Max.	Units	Test Conditions
High Resistance Limit	R _H	1000	2500		1500	3000		ohms	$I_{DC} = 0.01 \text{ mA},$ f = 100 MHz
Low Resistance Limit	RL		5	8		6	8	ohms	$I_{DC} = 20 \text{ mA},$ f = 100 MHz
Residual Series Resistance	R,		1.5	2.5		2	3.5	ohms	$I_{DC} = 100 \text{ mA},$ f = 100 MHz
2nd Order Distortion*	K2		70			-75		' dB	Two-channel test on 10 dB,
Cross Modulation*	C _m		62			-75		dB	75-ohm bridged T attenuator with 40 dBmV output on each channel $f_1 = 65 \text{ MHz}$ $f_2 = 100 \text{ MHz}^*$

* See Figures 3 and 4.



DC Bias Current (5082-3080).

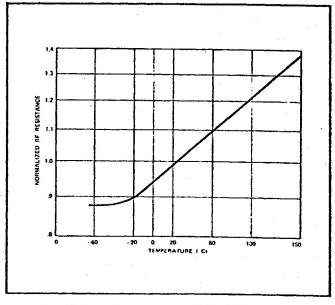


Figure 2. Typical Temperature Sensitivity of RF Resistance.

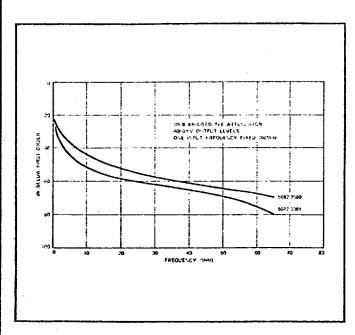


Figure 3. Typical Second Order Intermodulation Distortion.

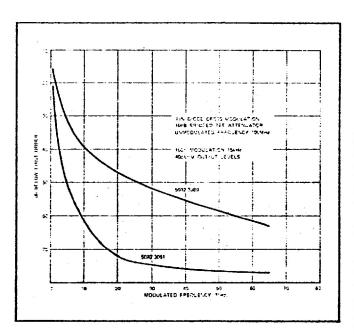


Figure 4. Typical Cross Modulation Distortion.

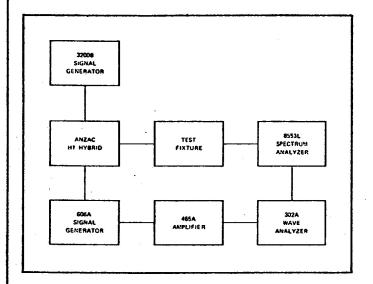


Figure 5. Cross Modulation Test Circuit.

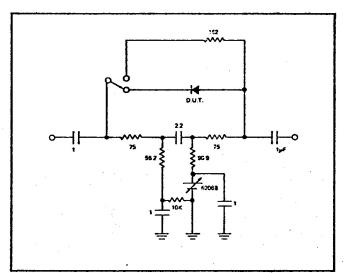


Figure 6. Bridged Tee Attenuator Test Circuit.



NUMERIC and HEXADECIMAL **INDICATORS**

5082-7300 **SERIES**

FEATURES

- Numeric 5082-7300/-7302
 Hexadecimal 5082-7340 - 0-9, Test State, Minus
 - Sign, Blank States
 - **Decimal Point**
 - 7300 Right Hand D.P.
 - 7302 Left Hand D.P.
- DTL TTL Compatible
- Includes Decoder/Driver with Memory 8 - 8421 Positive Logic Input
- 4 X 7 Dot Matrix Array
- Shaped Character, Excellent Readibility Standard .600 inch X .400 inch Dual-in-Line Package including Contrast Filter

- 0-9, A-F, Base 16

Blanking Control,

Conserves Power

- No Decimal Point

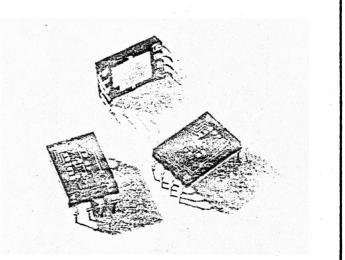
Operation

- **Categorized for Luminous Intensity**
- Assures Uniformity of Light Output from Unit to Unit within a Single Category

DESCRIPTION

The HP 5082-7300 series solid state numeric and hexadecimal indicators with on-board decoder/driver and memory provide a reliable, low-cost method for displaying digital information.

The 5082-7300 numeric indicator decodes positive 8421 BCD logic inputs into characters 0-9, a "-" sign, a test pattern, and four blanks in the invalid BCD states, The unit employs a right-hand decimal point. Typical applications include point-of-sale terminals, instrumentation, and computer systems.



The 5082-7302 is the same as the 5082-7300, except that the decimal point is located on the left-hand side of the digit.

The 5082-7340 hexadecimal indicator decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

The 5082-7304 is a "±1" overrange character, including decimal point, used in instrumentation applications.

FRONT VIEW 7302 (10.16) 7340 7300 (10.16) _____ 47 47 47 57.57.97 7'57 FUNCTION . .07 5082-7300 PIN 5082-7340 .07 (1.8 and 7302 17 41 Hexadecimal Numeric .55 .14 .14 1 Input 2 Input 2 2 Input 4 Input 4 (1.8 .09 ŧ 3 Input 8 Input 8 4 5 2 5 2 5 .14 4 Decimal Blanking .19 .19 4 B1 point control REAR VIEW SIDE VIEW END VIEW 5 Latch Latch enable enable 6 Ground Ground V_{cc} Input 1 V_{cc} Input 1 7 8 The x LUMICOUS INTENSITY CALL JORY 12.541 5022-DATE CODE 60 7300 NOTES: 1. Dimensions in inches and (millimeters). Unless otherwise spec-XYYZ PIN 1 KEY LOCATION 012 TYP ified, the tolerance on п (48) all dimensions is 2 +.015 inches. 12.51 .19

PACKAGE DIMENSIONS

ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Storage temperature, ambient	т _s	-40	+100	°c
Operating temperature, case	TC	-20	+85	°C
V _{sc} Pin potential to ground pin	V _{cc}	-0.5	+7.0	V
Voltage applied to input logic pins and decimal point (1)	Vin	-0.5	+5.5	V
Voltage applied to latch enable	VE	-0.5	+5.5	V
Voltage applied to blanking control (2)	VB	-0.5	+5.5	v

.

1.1

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NOTES: 1. Decimal point applies only to 7300/7302 2. Applies only to 7340 : .

RECOMMENDED OPERATING CONDITIONS

DESCRIPTION	SYMBOL	MIN	NOM	MAX	UNIT
Supply Voltage	V _{cc}	4.5	5.0	5.5	v
Logic voltage "O" state	V _{in(0)}	0		0.8	V
Logic voltage "1" state	V _{in(1)}	2.0	1	5.25	V
Latch enable voltage-date being entered	V _{E(0)}	0		0.8	V
Latch enable voltage-data not being entered	V _{E(1)}	2.0		5.25	V
Blanking control voltage-display not blanked (1)	V _{B(0)}	0		0.8	V
Blanking control voltage-display blanked (1)	V _{B(1)}	3.5		5.25	V

NOTE: 1. Applies only to 7340 ELECTRICAL/OPTICAL CHARACTERISTICS (T_C = -20°C to +85°C, unless otherwise specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current	I _{cc}	V _{cc} = 5.5V		94(1)	170 ⁽²⁾	ma
Power dissipation	PT	V _{cc} = 5.5V		470(1)	935(2)	mW
Luminous intensity per LED (Digit average) (3)	1	V _{cc} = 5.0V, T _C = 25°C	32	70		μcd
Time data must be presented to logic input prior to enable rising	^t setup	$V_{cc} = 5.0V, V_{E(0)} = 0.4V$ $V_{in(0)} = 0.4V, V_{E(1)} = 2.4V$ $V_{in(1)} = 2.4V, T_{C} = 25^{\circ}C$ $V_{cc} = 5.0V, V_{E(0)} = 0.4V$		30	50	ns
Timé data must be held after enable rises	^t hold	$V_{cc} = 5.0V, V_{E(0)} = 0.4V$ $V_{in(0)} = 0.4V, V_{E(1)} = 2.4V$ $V_{in(1)} = 2.4V, T_{C} = 25^{\circ}C$		30	50	ns
Time required for 90% change in display luminous intensity after change of state of V_B (4)	^t blank	V _{cc} = 5.0V, T _C = 25°C			500	ns
Blanking control current "O" state (4)	^I B(0)	V _{cc} = 5.5V, V _{B(0)} = 0.8V		ъ.,	200	μA
Blanking control current "1" state (4)	^I B(1)	V _{cc} = 5.5V, V _{B(1)} = 4.5V			2.0	mA
Logic and latch enable currents "O" state	lin(0), E(0)	V _{cc} ≠ 5.5V V _{in} , V _E = 0.4V			-1.6	mA
Logic and latch enable currents "1" state	^l in(1), l _{E(1)}	V _{cc} = 5.5V V _{in} , V _E = 2.4V			+250	μA
Peak wavelength	λpeak			655		nm
Spectral halfwidth	Δλ 1/2			30		nm
Weight				0.8		gm

1 NOTES: .

4. Applies only to 7340

1. V_{cc} = 5.0V with statistical average number of LED's lit.

a star alter a

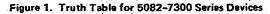
2. Worst case condition excluding test state on 5082-7300/-7302.

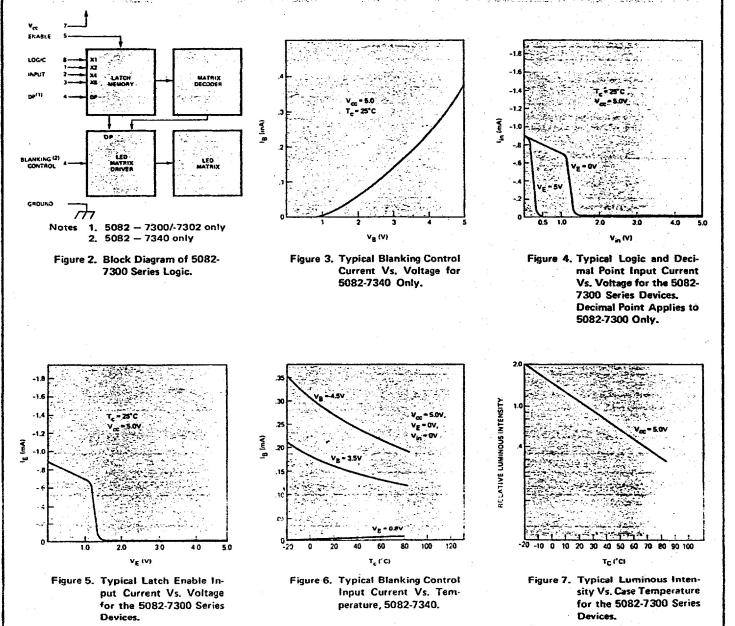
3. The digits are categorized for luminous intensity such that the variation from digit to digit within a category is not discernible to the eye. Intensity categories are designated by a letter located on the reverse side of the package contiguous with the Hewlett-Packard logo marking,

								· .			5				
CHARA	CTER			INPL	JTS			CHARA	CTER			INPL	UTS		
5082 7300/7302 Numeric	5082- 7340 Hex.	X 8	X4	X2	Х1	E	в ⁽¹⁾	5082- 7300/7302 NUMERIC	5082 7340 Hex.	X8	X4	X2	X1	E	B ⁽¹⁾
0	0	L	L	L	L	L	L	Test	A	H	L	н	L	ι	L
. 1	1	L	L	L	н	L	L	Blank	В	н	L	н	н	L	L
2	2	L	L	н	L	L	L	Blank	C	Н	н	L	L	L	L
3	3	L	L	н	н	L	L	Minus	D	н	н	L	Н	L	L
4	4	L	н	L	L	L	L	Blank	E	Н	н	Н	L	L	L
5	5	L	н	L	н	L	L	Blank	F	н	н	н	н	L	L
6	6	L	н	н	L	L	L	Hold	Hold	d	d	d	d	Н	d
7	7	L	н	н	н	L	L	-	Blank (1)	d	d	d	d	d	н
8	8	н	L	L	L	L	L	Decimal pt. on (2)	-			DPin	= L		-
9	9	н	L	L	н	Ł	L	Decimal pt. off (2)	-		•	DPin	≍H		

NOTES:

1. The blanking control input, B. pertains to the 5082-7340 Hexadecimal Indicator only. 2. The decimal point input pertains to the 5082-7300 and ~7302 Numeric Indicators only. 1 • 12

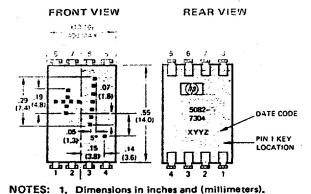


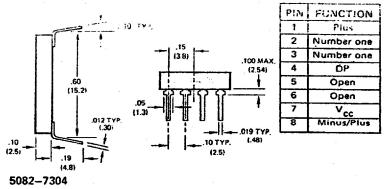


SOLID STATE PLUS/MINUS/ONE SIGN

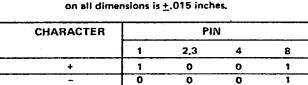
For display applications requiring a \pm or 1 designation, the 5082-7304 plus/minus/one sign including decimal point is available. This display module comes in the same package as the 5082-7300 series numeric indicator and is completely compatible with it.

SIDE VIEW





END VIEW



Unless otherwise specified, the tolerance

Figure 8. Truth table for 5082-7304

2.

ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Storage temperature, ambient	T,	-40	+100	°c
Operating temperature, case	TC	-20	+85	С
Forward current, each LED	I _F		10	mA
Reverse voltage, each LED	V _R		4	v

RECOMMENDED OPERATING CONDITIONS

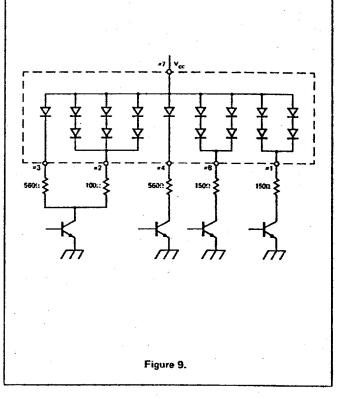
	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V _{cc}	4.5	5.0	5.5	v
Forward current, each LED	¹ F		5.0	10	mA

NOTE:

LED current must be externally limited. Refer to Figure 11 for recommended resistor values.

ELECTRICAL/OPTICAL CHARACTERISTICS (T_C = -20^oC TO +85^oC, UNLESS OTHERWISE SPECIFIED)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
LED forward voltage	V _F	I _F = 10 mA		1.6	2.0	v
Power dissipation	PT	I _F = 10 mA all diodes lit		250	320	mW
Luminous intensity per LED (DIGIT average)	ł	1 _F = 6 mA T _C = 25°C	32	70		μου
Peak wavelength	λ _{peak}			655		nm
Spectral halfwidth	Δλ1/2			30		nm
Weight				0.8		gm



TYPICAL DRIVING CIRCUIT FOR 5082-7304.

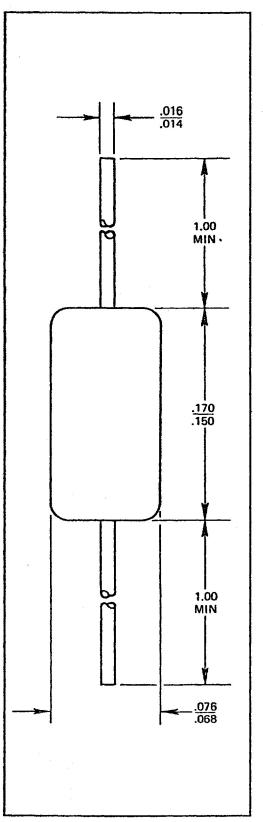
 <sup>1
 0
 1
 0
 0</sup> Decimal point
 0
 0
 1
 0

 Blank
 0
 0
 0
 0

NOTE: 0: Line switching transistor in Fig. 11 cutoff 1: Line switching transistor in Fig. 11 saturated



HOT CARRIER DIODES HP 5082-2800 SERIES



Features

LOW PRICE-50¢ at 1000 quantities allows use in any system.

FAST SWITCHING—Picosecond switching speed for high speed digital or logic circuits.

HIGH BREAKDOWN—70 volts breakdown allows high voltages in sampling gates, and wide dynamic range capability as UHF detector.

EXCELLENT ENVIRONMENTAL CAPABILITIES—200°C operating temperature. 20,000 G shock capability and overall ruggedness makes the 2800 family attractive for any military or other high reliability program.

Description

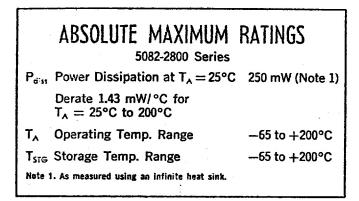
The HP 5082-2800 series is an epitaxial, planar, passivated diode whose construction utilizes a unique combination of both a conventional PN junction and a Schottky barrier. The manufacturing process (Patent No. 3463971), results in a device which has the high breakdown and temperature characteristics of silicon, the turn-on voltage of germanium, and the speed of a Schottky barrier, majority carrier device.

Applications

High level detection, switching, or gating; LOG or A-D converting; sampling or wave shaping are jobs the 2800 family will do better than conventional PN junction diodes. The low turn on voltage and subnanosecond switching makes it extremely attractive in digital circuits for DTL gates, pulse shaping circuits or other low level applications. Its high PIV allows wide dynamic range for fast high voltage sampling gates.

The 2800's low turn-on voltage gives low offsets. The extremely low stored charge minimizes output offsets caused by the charge flow in the storage capacitor. At UHF, the diodes exhibit 95% rectification efficiencies. Both their low loss and their high PIV allow the diodes to be used in mixer and modulator applications which require wide dynamic ranges.

The combination of these technical features with the low price make these devices the prime consideration for any dc or RF circuit requiring nonlinear elements.



MECHANICAL SPECIFICATIONS

The HP Outline 15 package has a glass hermetic seal with dumet leads. The leads on the Outline 15 package should be restricted so that the bend starts at least $\frac{1}{16}$ mm) from the glass body. With this restriction, Outline 15 package will meet MIL-STD-750, Method 2036, Conditions A and E [4 lb (1,8 kg)] tension for 30 minutes. The maximum soldering temperature is 230°C \pm 5°C for five seconds.

Outline 15 package inductance and capacitance is typically 2.3 nH and 0.17 pF, respectively.

Marking is by digital coding with a cathode band.

Diode Type	Specification	Symbol	Min	Max	Units	Test Conditions
5082-2800 2810 2811	Breakdown Voltage	V _{BR}	7Ò 20 15		Volts	$I_R = 10 \ \mu A$
5082-2800 2810 2811	Forward Voltage	V _{F1}		410 410 410	mV	$I_{\tilde{r}1} = 1 \text{ mA}$
5082-2800 2810 2811	Forward Current	I _{F1}	15 35 20		mA	$V_{F2} = 1$ volt (note 1)
5082-2800 2810 2811	Reverse Leakage Current	I _R	•	200 100 100	nA	$V_{R} = 50 V V_{R} = 15 V V_{R} = 8 V V_{R} = 5 V$
5082-2800 2810 2811	Capacitance	C _{ī(o)}	-	2.0 1.2 1.2	pF	$V_R = 0 V$ and $f = 1 MHz$
5082-2800 2810 2811	Effective Minority Carrier Lifetime	T ·		100 100 100	p sec	I _F = 5 mA Krakauer Method

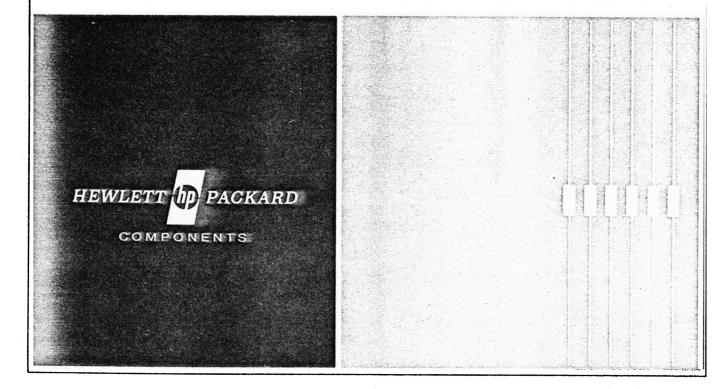
ELECTRICAL SPECIFICATIONS AT $T_A = 25$ °C

Note 1: The test condition and specification are interchanged to make the tabulation easier to read. The actual test condition is forward current; the

actual specification is forward voltage. The forward current is limited to prevent thermal runaway.

APPLICATION NOTE 936

HIGH PERFORMANCE PIN ATTENUATOR FOR LOW COST AGC APPLICATIONS



SUMMARY

PIN diodes offer an economic way of achieving excellent performance in AGC circuits. Significant improvements in crossmodulation and intermodulation distortion performance compared to transistors are obtained.

Other advantages of PIN diodes, such as good low frequency operation, constant impedance levels, and low power consumption will be discussed in this article.

INTRODUCTION

In the short time since its introduction, the PIN diode has found many areas of application. New developments in diode design have allowed the PIN diode to be useful at much lower frequencies than ever before. This article describes its use as an attenuator for automatic gain control and compares its performance to a transistorized AGC system in a television receiver.

The most important feature of the PIN diode is its inherent ability to act as a current controlled resistor at RF frequencies. Most diodes possess this capability to some degree, but the PIN diode is especially optimized in design to achieve a wide resistance range with consistently good linearity and low distortion. As typically shown in Figure 1, when the control current is varied continuously from 1 μ A to 100 mA, the resistance of a PIN diode will change from over ten thousand ohms to about one ohm. This characteristic variation of resistance with current makes the PIN diode ideally suited for application in automatic gain control systems.

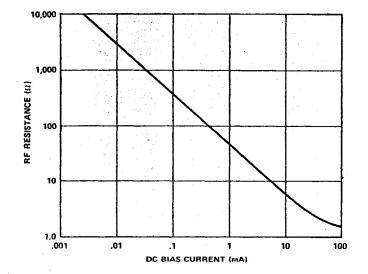


Figure 1. Typical Pin Diode Resistance Versus Control Current.

The PIN diode is similar to ordinary PN junction diodes except for an added intrinsic region (I-layer) sandwiched between the p^+ and n^+ layers. It is in

this I-layer that the control of minority carriers is enhanced. The high resistance and large width of the intrinsic layer result in a high breakdown voltage and low capacitance. When forward bias is applied between p^+ and n^+ layers, the injection of minority carriers into the intrinsic region increases the conductivity of the I-layer.

Above a limiting frequency the PIN diode acts as a pure resistance. This RF resistance is controlled by varying the forward bias. Below the limiting frequency, rectification occurs as in an ordinary PN diode. In the vicinity of the limiting frequency there is some rectification with resulting distortion in RF resistance. The amount of distortion is dependent on the bias current, RF power, the frequency, and minority carrier lifetime. Distortion becomes appreciable at a frequency of operation equal to about 10 times the inverse of the minority carrier lifetime. Diodes of the HP 5082-3080 series. especially designed for low frequency operation, have a lifetime in excess of 1 microsecond, and are thus useful below 10 MHz. As an example, these low frequency PIN diodes are suitable for use in the attenuator to be described here for AGC application in television receivers.

AUTOMATIC GAIN CONTROL SYSTEMS

Many receivers today use transistors to accomplish their AGC requirements. For normal operation these transistors are biased for maximum gain. When the signal exceeds a set threshold level, automatic gain control is achieved by an increase in bias current, which results in a gain reduction. The principle of forward AGC is applied.

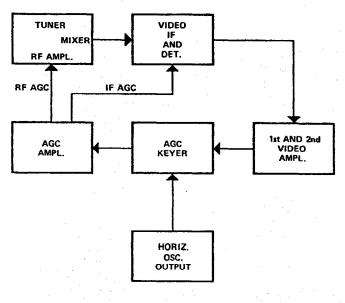


Figure 2. Block Diagram of a Typical AGC System in a TV Receiver.

A block diagram of a typical AGC system in a television receiver is shown in Figure 2. The objective is to keep the output of the video detector constant with increasing RF signal levels. The usual way of determining the signal strength of the incoming signal is to use the height of the horizontal pulses as a reference. A synchronized AGC keyer is used for this purpose. The threshold level required to trigger the keyer is preset. A winding in the flyback transformer supplies the horizontal pulses needed to bias the keyer transistor. When the keyer is off, the AGC amplifier supplies the required voltage to bias the RF and IF amplifiers for maximum gain. When the signal from the video amplifier exceeds the threshold level during the horizontal sync pulse, the keyer turns on and biases the AGC off. This results in an increased AGC voltage to the RF and IF amplifiers and thus a reduction in gain.

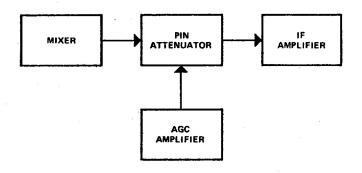


Figure 3. Use of a PIN Diode Attenuator as an Interstage for Providing AGC.

When AGC is applied to a transistor, the optimum operating point is disturbed, and the input and output impedances change drastically. This change will, of course, adversely affect the associated tuned circuit. The use of a PIN diode attenuator as an interstage, as shown in Figure 3, will provide a wide range of gain control without disturbing the optimum operating point of the associated circuit elements. This minimizes changes in impedance levels, phase shift and tuning, while achieving the required change in gain.

When the basic requirements of an attenuator for AGC application in a receiver are considered, the reasons for the superiority of PIN diodes over other PN junction diodes will become obvious. In particular, consider the use of 3 low frequency diodes in a π configuration attenuator as shown in Figure 4. The ratio of on to off resistance of PIN diodes is significantly greater than that of other diodes, so that the insertion loss is lower and the maximum attenuation is greater. In terms of AGC this means larger dynamic range. The linearity of resistance as a function of bias makes the PIN diode less susceptible to modulation distortion. In

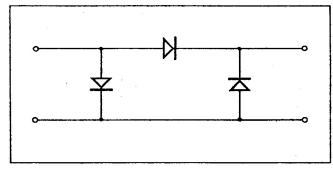


Figure 4. 3 Diode π Attenuator.

the VHF/UHF range distortion from partial rectification cannot be tolerated. The use of low frequency PIN diodes ensures that distortion be minimized at these low frequencies. HP 5082-3080 and 5082-3081 PIN diodes with lifetime, respectively, in excess of 1 and 1.5 microseconds are usable below 10 MHz.

PERFORMANCE CHARACTERISTICS

A transistorized amplifier stage and a low frequency PIN diode attenuator built for AGC performance comparison are shown, respectively, in Figures 5 and 6. In each case there is a fixed supply voltage of 12 volts and a variable voltage for AGC control.

In the transistor circuit the principle of forward AGC is applied. In addition to the fixed 12 volts an AGC voltage of -4.5 volts is required to bias the

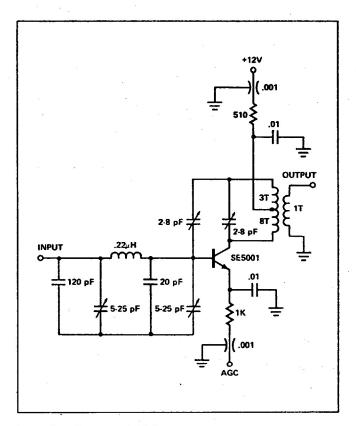


Figure 5. Transistor AGC Circuit.

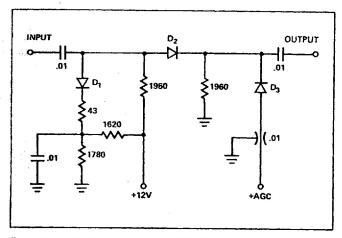


Figure 6. PIN Diode Attenuator AGC Circuit.

transistor for maximum gain. Further increase in AGC voltage results in a larger collector current and a reduction in gain. A curve of Gain Reduction versus AGC voltage at 45 MHz is shown in Figure 7. A maximum gain of approximately 40 dB is obtained at an AGC voltage of -4.5 volts. With more AGC voltage the gain decreases until a gain reduction of 40 dB is achieved at about 11.5 volts of AGC voltage.

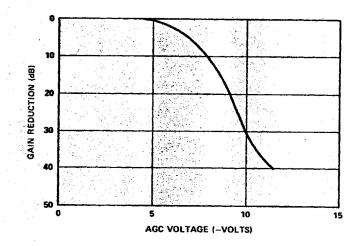


Figure 7. Gain Reduction Versus AGC Voltage Transistor AGC Circuit 45 MHz.

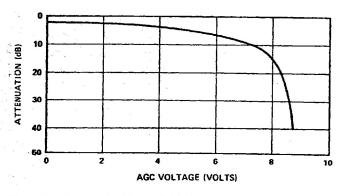


Figure 8. Attenuation Versus AGC Voltage PIN Diode Attenuator AGC Circuit 45 MHz.

Attenuation versus AGC voltage for the PIN attenuator circuit is shown in Figure 8. There is minimum attenuation when the AGC voltage is zero. The attenuation increases with AGC voltage until 40 dB of attenuation is obtained with 8.75 volts of AGC voltage. For 40 dB of attenuation the PIN attenuator requires 35 mW of power, while the transistor circuit consumes 120 mW for the same gain reduction.

Intermodulation and crossmodulation characteristics of the transistor and PIN attenuator AGC circuits are illustrated in Figures 9 through 14. A block diagram of the test equipment used for these distortion measurements is shown in Figure 15. The wave analyzer is used only for the crossmodulation tests. The tests are conducted with two equal amplitude input signals, one at 45 MHz and the other at 45.5 MHz. For the crossmodulation measurements one of the input signals is 100% modulated with a 15 KHz signal from the wave analyzer.

Examination of the distortion characteristics will reveal significant differences in performance of the two AGC circuits. Over a 30 dB dynamic range,

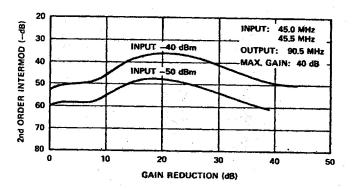


Figure 9. Second Order Intermodulation Versus Gain Reduction Transistor AGC Circuit.

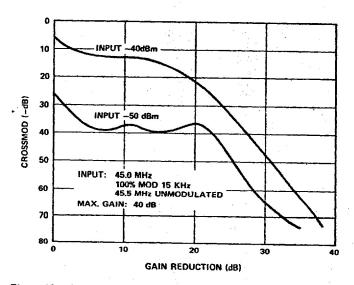


Figure 10. Crossmodulation Versus Gain Reduction Transistor AGC Circuit.

it is seen that second order intermodulation distortion at the same level of fundamental output is less in the PIN attenuator than in the transistor circuit. The difference at some points in the range is in excess of 10 dB. Longer lifetime HP 5082-3081 PIN diodes definitely show more favorable intermodulation characteristics than the HP 5082-3080 diodes. The superiority of the PIN attenuator as an AGC circuit is even more apparent with comparison of the crossmodulation characteristics. At some power levels, crossmodulation in the transistor circuit is seen to be 50 dB worse. A comparison of Figure 12 and 14 indicates better crossmodulation rejection when using HP 5082-3080 PIN diodes.

A comparison of the PIN and transistor AGC circuit performance is shown in Table 1.

ц	PINI	Transistor	
	5082-3080	5082-3081	
Power Consumption, mW	35	35	120
2nd Order Intermod, dB (20 dBm output)	-59	64	-55
Crossmodulation (20 dBm output)	68	59	-37

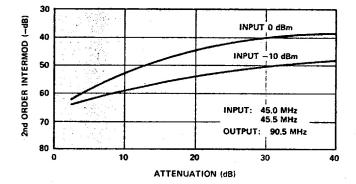
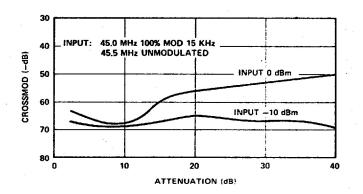
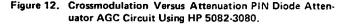
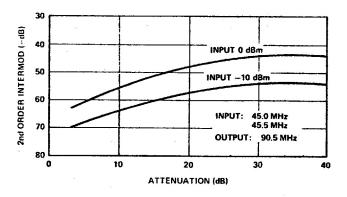


Figure 11. 2nd Order Intermodulation Versus Attenuation PIN Diode Attenuator AGC Circuit Using HP 5082-3080.









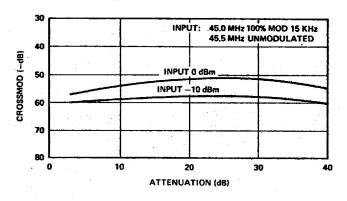


Figure 14. Crossmodulation Versus Attenuation PIN Diode Attenuator AGC Circuit Using HP 5082-3081.

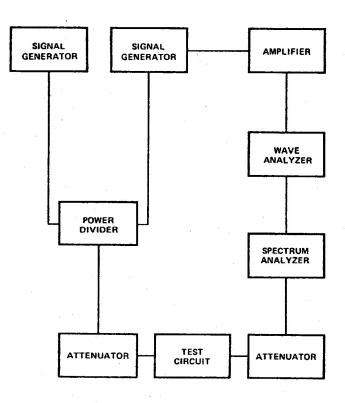


Figure 15. Block Diagram of Test Equipment used for Distortion Measurement.

CONCLUSION

Automatic gain control in a transistorized circuit requires that the optimum operating point of the AGC transistor be shifted. This produces a drastic change in the impedance level, which severely affects the adjoining tuned circuit.

The use of a PIN diode attenuator as the AGC

control element will provide the required gain control without the attendant problems of large impedance shift. The result is minimum distortion in the output coupled with low power consumption. The use of long lifetime PIN diodes gives added assurance of usefulness at low frequencies for low cost applications.

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