VLA TECHNICAL REPORT #5

MODULE T6

IF CONTROL

A. R. Thompson

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Interoffice Memorandum by S. Weinreb dated February 27, 1974

Subject: VLA Monitor and Control System-Summary

II. Theory of Operation

The IF Control module serves as an interface for transmission of control and monitor data between the IF Receiver modules and the data set.* It also makes provision for the use of either manual or automatic gain control. A block diagram of the unit is shown in Figure 1.

Input and output of data from the unit are controlled by four parallel address lines from the Data Set. These go to the address decoder which controls the input and output functions of two shift registers through a series of gates. When the appropriate address appears, a 24 bit command word is serially entered into the command shift register from the data set. This word is automatically loaded into the 24 bit latch as soon as it is received. To check the data link the word can then be read back from the command register into the Data Set if requested by the computer. The 12 least significant bits of the command word contain four sets of three bits which are used to select the required filters in the four IF Receiver modules. These four sets of bits enter four two-line to one-line multiplexers, the other inputs to which come from three front panel switches. The four multiplexers are individually controlled by four front panel switches, so the filter selection of any of the IF Receiver modules can either be controlled by the computer or manually, as desired. Under computer control the filter selection can be different for each IF Receiver, but in the manual mode the same three bit signal controls all modules.

From the monitor shift register a word can be read back to the computer. The 12 least significant bits of the monitor register input are connected to the multiplexer output lines to show the filter select signals actually being used, and the four most significant bits indicate the state of the four switches that

*One IF Control module is used for each antenna and is located in the central building, rack N, bin S, slot 12.

select the computer or manual control mode. These four switches also select the gain control voltages applied to the IF Receiver modules, which can be either the ALC voltages from the sampler units or manually adjustable voltages from four potentiometers. The four potentiometers are each mounted next to the corresponding mode selection switch on the front panel of the IF control module, and the position of each switch is labeled AUTO or MAN. In the automatic position the corresponding IF Receiver has its gain controlled by an ALC loop and the filter used is selected by the computer. In the manual switch position the potentiometer controls the IF gain and the filter used is selected by the three front panel switches which are labeled FILTER SELECT.

The IF Control module also contains an analog multiplexer which selects any one of sixteen input voltages to be monitored by the data set. This multiplexer is controlled by the same four address lines that control input and output of the digital data. The inputs to the multiplexer include ALC, IF level and power supply voltages, the last being reduced by resistive dividers when greater than ten volts positive or negative.

III. Circuit Details

All of the digital integrated circuits are standard types described in the Texas Instruments TTL Data Book and only a brief description of the circuitry will be given. A complete logic diagram is shown in Figure 2. All of the active components are mounted on a 4" x 6-1/4" wirewrap board. Switches and potentiometers are mounted on the front panel of the module and resistive dividers used in voltage monitoring are mounted on a separate terminal board. Location of parts on the wirewrap board is shown in Figure 3.

All inputs from the data set used low-true logic. The input circuits for the four address lines are of the low power type (74L04 inverting

gates) to reduce the load on those particular outputs of the data set. The address decoder is a 74154 in a 24 pin package.

The control shift register consists of three 74164 serial-in, parallel-out circuits. The input of data into this register is controlled by the input enable signal and the input clock. The output when reading back the word is controlled by the output ① enable signal and the output clock.

The latch consists of six 74177 integrated circuits and the data is loaded into them by the input strobe signal. The four two-line to one-line multiplexers are 74157 integrated circuits.

The monitor shift register consists of three 74165 parallel-in, serial-out circuits and the data is loaded into them by the output strobe. The shifting out of the data into the data set is controlled by the output ② enable signal and the output clock. Digital output circuits to the data set consist of 7438 gates with open collectors which drive a load resistor in the data set.

The analog multiplexer consists of two 507A (Harris Semiconductor) units with balanced inputs and outputs. Note that the two halves of each 507A are shown as separate blocks in Figure 2. The voltages connected to the multiplexer inputs are given in the following section.

IV. Addresses and Bit Assignments

(a) Digital Data

For input to the command shift register the required four-bit address code is 0000. The same four-bit address is used for reading back the command word. For output from the monitor shift register the 4-bit address is 0001. The command word input is connected to command output B of the Data Set

and the command readback and monitor word outputs are connected to monitor input C. The resulting octal addresses required are as follows:

	Octal Address
IF Control Command Word (input)	340
Readback of Command Word (output)	240
IF Control Monitor Word (output)	241

In assigning the bits in the control and monitor words two conventions have been followed:

(a) The most significant bit of the word is transmitted first

(b) Value strings should be right adjusted (i.e. towards the least significant end) in the words, and flag bits should be left adjusted. Bit assignments in the command and monitor words are given below.

<u>Command Word</u>

BIT NO.							
1 (LSB)	IF Receiver	1,	filter	select	LSB		Filter select signals from computer.
2	"	"	"	"	"		
3	"	"	"	"	"	MSB	
4	"	"	2	"	"	LSB	
5	"	"	"	"	"		
6	"	"	"	"	"	MSB	
7	"	"	3	"	"	LSB	
8	"	"	"	"	"		
9	"	"	"	"	"	MSB	
10	"	"	4	"	"	LSB	
11	"	"	"	"	"		
12	"	"	"	"	"	MSB	

Command Word (cont.)

BIT NO.	
13	Spare, to output connector P1 pin Y
14	" " " " " " Z
15	" " " " " " a
16	" " " " " " b
17	" " " " " " c
18	" " " " " " d
19	" " " " " " e
20	" " " " " " f
21	Unused
22	"
23	"
24 (MSB)	"

Monitor Word

1 (LSB)	IF Receiver	1,	filter	select	LSB		
2	"	"	"	"	"		
3	"	"	"	"	"	MSB	
4	"	"	2	"	"	LSB	Filter select
5	"	"	"	"	"		signals used,
6	"	"	"	"	"	MSB	from computer
7	"	"	3	"	"	LSB	or from
8	"	"	"	"	"		manual switches.
9	"	"	"	"	"	MSB	
10	"	"	4	"	"	LSB	
11	"	"	"	"	"		
12	"	"	"	"	"	MSB	
13	Unused						
14	"						
15	"						
16	"						

Monitor Word (cont.)

BIT NO.	
17	Spare, to output connector P1 pin h
18	" " " " " " j
19	" " " " " " k
20	" " " " " " m
21	IF Receiver 1 mode, AUTO=low, MAN=high
22	" " 2 " " " " "
23	" " 3 " " " " "
24 (MSB)	" " 4 " " " " "

(b) Analog Data

The output of the analog multiplexer is connected to analog channel 4 of the Data Set, and the sixteen address values are represented by octal numbers 100 to 117. These addresses and the corresponding analog signals monitored are given below.

OCTAL ADDRESS		
100	ALC voltage, IF Receiver 1	
101	" " " " 2	
102	" " " " 3	
103	" " " " 4	
104	Level monitor voltage, IF Receiver 1	
105	" " " " " 2	
106	" " " " " 3	
107	" " " " " 4	
110	Power supply voltage +5V	Power supplies in Rack N in the Control building (the IF/LO rack for each antenna).
111	" " " -5.2V	
112	" " " +15V/2	
113	" " " -15V/2	
114	" " " +28V/4	
115	" " " -28V/4	
116	Spare, to output connector P2, pins HH(+), JJ(-)	
117	" " " " " " KK(+), LL(-)	

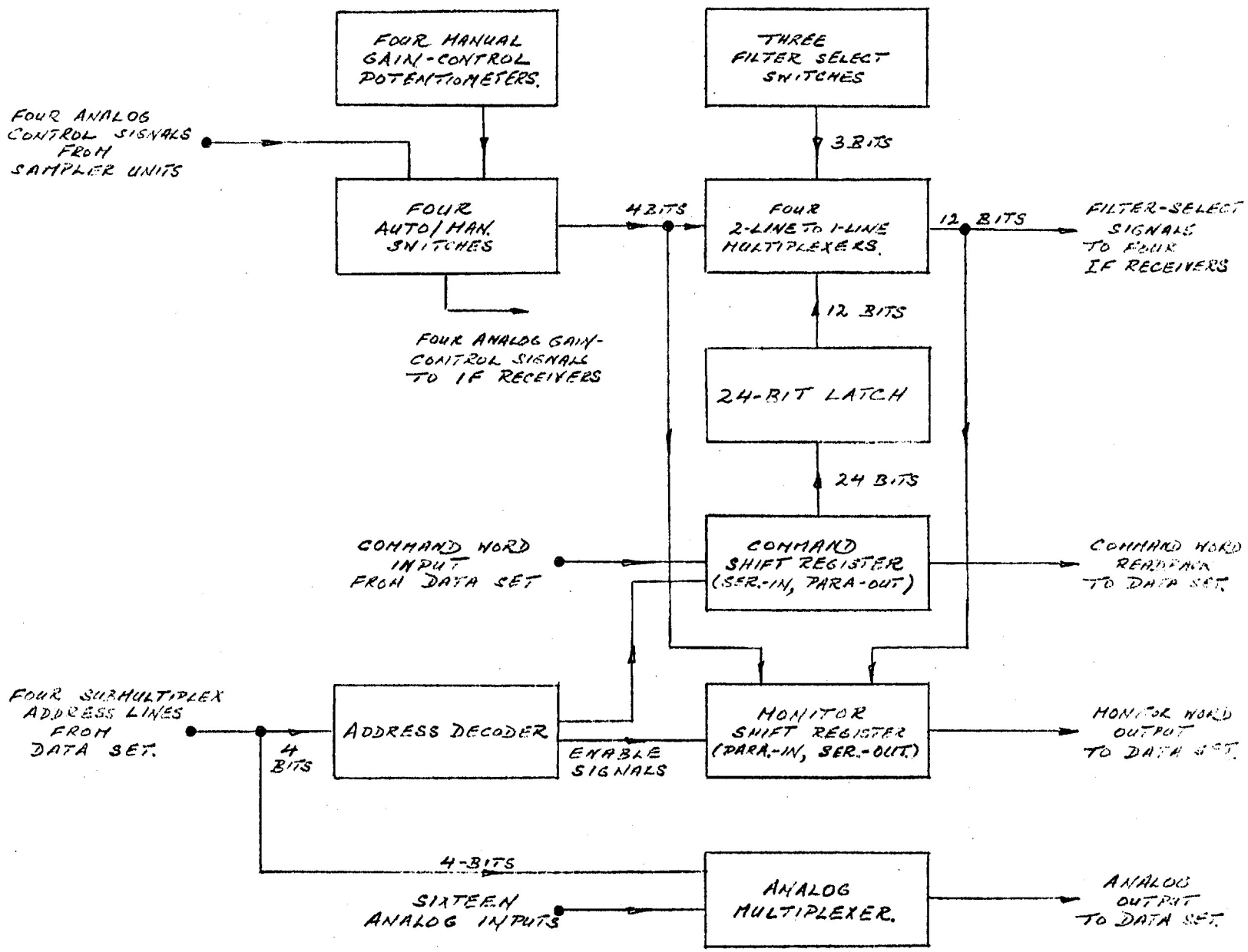
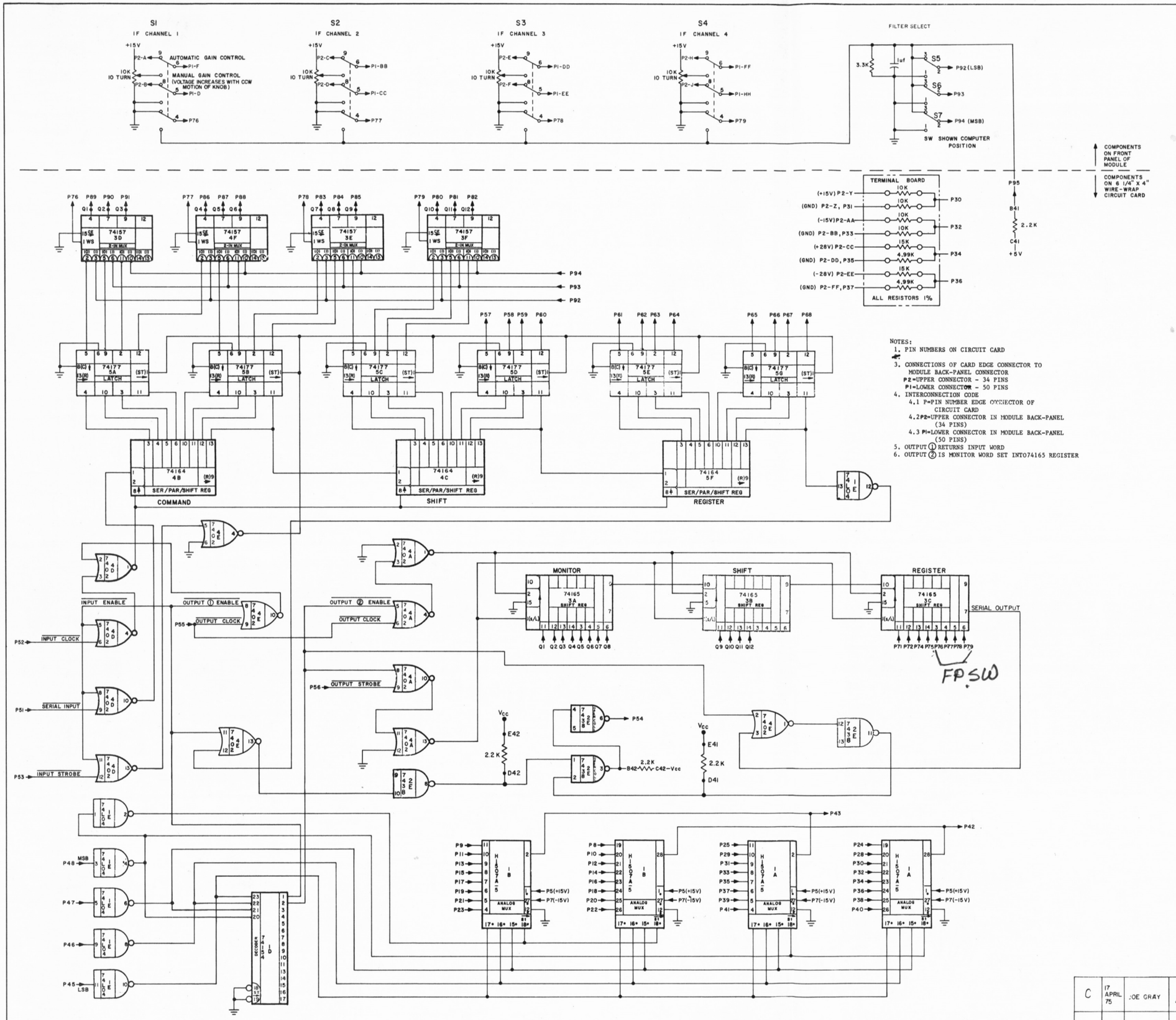


FIGURE 1. BLOCK DIAGRAM OF IF CONTROL MODULE.

A.R.T. 10/4/74



NOTES:
1. PIN NUMBERS ON CIRCUIT CARD
3. CONNECTIONS OF CARD EDGE CONNECTOR TO MODULE BACK-PANEL CONNECTOR
   P2=UPPER CONNECTOR - 34 PINS
   P1=LOWER CONNECTOR - 50 PINS
4. INTERCONNECTION CODE
   4.1 P=PIN NUMBER EDGE CONNECTOR OF CIRCUIT CARD
   4.2 P2=UPPER CONNECTOR IN MODULE BACK-PANEL (34 PINS)
   4.3 P1=LOWER CONNECTOR IN MODULE BACK-PANEL (50 PINS)
5. OUTPUT ① RETURNS INPUT WORD
6. OUTPUT ② IS MONITOR WORD SET INTO 74165 REGISTER

SEE NOTE 1

#			COLOR	SEE NOTE 3	
1	GND.		BLK	P1-B	
2	+5V		ORN	P1-C	
3	GND.		BLK	P1-B	
4	+5V		ORN	P1-C	
5	+15V		RED	P1-A	
6	GND.		BLK	P1-L	
7	-15V		YEL	P1-E	
8	1+ ANALOG MULTIPLEXER INPUT		RED	P2-A	ALC CONTROL VOLTAGE FROM SAMPLER
9	1- " " "		YEL	P2-B	
10	2+ " " "		GRN	P2-C	
11	2- " " "		BLU	P2-D	
12	3+ " " "		VIO	P2-E	
13	3- " " "		RED	P2-F	
14	4+ " " "		YEL	P2-H	
15	4- " " "		GRN	P2-J	
16	5+ " " "		BLU	P2-K	IF LEVEL SIG
17	5- " " "		VIO	P2-L	
18	6+ " " "		RED	P2-M	
19	6- " " "		YEL	P2-N	
20	7+ " " "		GRN	P2-P	
21	7- " " "		BLU	P2-R	
22	8+ " " "		VIO	P2-S	
23	8- " " "		RED	P2-T	
24	9+ " " "		YEL	P2-U	+5V
25	9- " " "		GRN	P2-V	GND
26					
27	GND.				
28	10+ ANALOG MULTIPLEXER INPUT		BLU	P2-W	-5V
29	10- " " "		VIO	P2-X	GND
30	11+ " " "		RED		TERMINAL BOARD
31	11- " " "		YEL	P2-Z	
32	12+ " " "		GRN		
33	12- " " "		BLU	P2-BB	
34	13+ " " "		VIO		
35	13- " " "		RED	P2-DD	
36	14+ " " "		YEL		
37	14- " " "		GRN	P2-FF	
38	15+ " " "		BLU	P2-HH	SPARE
39	15- " " "		VIO	P2-JJ	
40	16+ " " "		RED	P2-KK	
41	16- " " "		YEL	P2-LL	
42	ANALOG MULTIPLEXER OUTPUT (HIGH)		GRN	P2-MM	
43	" " " (GND)		BLU	P2-NN	
44					
45	ADDRESS BIT 0 (LSB) (LOW TRUE)		RED	P1-M	
46	" " 1 " "		YEL	P1-N	
47	" " 2 " "		GRN	P1-P	
48	" " 3 (MSB) " "		BLU	P1-R	
49	GND.				
50					
51	SERIAL INPUT (LOW TRUE)		VIO	P1-S	TO COMMAND OUTPUT B OF DATA SET
52	INPUT CLOCK		RED	P1-T	
53	INPUT STROBE		YEL	P1-U	
54	SERIAL OUTPUT		GRN	P1-V	TO MONITOR INPUT C OF DATA SET
55	OUTPUT CLOCK		BLU	P1-W	
56	OUTPUT STROBE		VIO	P1-X	
57	INPUT WORD BIT 13		RED	P1-Y	SPARE
58	" " " 14		YEL	P1-Z	
59	" " " 15		GRN	P1-a	
60	" " " 16		BLU	P1-b	
61	" " " 17		VIO	P1-c	
62	" " " 18		RED	P1-d	
63	" " " 19		YEL	P1-e	
64	" " " 20		GRN	P1-f	
65	" " " 21				
66	" " " 22				
67	" " " 23				
68	" " " 24				
69					
70					
71	OUTPUT WORD BIT 17		BLU	P1-h	SPARE
72	" " " 18		VIO	P1-j	
73	GND.				
74	OUTPUT WORD BIT 19		RED	P1-k	
75	" " " 20		YEL	P1-m	F.P. IF UNIT SELECT
76	" " " 21			F.P. SW. NO. 1	
77	" " " 22			" 2	
78	" " " 23			" 3	
79	" " " 24			" 4	
80	FILTER SEL. IF CH 4 BIT 1 LSB		GRN	P1-n	
81	" " " " 2		BLU	P1-p	
82	" " " " 3 MSB		VIO	P1-r	
83	" " " CH 3 " 1 LSB		RED	P1-s	
84	" " " " 2		YEL	P1-t	
85	" " " " 3 MSB		GRN	P1-u	
86	" " " CH 2 " 1 LSB		BLU	P1-v	
87	" " " " 2		VIO	P1-w	
88	" " " " 3 MSB		RED	P1-x	
89	" " " CH 1 " 1 LSB		YEL	P1-y	
90	" " " " 2		GRN	P1-z	
91	" " " " 3 MSB		BLU	P1-AA	
92	MANUAL FILTER SEL. BIT 1				
93	" " " " 2				
94	" " " " 3				
95	PULL UP RESISTOR FILTER SELECT	F.P. SW.			
96					
97	GND.		BLK	P1-B	
98	+5V		ORN	P1-C	
99	GND.		BLK	P1-B	
100	+5V		ORN	P1-C	

FIGURE 2

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
C	17 APRIL 75	JOE GRAY		CH'GD SER OUT FROM 74165-9 TO -7 ADDED 74LO4-12 TO 13 CIRCUIT ADDED RESISTOR AT E42 TO D42 ADDED RESISTOR AT E41 TO D41 ADDED IC 7438 AT 2E
B	3/15/75	J. GRAY		FILTER SELECT DIAGRAM SHOWED SW. IN TOGGLE UP POSITION. ADDED TERM. NOS. TO FILTER SEL. ADDED TERM. NOS. TO "S" THRU S4
A	10/18/74	J. GRAY		CHANGE OF DESIGNATIONS OF I.F. FILTER SEL. BITS & ADDRESS BITS

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
V L A				IF CONTROL MODULE TG
TITLE				IF CONTROL BOARD

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

DRAWN BY	Harold Ward	DATE	6-5-74
DESIGNED BY	A.H. THOMPSON	DATE	6-4-74
APPROVED BY		DATE	

SHEET NUMBER | DRAWING NUMBER D13450L3 | REV C | SCALE

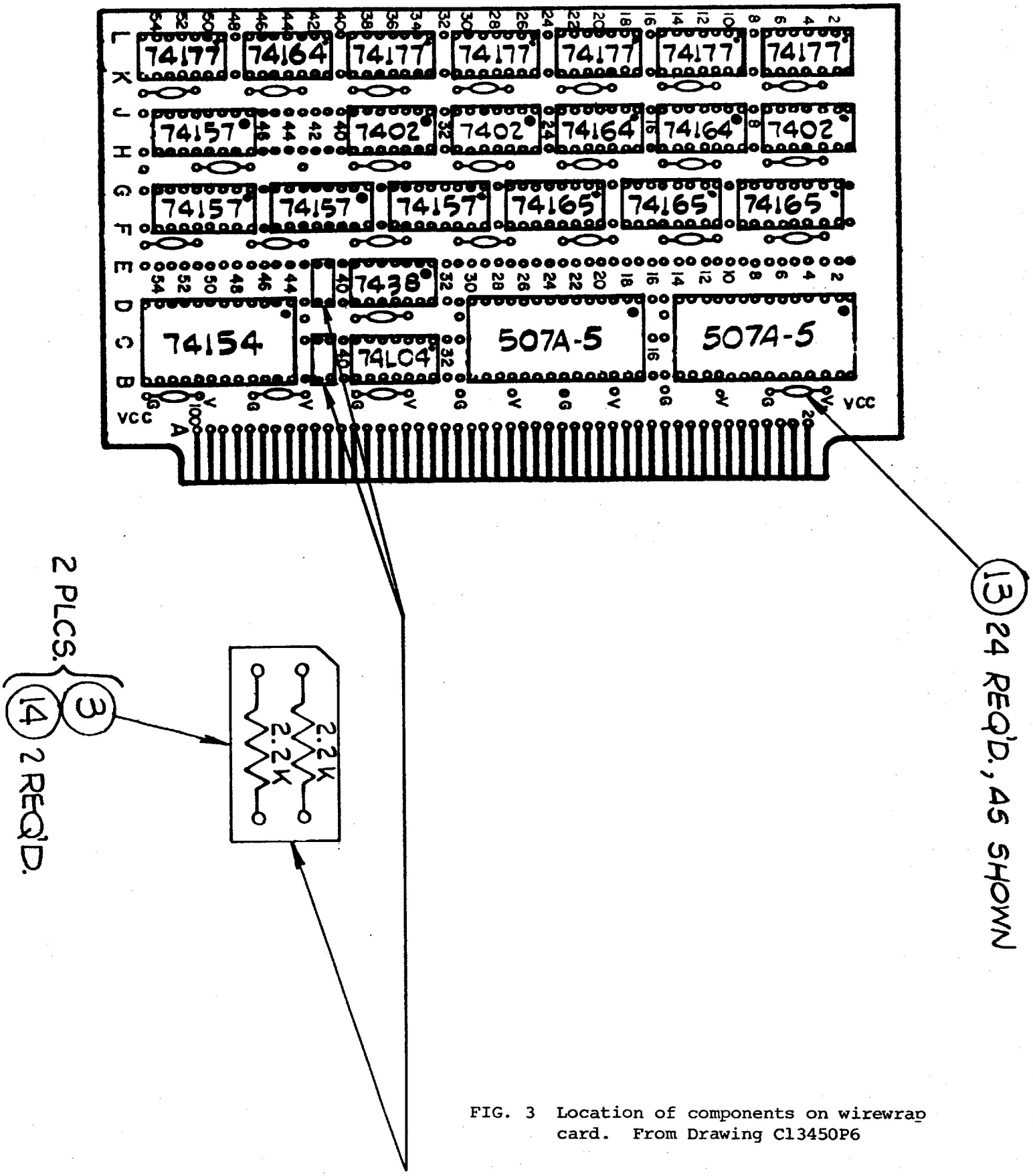


FIG. 3 Location of components on wirewrap card. From Drawing C13450P6

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[X] ELECTRICAL [ ] MECHANICAL BOM # A1345025 REV A DATE _____ PAGE 1 OF 1

MODULE # T6 NAME I.F.CONTROL DWG # C13450P6 SUB ASMB 5 Row, 100 Pin WIRE WRAP CD. DWG # C13450P6

SCHEMATIC DWG # _____ LOCATION _____ QUA/SYSTEM _____ PREPARED BY JOE GRAY APPROVED C Pace

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		N.R.A.O.	C13450P6	10 ROW,100 PIN, WIRE WRAP CARD ASS'Y.		
2		N.R.A.O.	D13520M2	WIRE WRAP BOARD	1	
3		N.R.A.O.	B13250M18	4 PIN COMPONENT MOUNTING PLATFORM	2	
4		TEXAS INSTRUMENTS	74165	SHIFT REG.	3	
5			74157	2 LINE TO 1LINE MUX.	4	
6			7438	2 INPUT NAND OPEN COLLECTOR	1	
7			74L04	HEX INVERTER	1	
8			74154	16 LINE TO 1 LINE MUX	1	
9			7402	NOR	3	
10			74164	SHIFT REG.	3	
11			74177	LATCH	6	
12		HARRIS	507A-5	ANALOG MUX	2	
13		ERIE	8121-050-651-223M	.022 ufd CAPACITOR	24	
14			2.2k, ¼w, ± 5%	RESISTOR	4	
15		A.R. GORE	#30 AWG, VIOLET	SP 135 SINGLE STRAND, MYLENE INSUL WIRE	91 ft.	

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[X] ELECTRICAL [ ] MECHANICAL BOM # A1345076 REV _____ DATE _____ PAGE 1 OF 5

MODULE # T6 NAME I.F. CONTROL DWG # D13450P7 SUB ASMB _____ DWG # _____

SCHEMATIC DWG # _____ LOCATION _____ QUA/SYSTEM _____ PREPARED BY Joe Gray APPROVED [signature]

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		N.R.A.O.	D13450P7	I.F. CONTROL ASSEMBLY	~	
2		N.R.A.O.	B13450P8	TERMINAL BD. ASSEMBLY	1	
3		N.R.A.O.	C13450P6	WIRE WRAP BOARD ASS'Y.	1	
4		WINCHESTER	HWL5000-112	100 PIN CARD EDGE CONN.	1	
5		G.C. ELECTRONICS	5706-C	GROUND LUG	1	
6		SPECTRAL	HEL05-10	10K, 10 TURN, POT.	4	
7		ROGAN CORP.	RB67-0 MAHE	KNOB, NO INLAY	4	
8		J.B.T.	JMT 323	3 P., D.T. TOGGLE SWITCH	4	
9		J.B.T.	JMT 123	1 P., D.T. TOGGLE SWITCH	3	
10		AMP SPECIAL INDUST.	201358-3	50 PIN CONNECTOR	1	
11			201357-3	34 PIN CONNECTOR	1	
12			66460-6	WIRE WRAP PIN	59	
13			202725-1	CRIMP PIN	22	
14			202394-2	50 PIN CONN. SHIELD	1	
15		AMP SPECIAL INDUST.	202434-4	34 PIN CONN. SHIELD	1	

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NATIONAL RADIO ASTRONOMY OBSERVATORY

[X] ELECTRICAL [ ] MECHANICAL BOM # A1345076 REV _____ DATE _____ PAGE 2 OF 5

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
16		AMP SPECIAL INDUST.	203964-6	GUIDE SOCKET	4	
17			200833-4	GUIDE PIN	2	
18		AMP SPECIAL INDUST.	202514-1	GUIDE PIN	2	
19		ERIE	8131-050-651 -105M	1.0 μf CAPACITOR	1	
20			3.3 K, 1/4 W, ± 5%	RESISTOR	1	
21		A.R. GORE	#SP135, 30 AWG	"MYLENE" INSUL., SING. STRAND WIRE	150 FT.	
22		PENNTUBE PLASTICS CO.	0-6591A, 22 AWG 1W NATURAL	TEFLON TUBING	24 IN	
23		ALPHA	8021-100, 22 AWG TINNED COPPER	WIRE, BUS	24 IN	
24			#22 AWG, BLK.	WIRE, HOOK-UP, P.V.C.	70 IN	
25			, ORN.		70 IN	
26			, RED		80 IN	
27			, YEL.		60 IN	
28			, BLU		50 IN	
29			, GRN.		40 IN	
30			, VIO.		24 IN	
31			, GRY		40 IN	
32		ALPHA	#22 AWG, BRN	WIRE, HOOK-UP, P.V.C.	26 IN	

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NATIONAL RADIO ASTRONOMY OBSERVATORY

[X] ELECTRICAL [ ] MECHANICAL BOM # 41345026 REV _____ DATE _____ PAGE 3 OF 5

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
33		ALPHA	#22 AWG, WHT/BLK.	WIRE, HOOK-UP, P.V.C.	8 IN	
34		ALPHA	#18 AWG, BLK.	WIRE, HOOK-UP, P.V.C.	40 IN	
35						
36						
37						
38						
39						
40						
41						
42						
43						
44						
45						
46						
47						
48						
49						

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NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM # 41345076 REV _____ DATE _____ PAGE 4 OF 5

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
50		N.R.A.O.	C13450M19	LEFT SIDE PLATE	1	
51			B13450M17	FRONT PANEL	1	
52			B13050M3	BAR SUPPORT, TOP & BOT.	2	
53			C13050M7	TOP COVER	1	
54			B13050M17	FASTENER, PERF. COVER	2	
55			B13050M4	GUIDE, MODULE	2	
56		N.R.A.O.	B13250M15	SUPPORT, CONNECTOR	2	
57		SOUTHCO CORP.	47-11-204-10	SCREW, CAPTIVE	2	
58		H.H. SMITH	8781	SPACER, .81 LONG	4	
59			#4-40 x 1/4" LG.	ST. ST'L., FLT. HD. SLOT. MACH. SCR.	4	
60			#4-40 x 1/4" LG.	ST. ST'L., PAN HD., SLOT., MACH. SCR.	4	
61			#4-40 x 1/2" LG.		1	
62			#4-40 x 3/4" LG.	ST. ST'L., PAN HD., SLOT., MACH. SCR	1	
63			#4-40	ST. ST'L. HEX NUT	1	
64			#4 NOM	TEFLON FLAT WASHER	2	
65		N.R.A.O.	B13050M32	MODULE REAR PANEL	1	
66						

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM # A134-50E6 REV _____ DATE _____ PAGE 5 OF 5

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
67			#6-32 × 1/4" LG.	ST. ST'L., FL'T. HD., SLOT., MACH. SCR.	10	
68			#6-32 × 5/8" LG.	ST. ST'L., PAN HD., SLOT., MACH. SCR.	2	
69			#6-32 × 3/4" LG.	ST. ST'L., PAN HD., SLOT., MACH. SCR.	2	
70			#6-32 × 3/8" LG.	ST. ST'L., HEX SOC. HD. CAP SCR.	2	
71						
72						
73						
74						
75						
76						
77						
78						
79						
80						
81						
82						
83						

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

[X] ELECTRICAL [ ] MECHANICAL BOM # A1345077 REV _____ DATE _____ PAGE 1 OF 1

MODULE # T6 NAME I.F. CONTROL DWG # 13450P7 SUB ASMB TERMINAL BD. ASS'Y DWG # B13450P8

SCHEMATIC DWG # _____ LOCATION _____ QUA/SYSTEM _____ PREPARED BY JOE GRAY APPROVED [illegible]

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		N.R.A.O.	B13450P8	ASS'Y.	~	
2						
3		KEYSTONE	15289	MINIATURE TURRET TERM. BD.	1	
4		CORNING	NC4	RESISTOR, 4.99 K, ± 1%	2	
5		↓	↓	↓ , 15 K, ± 1%	2	
6		CORNING	NC4	RESISTOR, 10 K, ± 1%	4	
7						
8						
9						
10						
11						
12						
13						
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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HI-507A

Dual 8 Channel Analog Multiplexer with Overvoltage Protection

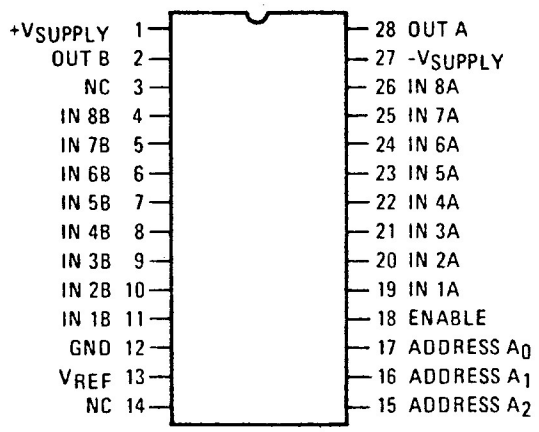
FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS
- BREAK BEFORE MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME 500ns TYP.
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE 4mA TYP.
- STANDBY POWER 7.5mW TYP.

DESCRIPTION

The HI-507A is a monolithic dual 8 channel analog multiplexer constructed with Harris Dielectric Isolation, complementary MOS process. Digital and Analog inputs are protected from overvoltage inputs that exceed either supply voltage with no channel interaction. Channel interaction is also eliminated in the event of power loss (open or shorted). One of 8 channel selection is controlled by a 3-bit binary word blus an Enable-Inhibit input which conveniently controls ON-OFF operation of several multiplexers in a system. The devices are packaged in a 28 pin dual in-line package and are available in both military and commercial temperature ranges.

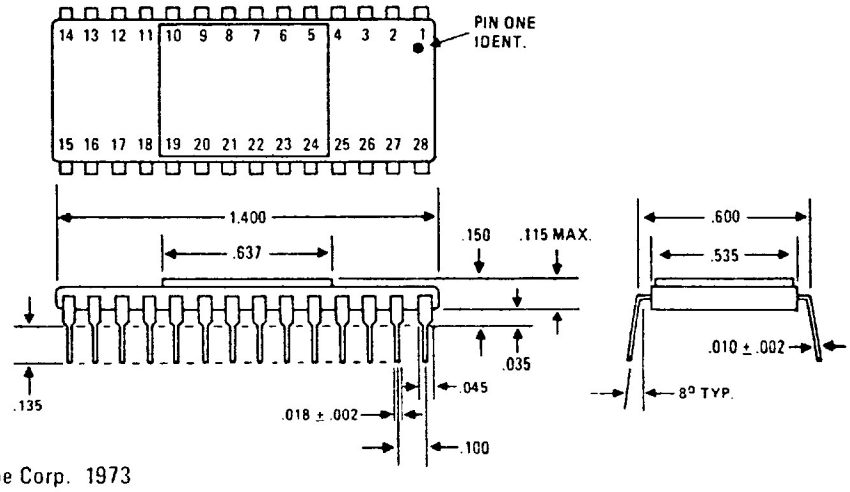
PIN OUT/TRUTH TABLE



A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

PACKAGE

28 LEAD D.I.P.



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 — 40V

V_{REF} to Ground — +20V

V_{EN}, V_A, Digital Input Overvoltage:

V_A { $V_{Supply}(+)$ +4V; $V_{Supply}(-)$ -4V }

Analog Input Overvoltage:

V_S { $V_{Supply}(+)$ +20V; $V_{Supply}(-)$ -20V }

Total Power Dissipation* — 1200mW

Operating Temperature:

HI-507A-2 — -55°C to +125°C

HI-507A-5 — 0°C to +75°C

Storage Temperature — -65°C to +150°C

*Derate 10mW/°C above 70°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified.

Supplies = +15V, -15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V

For Test Conditions, consult Performance Characterisitcs section.

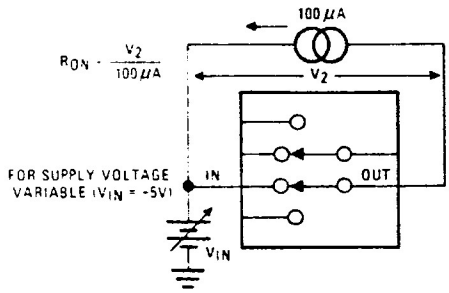
PARAMETER	TEMP.	-55°C to +125°C MIN.	TYP.	MAX.	0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	2.0		2.0	2.0	KΩ
$I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C		1.0			1.0		nA
	Full			±250			±250	nA
$I_{D(OFF)}$ with Input Overvoltage Applied (Note 2)	+25°C		4.0			4.0		nA
	Full			2.0			2.0	μA
$I_{D(ON)}$, On Channel Leakage Current	+25°C		0.1			0.1		nA
	Full			±500			±500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold (TTL Drive)	Full			0.8			0.8	V
V_{AH}, Input High Threshold (TTL Drive)	Full	4.0			4.0			V
V_{AL} (MOS Drive (Note 3))	+25°C			0.8			0.8	V
V_{AH} (MOS Drive (Note 3))	+25°C	6.0			6.0			V
I_A, Input Leakage Current (High or Low)	Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break - Before Make Delay	+25°C		80			80		ns
$t_{ON\ (EN)}$, Enable Delay (ON)	+25°C		300			300		ns
$t_{OFF\ (EN)}$, Enable Delay (OFF)	+25°C		300			300		ns
"Off Isolation" (Note 4)	+25°C		65			65		dB
$C_{S\ (OFF)}$, Channel Input Capacitance	+25°C		5			5		pF
$C_{D\ (OFF)}$, Channel Output Capacitance	+25°C		50			50		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS\ (OFF)}$, Input to Output Capacitance	+25°C		1			1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
I+, Current Pin 1 (Note 5)	Full		0.5	2.0		0.5	5.0	mA
I-, Current Pin 27 (Note 5)	Full		0.02	0.5		0.02	2.0	mA
I+, Standby (Note 6)	Full		0.5	2.0		0.5	5.0	mA
I-, Standby (Note 6)	Full		0.02	0.5		0.02	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -100μA
2. Analog Overvoltage = ±33V
3. V_{REF} = +10V
4. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500kHz
5. V_{EN} = +4.0V
6. V_{EN} = 0.8V

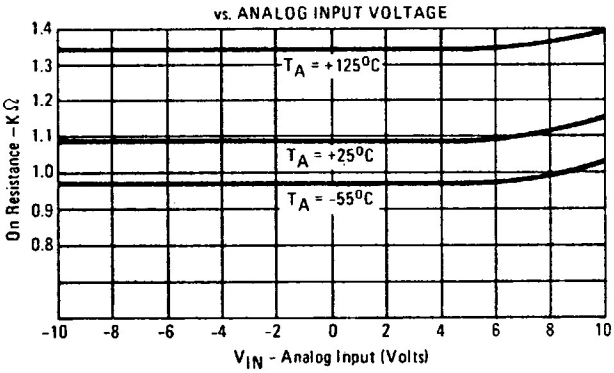
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$ AND V_{REF} = OPEN)

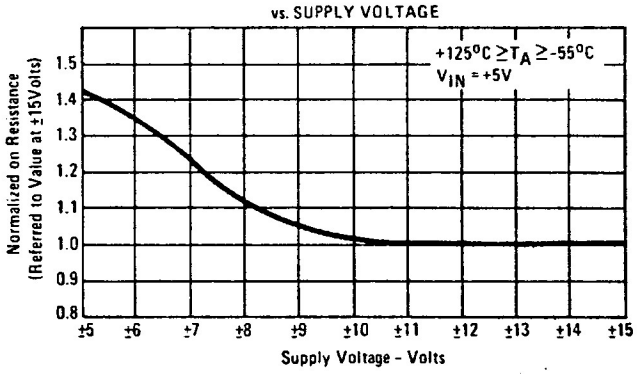
ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE



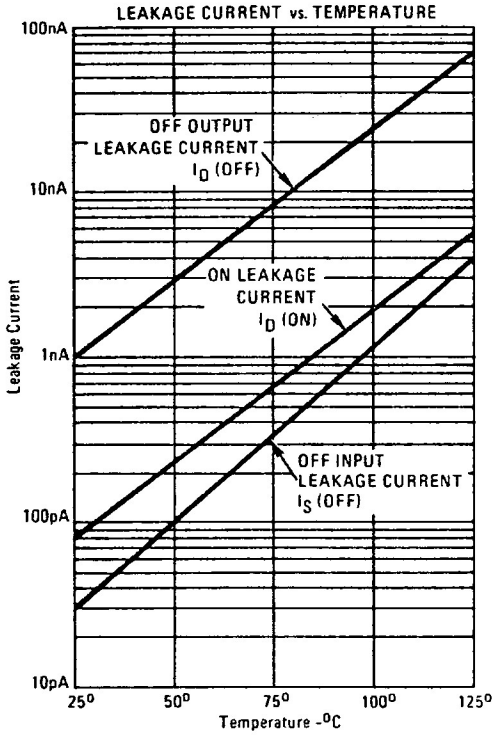
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



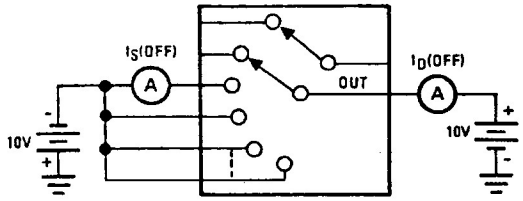
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



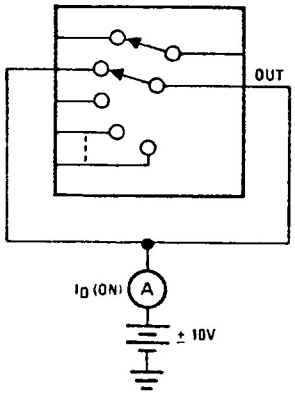
LEAKAGE CURRENT vs. TEMPERATURE



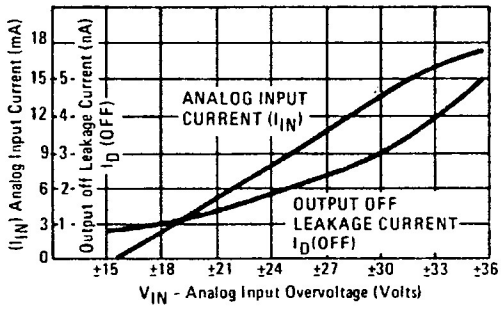
OFF LEAKAGE CURRENT vs. TEMPERATURE



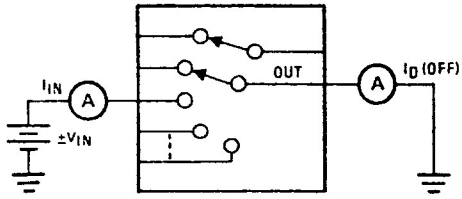
ON LEAKAGE CURRENT vs. TEMPERATURE



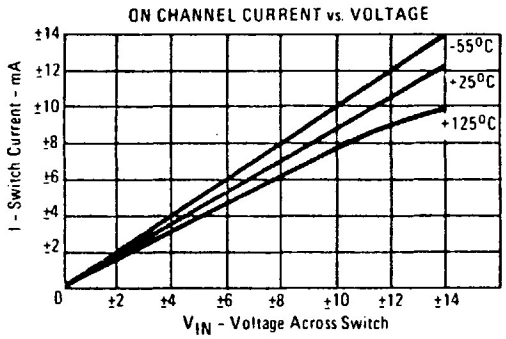
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

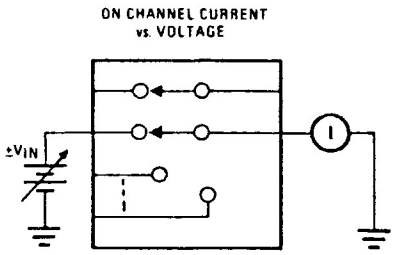


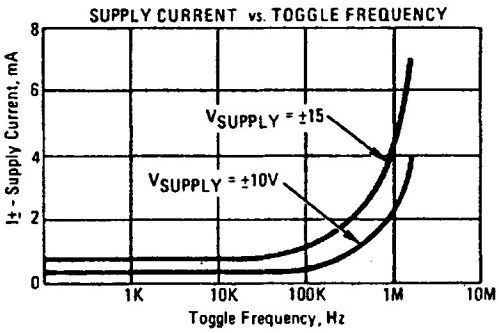
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

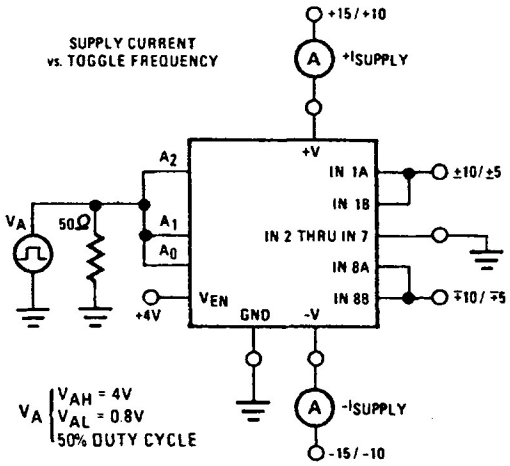


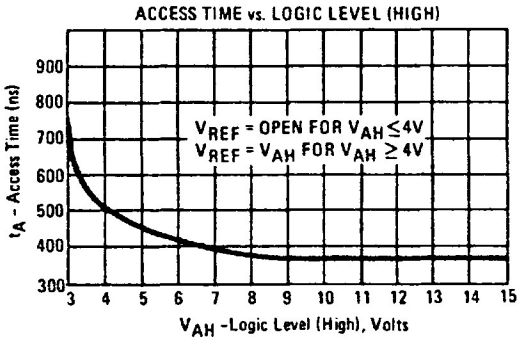
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

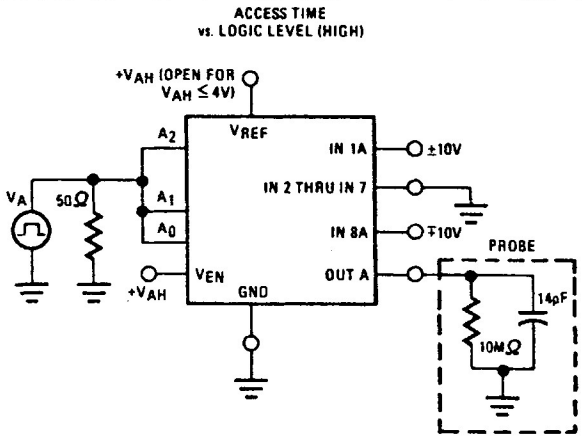




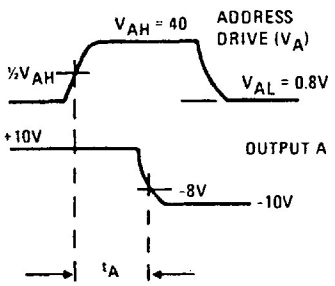


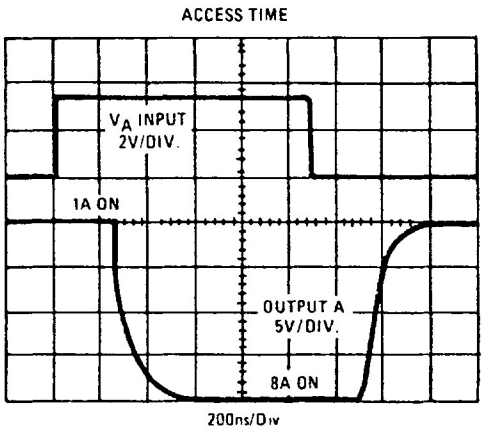




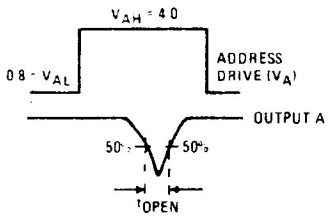


SWITCHING WAVEFORMS

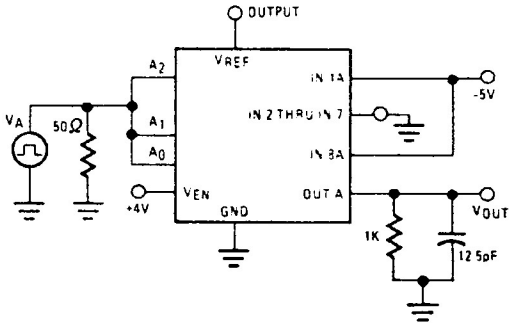




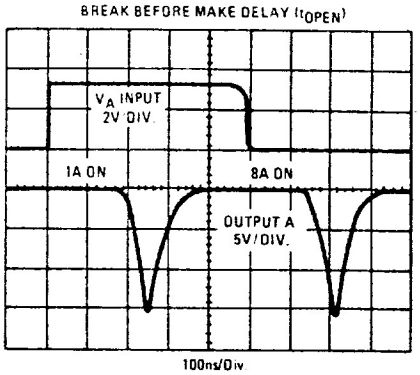
SWITCHING WAVEFORMS (continued)

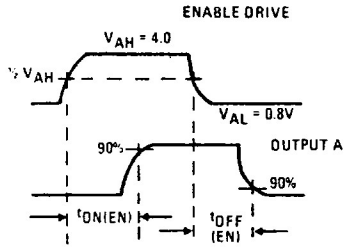


BREAK BEFORE MAKE DELAY (t_{OPEN})

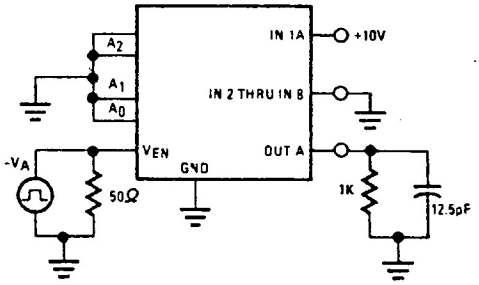


BREAK BEFORE MAKE DELAY (t_{OPEN})

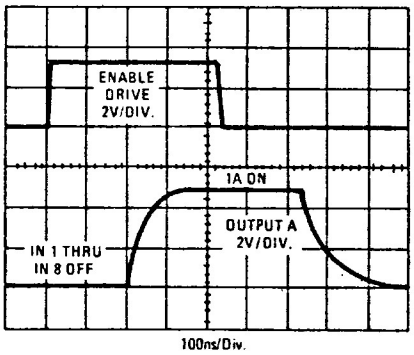




ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

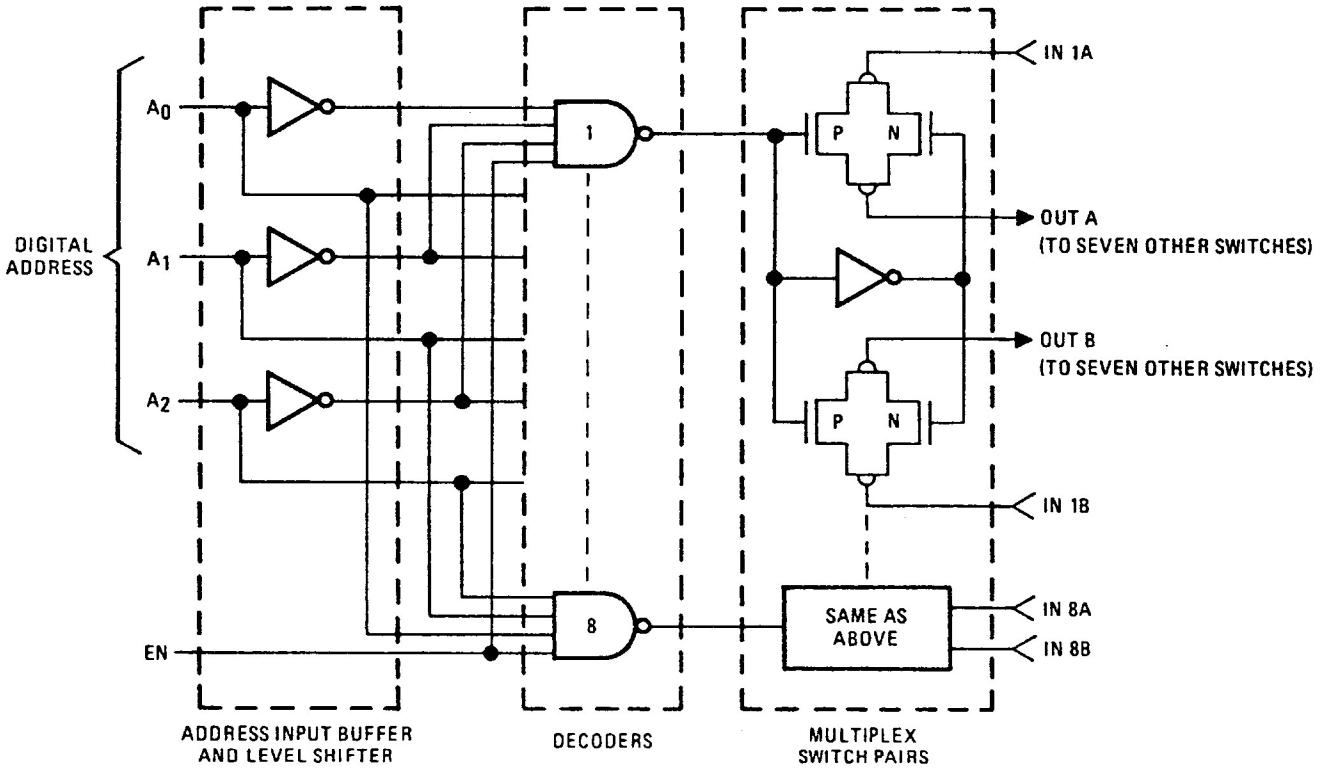


ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

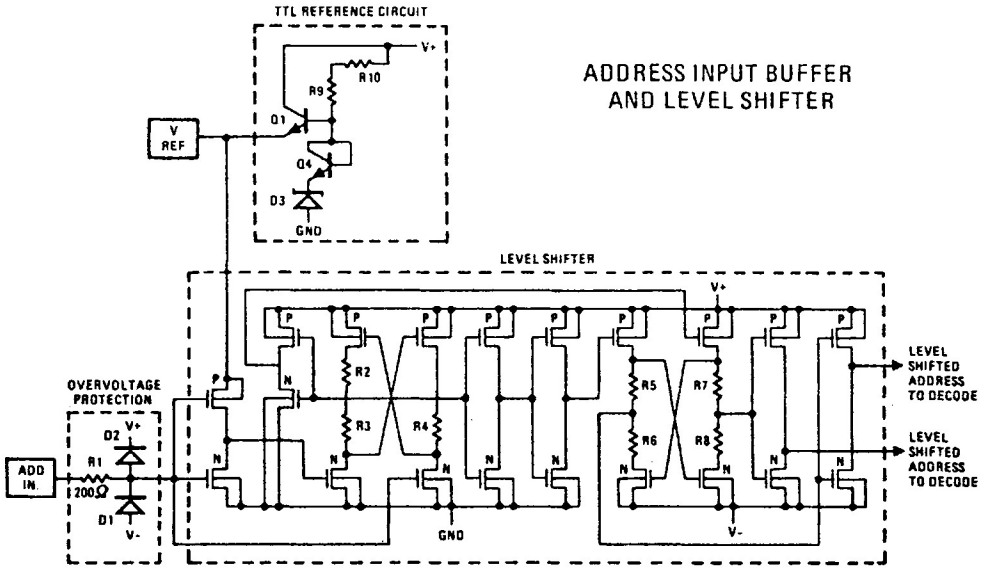


SCHEMATIC DIAGRAMS

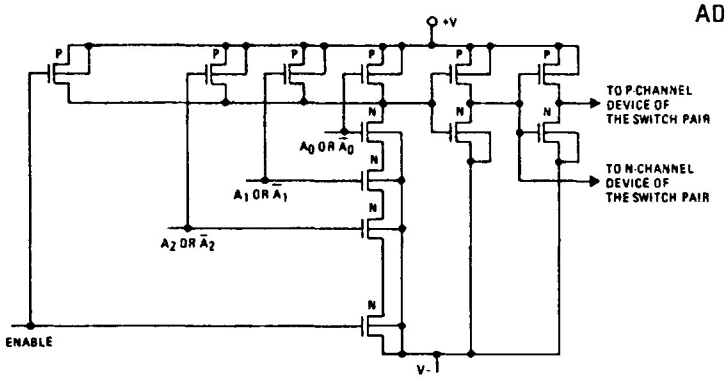
FUNCTIONAL BLOCK DIAGRAM HI-507A



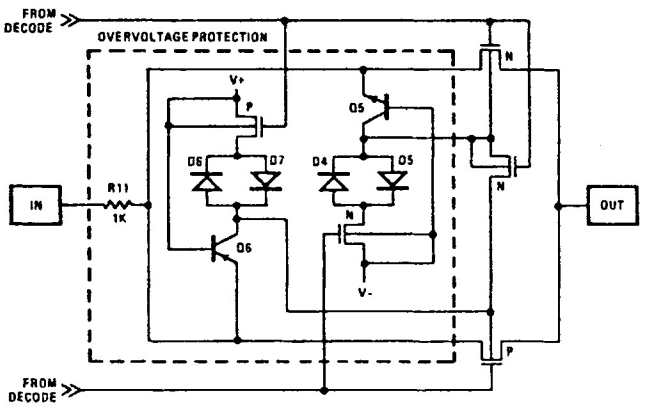
SCHEMATIC DIAGRAMS (continued)



ADDRESS INPUT BUFFER AND LEVEL SHIFTER



ADDRESS DECODER



MULTIPLEX SWITCH

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