VLA TECHNICAL REPORT #9

MODULE F1

BIAS CIRCUITS

S. Weinreb

March 1975

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   Raytheon - Monolithic Dual High-Gain Operational Amplifier

   Analog Devices - 8 and 16 Channel Analog Multiplexers

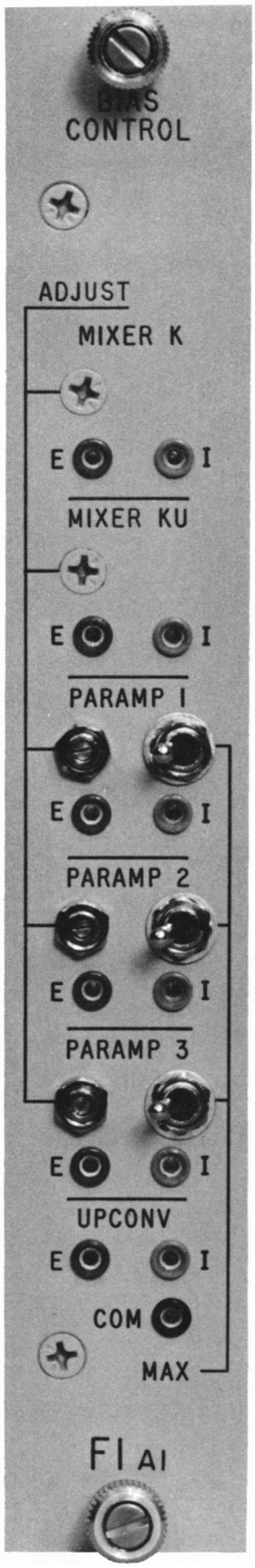


FIGURE 1 – Bias Module Front Panel

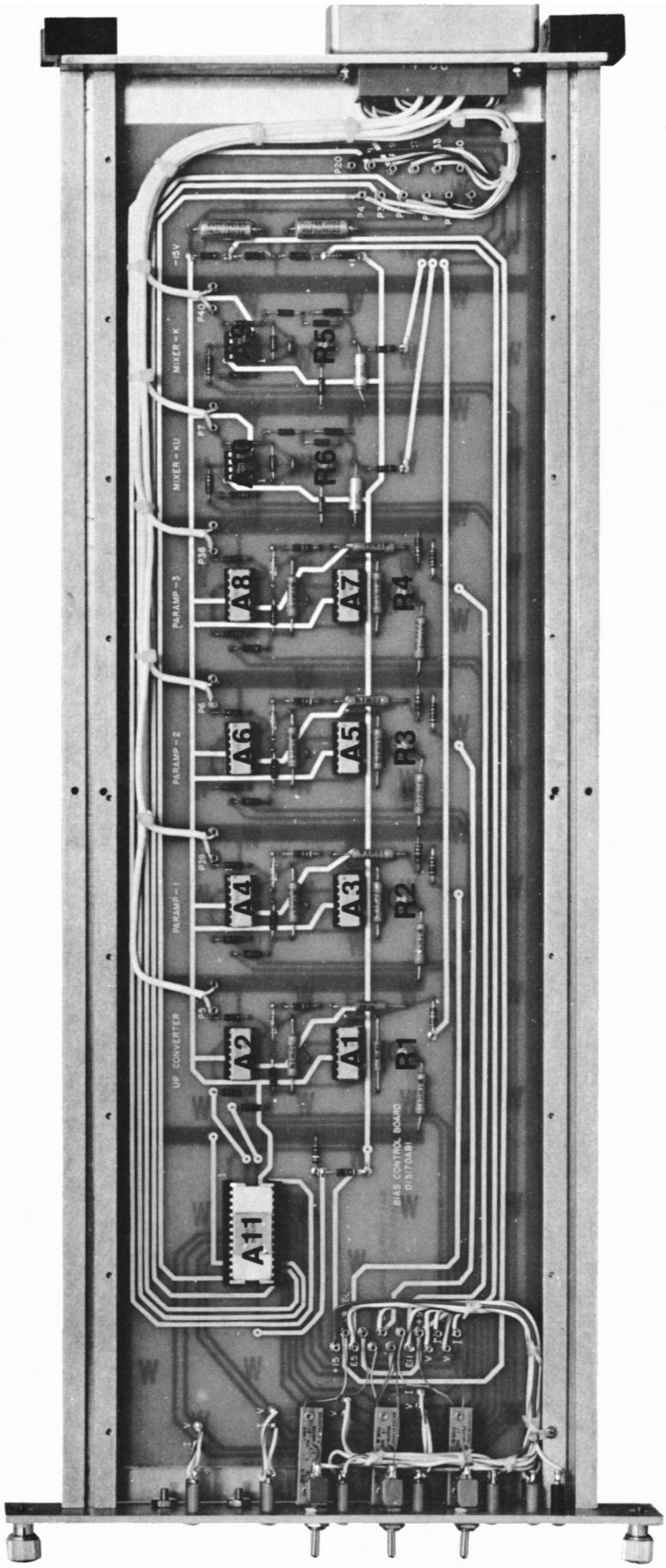


FIGURE 2 – Bias Module Side View, Cover Removed

1.0 BIAS MODULE DRAWING LIST

SCHEMATIC DIAGRAMS

Varactor Bias Circuit	B13170S1
Paramp #1 Bias Circuit	B13170S2
Paramp #2 Bias Circuit	B13170S3
Paramp #3 Bias Circuit	B13170S4
Ku Mixer Bias Circuit	B13170S5
K Mixer Bias Circuit	B13170S6
Multiplex and Power	B13170S7
Module Tester	B13170S8
Printed Circuit Layout	D13170AB1
Module Rails	D13170M65
Module Rear Panel	B13050M2
Module Side Covers	B13050M6 and B13050M7
Module Front Panel	C13170M64
Bill-of-Material	A13170Z41

2.0 FUNCTION

The Bias Module contains 6 circuits to bias diodes in the Up Converter, 3-paramp stages, 15 GHz mixer, and 23 GHz mixer. Two bias modules, for AB and CD channels, are needed for each front-end.

A functional diagram of each circuit is shown below:

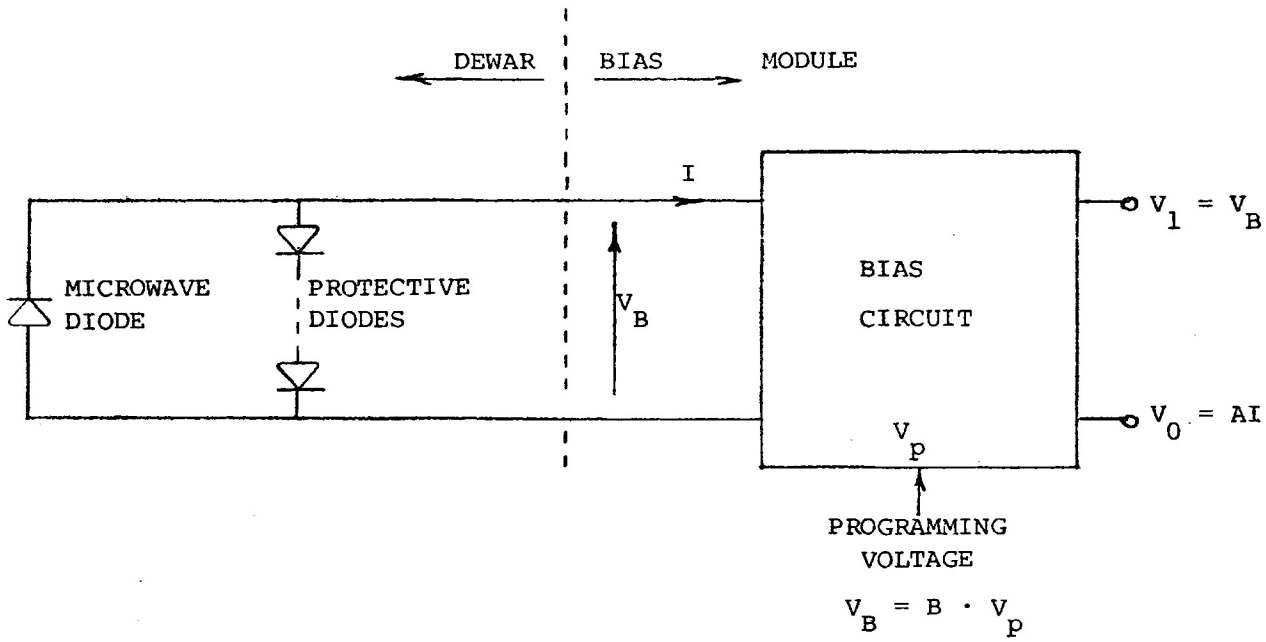


FIGURE 3

The circuit provides a DC bias, V_B, from a low impedance source. V_B can be programmed by application of a programming voltage, V_p; i.e. $V_B = B \cdot V_p$ where B is a proportionality constant given in the table below for each source. The circuit provides an isolated monitor voltage, $V_1 = V_B$, and a current monitor voltage, $V_o = A \cdot I$ where I is the diode current and A is given in the table below. The allowed range of V_B and source of programming voltage are also given in the table.

TABLE I

BIAS CIRCUIT PARAMETERS

CIRCUIT	A	B	V_B RANGE	SOURCE OF PROGRAMMING VOLT.
Up-Converter	10V/μA*	0.83	0 to +5V	Up-Converter Pump Module
Paramp 1, 2, 3	10V/μA*	0.10	-0.9 to +0.9V	Bias Module Front-Panel Pot
23 GHz Mixer 15 GHz Mixer	1V/mA	0.13	0 to -1.2V	23 GHz/15 GHz LO Module

*This value applies for $-1.3\mu A \leq I \leq +0.7\mu A$; for $I > 0.7\mu A$ (or $V_0 > 7$ volts) see Figure 1.

Note the following sign convention.

TABLE II

BIAS CIRCUIT POLARITIES

$V_B \equiv V_1$		I	V_0	INTERPRETATION
−	FORWARD BIAS VOLTAGE	+	−	Forward DC Current
−		−	+	Not Possible
+	REVERSE BIAS VOLTAGE	+	−	Rectified DC Current
+		−	+	Leaky Diode or Conducting Protective Diode

Pin connections for the 42-pin rear panel connector are given in Section 5, Table III.

Up-converter and paramp bias circuits current limit for I = -1.3μA or I = +400μA. Mixer bias circuits current limit at I = ±13mA.

A multiplexer is provided within each bias module to allow computer monitoring of bias voltage or current in each of the 6 circuits. The Data-Set module provides 4 address bits which are applied to the multiplexer to read out one of the 12 monitor points on a single output monitor line from each bias module. The monitor system addresses for this data are shown in Section 5, Table IV.

3.0 PRINCIPLE OF OPERATION

All six bias circuits are variations of the simplified circuit shown below:

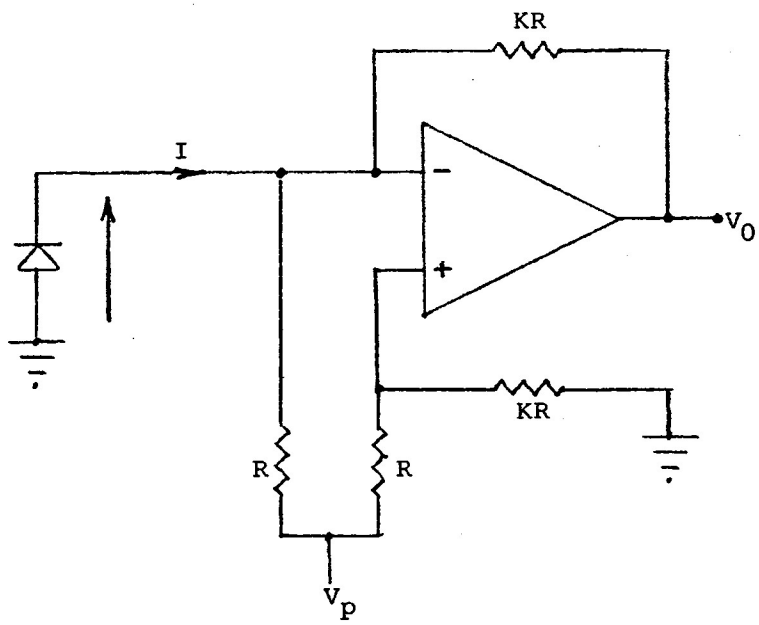


FIGURE 4 - Basic Bias-Circuit

We first assume I = 0 and recognize that a balanced differential amplifier exists with V_p as a common-mode input signal. The output, V_0, is thus zero independent of V_p. The bias voltage, V_B, is the voltage of the positive op-amp input terminal which is $V_p \times K/(K+1)$. When I becomes non-zero it is cancelled by an equal and opposite current flowing from the op-amp output. This current flows thru the feedback resistance, KR, and produces an output voltage $V_0 = KRI$. Thus the circuit functions as a bias voltage source with a monitor of the current drawn from the source.

Values of K >> 1 should be avoided because the op-amp offset and drift are multipled by K. Making K << 1 requires $V_p >> V_B$ and is unnecessary. (The effect of resistor unbalance is independent of K.) A value of K = 1 was chosen for all 6 circuits. The value of R is chosen at 10 megohms in up-converter and paramp bias circuits (to give 1 volt per 100 NA varactor current) and 1K ohm in mixer bias circuits (to give 1 volt per mA).

The circuit functions as an ideal voltage source only for values of I which do not saturate the op-amp output ($|V_0| \leq 13$ volts). After saturation the bias source has high impedance. This causes an instability in paramp operation due to a negative-resistance I-V characteristics exhibited by some pumped varactors. For this reason a low-leakage zener diode has been added in parallel with the feedback resistor in paramp and up-converter bias circuits. This allows bias currents of up to 400 μA to be supplied from a low impedance voltage source; without the zener diode the limit is 1.3 μA. The addition of the zener diode causes a non-linear relation, shown in Figure 5, between current, I, and current-monitor voltage, V_0, for values of $I \geq 0.7$ μA.

Other additions to the circuit are a unity-gain buffer to allow bias voltage to be monitored and a common-mode adjustment pot to remove resistor unbalance effects. The pot is adjusted so there is no change in output voltage, V_0, as V_B is varied with no load on the bias terminal. The op-amp offset voltages are small enough (≤ 6 mV) to be neglected and no offset adjustments are required.

4.0 ADJUSTMENT AND TEST

Most of the failures of the Bias-Circuits modules will be failures of LH0022 or RC4558 operational amplifiers or perhaps the AD7506 multiplexer; these are all plug-in components and no adjustments are required when a unit is replaced. The only adjustment in each circuit is a common-mode balance pot. This adjustment compensates for differences in the 1% resistors which make up the basic bias circuit (Figure 2). When properly adjusted the offset in the current-monitor voltage is independent of the bias voltage.

No operational-amplifier offset pots are included because the offsets should be small enough ($\leq$ 6 mV for LH0022; $\leq$ 7.5 mV for RC4558) to be tolerable. If necessary the LH0022 can be replaced with the LH0052 to give less than 1 mV offset. Another contributor to offset is circuit board leakage. If offset voltages cannot be adjusted within specified limits the problem may be due to circuit board leakage. A resistance of 15,000 megohms to $\pm$15 volts will produce 1 nA of current or 10 mV of monitor offset voltage. Thorough cleaning of the board and an insulating spray coating will alleviate this effect.

4.1 Test Set

A simple test-set provides DC power, programming voltages for up-converter and mixer circuits, multiplexer output bits, switched-output loads and monitor jacks. A schematic diagram is shown in Section 5.0.

4.2 Procedure

Test and adjustment can be systematically performed by following the form shown in Figure 6 (filled in) and Figure 7 (blank).

The column marked "LOAD" refers to the setting of the test-set load toggle-switch (center is open). The "POT" column refers to the test-set programming pot for up-converter and mixer bias; for paramp circuits it refers to the module front-panel pots. The word "BYPASS" in this column means the bias-module bypass switch is in the right-hand position; it is towards center for all other cases. The "MEAS" columns refer to the voltage measured with a 4-digit DVM at the module E and I monitor jacks.

Test procedure consists of recording the E and I voltage readings at listed settings of pots and load switches. The internal common-mode pots R1 thru R6 are adjusted to make the I voltage identical for the first and second programming pot settings.

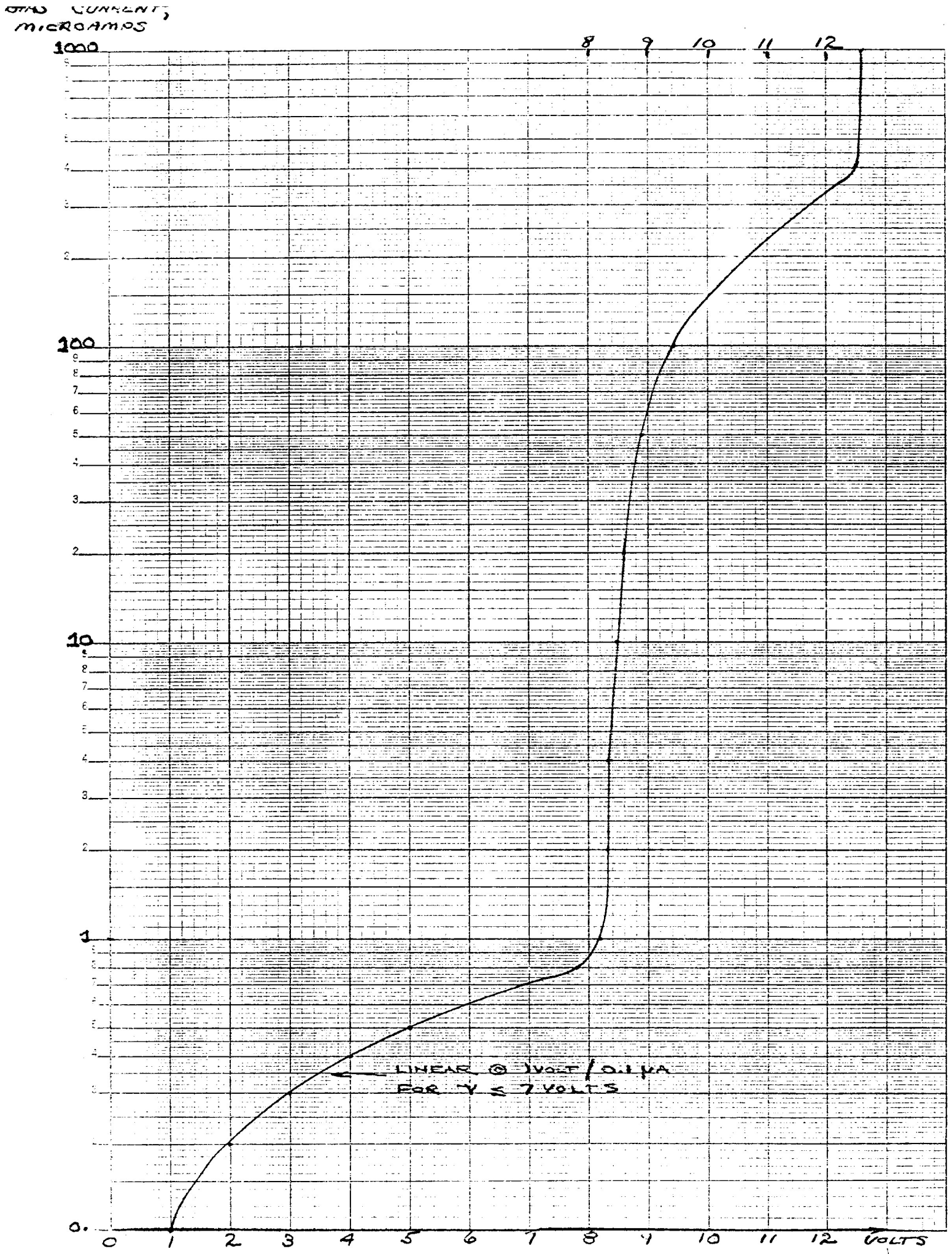


FIGURE 5 - Bias current as a function of current-monitor voltage, V_o

If an offset is out of limits change the appropriate op amp. If the 100μA load I reading is out of limits replace the 1N4101 zener diode for that circuit.

SERIAL NO.	2	BIAS MODULE TEST SET DATA, MODULE F1	DATE	3/25/75	BY	S.W.
COMMENTS						

CIRCUIT	LOAD	POT	E MONITOR MIN	E MONITOR MAX	E MONITOR MEAS	I MONITOR MIN	I MONITOR MAX	I MONITOR MEAS	COMMENT
K MIXER	OPEN	CCW	-.02	.02	+.003	-.02	.02	+.004 (1)	ADJUST R5 SO (2) = (1)
	OPEN	CW	-1.3	-1.1	-1.173	-.02	.02	+.004 (2)	
	10MA	CCW	.09	.11	+.104	-10.3	-9.7	-10.054	
Ku MIXER	OPEN	CCW	-.02	.02	+.001	-.02	.02	+.001 (1)	ADJUST R6 SO (2) = (1)
	OPEN	CW	-1.3	-1.1	-1.162	-.02	.02	+.001 (2)	
	10MA	CCW	.09	.11	+.101	-10.3	-9.7	-10.019	
PARAMP #1	OPEN	ZERO E	-.02	.02	+.001	-.02	.02	+.011 (1)	ADJUST R2 SO (2) = (1)
	OPEN	BYPASS	1.4	1.6	+1.443	-.02	.02	+.011 (2)	
	0.5μA	CCW	-.95	-.80	-.820	-5.6	-4.8	-5.387	
	100μA	CW	.80	.95	+.818	-10.5	-8	-9.240	
PARAMP #2	OPEN	ZERO E	-.02	.02	.000	-.02	.02	+.008 (1)	ADJUST R3 SO (2) = (1)
	OPEN	BYPASS	1.4	1.6	+1.475	-.02	.02	+.007 (2)	
	0.5μA	CCW	-.95	-.80	-.839	-5.6	-4.8	-5.405	
	100μA	CW	.80	.95	+.836	-10.5	-8	-9.078	
PARAMP #3	OPEN	ZERO E	-.02	.02	+.003	-.02	.02	-.001 (1)	ADJUST R4 SO (2) = (1)
	OPEN	BYPASS	1.4	1.6	+1.434	-.02	.02	.000 (2)	
	0.5μA	CCW	-.95	-.80	-.824	-5.6	-4.8	-5.395	
	100μA	CW	.80	.95	+.810	-10.5	-8	-9.057	
UP CONVERTER	OPEN	CCW	-.02	.02	+.007	-.02	.02	-.001 (1)	ADJUST R1 SO (2) = (1)
	OPEN	CW	4.5	5.5	+5.103	-.02	.02	+.002 (2)	
	0.5μA	CCW	-.02	.02	+.007	-5.6	-4.8	-5.092	
	100μA	CCW	-.02	.02	+.006	-10.5	-8	-10.023	

FIGURE 6

MODULE HISTORY

DATE	ACTION	BY
3/27/75	INSTALLED IN FRONT END #1	S.W.
3/30/75	470 PF CAPACITORS INSTALLED	S.W.
	TO STOP OSCILLATION	
4/14/75	SHIPPED TO SITE	S.W.

SERIAL NO.		BIAS MODULE TEST SET DATA, MODULE F1	DATE		BY	
COMMENTS						

CIRCUIT	LOAD	POT	E MONITOR MIN	E MONITOR MAX	E MONITOR MEAS	I MONITOR MIN	I MONITOR MAX	I MONITOR MEAS	COMMENT
K MIXER	OPEN	CCW	-.02	.02		-.02	.02	(1)	ADJUST R5 SO (2) = (1)
	OPEN	CW	-1.3	-1.1		-.02	.02	(2)	
	10MA	CCW	.09	.11		-10.3	-9.7		
Ku MIXER	OPEN	CCW	-.02	.02		-.02	.02	(1)	ADJUST R6 SO (2) = (1)
	OPEN	CW	-1.3	-1.1		-.02	.02	(2)	
	10MA	CCW	.09	.11		-10.3	-9.7		
PARAMP #1	OPEN	ZERO E	-.02	.02		-.02	.02	(1)	ADJUST R2 SO (2) = (1)
	OPEN	BYPASS	1.4	1.6		-.02	.02	(2)	
	0.5μA	CCW	-.95	-.80		-5.6	-4.8		
	100μA	CW	.80	.95		-10.5	-8		
PARAMP #2	OPEN	ZERO E	-.02	.02		-.02	.02	(1)	ADJUST R3 SO (2) = (1)
	OPEN	BYPASS	1.4	1.6		-.02	.02	(2)	
	0.5μA	CCW	-.95	-.80		-5.6	-4.8		
	100μA	CW	.80	.95		-10.5	-8		
PARAMP #3	OPEN	ZERO E	-.02	.02		-.02	.02	(1)	ADJUST R4 SO (2) = (1)
	OPEN	BYPASS	1.4	1.6		-.02	.02	(2)	
	0.5μA	CCW	-.95	-.80		-5.6	-4.8		
	100μA	CW	.80	.95		-10.5	-8		
UP CONVERTER	OPEN	CCW	-.02	.02		-.02	.02	(1)	ADJUST R1 SO (2) = (1)
	OPEN	CW	4.5	5.5		-.02	.02	(2)	
	0.5μA	CCW	-.02	.02		-5.6	-4.8		
	100μA	CCW	-.02	.02		-10.5	-8		

FIGURE 7

MODULE HISTORY

DATE	ACTION	BY

TABLE III - 42 PIN CONNECTOR WIRE LIST

RACK:	BIN: G	SLOT: 13	MODULE: BIAS - AB and CD	TYPE: F1
LIST BY:		WIRE BY:		
CONNECTOR TYPE:		CONNECTOR PAGE:		

PIN	FUNCTION	WIRE	FROM	TO
1	SMA Ø "1" ADDRESS	CONTROL MODULE		
2	SMA 1 "2" ADDRESS			
3	SMA 2 "4" ADDRESS			
4	SMA 3 "8" ADDRESS			
5C	UP CONV BIAS	DEWAR		
6C	PARAMP #2 BIAS			
7C	15 GHZ BIAS KU			
8				
9				
10	+5	POWER BUS		
11				
12				
13				
14				
15				
16	+15	POWER BUS		
17	-15			
18				
19	MONITOR OUT	CONTROL MODULE		
20	MONITOR GND			
21				
22				
23				
24				
25				
26	UP CONV BIAS PROG. GND			
27	UP CONV BIAS PROG.	UP CONVERTER PUMP	MODULE	
28				
29	GND			
30	23 GHZ MIXER BIAS PROG.	LO MODULE		

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE:
TITLE:		REV:
	DWG. NO.	SHEET OF

TABLE III - CONTINUED

WIRE LIST

RACK:	BIN: G	SLOT: 13	MODULE: BIAS - AB and CD	TYPE: F1
LIST BY:		WIRE BY:		
CONNECTOR TYPE:		CONNECTOR PAGE:		

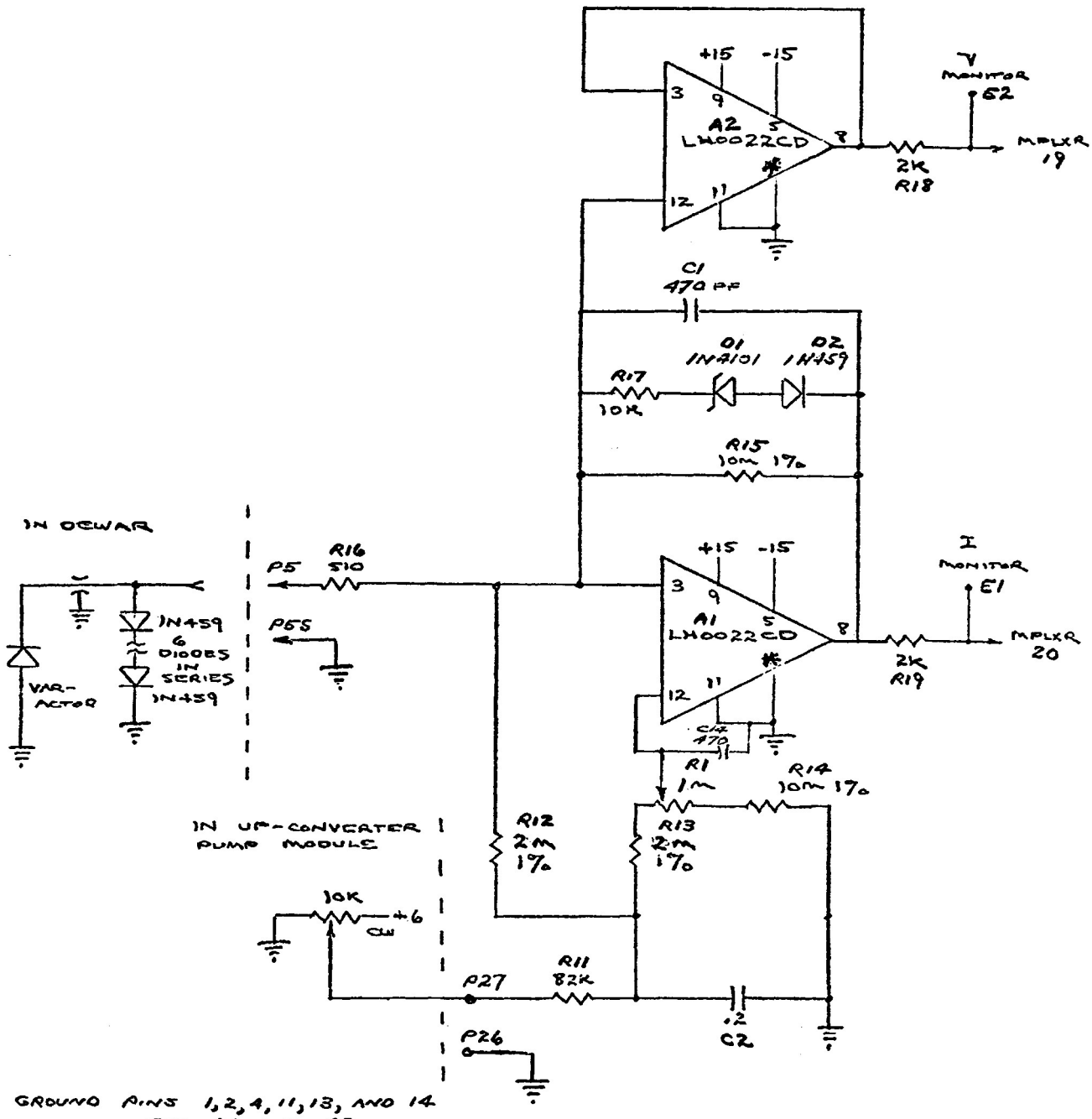
PIN	FUNCTION	WIRE	FROM	TO
31				
32	GND			
33	15 GHZ MIXER BIAS PROG.	LO MODULE		
34	GND			
35				
36				
37				
38C	PARAMP #3 BIAS			
39C	PARAMP #1 BIAS	DEWAR		
40C	23 GHZ MIXER BIAS K			
41				
42				
J1				
J2				
J3				
J4				
	NOTE: *MARK WITH WIRE MARKER			

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE:
TITLE:		REV:
	DWG. NO.	SHEET OF

TABLE IV - MONITOR WORDS ADDRESS

DATA SET ADDRESS: 1	LOCATION: Front-End
DATE: 9/26/74	PREPARED BY: SW

ADDRESS	DESCRIPTION
INPUT LINE NUMBER 6 - AB BIAS MODULE	
140	UP CONV BIAS VOLTAGE
141	UP CONV BIAS CURRENT
142	PARAMP 3 BIAS VOLTAGE
143	PARAMP 3 BIAS CURRENT
144	PARAMP 2 BIAS VOLTAGE
145	PARAMP 2 BIAS CURRENT
146	PARAMP 1 BIAS VOLTAGE
147	PARAMP 1 BIAS CURRENT
150	15 GHZ LO MIXER VOLTAGE
151	15 GHZ LO MIXER CURRENT
152	23 GHZ LO MIXER VOLTAGE
153	23 GHZ LO MIXER CURRENT
154	
155	
156	
157	
INPUT LINE NUMBER 7 - CD BIAS MODULE	
160	UP CONV BIAS VOLTAGE
161	UP CONV BIAS CURRENT
162	PARAMP 3 BIAS VOLTAGE
163	PARAMP 3 BIAS CURRENT
164	PARAMP 2 BIAS VOLTAGE
165	PARAMP 2 BIAS CURRENT
166	PARAMP 1 BIAS VOLTAGE
167	PARAMP 1 BIAS CURRENT
170	15 GHZ LO MIXER VOLTAGE
171	15 GHZ LO MIXER CURRENT
172	23 GHZ LO MIXER VOLTAGE
173	23 GHZ LO MIXER CURRENT
174	
175	
176	
177	



* GROUND PINS 1, 2, 4, 11, 13, AND 14 ON A1 AND A2

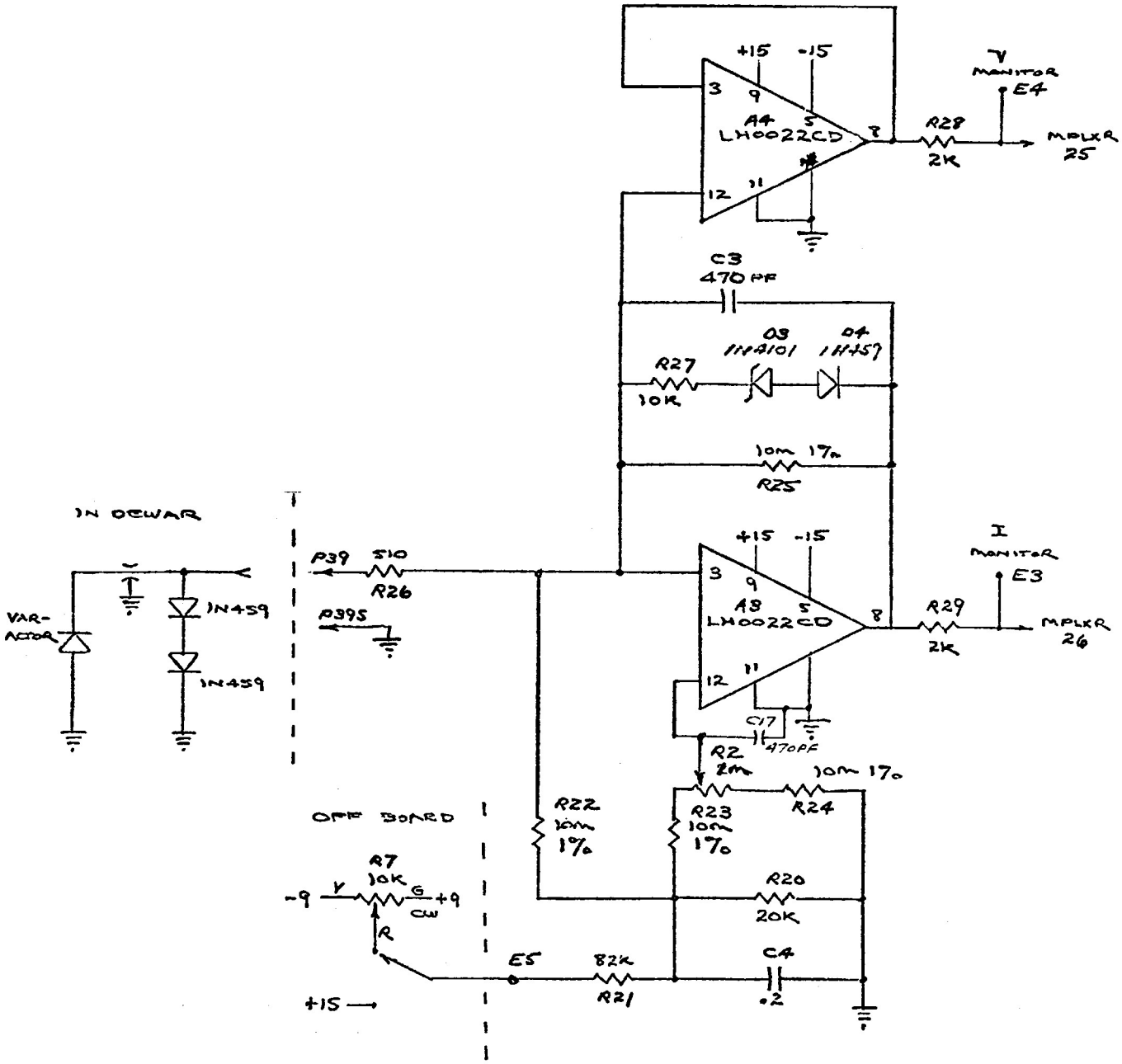
NOTES:

1) PJK REFERS TO PIN JK ON 42 PIN REAR PANEL CONNECTOR AND TERMINAL ON CIRCUIT BOARD

2) EJK REFERS TO TERMINAL ON CIRCUIT BOARD

3) ALL RESISTORS 5% 1/4W UNLESS NOTED

VARACTOR BIAS CIRCUIT
UPCONVERTER
B13170S1
S. Weinreb
Jan. 22, 1975



NOTES

*GROUND PINS 1, 2, 4, 11, 13, AND 14 ON A3 AND A4.

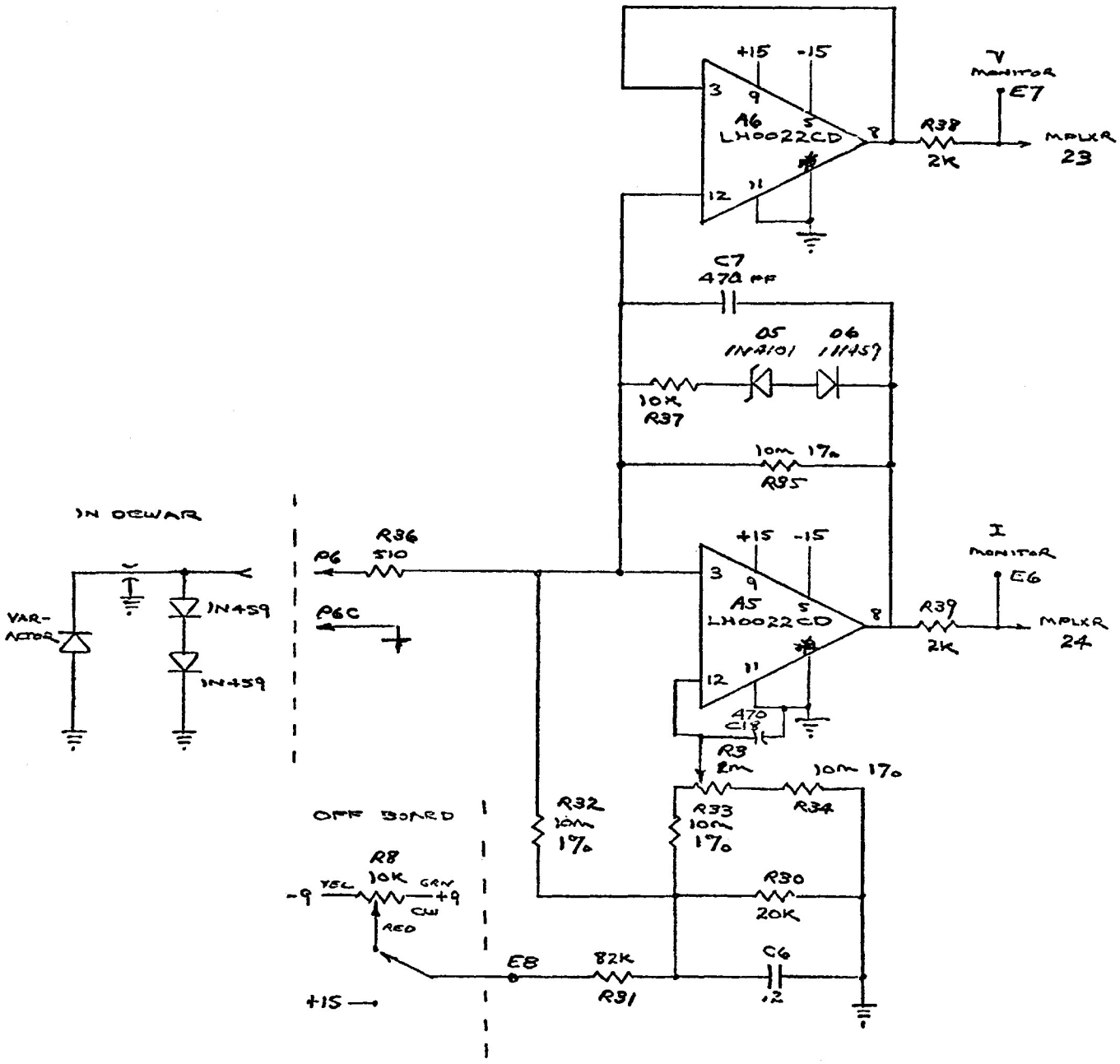
1. PJK REFERS TO PIN JK ON 42 PIN REAR PANEL CONNECTOR
2. EJK REFERS TO TERMINAL ON CIRCUIT BOARD
3. ALL RESISTORS 5% 1/4W UNLESS NOTED

PARAMP 1 BIAS CIRCUIT

B13170S2

S. Weinreb

Jan. 22, 1975



NOTES

*GROUND PINS 1, 2, 4, 11, 13, AND 14 ON A5 AND A6

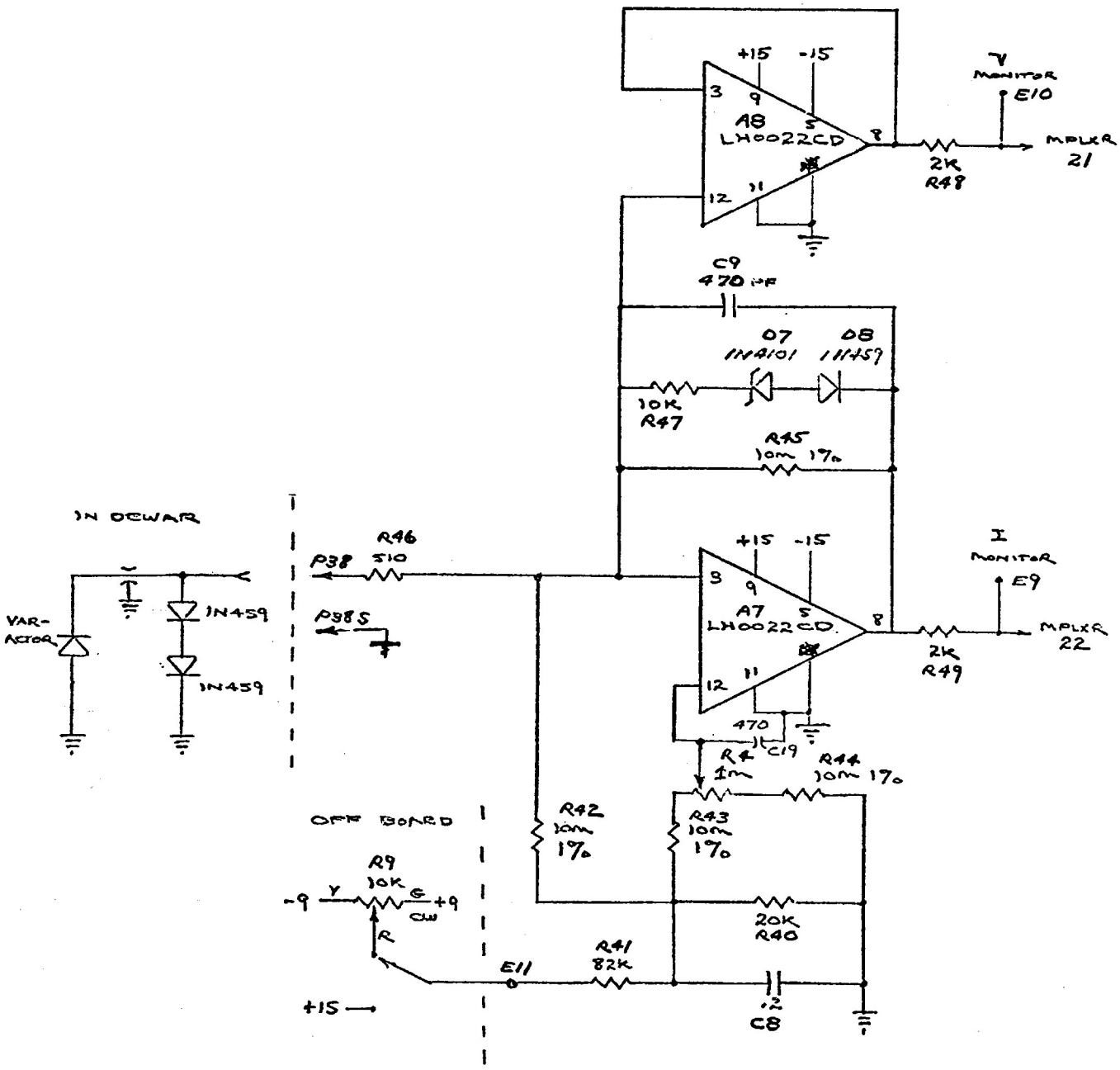
1. PJK REFERS TO PIN JK ON 42 PIN REAR PANEL CONNECTOR
2. EJK REFERS TO TERMINAL ON CIRCUIT BOARD
3. ALL RESISTORS 5% 1/4W UNLESS NOTED

PARAMP 2 BIAS CIRCUIT

B13170S3

S. Weinreb

Jan. 22, 1975



NOTES

*GROUND PINS 1, 2, 4, 11, 13, AND 14 ON A7 AND A8

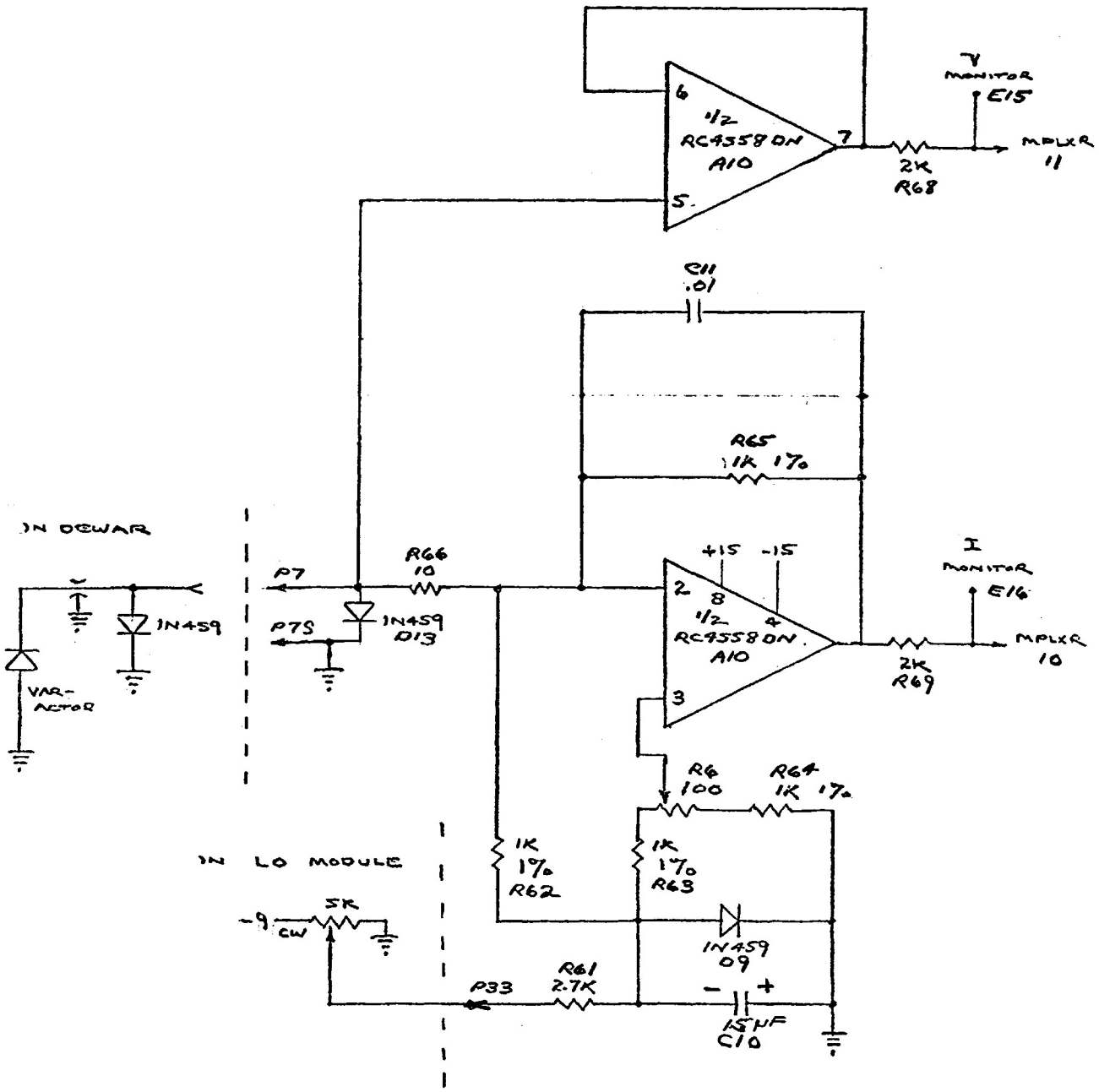
1. PJK REFERS TO PIN JK ON 42 PIN REAR PANEL CONNECTOR
2. EJK REFERS TO TERMINAL ON CIRCUIT BOARD
3. ALL RESISTORS 5% 1/4W UNLESS NOTED

PARAMP 3 BIAS CIRCUIT

B13170S4

S. Weinreb

Jan. 22, 1975

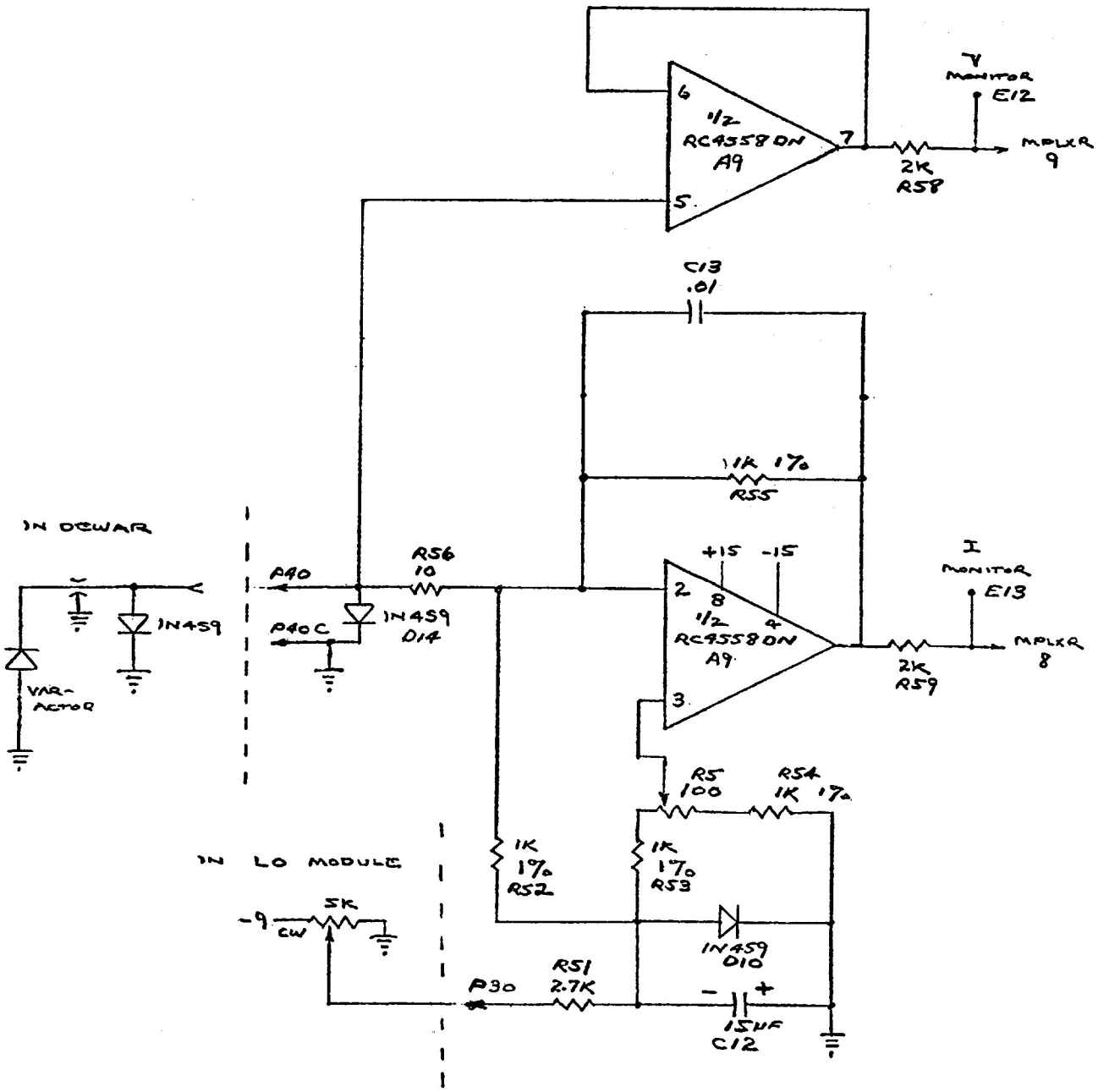


KU MIXER BIAS CIRCUIT

B13170S5

S. Weinreb

Jan. 22, 1975

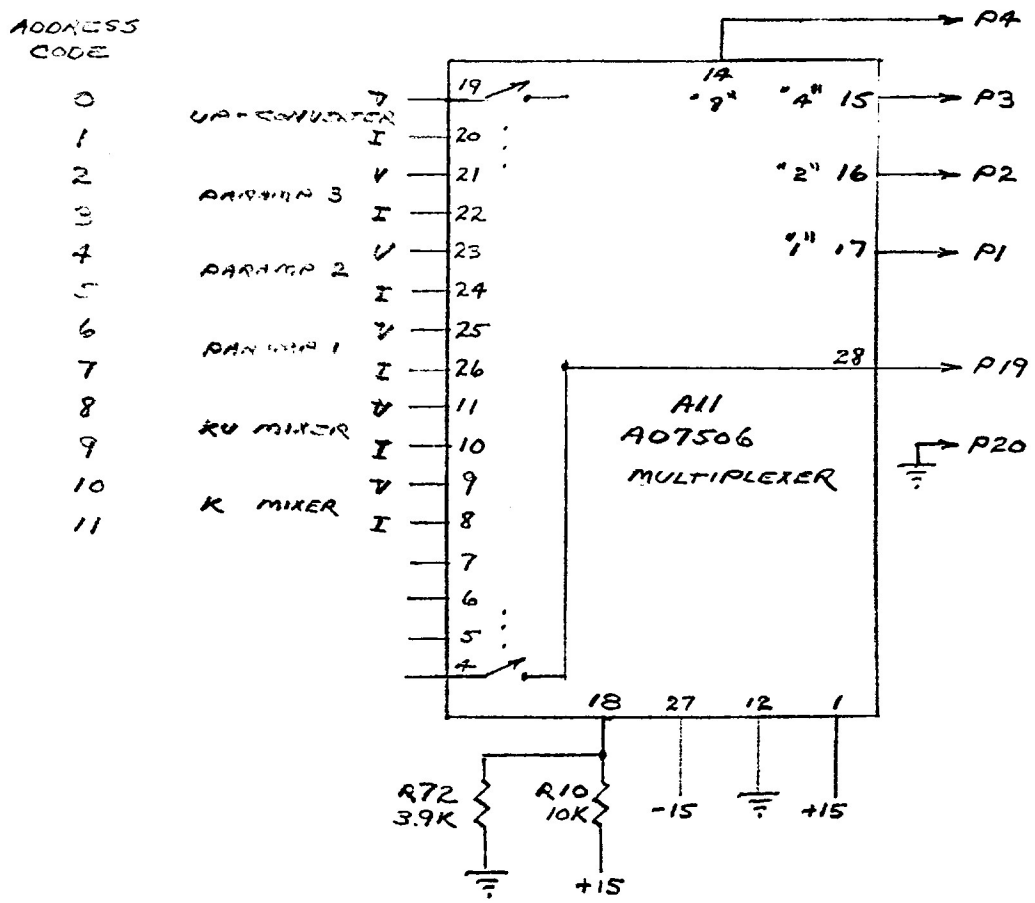


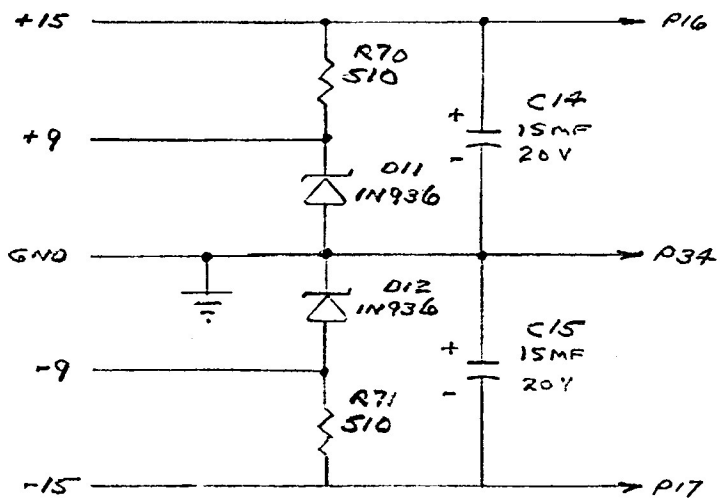
K MIXER BIAS CIRCUIT

B13170S6

S. Weinreb

Jan. 22, 1975



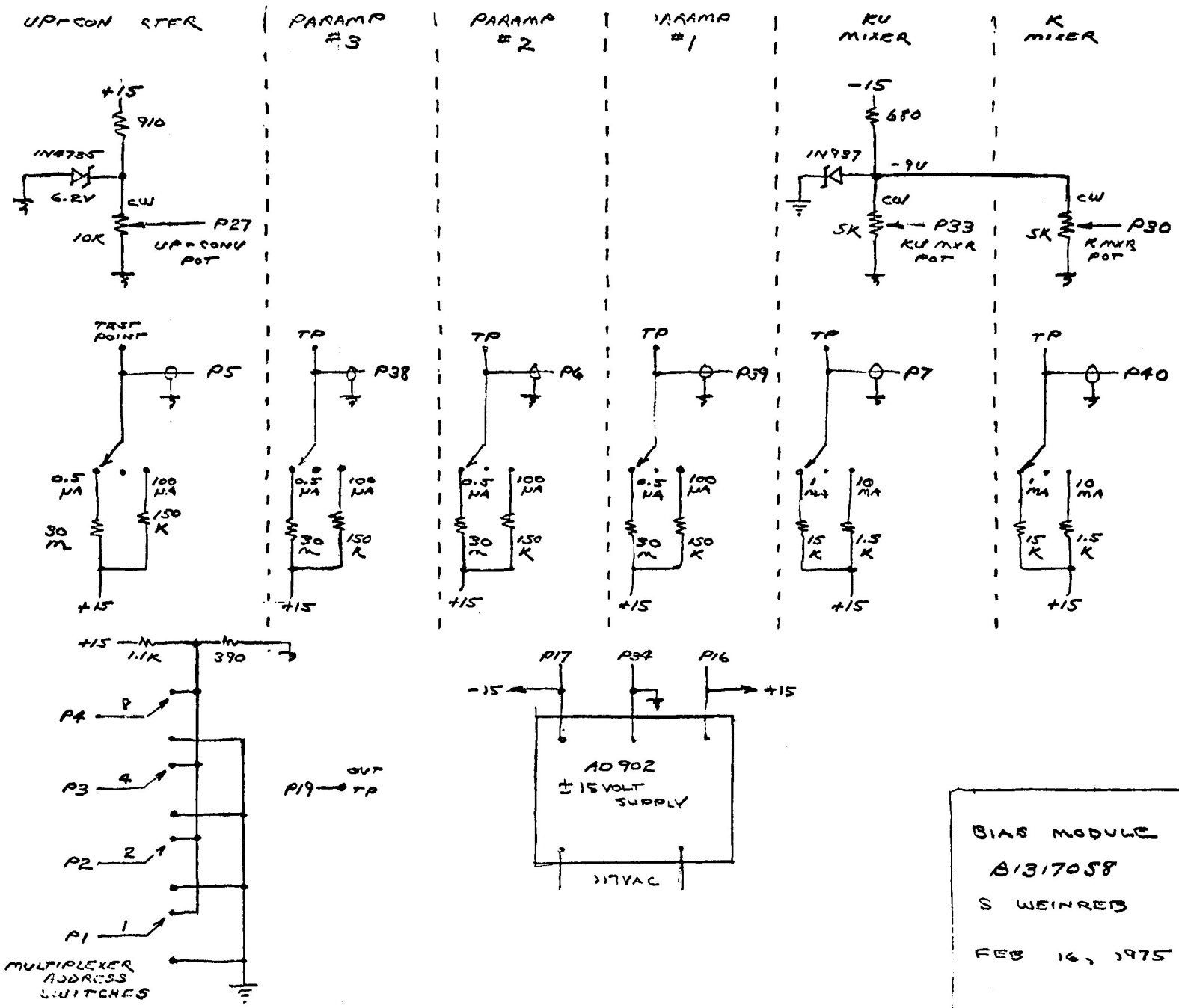


BIAS CKTS, MULTIPLEX AND POWER

B1317057

S. WEINREB

FEB 7, 1975



BIAS MODULE TESTER

B1317058

S WEINREB

FEB 16, 1975

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

[XX] ELECTRICAL [ ] MECHANICAL BOM # A13170Z41 REV _____ DATE _____ PAGE 1 OF 3

MODULE # F1 NAME Bias DWG # _____ SUB ASMB _____ DWG # _____

SCHEMATIC DWG # _____ LOCATION Front-End QUA/SYSTEM 2 PREPARED BY S.W. APPROVED _____

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	PO
1	A1,A2,A3,A4 A5,A6,A7,A8	National	LH0022CD	IC FET OP AMP	8	52713
2	A9,A10	Raytheon	RC4558DN	IC Dual OP AMP	2	52635
3	A11	Analog Devices*	AD7506KN	IC Multiplexer	1	52734
4	D1, D3 D5, D7	Motorola	1N4101	8.2V Zener Diode	4	52635
5	D2,D4,D6,D13 D8,D9,D10, D14	Any	1N459	Diode	6	52635
6	D11,D12	Any	1N936	Diode	2	52635
HARDWARE						
7	---	Robinson-Nugent	ICN-083-S3	8-Pin DIL Socket	2	52771
8	---	Robinson-Nugent	ICN-143-S3	14-Pin DIL Socket	8	52771
9	---	Robinson-Nugent	ICN-286-S1	28-Pin Socket	1	52771
10		E. F. Johnson	105-1050-001	Blue Socket	6	52401
11		E. F. Johnson	105-1044-001	Green Socket	6	52401
12		E. F. Johnson	105-1043-001	Black Socket	1	52401
13		JBT	JMT-123	SPDT Switch	3	
14		Keystone	1562-2	Terminal	50	

*Siliconix DG506BR may be substituted

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

[XX] ELECTRICAL [ ] MECHANICAL BOM # A13170Z41 REV _____ DATE _____ PAGE 2 OF 3

RESISTORS

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	PO
1	R1,R2 R3,R4	Bourns	3339P	1 MEG Pot	4	52766
2	R5,R6	Bourns	3339P	100 ohm Pot	2	
3	R7,R8 R9	Bourns	3012L-1-103M	10K Panel-Mount Pot	3	
4	R10,R17,R27 R37,R47	Allen-Bradley	CB	10K, 1/4W, 5%	5	52635
5	R11,R21 R31,R41	Allen-Bradley	CB	82K, 1/4W, 5%	4	
6	R20,R30 R40	Allen-Bradley	CB	20K, 1/4W, 5%	3	
7	R18,R19,R28,R38,R39 R48,R49,R58,R59,R68,R69	Allen-Bradley	CB	2K, 1/4W, 5%	12	
8	R16,R26,R70 R36,R46,R71	Allen-Bradley	CB	510 ohm, 1/4W, 5%	6	
9	R56,R66	Allen-Bradley	CB	10 ohm, 1/4W, 5%	2	
10	*	Any	RN20X	10 Meg, 1%	14	52721
11	R52,R53,R54,R55 R62,R63,R64,R65	Any	Rn55D	1K, 1%	8	52721
12	R72	Allen-Bradley	CB	3.9K, 1/4W, 5%	1	Stock
13	R12,13	ANY		2 MEG, 1%		

*R14, R15, R22, R23, R24, R25, R32, R33, R34, R35, R42, R43, R44, R45

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

[XX] ELECTRICAL [ ] MECHANICAL BOM # A13170Z41 REV _____ DATE _____ PAGE 3 OF 3

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1	C1,C3,C14,C17, C7,C9,C18,C19	Erie	8101-100-651-471M	470PF/100V Ceramic Cap	4	52912
2	C2,C4 C6,C8	Erie	8131-050-651-224M	.22MF/50V Ceramic Cap	4	
3	C11, C13	Erie	8121-050-651-103M	.01MF/200V Ceramic Cap	2	
4	C15,C16 C10,C12	Any	MIL CS13B	15MF/20V Tantalum	4	

Operational Amplifiers

		25-99	100-
LH0022/LH0022C* high performance FET op amp	D	9.90	8.30
LH0042/LH0042C low cost FET op amp	D	5.25	4.45
LH0052/LH0052C precision FET op amp	D	22.50	18.80

general description

The LH0022/LH0042/LH0052 are a family of FET input operational amplifiers with very closely matched input characteristics, very high input impedance, and ultra-low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. The internally laser nulled LH0052 offers 200 microvolts maximum offset and 5 μV/°C offset drift. Input offset current is less than 100 femtoamps at room temperature and 100 pA maximum at 125°C. The LH0022 and LH0042 are not internally nulled but offer comparable matching characteristics. All devices in the family are internally compensated and are free of latch-up and unusual oscillation problems. The devices may be offset nulled with a single 10k trimpot with neglible effect in offset drift or CMRR.

The LH0022, LH0042 and LH0052 are specified for operation over the −55°C to +125°C military temperature range. The LH0022C, LH0042C and LH0052C are specified for operation over the −25°C to +85°C temperature range.

features

- Low input offset current – 100 femtoamps max. (LH0052)
- Low input offset drift – 5 μV/°C max (LH0052)
- Low input offset voltage – 100 microvolts-typ.
- High open loop gain – 100 dB typ.
- Excellent slew rate – 3.0 V/μs typ.
- Internal 6 dB/octave frequency compensation
- Pin compatible with standard IC op amps (TO-5 package)

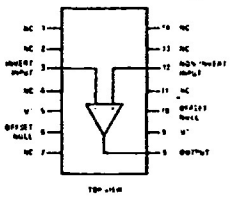
The LH0022/LH0042/LH0052 family of IC op amps are intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents and tightly matched input offsets. The LH0052 is particularly suited for long term high accuracy integrators and high accuracy sample and hold buffer amplifiers. The LH0022 and LH0042 provide low cost high performance for such applications as electrometer and photocell amplification, pico-ammeters, and high input impedance buffers.

Special electrical parameter selection and custom built circuits are available on special request.

For additional application information and information on other National operational amplifiers, see *Available Linear Applications Literature.*

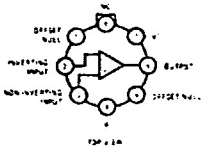
schematic and connection diagrams

Dual-In-Line Package



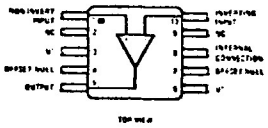
Order Number LH0022D or LH0022CD or LH0042D or LH0042CD or LH0052D or LH0052CD
See Package 1

Metal Can Package

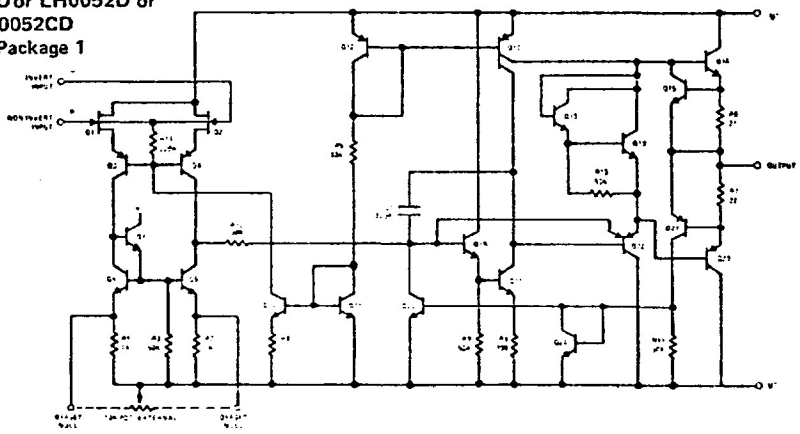


Order Number LH0022H or LH0022CH or LH0042H or LH0042CH or LH0052H or LH0052CH
See Package 11

Flat-Package



Order Number LH0022F or LH0022CF or LH0042F or LH0042CF
See Package 3



*Previously Called NH0022/NH0022C

absolute maximum ratings

Supply Voltage	±22V
Power Dissipation (see graph)	500 mW
Input Voltage (Note 1)	±15V
Differential Input Voltage (Note 2)	±30V
Voltage Between Offset Null and V^-	±0.5V
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0022, LH0042, LH0052	−55°C to +125°C
LH0022C, LH0042C, LH0052C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

dc electrical characteristics For LH0022/LH0022C (Note 3)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0022			LH0022C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\ k\Omega$; $T_A = 25°C$		2.0	4.0		3.5	6.0	mV
	$R_S \leq 100\ k\Omega$			5.0			10.0	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		5	10		5	15	μV/°C
Offset Voltage Drift with Time			3			4		μV/week
Input Offset Current	$T_A = 25°C$		0.2	2.0		1.0	5.0	pA
				200			200	pA
Temperature Coefficient of Input Offset Current		Doubles every 20°C			Doubles every 20°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	$T_A = 25°C$		5	10		10	25	pA
				1.0			1.0	nA
Temperature Coefficient of Input Bias Current		Doubles every 20°C			Doubles every 20°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	$V_S = \pm15V$	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm10V$	80	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm5V \leq V_S \leq \pm15V$	80	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2\ k\Omega$, $V_{OUT} = \pm10V$, $T_A = 25°C$, $V_S = \pm15V$	100	200		75	160		V/mV
	$R_L = 2\ k\Omega$, $V_{OUT} = \pm10V$, $V_S = \pm15V$	50			50			V/mV
Output Voltage Swing	$R_L = 1\ k\Omega$, $T_A = 25°C$, $V_S = \pm15V$	±10	±12.5		±10	±12		V
	$R_L = 2\ k\Omega$, $V_S = \pm15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm10V$, $T_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	$V_S = \pm15V$		2.0	2.5		2.4	2.8	mA
Power Consumption	$V_S = \pm15V$			75			85	mW

ac electrical characteristics For all amplifiers (T_A = 25°C, V_S = ±15V)

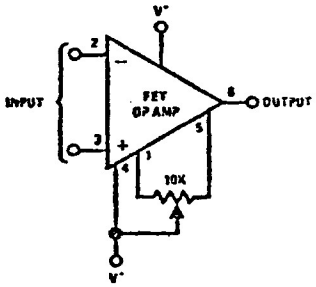
PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0022/42/52			LH0022C/42C/52C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	Voltage Follower	1.5	3.0		1.0	3.0		V/µs
Large Signal Bandwidth	Voltage Follower		40			40		kHz
Small Signal Bandwidth			1.0			1.0		MHz
Rise Time			0.3	1.5		0.3	1.5	µs
Overshoot			10	30		15	40	%
Settling Time (0.1 %)	ΔV_{IN} = 10V		4.5			4.5		µs
Overload Recovery			4.0			4.0		µs
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 Hz		150			150		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 100 Hz		55			55		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 1 kHz		35			35		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 kHz		30			30		nV/√Hz
Input Noise Voltage	BW = 10 Hz to 10 kHz, R_S = 10 kΩ		12			12		µVrms
Input Noise Current	BW = 10 Hz to 10 kHz		<.1			<.1		pArms

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

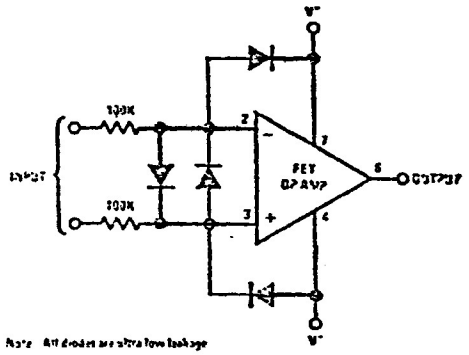
Note 2: Rating applies for minimum source resistance of 10 kΩ. For source resistances less than 10 kΩ, maximum differential input voltage is ±5V.

Note 3: Unless otherwise specified, these specifications apply for ±5V ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ +125°C for the LH0022, LH0042 and LH0052 and −25°C ≤ T_A +85°C for the LH0022C, LH0042C and LH0052C. Typical values are given for T_A = 25°C.

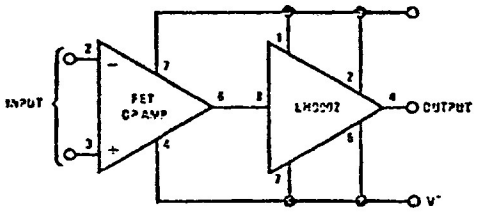
auxiliary circuits (shown for TO-5 pin out)



Offset Null

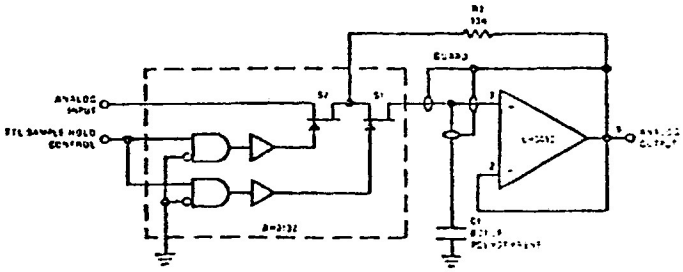


Protecting Inputs From ±150V Transients

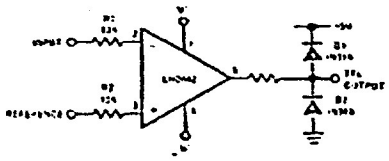


Boosting Output Drive to ±100 mA

typical applications



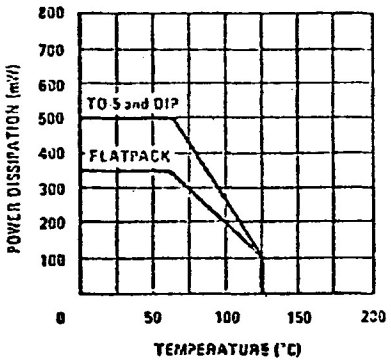
Alternate Low Drift Sample



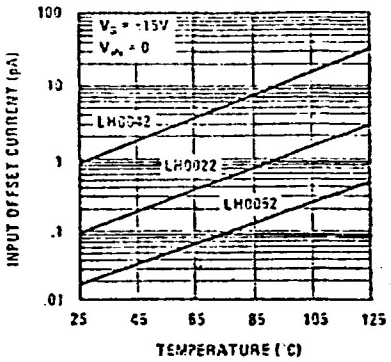
Precision Voltage Comparator

typical performance characteristics

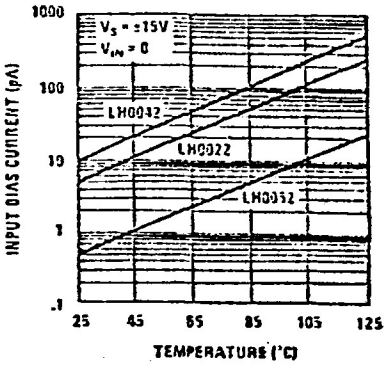
Maximum Power Dissipation



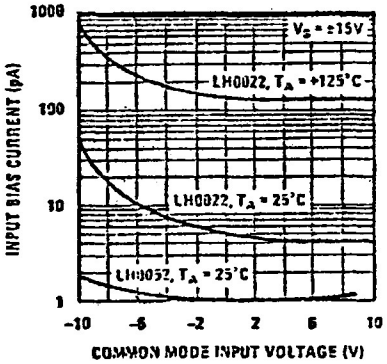
Input Offset Current vs Temperature



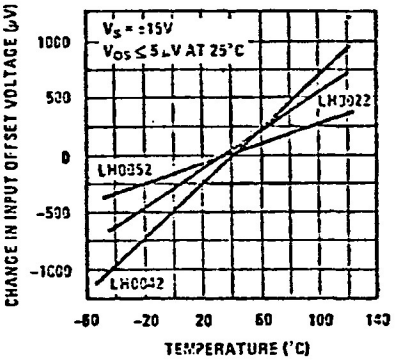
Input Bias Current vs Temperature



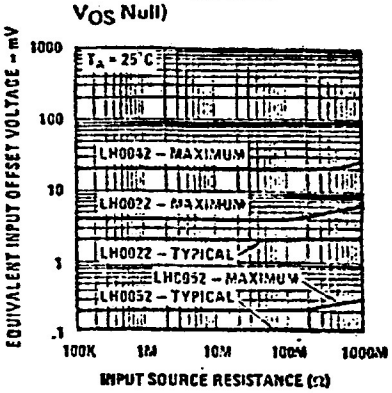
Input Bias Current vs Input Voltage*



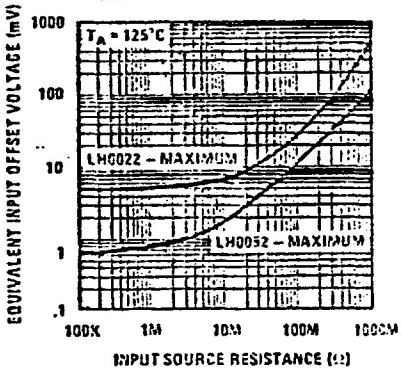
Input Offset Current vs Temperature



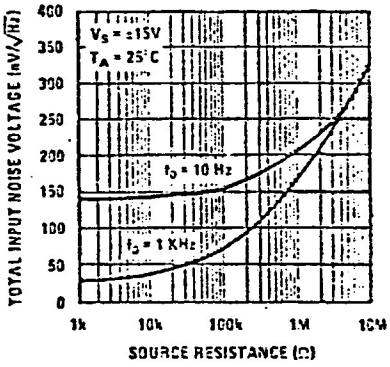
Offset Error (Without V_{OS} Null)



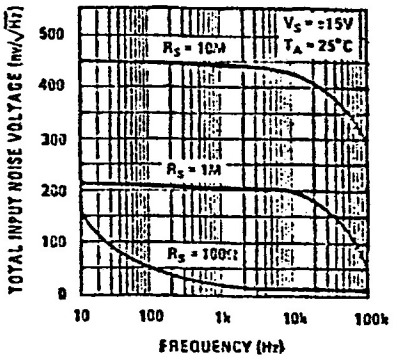
Offset Error (Without V_{OS} Null)



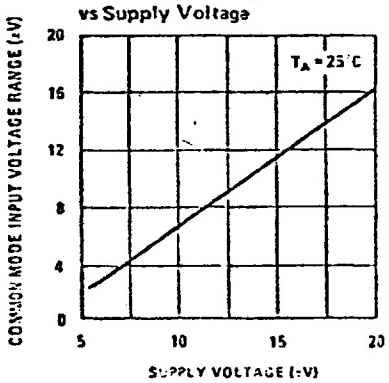
Total Input Noise Voltage* vs Source Resistance



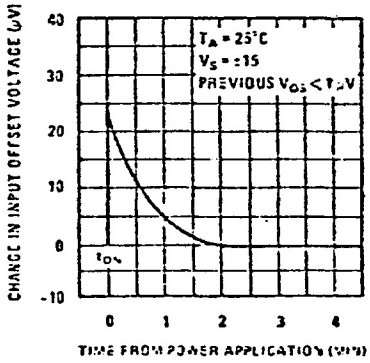
Total Input Noise Voltage* vs Frequency



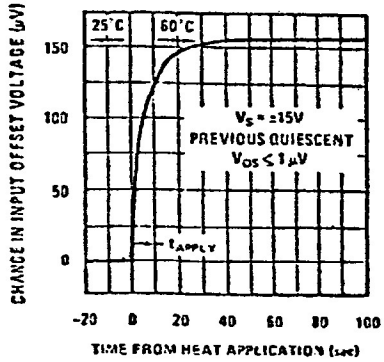
Common Mode Input Voltage vs Supply Voltage



Stabilization Time of Input Offset Voltage from Power Turn-On



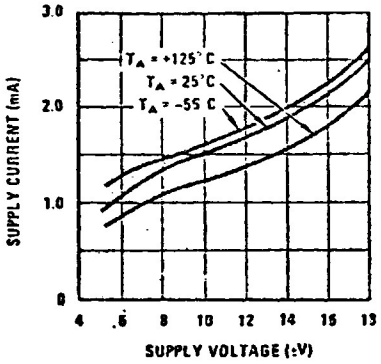
Change in Input Offset Voltage Due to Thermal Shock vs Time



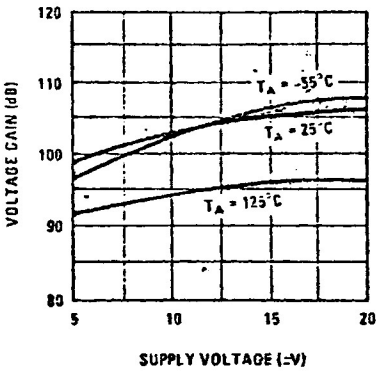
*Noise Voltage Includes Contribution from Source Resistance

typical performance characteristics (con't)

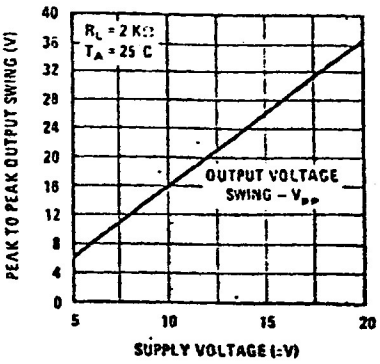
Supply Voltage vs Supply Current



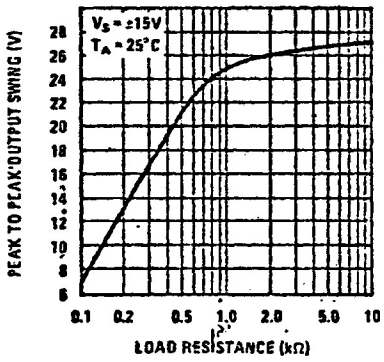
Voltage Gain



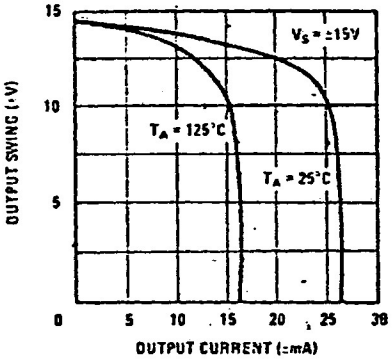
Output Swing vs Supply Voltage



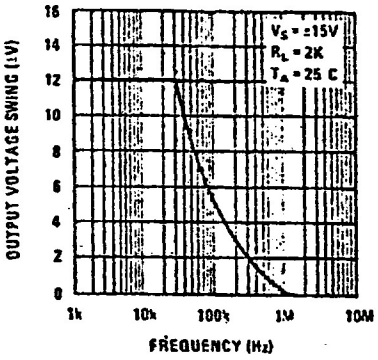
Output Voltage Swing vs Load Resistance



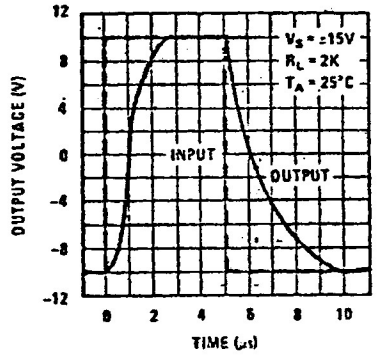
Current Limiting



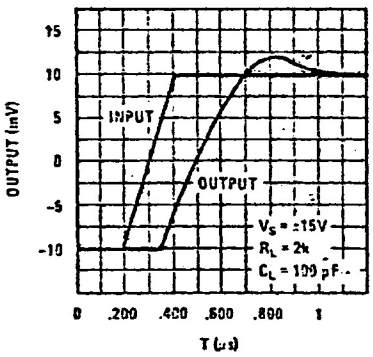
Output Voltage Swing vs Frequency



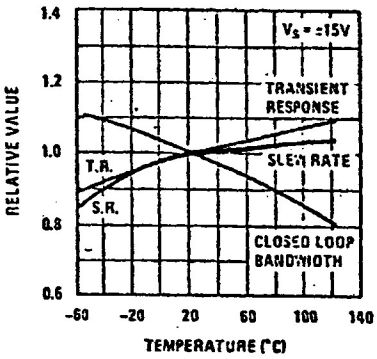
Voltage Follower Large Signal Response



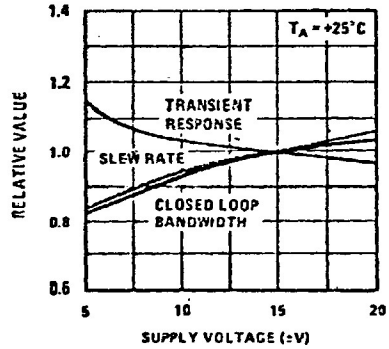
Transient Response



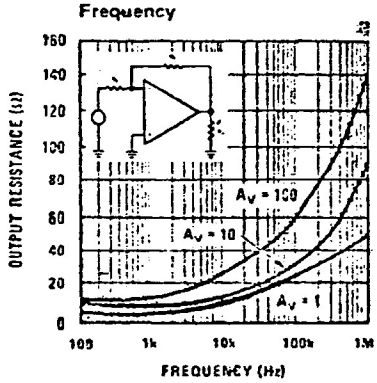
Frequency Characteristics vs Ambient Temperature



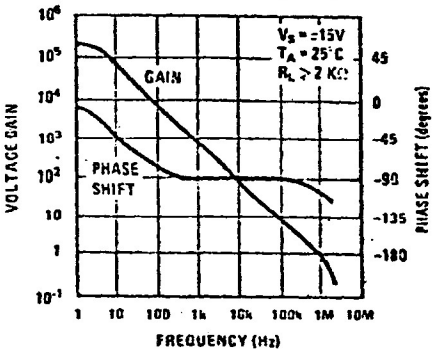
Frequency Characteristics vs Supply Voltage



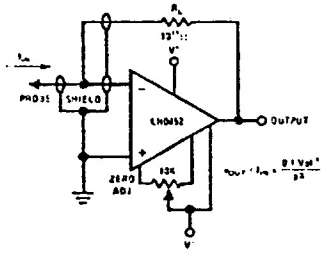
Output Resistance vs Frequency



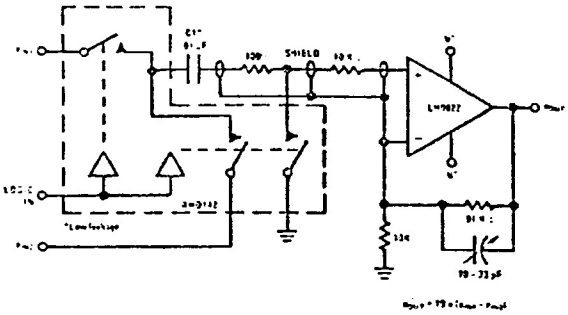
Open Loop Transfer Characteristics vs Frequency



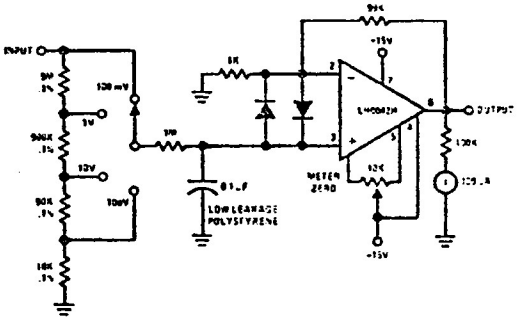
typical applications (con't)



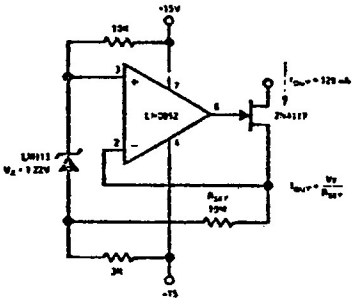
Picoamp Amplifier for pH Meters and Radiation Detectors



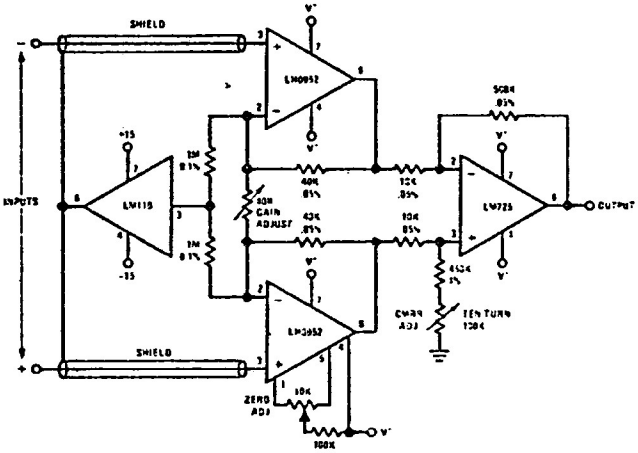
Precision Subtractor for Automatic Test Gear



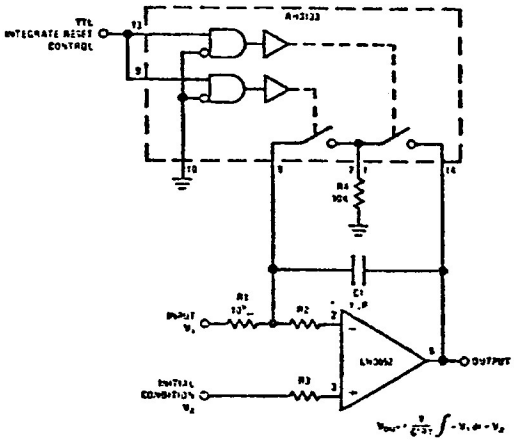
Sensitive Low Cost "VTVM"



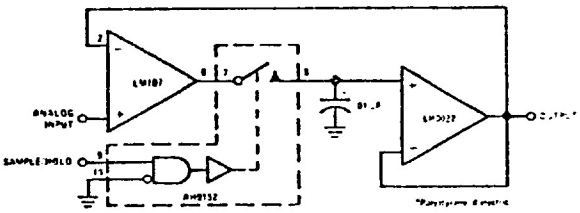
Ultra Low Level Current Source



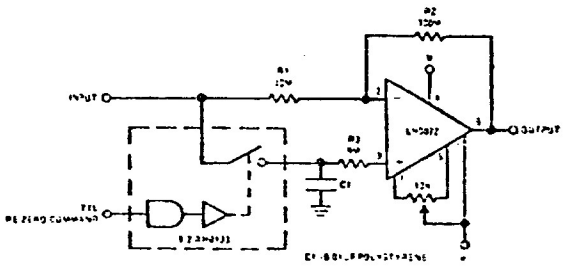
True Instrumentation Amplifier



Precision Integrator



Precision Sample and Hold



Re-Zeroing Amplifier

MONOLITHIC DUAL HIGH-GAIN OPERATIONAL AMPLIFIER

4558

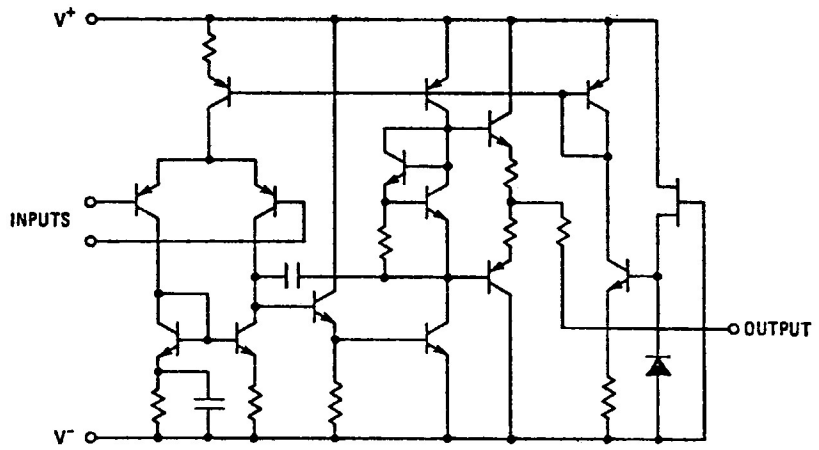
DESIGN FEATURES

- Supply voltage ±18V
- Continuous Short-circuit protection
- No Frequency Compensation Required
- No Latch-up
- Unity Gain Bandwidth 3MHz
- Large Common-mode and Differential Voltage Ranges
- Low Power Consumption
- Parameter Tracking Over Temperature Range
- Gain and Phase Match Between Amplifiers

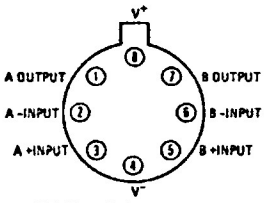
The RC4558 integrated circuit is a high gain operational amplifier internally compensated and constructed on a single silicon chip using the planar epitaxial process. It operates from 0°C to +70°C.

Combining all of the outstanding features of the 741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allows the use of the dual device in all single 741 operational amplifier applications providing the highest possible packaging density. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

SCHEMATIC DIAGRAM

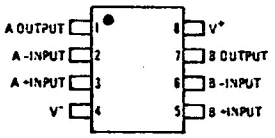


CONNECTION INFORMATION



TE Metal Can Package
(Top View)

Order Part No.:
RC4558T



DN Dual In-line Plastic Package
(Top View)

Order Part No.:
RC4558DN

MONOLITHIC DUAL HIGH-GAIN OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60s)	300°C
Output Short-circuit Duration (Note 3)	Indefinite

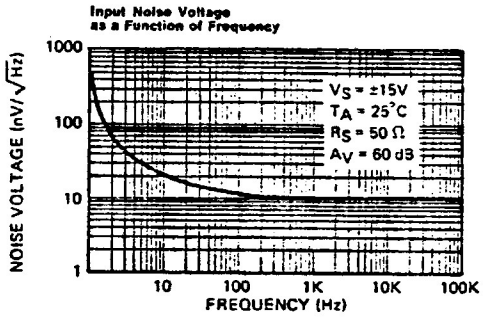
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = ±15V unless otherwise specified)

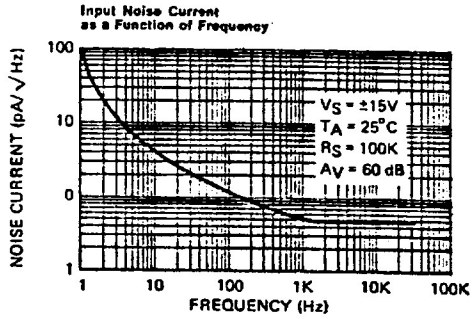
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		0.5	6.0	mV
Input Offset Current			5.0	200	nA
Input Bias Current			40	500	nA
Input Resistance		0.3	5.0		MΩ
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ V_{out} = ±10V	20,000	300,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Power Consumption			105	170	mW
Transient Response (unity gain) Risetime	V_{IN} = 20 mV R_L = 2 kΩ $C_L \leq 100$ pF		0.13		μs
Transient Response (unity gain) Overshoot	V_{IN} = 20 mV R_L = 2 kΩ $C_L \leq 100$ pF		5.0		%
Slew Rate (unity gain)	$R_L \geq 2$ kΩ		1.0		V/μs
Channel Separation	f = 10 kHz R_S = 1 kΩ		105		dB
Equivalent Noise Voltage Referred to Input	A_V = 100 R_S = 1 kΩ BW = 1 Hz		10		nV(Hz)½
Unity Gain Bandwidth (open-loop)			3.0		MHz
The following specifications apply for 0°C ≤ T_A ≤ 70°C unless otherwise specified.					
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ V_{out} = ±10V	15,000			
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V
Power Consumption	V_S = ±15V				mW
	T_A = 70°C		90	150	
	T_A = 0°C		120	200	

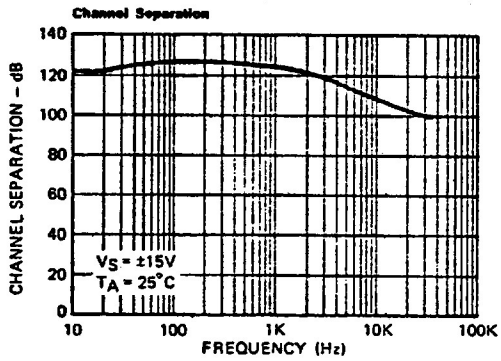
NOTES:

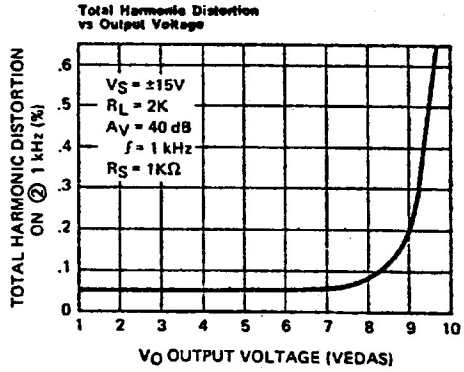
1. Rating applies for ambient temperatures to +25°C; derate linearly at 6.4 mW/°C for ambient temperatures above +25°C.
2. For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground, one amplifier only. I_{SC} = 45mA (typical).

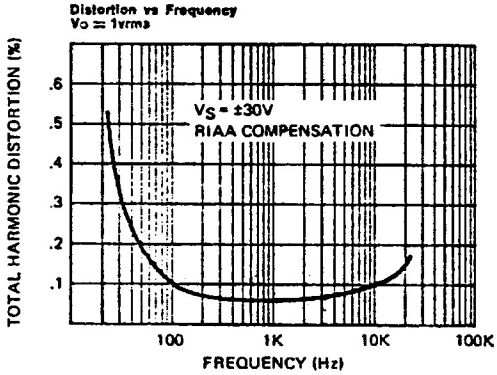
TYPICAL ELECTRICAL DATA



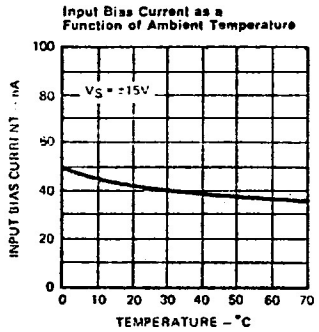


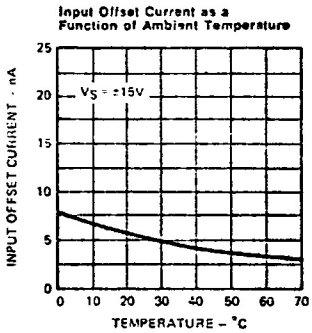


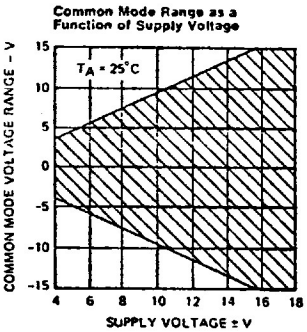


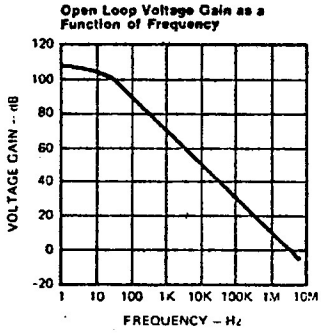


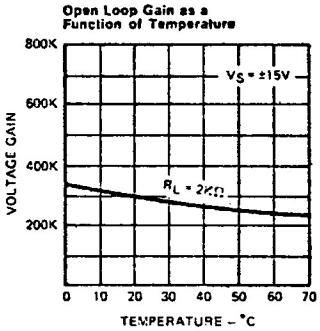
TYPICAL ELECTRICAL DATA

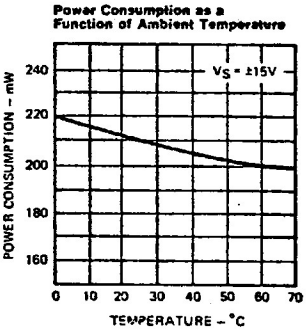


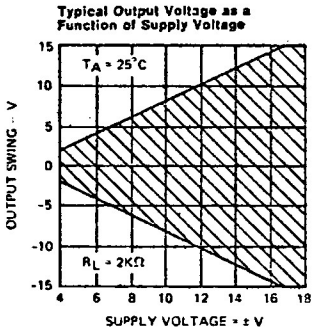


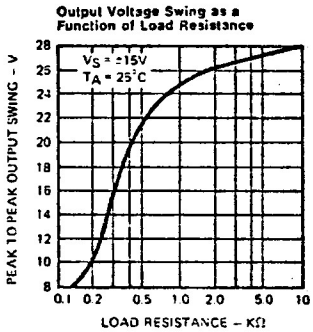


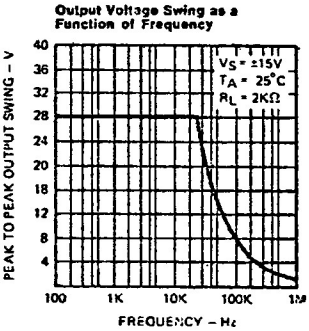


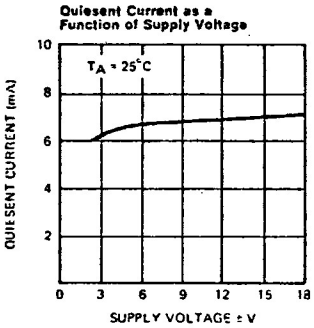


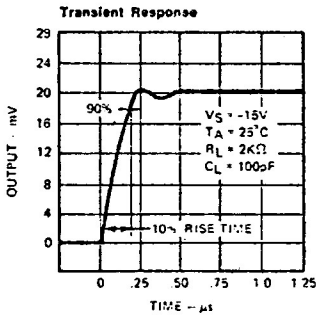


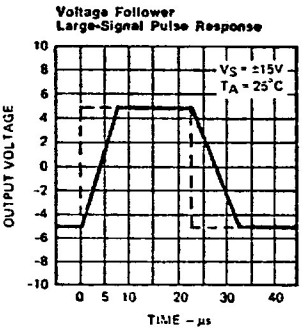












ANALOG DEVICES

CMOS 8 and 16 Channel Analog Multiplexers

PRELIMINARY DATA SHEET

AD7506/AD7507

FEATURES

R_{ON}	300Ω
Power Dissipation	1.5 mW

TTL/DTL/CMOS Compatible
Break Before Make Switching
Silicon Nitride Passivation
Replaces DG506/DG507

GENERAL DESCRIPTION

The AD7506 is a monolithic CMOS 16-channel analog multiplexer packaged in a 28-pin DIP. It switches a common output to one of 16 inputs, depending on the state of four address lines and an "enable". The AD7507 is identical to the AD7506 except it has two outputs switched to two of 16 inputs depending on three binary address states and an "enable".

The AD7506 and AD7507 are excellent examples of a high breakdown CMOS process combined with a double layer interconnect for high density. Both units are silicon/nitride passivated featuring increased stability and reliability.

ORDERING INFORMATION

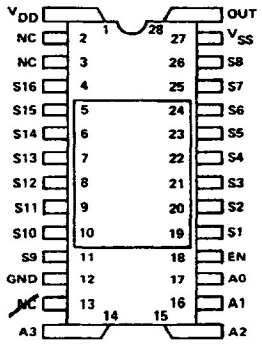
AD7506J	:	0°C to +75°C
AD7506K	:	0°C to +75°C
AD7506S	:	−55°C to +125°C
AD7506T	:	−55°C to +125°C
AD7507J	:	0°C to +75°C
AD7507K	:	0°C to +75°C
AD7507S	:	−55°C to +125°C
AD7507T	:	−55°C to +125°C

PACKAGE VERSIONS

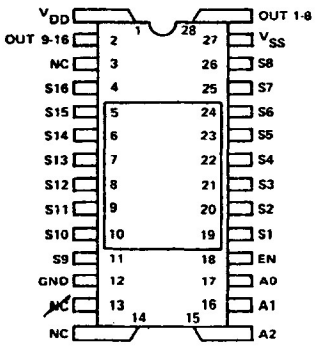
Suffix "D": 28-pin Ceramic DIP

PIN CONFIGURATION (TOP VIEW)

AD7506

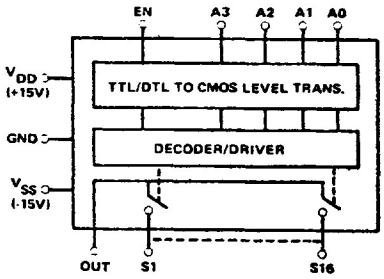


AD7507

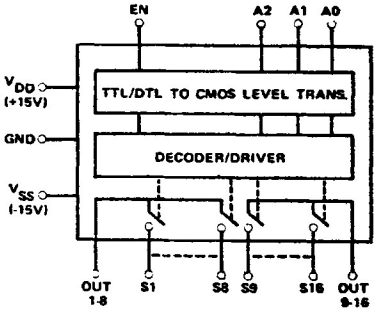


FUNCTIONAL DIAGRAMS

AD7506



AD7507



TRUTHTABLE

AD7506

A_3	A_2	A_1	A_0	E_n	ON SWITCH
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16
X	X	X	X	0	NONE

AD7507

A_2	A_1	A_0	E_n	ON SWITCH PAIR
0	0	0	1	1 & 9
0	0	1	1	2 & 10
0	1	0	1	3 & 11
0	1	1	1	4 & 12
1	0	0	1	5 & 13
1	0	1	1	6 & 14
1	1	0	1	7 & 15
1	1	1	1	8 & 16
X	X	X	0	NONE

ABSOLUTE MAXIMUM RATINGS

V_{DD} (to GND)	+17 V
V_{SS} (to GND)	−17 V
Switch Voltage (to V_{SS})	+27 V
Digital Input Voltage Range	V_{DD} to GND
Switch Current	10 mA
Power Dissipation (Package)	
To +70°C	1200 mW
Derate Above +70°C by	10 mW/°C
Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6777

SPECIFICATIONS (V_{DD} = +15 V, V_{SS} = −15 V unless otherwise noted)

PARAMETER		VERSION	SWITCH CONDITION	@ 25°C MIN	@ 25°C TYP	@ 25°C MAX	Over Specified Temp. Range MIN	Over Specified Temp. Range MAX	UNITS	TEST CONDITIONS
ANALOG SWITCH										
R_{ON}		J, K	ON		300	+50		550		V_S = −10 V to +10 V, I_S = 1 mA
		S, T	ON			400		500		
R_{ON} vs. V_S		All	ON		15				%	
R_{ON} vs. Temperature		All	ON		0.5				%/°C	V_S = 0 V, I_S = 1 mA
R_{ON} Between Switches		All	ON		4				%	
R_{ON} Between Switches vs. Temperature		All	ON		0.05				%/°C	
I_S		J, K	OFF		0.05	5		50	nA	V_S = −10 V, V_{OUT} = +10 V and V_S = +10 V, V_{OUT} = −10 V "Enable" Low
		S, T	OFF		0.05	1		50	nA	
I_{OUT}	AD7506	J, K	OFF		0.3	20		500	nA	
		S, T	OFF		0.3	10		500	nA	
	AD7507	J, K	OFF		0.3	10		250	nA	
		S, T	OFF		0.3	5		250	nA	
$I_{OUT} - I_S$	AD7506	J, K	ON		0.3	20		500	nA	V_S = 0
		S, T	ON		0.3	10		500	nA	
	AD7507	J, K	ON		0.3	10		250	nA	
		S, T	ON		0.3	5		250	nA	
DIGITAL CONTROL										
V_{INL}								0.8	V	Note 2
V_{INH}		J, S					3.0		V	
		K, T					2.4		V	
I_{INL} or I_{INH}		All				10		30	μA	
C_{IN}		All			3				pF	
DYNAMIC CHARACTERISTICS										
$t_{transition}$		J, S			700				ns	V_{IN}: 0 to 3.0 V
		K, T			700	1000			ns	
t_{open}		All			100				ns	
$t_{on(En)}$		J, S			0.8				μs	V_{EN}: 0 to 3.0 V
		K, T				1.5			μs	
$t_{off(En)}$		J, S			0.8				μs	
		K, T				1			μs	
"OFF" Isolation		All			70				dB	V_{EN} = 0, R_L = 200 Ω, C_L = 3.0 pF, V_S = 3.0 VRMS, f = 500 kHz
C_S		All	OFF		5				pF	
C_{OUT}		All	OFF		40				pF	
C_{S-OUT}		All	OFF		0.5				pF	
C_{SS} Between Any Two Switches		All	OFF		0.5				pF	
POWER SUPPLY										
I_{DD} (Standby)		J, K	OFF		0.05	1			mA	All Digital Inputs Low
		S, T	OFF		0.05	1		2	mA	
I_{SS} (Standby)		J, K	OFF		0.05	1			mA	
		S, T	OFF		0.05	1		2	mA	
I_{DD}		J, K	ON		0.3	1			mA	All Digital Inputs High
		S, T	ON		0.3	1		2	mA	
I_{SS}		J, K	ON		0.05	1			mA	
		S, T	ON		0.05	1		2	mA	
PRICE (1-49)	AD7506	J			38.00				$	
		K			40.00				$	
		S			76.00				$	
		T			80.00				$	
	AD7507	J			38.00				$	
		K			40.00				$	
		S			76.00				$	
		T			80.00				$	

NOTES:
1. Specifications subject to change without notice.
2. A pull-up resistor, typically 1–2 kΩ is required to make the J and S versions compatible with TTL/DTL. The maximum value is determined by the output leakage current of the driver gate when in the high state.