VLA TECHNICAL REPORT #12

MODULE L8

DIGITAL DIVIDER

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CONTENTS

I. RELATED DRAWINGS

L8 Top Assemble	D13230P6
L8 Logic Diagram	D13230L8
Control Board Assembly	D13230P42
L8 L/M	A13230Z6
Control Board L/M	A13230Z38
L8 Front Panel	C13230M81
L8 Left Side Plate	B13230M82
L8 Specification	A13710N2

NATIONAL RADIO ASTRONOMY OBSERVATORY
Socorro, New Mexico
VERY LARGE ARRAY PROJECT

SPECIFICATION NO: A13710N2, Rev. A

NAME: L8 Divider Timing and Interface Specification

DATE: June 14, 1976

PREPARED BY: _____ APPROVED BY: _____

1. SCOPE

This specification will define the requirements, design, and interface of the L8 Divider, a part of the NRAO Very Large Array. Both the basic 19.2 Hz and 6.4 Hz system communication cycles are derived within this unit both in the control room and at each antenna. The Waveguide Communication System is used to synchronize antenna L8 units to the control room L8 master. A block diagram of the L8 interconnection is seen in Figure 1.

2. REQUIREMENTS

A. Communication and Waveguide Modems

The L8 Divider establishes the fundamental communication cycle of 19.2 Hz for transfer of data between antennas and control room and vice versa. The basic 1000 μsec interval, Command Time, in which commands flow through the Digital Communication System from control room to antenna is seen in Figure 2-A and Figure 2-B. The digital communication hardware is synchronized by the signal QQ seen in Figure 2-B. This signal initializes divider circuitry both at the antennas and in the control room.

Both Control Room and Antenna Digital Communication System units receive 5 MHz clock signals from the L8.

The signal T/R controls the waveguide communication modems switching control room modems from receive to transmit 106 μsec before Command Time and from transmit to receive 16 μsec after Command Time. At the antenna modems are switched to receive during Command Time.

The T/R signal has a time out feature that, after extended loss of sync by an antenna L8, will force a prolonged receive period of about one second each approximately 20 seconds that an antenna L8 displays the out of sync condition. If the remote L8 does not turn on antenna modem receivers during command time (as defined by the control room L8), as for instance after power turn on, no sync pulse will ever be received and synchronization cannot be acquired. The time out will, however, force a prolonged receive condition which will insure reception of several sync pulses from the control room L8 and insure synchronization.

B. Master LO, Central LO, and Antenna LO

The L8 Divider generates 19.2 and 6.4 Hz signals which allow the LO system to establish epoch timing within the VLA. A 6.4 Hz signal is generated by the L8 Divider which will allow the LO to signiture specific 5 MHz cycles within the control room and transmit this information via the Waveguide Communication System to all antennas.

The basic 19.2 and 6.4 Hz timing signals developed for the master LO in the control room by the L8 is the 1200 MHz Carrier On. The 1200 MHz Carrier On signal is a 19.2 Hz signal with a 6.4 Hz irregularity and controls the 1200 MHz carrier within the Waveguide Communication System. The 1200 MHz carrier, amplitude modulated with 5 MHz, will always turn on during a positive going zero crossing of 5 MHz sinewave. This requirement introduced the 6.4 Hz irregularity in the Carrier On signal since there is not an even number of 5 MHz cycle in a 19.6 Hz period.

At each antenna the fast turn on of the 1200 MHz carrier signatures the leading 5 MHz modulated cycle which is detected at the LO and used to synchronize the remote L8 Divider.

Synchronization within the L8 is a dual function operation featuring a narrow band sync monitor mode when in sync and a wide band sync acquation mode when attempting to achieve sync. When in sync at least 8 errors must be observed by the L8 in order to lose sync whereas once sync is lost 8 valid sync detections are required before the out-of-sync flag is removed. Figure 3 illustrates the remote L8 synchronization operation in flow chart form.

The L8 Divider also provides the LO system with 5 MHz and 600 MHz track/hold signals with which to lock phase lock loops at the antenna to received 5 and 600 MHz signals. These signals are, however, only valid after

the L8 has achieved synchronization. Prior to this time the LO system must achieve initial 5 MHz phase lock unaided.

C. Delay/Multiplier System

The control room L8 Divider provides the delay/multiplier system with a data invalid signal. When at logic one this signal indicates the potential of invalid data at the delay line output and is used to inhibit multiplications and hence integration.

Delay line output data will not be valid antenna information between the interval from Switch to Transmit in the control room Waveguide Communication System until the delay lines are again filled with valid antenna data. Below is a review of the timing involved referenced to T = 0 as defined in Figure 1:

1.	Data goes invalid	- 106 µsec
2.	Control room SW to Receive	1016 µsec
	Round trip to far antenna of SW signal	150 µsec
	Transmitter warm-up	100 µsec
	Max delay line thru-put time	203 µsec
	Data goes valid	1469 µsec

Actually a delay line will continue to provide good data for at least 40 µsec (minimum delay line thru-put time) after -106 µsec unless its delay is re-pregrammed immediately at -106 µsec. The L8 data invalid signal spans the interval from -106 µsec to +1497 µsec.

D. Fringe Generator

A 100 kHz clock is provided to the fringe generator at each antenna. This signal is a symmetrical signal in precise time relation to 6.4 Hz sync at each unit. The duty cycle of this signal is 50%.

In addition to this function the sync status bit within the L8 is reported to the computer via a Digital Communication System monitor word which originates from one of the fringe generators.

Some logic completely unrelated to the L8 Divider functions is physically within the L8 module. This hardware functions via the Digital Communication System to control phase reversals within both the fringe generator and samplers, but will not be discussed in detail in this specification.

E. Front Ends

The L8 Divider provides a 9.6 Hz square wave signal to the front ends at each antenna.

F. Time of Day Clock

The L8 Divider in the control room provides a 19.2 Hz signal to a time of day clock. This clock divides its 19.2 Hz input down to 0.1 Hz which is used to drive a Digital Clock. Both the 19.2 Hz count and the time of day are reported to the computer.

The L8 Divider will accept a reset pulse generated from a time standard so as to time its 19.2 Hz "ticks" with standard time. The 19.2 Hz to 0.1 Hz Divider also is reset by this pulse to time its 10 second "ticks" with time of day. Since the divider string that ultimately drives the time clock starts at 5 MHz the resulting time set is good to 200 ηsec.

III. INTERFACE SPECIFICATION

Three cable interface methods are used and are described below.

Differential TTL:

Communication is via 75183-75182 differential driver-receiver using Beldon 8451 twisted shielded cable. The shield is to be grounded at both ends with the differential pair being AC terminated in 100 ohms.

Single Ended TTL:

Communication is via 7437 driver-TTL load receiver using Beldon 8451 twisted shielded cable. The shield is to be grounded at both ends and the black conductor is to be grounded at both ends, and the signal conductor AC terminated in 100 ohms.

50 ohm Coax:

Communication is via 74128 TTL driver using coaxial cable. Cable is to be DC terminated in 50 ohms to ground.

The single ended interface could reduce down to a bare unterminated point to point wire for short runs.

Table 1 give a unit breakdown of signals, interface type, and timing of the L8 interface.

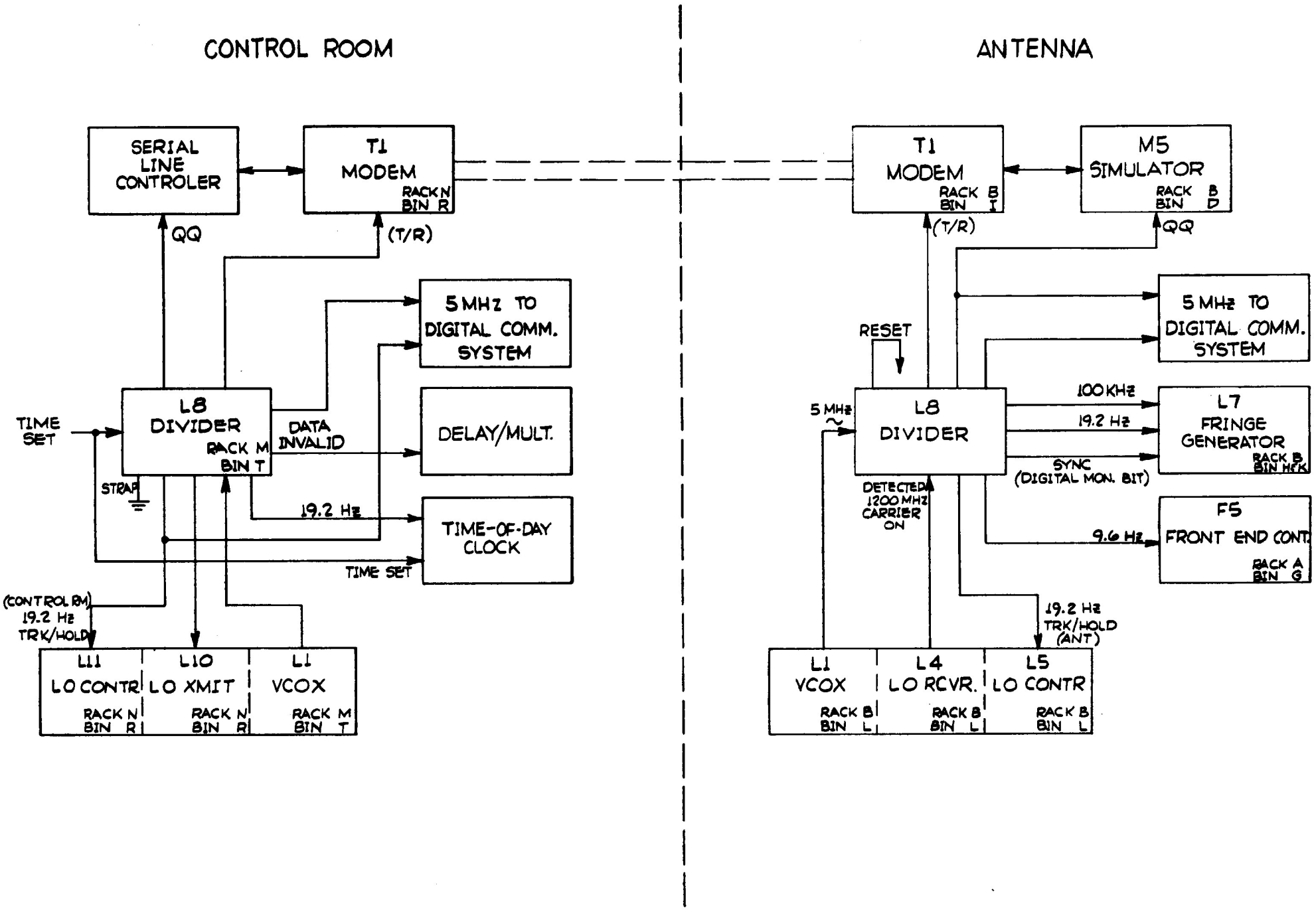

CONTROL ROOM
ANTENNA
SERIAL LINE CONTROLER
T1 MODEM
RACK N BIN R
QQ
(T/R)
5 MHz TO DIGITAL COMM. SYSTEM
L8 DIVIDER
RACK M BIN T
TIME SET
DATA INVALID
DELAY/MULT.
STRAP
19.2 Hz
TIME-OF-DAY CLOCK
TIME SET
(CONTROL RM) 19.2 Hz TRK/HOLD
L11 LO CONTR RACK N BIN R
L10 LO XMIT RACK N BIN R
L1 VCOX RACK M BIN T
T1 MODEM
RACK B BIN I
M5 SIMULATOR
RACK B BIN D
(T/R)
QQ
RESET
5 MHz TO DIGITAL COMM. SYSTEM
5 MHz
L8 DIVIDER
100 KHz
19.2 Hz
SYNC (DIGITAL MON. BIT)
L7 FRINGE GENERATOR
RACK B BIN H&K
DETECTED 1200 MHz CARRIER ON
F5 FRONT END CONT.
RACK A BIN G
9.6 Hz
19.2 Hz TRK/HOLD (ANT)
L1 VCOX RACK B BIN L
L4 LO RCVR. RACK B BIN L
L5 LO CONTR RACK B BIN L

FIG. 1

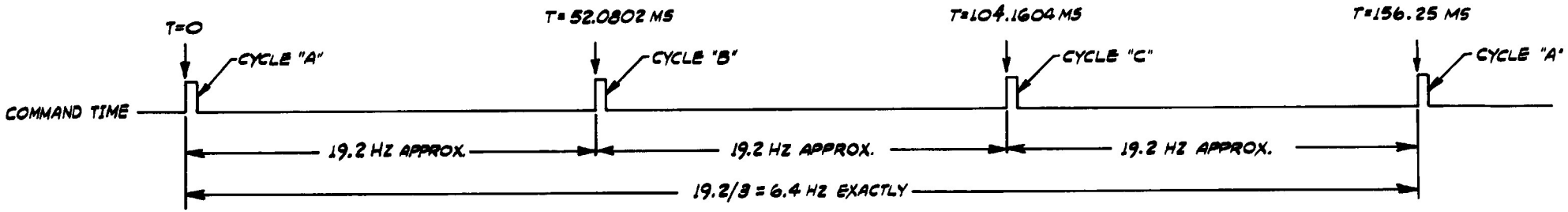
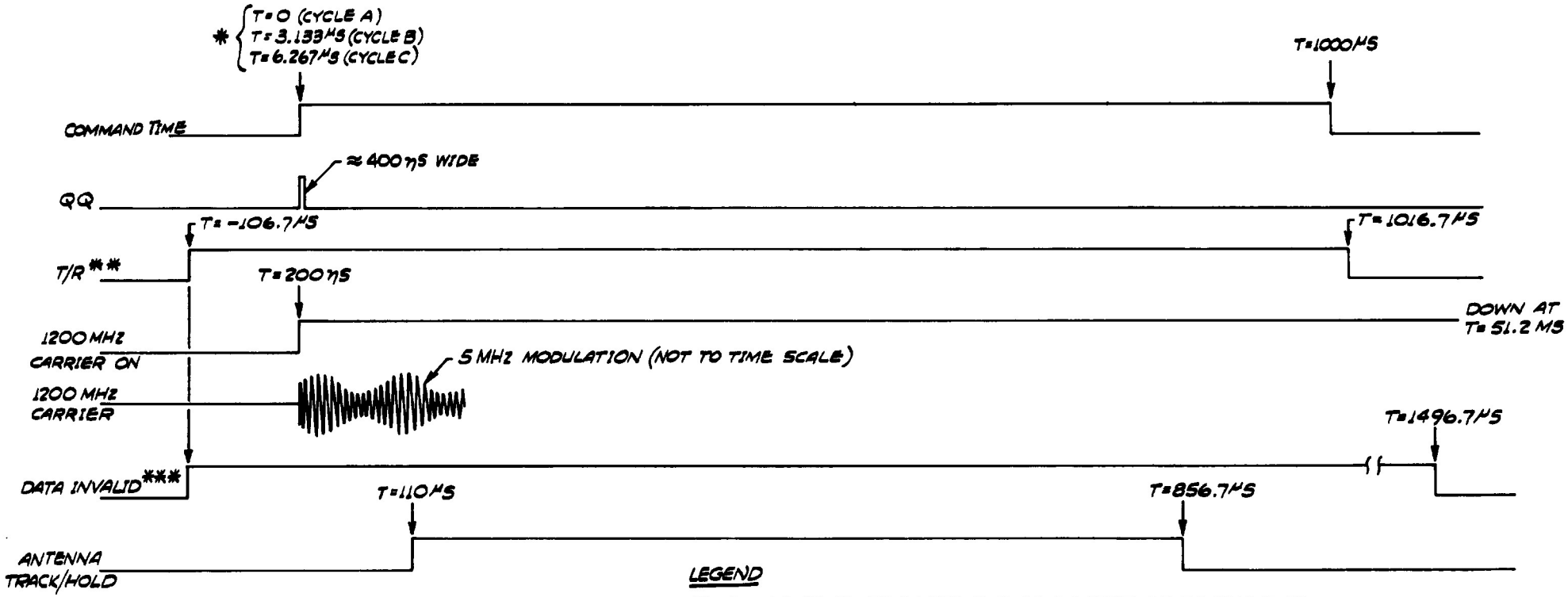


FIG. 2-A



LEGEND

* - ALL OTHER TIMES IN FIG. 2-B CALCULATED AS IF COMMAND TIME STARTED AT T=0 EXACTLY.

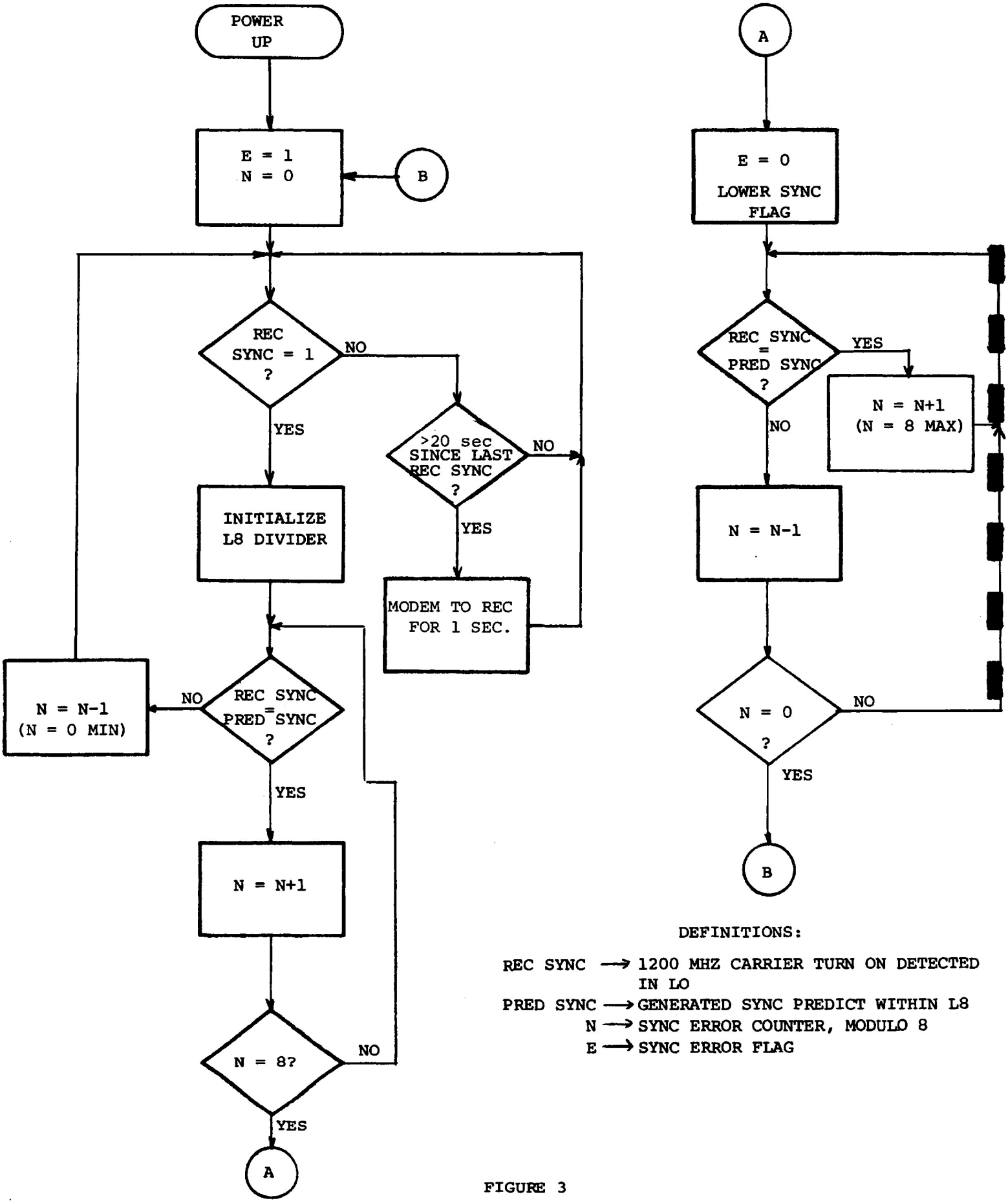
** - INVERTED AT ANTENNA

*** - ALSO LOCAL TRACK/HOLD

FIG. 2-B

TABLE I

SYSTEM	L8 INPUT/OUTPUT	SIGNAL FUNCTION	LOCATION	INTERFACE
Digital Communication System	Output	QQ	Local and Antenna	Differential TTL 400 nsec positive pulse
	Output	Sync Timeout	Antenna	Single ended TTL Logic one for error
Waveguide Communication Channel	Output	Switch to transmit (T/R)	Local and Antenna	Single ended TTL Logic one for transmit
	Input	Master/Ant Strap	Local	GND at Control Room Open at antenna
LO System	Input	5 MHz sinewave	Local and Antenna	50 ohm coax, AC terminated In 50 ohms 0 dBm level
	Output	Control Room Track/Hold (CTH)	Local	Single ended TTL Logic one to track
	Output	1200 MHz carrier on (CARON)	Local	50 ohm coax Logic one for carrier on
	Output	Antenna Track/Hold (ATH)	Antenna	Single ended TTL Logic one to track
	Input	Detected 1200 MHz carrier on (DCO)	Antenna	50 ohm coax Logic one for carrier on
Delay/Multiplier	Output	Data invalid (DINV)	Local	Differential TTL Logic one for invalid data
Digital Clock	Output	19.2 Hz	Local	Single ended TTL
Fringe Generator	Output	100 kHz Clock	Antenna	50 ohm coax (4 individual outputs)
	Output	Sync Error (E)	Antenna	Single ended TTL Logic one indicates sync error
Front End	Output	9.6 Hz	Antenna	Single ended TTL



DEFINITIONS:

REC SYNC ⟶ 1200 MHZ CARRIER TURN ON DETECTED IN LO
PRED SYNC ⟶ GENERATED SYNC PREDICT WITHIN L8
N ⟶ SYNC ERROR COUNTER, MODULO 8
E ⟶ SYNC ERROR FLAG

FIGURE 3

III. CIRCUIT DETAILS

A block diagram of the L8 is shown in Figure 1. The 5 MHz input to the L8 is a 0 dBm sinewave that is shaped into a square wave clock in the 1A comparator. IC's 2A and 2B form a ÷ 50 circuit with a 100 kHz output. The 100 kHz square wave output of this divider drives a digital X3 multiplier which at each falling edge of 100 kHz clock (CO.1) will meter out three 5 MHz clock pulses (see timing relationship on logic diagram). The result, CO.3, will average out to 300 kHz long term. This highly non-symmetrical 300 kHz clock produces time jitter on all of the 19.2 Hz L8 digital outputs. This jitter is observable on the 19.2 Hz signals with an oscilloscope producing three distinctive transition times of any signal.

IC's 2C, 2D, 2E, and 2F form a ÷ 15625 counter that produces a 19.2 Hz output from the 300 kHz clock. Various states of this counter are decoded to produce signals required of the L8.

The logic associated with IC's 4G, 7D and 4F serve to synchronize slave L8's from the DETECTED CARRIER ON signal supplied by the L4 LO receiver. The sync circuit works in a wide bandwidth mode during initial sync-up and a narrow bandwidth mode during sync monitoring. In sync acquation mode the register 7D will be at all one's since bad sync will fill it with such. In this mode each DETECTED CARRIER ON positive transition will produce a pulse on the RESET OUT line which in a slave L8 is strapped to RESET IN. The reset pulse will initialize both ÷ 50 and ÷ 15625 counters. The DETECTED CARRIER ON logic signal is derived from the 1200 MHz carrier turning on which is generated by the 1200 MHZ CARRIER ON signal which originates within the Control Room L8. This signal has a 19.2 Hz rate with a 6.4 Hz irregularity which forces the antenna L8 into a trial and error sync-up mode. The 6.4 Hz component in the 1200 MHZ CARRIER ON signal produces three distinct cycles as defined in the L8 specification, only one of these cycles will produce a sync pulse that will properly set the ÷ 50 and ÷15625 counters. Thus between 1 and 3 19.2 Hz cycles will go by until the L8 is correctly initialized. However, the wide-band operation will continue until at least 8 valid sync comparisons are observed and the sync flag lowered.

Received sync (IC 4G-8) is compared against predicted sync (IC 4G-6) in gates 5E-3 and 5D-8. Good comparison produces a pulse at 5D-8 right shifting zero's into 7D and bad comparison produces a pulse at 5E-3 left shifting one's

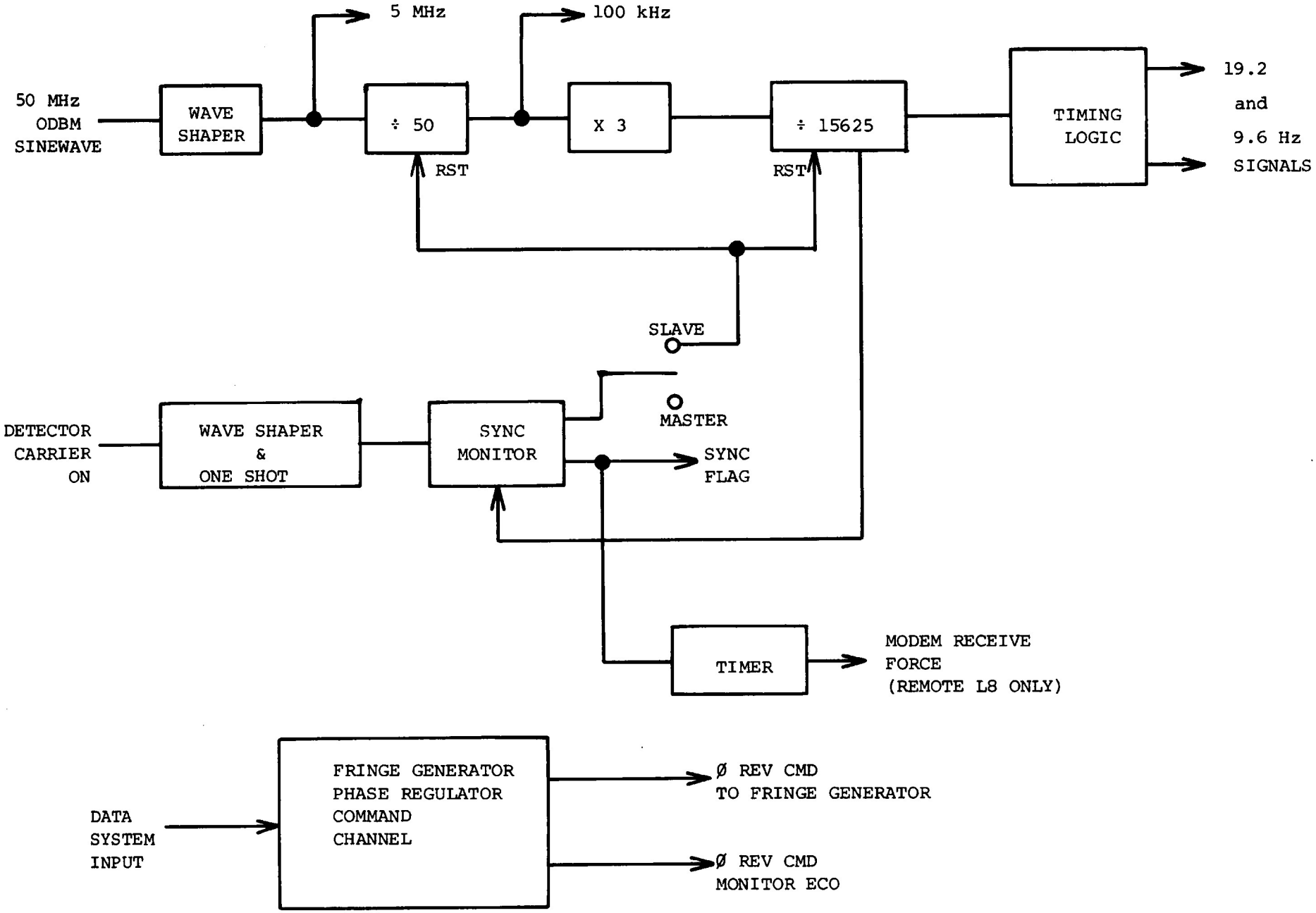
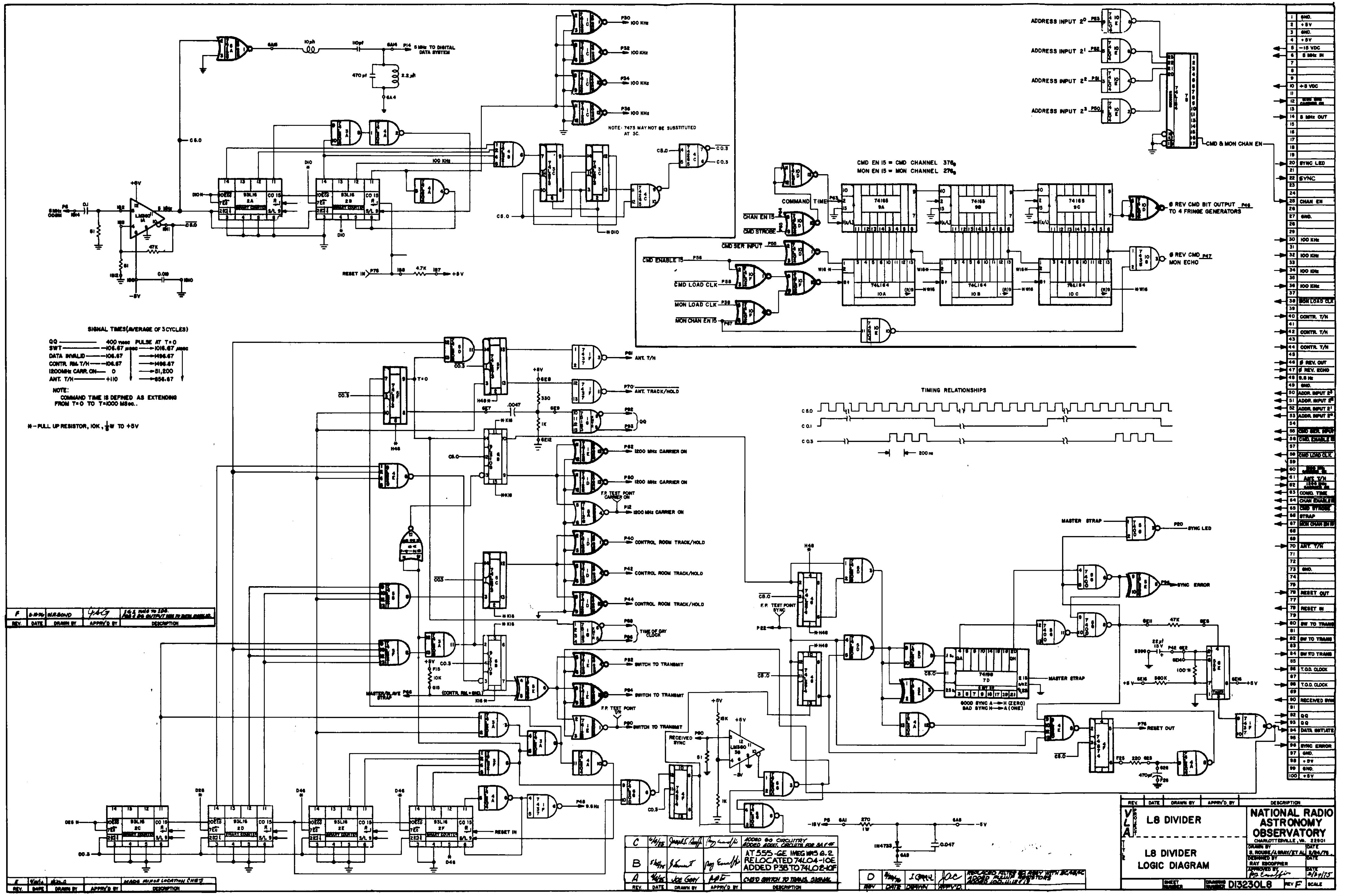

5 MHz
100 kHz
50 MHz
ODBM
SINEWAVE
WAVE
SHAPER
÷ 50
X 3
÷ 15625
TIMING
LOGIC
19.2
and
9.6 Hz
SIGNALS
RST
RST
SLAVE
MASTER
DETECTOR
CARRIER
ON
WAVE SHAPER
&
ONE SHOT
SYNC
MONITOR
SYNC
FLAG
TIMER
MODEM RECEIVE
FORCE
(REMOTE L8 ONLY)
DATA
SYSTEM
INPUT
FRINGE GENERATOR
PHASE REGULATOR
COMMAND
CHANNEL
Ø REV CMD
TO FRINGE GENERATOR
Ø REV CMD
MONITOR ECO

FIGURE 4



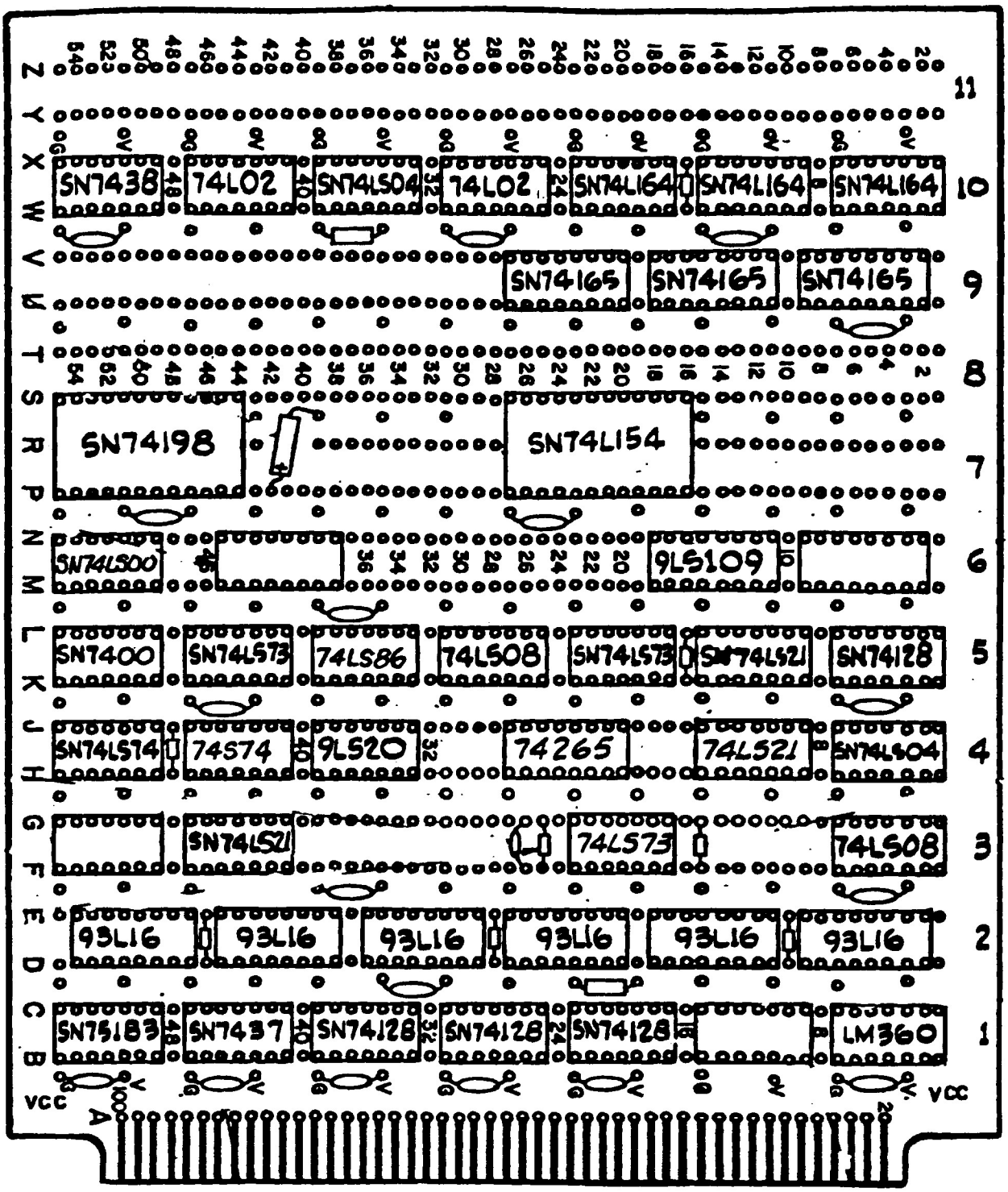
SIGNAL TIMES (AVERAGE OF 3 CYCLES)
QQ — 400 nsec PULSE AT T=0
SWT — -106.67 μsec → 1016.67 μsec
DATA INVALID — -106.67 → 1496.67
CONTR. RM. T/H — -106.67 → 1496.67
1200MHz CARR. ON — 0 → 51,200
ANT. T/H — +110 → 656.67
NOTE:
COMMAND TIME IS DEFINED AS EXTENDING FROM T=0 TO T=1000 MSec.
✻ - PULL UP RESISTOR, 10K, ¼W TO +5V
NOTE: 7473 MAY NOT BE SUBSTITUTED AT 3C.
5 MHz TO DIGITAL DATA SYSTEM
CMD EN 15 = CMD CHANNEL 376₈
MON EN 15 = MON CHANNEL 276₈
8 REV CMD BIT OUTPUT TO 4 FRINGE GENERATORS
8 REV CMD MON ECHO
ADDRESS INPUT 2⁰
ADDRESS INPUT 2¹
ADDRESS INPUT 2²
ADDRESS INPUT 2³
CMD & MON CHAN EN
TIMING RELATIONSHIPS
ANT. T/H
ANT. TRACK/HOLD
1200 MHz CARRIER ON
CONTROL ROOM TRACK/HOLD
TIME OF DAY CLOCK
SWITCH TO TRANSMIT
MASTER/SLAVE STRAP
RECEIVED SYNC
SYNC LED
SYNC ERROR
MASTER STRAP
GOOD SYNC A → H (ZERO)
BAD SYNC H → A (ONE)
RESET OUT
RESET IN
9.6 Hz
F | WRBOND | 1 & 2 MHz TO 12S. | REV. | DATE | DRAWN BY | APPR'D BY | DESCRIPTION
E | MADE MINOR LOCATION CHG'S | REV. | DATE | DRAWN BY | APPR'D BY | DESCRIPTION
C | 6/4/75 | Joseph S. ... | ... | ADDED GG CIRCUITRY ADDED ADDIT. CIRCUITS FOR 5A & 4F
B | 5/.../75 | ... | ... | AT 555-GE IMEG WAS 6.2 RELOCATED 74LO4-10E ADDED P38 TO 74LO2-10F
A | .../75 | JOE GRAY | ... | CHG'D SWITCH TO TRANS. SIGNAL
REV. | DATE | DRAWN BY | APPR'D BY | DESCRIPTION
D | ... | I GRAY | JAC | REPLACED FILTER ... ADDED PULLUP RESISTORS
REV | DATE | DRAWN | APPR'D.
VLA PROJECT: L8 DIVIDER
TITLE: L8 DIVIDER LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901
DRAWN BY S. ROUSE/L GRAY/ET AL DATE 2/24/75
DESIGNED BY RAY ESCOFFIER
APPROVED BY DATE 2/24/75
DRAWING NUMBER D13230L8 REV F SCALE

into 7D. The 8 bit register 7D provides the bandwidth switching capacity in sync operation requiring 8 good sync comparisons to achieve sync or 8 bad sync comparisons to lose sync.

IC 3G is a comparator that sets the latch on the leading edge of the received sync input. This latch is enabled about 25 μsec before sync time. IC's 4G-8 and 5D-6 allow only the rising edge of received sync to enter into sync comparison.

The NE555 IC 6E is a one shot used to force antenna modems to receive after a prolonged loss of sync. The 1200 MHz carrier, modulated with 5 MHz is transmitted from the control station only during command time as determined by the control room L8. The remote L8, which uses the 5 MHz modulation as received sync, can "Look" for this carrier only when remote modems are in receive which is controlled by the antenna L8. A gross timing error in the antenna L8 will result in antenna receivers never being on during a 5 MHz sync burst. The NE555 timer will, after loss of sync of about 20 seconds, force antenna modems to receive for about 1 second insuring reception of several 5 MHz sync bursts. Once initialized the antenna L8 can take over and turn remote modems to receive at the proper time for the 5 MHz sync pulse and normal operation will result.

Also within the L8 module is some logic that provides phase reversal information for the fringe generator. This circuit decodes command and monitor channel addresses from the Digital Communication System into registers 10A, 10B, and 10C. This digital data is supplied to the fringe generator one bit each 19.2 Hz frame from registers 9A, 9B, 9C. An echo output is supplied back into the Digital Communication System thru Gate 10G-3.


SN7438
74L02
SN74LS04
74L02
SN74LI64
SN74LI64
SN74LI64
SN74165
SN74165
SN74165
SN74198
SN74L154
SN74LS00
9LS109
SN7400
SN74LS73
74LS86
74LS08
SN74LS73
SN74LS21
SN74128
SN74LS74
74S74
9L520
74265
74L521
SN74LS04
SN74LS21
74L573
74LS08
93L16
93L16
93L16
93L16
93L16
93L16
SN75183
SN7437
SN74128
SN74128
SN74128
LM360
VCC
VCC

IV. ADJUSTING AND SERVICING

Servicing the L8 may be accomplished with the L8 automatic test fixture. This test fixture will accept either a card or module L8 (But Not Both) and provide for a GO/NO GO test. Both +5 and -15 VDC are required for this test fixture. Below is a complete checkout procedure for using the L8 Auto Test fixture:

Step 1. Plug card or module into test fixture.

Step 2. Apply +5 VDC $\pm$0.10V @ 1A and -15 VDC $\pm$0.1V @ 250 mA to the test fixture.

Step 3. Master/Slave switch to Master, allow for $\approx$20 second time out.

Step 4. Press, release reset switch, all lamps go off and remain off.

Step 5. Switch Master/Slave switch to Slave Position. Only after about 20 seconds the sync error lamp will go off.

Step 6. Press, release reset switch - all lamps go off and remain off.

Step 7. Re-initiate the sync-up process several times to insure proper sync-up capacity by pressing the sync re-initiate switch (reset errors after each time with the reset switch after the sync error lamp has gone out).

The error lamps on this fixture are latched errors and any momentary error will be latched on, thus if intermittent errors are suspected let the unit play for long periods of time.

V. L8 TROUBLESHOOTING NOTES

The most complex operation performed by the L8 is in acquiring and maintaining synchronization. Failure of other L8 functions, such as loss of a specific signal, should be straightforward and troubleshooting and repair will present no problems. The complexity of a X3 multiplier in the divider string, however, makes the acquisition of sync a difficult process to troubleshoot.

Some prerequisites are necessary before an antenna L8 can be expected to acquire sync:

1) 0 dBm 5 MHz sinewave from the LO system. This signal provides the central clock for all L8 functions.

2) 5 MHz phase-lock-loop in lock. Initially this PLL cannot be phase locked to the control room master oscillator since it is the L8's function to provide its track/hold timing. However, once the L8 has received a single sync pulse (which may have to wait for the NE555 timer circuit discussed earlier to command a prolonged receive condition in the antenna modem) the L8 should be within a few hundred nanoseconds of its correct timing and will yield a 5 MHz track/hold signal sufficiently close to allow 5 MHz PLL lock. Only after stabilization of the 5 MHz PLL can sync acquisition by the L8 be completed. The symptom displayed at the L8 if 5 MHz PLL never locks is a blinking sync light. The blink rate will be at the beat frequency between master and remote 5 MHz oscillators. If this beat frequency is above about 2.5 Hz the L8 will remain permanently out of sync.

3) Sync pulse. This sync pulse is the demodulated 1200 MHz carrier as detected at the antenna. It's amplitude must be above the threshold of the LM360 comparator (0.3V) and if it dips below threshold after its initial rise it must stay below threshold for the duration of the sync pulse. To desensitize the sync acquisition process to spikes or noise on the sync line a sync window is opened only 25 microseconds prior to an expected sync pulse (as defined by the output of a pulse at Gate 5D-3). Thus if the L8 ever "sees" the rise back above threshold of a sync pulse it will never "look" more than 25 microseconds prior to this on successive cycles and may be trapped in the valley so to speak. Spikes that occur at a 19.2 Hz rate, or that occur in the 25 microsecond window can also prevent proper synchronization.

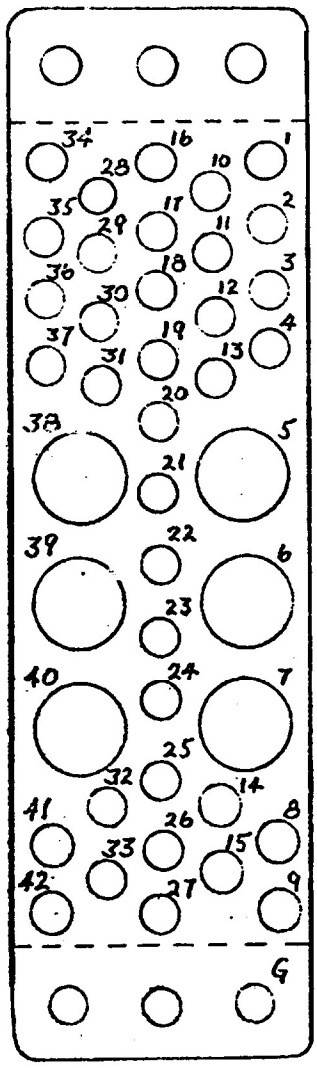
The extended 1200 MHz Carrier On signal at the master L8 will result in a very long sync pulse (50 msec) if the control room modem is manually switched into permanent transmit. Since the L8 can only move by 25 microseconds per 19.2 Hz cycles under such conditions an extended sync-up period will result. Once synchronization is achieved, however, normal operation will result.

4) Correct timing of the sync pulse. The sync pulse should be timed relative to the internal 5 MHz clock in the L8 such that no race exists at the three places it must be captured. Flip/flop 4G-9 must capture the latch output that is set by the sync pulse rising edge. The flip/flop 4F-5 must also capture this same edge after several more levels of gating. The IC 7D must also capture this edge at pin 1. In each case capture is on falling edge of 5 MHz clock (rising edge of clock not). Only the leading edge of the sync pulse must be timed properly with respect to 5 MHz. Trailing edges are IC propagation delays and are raceless.

Two main problems are encountered in troubleshooting the L8, the low rep-rate (19.2 Hz) combined with the close timing (50 nanosecond) and the three in one wobble in the 19.2 Hz signals. No good way exists to overcome these handicaps. Long exposure photographs can offset the low-rep rate and using the the 1200 carrier on signal for scope sync can reduce the inconvenience of the 6.4 Hz component in some 19.2 Hz signals.

One additional problem in working on an L8 trying to acquire sync is that the reset pulses which occur each 19.2 Hz cycle render most signals unstable cycle to cycle. Hence this connection (pin 76 to 78 of the PC board) must sometimes be broken to stabilize the unit.

L 8



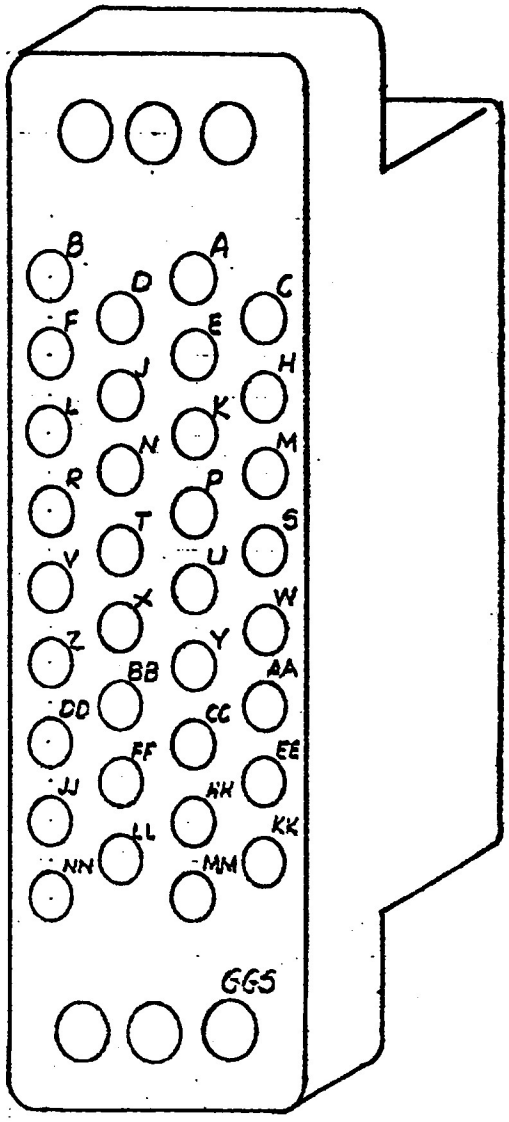
MODULE REAR VIEW

PIN	FUNCTION	BIN COLOR	MODULE P.C. CONN. PIN
1	100 KHz	TW. PAIR	30
2	(GND RET FOR 1)	↓ ↓	29
3	100 KHz	TW. PAIR	36
4	100 KHz	↓ ↓	35
5	5 MHz Ø IN	RG-174/U	G
6	1200 MHz CARR. ON	RG-174/U	60
7	RECEIVE SYNC.	RG-174/U	90
8	CONTR. ROOM T/R	WHT./GRN	40
9	CONTR. ROOM T/R	WHT./BLU	42
10	+5.0 V	ORANGE	2
11	-5.0 V	BROWN	
12	(GND RET FOR 3)	TW. PAIR	27
13	(GND RET FOR 4)	↓ ↓	27
14	ANT. TRACK/HOLD	WHT./BRN.	70
15	1200 MHz CARR. ON	WHT./PUR.	62
16	+15 V	RED	
17	-15 V	YELLOW	5
18	RESET OUT	WHT./GRY	76
19	RESET IN	WHT./BLK	78
20	SWITCH TO TRANS.	BROWN	80
21	↑ ↓ ↓	WHT./RED	82
22	1200 MHz CARR. ON	WHT./ORN.	12
23	T.O.D. CLOCK	WHT./YEL.	86
24	↓ ↓	WHT./GRN.	88
25	QQ	WHT./BLU	92
26	QQ	WHT./RED	93
27	MON. DATA INITIATE	WHT./PURP.	94
28	-28 V	GREEN	
29	+28 V	GRAY	
30	SYNC. ERROR	WHT./GRY.	96
31	9.6 HZ	WHT./BRN	48
32	5 MHZ OUT	TW. PAIR	14
33	5 MHZ RETURN	↓ ↓	1-3
34	PWR RETURN GND	BLACK	1-3
35	STRAP	WHT./BLK.	66
36	100 KHz	TW. PAIR	32
37	(GND RET FOR 36)	↓ ↓	27
38	SW. TO TRANSMIT	RG-174/U	84
39	ANT. T/H	RG-174/U	61
40	CONTR. ROOM T/H	RG-174/U	44
41			
42	HIGH QUALITY GND		
G	GND GUIDE PIN		

34 PIN "AMP" MODULE CONNECTOR

"L8"

NO.	FUNCTION	COLOR CODE	REMARKS
A	Ø REV. OUT	WHT./BLU	P.C. CONN. 46
B	Ø REV. ECHO	WHT./RED	47
C	ADD. INPUT 2^3	WHT./ORN.	50
D	ADD. INPUT 2^2	WHT./GRN.	51
E	ADD. INPUT 2^1	WHT./BRN.	52
F	ADD. INPUT 2^0	WHT./VIO.	53
H	$\overline{\text{CMD. SER. INPUT}}$	WHT./GRY.	55
J	$\overline{\text{CMD. STROBE}}$	VIO.	65
K	CMD. TIME	BLU.	63
L	$\overline{\text{COMMAND CLK.}}$	WHT./BLK.	P.C. CONN. 58
M	GND.	BLK.	
N	GND.	BLK.	
P	CLK. I-3	WHT.	P.C. CONN. 38
R	GND.	BLK.	
S	GND	BLK.	
T			
U			
V	+5 VDC	RED	P.C. CONN 10
W			
X			
Y			
Z			
AA			
BB			
CC			
DD			
EE			
FF			
HH			
JJ			
KK			
LL			
MM			
NN			



REVISION SHEET
BILL OF MATERIALS

REV LTR	DESCRIPTION OF CHANGE	DRAWN BY	DATE	APPRV'D BY	DATE

DATE 3/1/76 BY KW REV. LT. —

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ: VLA
TITLE: DIGITAL DIVIDER ASSEMBLY "L8" MODULE	DWG.NO. A1323026

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

[X] ELECTRICAL [ ] MECHANICAL BOM # A13230Z6 REV _____ DATE 3/75 PAGE 1 OF 2

MODULE # L8 NAME DIGITAL DIVIDER DWG # D13230P6 SUB ASMB _____ DWG # _____

SCHEMATIC DWG # D13230L8 LOCATION _____ QUA/SYSTEM _____ PREPARED BY JOE GRAY APPROVED [signature]

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		N.R.A.O.	A13230Z6	DIGITAL DIVIDER ASS'Y.	~	
2						
3		N.R.A.O.	A13230Z38	CONTROL BOARD ASS'Y.	1	
4						
5		YIKING	3YH50/1JN5	100 PIN CARD EDGE CONN.	1	
6		AMP SPECIAL INDUST.	204186-5	42 PIN MODULE CONN.	1	
7			202394-2	CONNECTOR SHIELD	1	
8			201357-3	34 PIN MODULE CONN.	1	
9			202434-4	CONNECTOR SHIELD	1	
10			204188-1	CRIMP PIN	41	
11			201143-5	COAX CABLE CONN.	6	
12			200833-4	GUIDE PIN	2	
13			203964-6	GUIDE SOCKET	4	
14		AMP SPECIAL INDUST.	202514-1	GROUND GUIDE PIN	2	
15	CR	HEWLETT PACKARD	5082-4860	PANEL MTG. L.E.D.	1	

DATE 3/1/76 [illegible]

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM #A1323076 REV _____ DATE _____ PAGE 2 OF 2

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
16		N.R.A.O.	B13230M81	FRONT PANEL	1	
17			C13230M82	LEFT SIDE PLATE	1	
18			B13050M3	TOP & BOTTOM BAR SUPTS.	2	
19			C13050M7	PERFORATED COVER	1	
20			B13050M17	COVER MTG. HDWRE	2	
21			B13050M32	REAR PANEL	1	
22		N.R.A.O.	B13050M4	REAR GUIDE	2	
23		AMATOM	8158-A-04 40	#4-40 x 5/8" LG. THR'D. STANDOFF	4	
24			#4-40 x .25 LG.	ST. ST'L., FLT. HD. SLOTT. MACH. SCR.	4	
25			#4-40 x .25 LG.	ST. ST'L., PAN HD. SLOTT., MACH SCR.	2	
26			#4-40 x .25 LG.	NYLON, PAN HD. SLOTT. SCR.	1	
27			#6-32 x .25 LG.	ST. ST'L., FLT. HD. SLOTT. MACH. SCR.	6	
28			#6-32 x .38 LG.	ST. ST'L. FLT. HD. SLOTT., MACH. SCR.	2	
29			#6-32 x .62 LG.	ST. ST'L., PAN HD. SLOTT., MACH. SCR.	2	
30			#6-32 x .75 LG.	ST. ST'L., PAN HD. SLOTT., MACH. SCR.	2	
31			#6-32 x .38 LG.	ST. ST'L., HEX SOC. HD. CAP SCR.	2	
32		SOUTHCO	#47-10-204-10	CAP SCR.	2	

3/1/76 HJ

REVISION SHEET
BILL OF MATERIALS

REV LTR	DESCRIPTION OF CHANGE	DRAWN BY	DATE	APPRV'D BY	DATE
A	REMOVED ITEM NO. 12 ITEM NO. 27 WAS 6.2 MEG RESISTOR ADDED ITEM NO 52	J.Gray	4/6/75	RPE	6/4/75
B	ADDED ITEMS NO. 28, 53, 55, & 56 QUANTITIES FOR ITEMS; 16 was 1 reqd. 23 was 3 reqd. 43 was 2 reqd. 44 was 2 reqd. REMOVED ITEM 3	J.S.G.	3/26/76	[illegible]	3/29/76

MICRO

DATE_____ REV. LTR_____

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ: VLA
TITLE: CONTROL BOARD SUB-ASS'Y.	
"L8" DIGITAL DIVIDER MODULE	DWG.NO. A13230738

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☒ ELECTRICAL ☐ MECHANICAL BOM # A13230Z38 REV B DATE 3-26-76 PAGE 1 OF 4

MODULE # L8 NAME DIGITAL DIVIDER MODULE DWG # A13230Z6 SUB ASMB CONTROL BOARD SUB-ASS'Y. DWG # D13230P42

SCHEMATIC DWG # D13230L8 LOCATION _____ QUA/SYSTEM _____ PREPARED BY JOE GRAY APPROVED

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		N.R.A.O.	A13230Z38	DIGITAL DIVIDER CONTR. BD. ASS'Y.	~	
2						
3						
4						
5		E.M.C.	1790F-369	2 WRAP VERSION OF N.R.A.O. WIRE WRAP BOARD, NO. D1352OM1-A	1	
6		COMPONENT MFG. SERVICE	R1008-16	COMPONENT MTG. PLATFORM	2	
7		COMPONENT MFG. SERVICE	R1008-14	COMPONENT MTG. PLATFORM	2	
8		ERIE	8131-(5)-A050-651-193Z	RED CAP CAPACITOR, .019 μf, 50V	20	
9			8121-050-651-473M	,.047 μf	1	
10			8121-050-651-472M	,.0047 μf	1	
11		ERIE	8121-050-651-104M	,0.1 μf	1	
12						
13		CORNING COMPONENT INC.	S10GA	CAPACITOR, 10 μf, 25 V	2	
14		KEMET	C513BD226K	CAPACITOR, 22 μf, 15V	1	
15		ARCO	CM4FD111J03	CAPACITOR, 110 pf	1	

MIC.

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☒ ELECTRICAL ☐ MECHANICAL BOM #A13230238 REV B DATE 3-26-76 PAGE 2 OF 4

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
16		ERIE	8101-050-651-471M	CAPACITOR, 470pf	2	
17	CR	MOTOROLA	1N4733	SEMICONDUCTOR DIODE	1	
18	L	MILLER	9230-28	INDUCTOR, 2.2 μh	1	
19	L	MILLER	9230-44	INDUCTOR, 10 μh	1	
20	R		RCR32271-55	RESISTOR, 270 Ω, 1W	1	
21	R		RCR05331-55	, 330 Ω, 1/8 W	1	
22	R		RCR05510-55	, 51 Ω, 1/8 W	3	
23	R		RCR05102-55	, 1K, 1/8 W	2	
24	R		RCR05472-55	, 4.7K, 1/8 W	1	
25	R		RCR05153-55	, 15 K, 1/8 W	1	
26	R		RCR05473-55	, 47K, 1/8 W	2	
27	R		RCR05564-55	RESISTOR, 560 K, 1/8 W	1	
28	R		RCR05103-55	, 10K, 1/8 W	7	
29	U	FAIRCHILD	9LS109	DUAL J-$\bar{K}$ FLIP-FLOP	1	
30	U		74LS74	DUAL 4-INPUT NAND GATE	1	
31	U		74S74	DUAL D FLIP-FLOP	1	
32	U	FAIRCHILD	93L16	4 BIT BINARY COUNTER	6	

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☒ ELECTRICAL ☐ MECHANICAL BOM # A13230738 REV B DATE 3-26-76 PAGE 3 OF 4

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
33		NAT'L. SEMICONDUCTOR	74L02	QUAD 2 INPUT NOR GATE	2	
34			74LS86	QUAD EX-OR GATE	1	
35			LM360	COMPARATOR	3	
36		NAT'L. SEMICONDUCTOR	555	TIMER	1	
37						
38		TEXAS INSTRUMENTS	74L164	8 BIT SHIFT REGISTOR	3	
39			74L154	4 TO 16 DEMUX	1	
40			7400	QUAD 2 INPUT NAND GATE	1	
41			74LS04	HEX INVERTER	2	
42			74LS08	QUAD 2 INPUT AND GATE	2	
43			74LS21	DUAL 4 INPUT AND GATE	3	
44			74LS73	DUAL J-K FLIP-FLOP	3	
45			74LS20	DUAL 4 INPUT NAND GATE	1	
46			7437	QUAD 2 INPUT DRIVER	1	
47			7438	QUAD 2 INPUT NAND GATE	1	
48			74128	QUAD 50 OHM LINE DRIVER	4	
49		TEXAS INSTRUMENTS	74165	8 BIT SHIFT REGISTER	3	

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☐ MECHANICAL BOM # A13230Z38 REV B DATE 3-26-76 PAGE 4 OF 4

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
50	U	TEXAS INSTRUMENTS	75183	DUAL DIFFERENTIAL DRIVER	1	
51	U	↓	74198	8 BIT SHIFT REGISTER	1	
52	U	TEXAS INSTRUMENTS	74L500	QUAD 2 INPUT POS. NAND GATE	1	
53	U	↓	74265			
54						
55	R		RCR05104-S5	RESISTOR, 100K, 1/8W	1	
56	R		RCR05221-S5	〃 , 220Ω, 1/8W	1	
57						
58						