VLA TECHNICAL REPORT #16

DIGITAL DELAY AND MULTIPLIER SYSTEM TWO ANTENNA PROTOTYPE

OBSERVER'S MANUAL

A. M. Shalloway and R. P. Escoffier

May 1975

I. INTRODUCTION

The digital delay and multiplier system, under instructions from the on-line computer system:

a. accepts digitized data from the samplers,

b. delays the data,

c. cross multiplies the data,

d. preprocesses the data,

e. and transmits the data to the on-line computer system.

This report will describe, in block diagram form, the system's theory and operation. Although the operation is completely automatic once the power switches are turned on, it is felt that many observers will want to know the systems theory of operation to know its influence on their total VLA results; and if there is a question about the systems operation, the observer may want to know how to run some of the diagnostic tests.

This report is divided into six sections:

a. Introduction

b. Specifications

c. Digital Delay System

d. Multiplier System

e. System Controller

f. Appendix

There are only two main interfaces, the input from the samplers and the input-output to the on-line computer system. The only other connections are a 100 MHz clock and a data invalid signal from the VLA L2 and L8 modules in control room rack M. The data invalid signal will henceforth, in this report, be referred to as blanking time (BT) signal, as that is its main purpose in the system.

II. SPECIFICATIONS

1. Detailed Specifications

Number of Antennas: 2

Bandwidth per Signal: 50 MHz (actual input = 49 MHz)

Multiplication Rate: 100×10^6 per second

Signal Composition: 2 bits, 3 level

Sensitivity Relative to a Continuous Correlator: 0.81

Delay Resolution: Digital = 10 ns

Analog (before samplers) = 625 ps

Range of Delays: 70 ns to 163.83 ms

Timing Rates and Periods: Maximum rate at which delay lines may be changed = 19.2 times per second (52.08333 ms period).

Continuous Integration Period: 50.48 ms.

Blanking Time: 1.60333 ms.

Maximum number of Integration Periods that can be stored in System Controller: 6 (13 with modification of System Controller).

Dump Time to Computer: n(52.08333) where n = any integer from 1 to 6. (1 to 13 with modification of system controller).

2. Breakdown of Antenna Outputs, Delays and Multipliers

Antennas: Each antenna will produce two right (R) and two left (L) polarization outputs. The two signals for each polarization will consist of two adjacent 49 MHz bandwidth signals (hereafter referred to as A and B). Each signal produces a sine (S) and cosine (C) output from the samplers. Thus there are a total of sixteen signals (two bits, three levels each) to be delayed:

A1LS B1LS A1RS B1RS A1LC B1LC A1RC B1RC
A2LS B2LS A2RS B2RS A2LC B2LC A2RC B2RC

Delays: Each sampler signal output requires two delay cards - one for each bit. Because the sine and cosine signals are generated just prior to the samplers, associated sine

2. (continued)

Delays: (continued)

and cosine signals (e.g. A1LS and A1LC) from the same antenna receive the same delay. Therefore in the digital delay system there are 8 different delays possible; thus the system is designed with 8 control units which control the delay for 16 delay lines which consist of 32 delay cards (one card per bit).

Multipliers: The following multiplications are provided:

SIN x COS for each signal - total of eight.

SELF MULTIPLICATIONS (e.g. A1RS x A1RS) for each signal - total of sixteen.

CROSS MULTIPLIERS - consist of the following sets for each of the 49 MHz bandwidths (A & B):

1RS x 2RS 1RS x 2RC 1LS x 2LS 1LS x 2LC

1RC x 2LC 1RC x 2LS 1LC x 2RC 1LC x 2RS

Racks: 2. One contains the delays, multipliers and integrators. The other contains the System Controller and the samplers.

III. DIGITAL DELAY SYSTEM

The Digital Delay System provides variable delays for each of the 32 digital outputs of the sampler system. Each of the sampler digital outputs is a 100 MHz data rate ECL logic signal. The logic to provide 0 to 163.83 μs of delay in 10 ns increments for a single 100 MHz logic signal is contained on a single multilayer delay line card. The 32 delay line cards and associated control logic cards are interconnected on two multilayer mother boards. See Figure III-1.

The sampler outputs consists of groups of 4 signals that correspond to two bits each for two quadrature signals. Since these four digital outputs have a common analog path equal delays are provided thru the four corresponding delay line cards. The delay programming signals for four delay line cards thus come from common control logic. The logic required to provide control for two independent groups of four delay line cards is contained on a single multilayer PC card. This card accepts, for each quad of delay line cards, a 20-bit delay program word that contains 14 bits of delay information and several bits of program data. The 14 bit delay word is a binary progression to program the 0 to 163,830 ns delay with the LSB being weighted at 10 ns. Each delay line has a minimum thru-put time of approximately 40 μs, thus a delay line thru-put varies from 40 to 203.83 μs in 10 ns steps.

Each delay line card contains ECL, TTL, and MOS logic to optimize cost and performance, bulk delay being provided in low speed parallel path MOS logic, intermediate resolution at higher speed TTL circuits and the fine 10 ns timing accomplished in ECL logic. Each delay line card has a single 100 MHz logic undelayed input port and two auxiliary digital inputs to allow system testing capacity and self healing capability. Delay card outputs include an undelayed output to allow self test capability and eight parallel delayed digital outputs to provide fan out to the many multiplier loads.

The self test and self healing feature is accomplished by having a quad of unassigned delay line cards to verify correct operation. The test delay line inputs are connected through an input multiplexer to the undelayed output of any given dedicated delay line and its output checked against that of the dedicated delay line. If error is indicated the test delay line is itself checked against the other delay lines and if satisfactory operation is indicated the delayed output of the test delay line is substituted for that of the delay line under test. The cabling delays encountered in such an arrangement require that the delay used to program the test delay line be smaller by a

constant number than the delay used to program the delay line under test, hence a minimum delay value equal to this constant (70 ns) is required by the delay system and the delay range of the delay system is more accurately stated as 70 to 163830 ns in 10 ns increments.

Included in the self test circuitry is a multiplier test capacity. The cabling used to carry data, from test delay lines, that is to be substituted for that of detected bad delay lines can also be used to carry the logic data of a pseudorandom data generator. By substituting this data for all delay line outputs all multipliers can be made to see identical data inputs and their outputs checked for uniformity. Thus all multipliers, including the sine-cosine multipliers, will produce the same integration results. The 8-wired self multipliers are an exception to the above statement since wired self multipliers have only one set of inputs and their integration result, during multiplier test, will be themselves uniform but different from all other multiplier results.

Advantage is also taken of the fact that all delayed outputs of the delay system appear at the GO/NO GO detector of the delay line self test circuitry. The sine-cosine outputs of each antenna are multiplied together at this point to provide calibration information for the VLA computer. Since the sine-cosine multiplier results are not needed continuously only two sine-cosine multipliers exists and their inputs are time shared between the antennas. These two sine-cosine multipliers are always connected in parallel and provide redundant information about the same sampler.

In general a 300 ms dump time is used and between each dump time the four delay line cards of one of the eight samplers is paralleled and checked by the test delay lines and their sine-cosine multiply product integrated. During the next dump time the next four delay line cards in line are checked and their sine-cosine product integrated. A closed loop of 27 sets of four delay line cards around which the test delay lines circulate exists in the hardware. In the two antenna system only eight of these 27 stops have active data; thus delay line test and sine-cosine integration produce valid information 30% of the time. If a bad delay line is detected and exchanged, the sine-cosine cycle is still performed and this information is not lost.

If more than one delay line is flagged as defective by the test delay lines in their circulation thru the system the System Controller will take this as an indication that the test delay line is itself defective and substitution is inhibited.

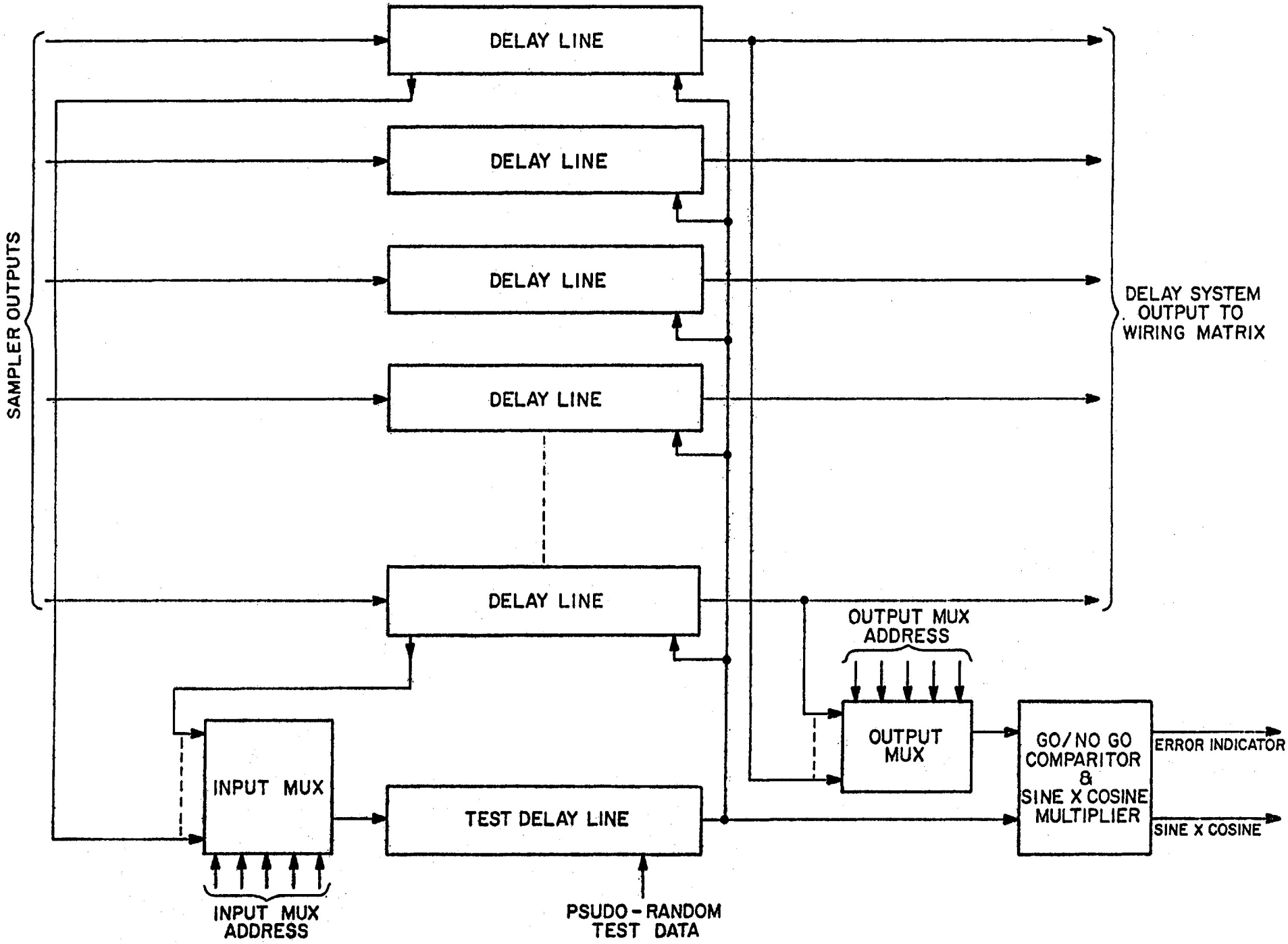

DELAY LINE
DELAY LINE
DELAY LINE
DELAY LINE
DELAY LINE
SAMPLER OUTPUTS
DELAY SYSTEM OUTPUT TO WIRING MATRIX
OUTPUT MUX ADDRESS
OUTPUT MUX
GO/NO GO COMPARITOR & SINE X COSINE MULTIPLIER
ERROR INDICATOR
SINE X COSINE
INPUT MUX
TEST DELAY LINE
INPUT MUX ADDRESS
PSUDO-RANDOM TEST DATA

FIGURE III-1

IV. MULTIPLIER SYSTEM

A two bit, three level digital signal is produced by the samplers. For details on this type of signal, reference should be made to:

Australian Journal of Physics; Correlators With Two-Bit Quantization, B.F.C. Cooper; 1970, 23, p.521-7.

The output code of the samplers indicate that the signal is in one of three levels as follows:

LEVEL OF SIGNAL(S)	ASSIGNED VALUE	OUTPUT CODE OF SAMPLER		
			M A1	L A0
S > +0.612 RMS of Signal	+1		0	1
-0.612 RMS < S < 0.612 RMS	0		0	0
-0.612 RMS > S	-1		1	0

Arbitrary Designations:
M=MSB L=LSB
A= Antenna Number

The value 0.612 was obtained from the above reference along with the assigned values of +1, 0 and -1 to provide the best combination of digital simplicity and high receiver sensitivity.

The output code is chosen arbitrarily to simplify the logic. A normal multiplication table for the above would be:

ANT. A → ANT. B ↓	-0	0	+1
-1	+1	0	-1
0	0	0	0
+1	-1	0	+1

To perform this multiplication and integrate the results would require reversible counters. To simplify the system, an altered multiplication table is used in which +1 is added to each multiplication result:

	A1 A0 (output code) →	10	00	01
B1 B0 (output code) ↓	ANT. A → ANT. B ↓ (output value)	-1	0	+1
10	-1	2	1	0
00	0	1	1	1
01	+1	0	1	2

The control section can correct for this change simply:

$$V'_n - V_s = V_n \qquad \text{(IV-1)}$$

where V'_n = results of integration of multiplier N after a period T,

V_s = number of multiplications performed (also number of samples taken) during T, and

V_n = results desired; that is, the results that would have been obtained with the unmodified multiplication table.

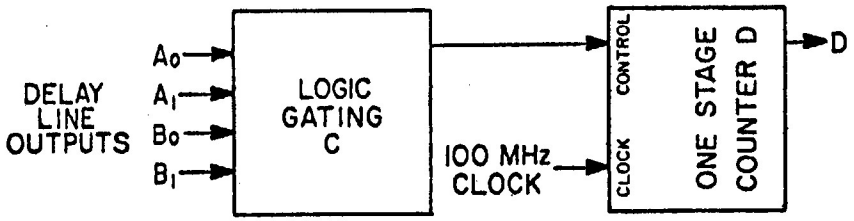
A block diagram of the multiplier card is shown in Figure IV-1A. Each multiplier card contains 14 multipliers. One multiplier is a self multiplier and thirteen multipliers are cross multipliers. This arrangement and the arrangement of the mother boards in the system were designed for the final system of 27 antennas. Because of this, an optimum arrangement of multipliers for two antennas is not obtained, and there are many redundant and illegal multiplications generated, which are ignored.

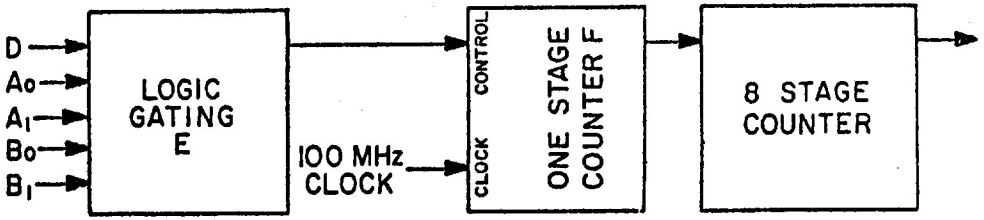
A block diagram of one multiplier and its integrator is shown in Figure IV-1B. As can be seen, the first seven-least significant-stages of the integrator are thrown away. Nineteen stages - one of which is considered an overflow-bit are saved and sent to the core computer.

With a minimum integration period of 50.48 ms:

$$\text{RMS NOISE} = \sqrt{fs \cdot I} = \sqrt{(10 \times 10^7)(50.48 \times 10^{-3}} = 2247 \qquad \text{(IV-2)}$$

where fs = sampling frequency, I = integration period.



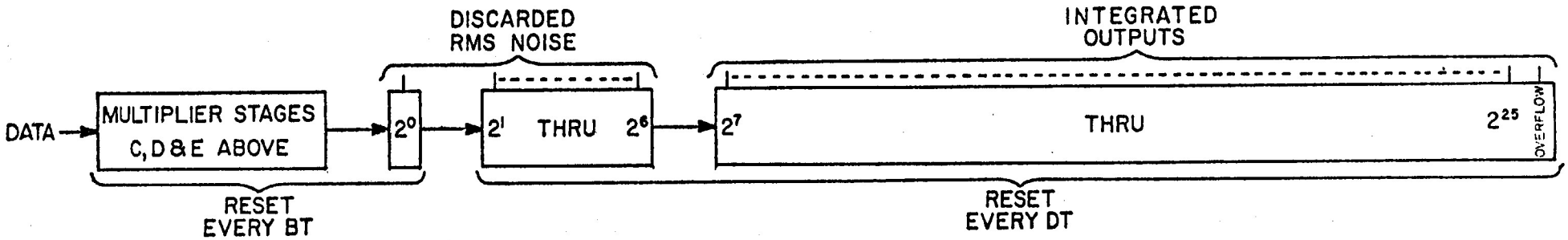


$$C = \overline{A_0 \cdot A_1} + \overline{B_0 \cdot B_1}$$

$$E = (\overline{A_0 \cdot A_1} + \overline{B_0 \cdot B_1}) \cdot D + A_0 \cdot B_0 + A_1 \cdot B_1$$

NOTE: · = LOGIC "AND"; + = LOGIC "OR"; A LOGIC 1 (OR TRUE) ON THE COUNTER COUNTROL CAUSES IT TO COUNT WHEN A CLOCK OCCURS.

FIGURE IV-1A



NOTE: IF $2^0 = 1$ AT THE BEGINNING OF BT, THERE WILL BE A CARRY TO 2^1 WHEN BT RESETS 2^0.

FIGURE IV-1B

MULTIPLIERS & INTEGRATORS

$$2247 > 2^{11} \qquad \text{(IV-3)}$$

Therefore, the eleven least significant bits of the counters (integrators) contain mostly noise. By throwing away only seven of the least significant bits, we are introducing very little error in the final results.

As shown in Figure IV-1B, the two counter flip-flops associated with the multiplier are reset every BT. The remaining counters are reset each DT after the data is removed from the counters. The Vs counters are not reset at any time, their inputs are merely gated off during BT and DT. The Vs counter is a 19 stage counter (one of which is considered an overflow bit) fed by the system 100 MHz clock.

In systems beyond the prototype, some multiplier outputs will have to be negated because of the resultant multiplication received due to hardware considerations as shown in the following table:

MRS x NRC = - NRS x MRC
MLS x NLC = - NLS x MLC
MRC x NLS = - NLC x MRS
MLC x NRS = - NRC x MLS

where M and N represent two different antennas.

In the prototype this need only be done on certain redundant multipliers which are not normally used. When the multipliers are negated, the result sent to Core computer is in one's complement instead of two's complement. The reasoning for this and for the fact that the Vs counteres are not reset are covered in a memo dated March 6, 1975, to A. Shalloway from B. Clark, Subject: Systematic Effects in the VLA Correlator.

If pulsar observations are to be made with the VLA, certain limitations must be considered. The following statements assume that the necessary hardware changes could be made to change the VLA timing beyond those listed in the specifications of Part II. To send a full set of multipliers associated with 27 antennas from the delay-multiplier system to the computers require approximately 25 ms. Therefore, in the final system, unless a smaller number of multipliers is acceptable, the minimum integration period would be 25 ms. In the prototype, the transfer of multipliers to the computers is less than 2.5 ms. If we consider a minimum integration time of 5 ms - which will cover practically all pulsars - we obtain an RMS noise of:

$$\text{RMS NOISE} = \sqrt{(10 \times 10^{7})(5 \times 10^{-3})} = 710.5 > 2^{9} \qquad \text{(IV-4)}$$

Therefore, since we throw away seven bits, observations could be made but with some error influencing the final results.

V. SYSTEM CONTROLLER

The System Controller (SC) is a computer which can be programmed to a limited extent by changing programmable read only memories (PROM's). The SC is electrically between the sampler-delay-multiplier systems and the on-line computing system. It performs the following control, test and display functions:

1. CONTROL:

a. Distributes delay values to delay line control cards and samplers every blanking time (BT).

b. Disables delay card outputs as required.

c. Inverts sampler output signals as required.

d. Detects delay line GO/NO GO errors and transmits the data to the front panel and the core computer. Makes a decision about the cause of the error, and if it is one or more delay line cards associated with one output from one antenna, substitutes the test delay line(s) for the defective line(s).

e. Accepts the integrated data from the multipliers, and Vs counters every dump time (DT) and stores the data.

f. Checks the Vs data to upper and lower limits. If the Vs data is out of specification, the theoretical value, which the data should be for the integration period being used, is substituted for the bad data.

g. Subtracts the Vs value from each multiplier value. This returns the multiplier value to normal as indicated by equation IV-1.

h. Transmits all necessary data to the core computer once per DT.

i. Receives from the core computer, the delays and other data once per BT.

2. TEST:

Tests may be carried out by use of the CRT terminal or the Monty computer. A special message from the Boss computer to the SC will turn over the CRT terminal input of the SC to the Monty computer (see Appendix). Monty computer can then carry out the tests, and the communications between the Monty computer and the SC can be monitored by the SC's CRT terminal if it is put "on-line".

A summary of the tests possible are:

a. Enter a control word (computer word 0, see Appendix).

b. Enter delays into one or more delay lines and samplers.

c. Lock up test delay lines so they continually check one set of delay lines.

d. Replace from one to four delay cards of a set-associated with one output from one antenna-with the test delay cards.

e. Run a multiplier test. In this test a random noise generator is fed into all multipliers and a known output is obtained.

f. Runs a delay line test by varying the delay in a known fashion to test all possible combinations of delay. This may be done on one delay line set continuously; that is, the test is run over and over again. It may also be set to rotate to the next delay line set as soon as the test is completed on the first set, and continue this procedure until stopped.

Certain tests are running all the time in normal operation: These are:

a. Comparison of test delay lines with operating delay lines as described in Section III.

b. Tests every DT of Vs values to see that they are within specified limits.

c. Parity checks - VLAC to SC, SC to VLAC, temporary storage to SC, and CRT terminal to SC.

d. Overflow of Vs and multiplier counters.

e. System monitor section of the SC, checks all voltages, 100 MHz clock amplitudes and temperatures throughout the racks.

f. SC clock oscillator. If this oscillator misses a cycle, a monitoring system switches over to a spare oscillator and the system continues to operate.

As part of the testing capabilities, the CRT terminal can display much of the information contained in the delay-multiplier system. The front panel of the SC is designed as a diagnostic device only. If an error is detected, one of the lights in the column of lights on the left will light up, the ring of lights around the alarm will light up and the alarm will sound. This will indicate the area of the problem and the CRT terminal display can then be used to pinpoint the problem. To stop the alarm but leave the lights on, depress the switch below the alarm. To test the alarm and lights depress the "indicator test" button in the left column of switch-lights. After a fault has been

repaired, the lights and stored indicating data can be reset by depressing and holding the appropriate switch in the left column while simultaneously depressing momentarily the "function reset interlock" switch on the right side of the panel. As soon as the "function reset interlock" light goes out, the switch in the left column may be released.

A summary of the CRT terminal displays possible are:

a. Control word
b. Multipliers
c. Delays
d. System Monitor
e. GO/NO GO Data
f. VLAC → SC Parity Error Address
g. Addresses of Multipliers Requested

A switch on the left of the power control panel, just above the system controller, connects the CRT terminal to either the SC input or the Monty computer input. A light above the switch indicates the connection. If Core computer connects the Monty computer to the SC's CRT interface, it over-rides the switch and both the upper and lower portion of the light is illuminated.

CRT terminal entries required for all of the previously described tests and displays are covered in the specification in the index. This specification also describes all data transferred between the VLAC and the SC.

NATIONAL RADIO ASTRONOMY OBSERVATORY
Charlottesville, Virginia
VERY LARGE ARRAY PROJECT

SPECIFICATION NO.: A13500N3, Rev. B

NAME: Communications Between Digital Delay-Multiplier System and VLA Synchronous Computers

DATE: May 8, 1975

PREPARED BY: Curtis M. Holloway APPROVED BY: J. Weimer

DESCRIPTION:

All data between the Digital Delay-Multiplier System and the VLA Synchronous Computer (VLAC) will be controlled by a unit referred to as the System Controller (SC), which is the interface into and out of the Delay-Multiplier System. The only exceptions are monitored from the Samplers and, in the two antenna systems, one analog signal which is a combined total power signal. The exceptions will not be covered by this specification.

A block diagram of the communication system is shown in Figure 1. Two System Controllers (SC) are shown -- one for each 50 MHz system. In the prototype -- two antenna system -- there is only one SC, and all delays and multipliers are handled as though they were in the left polarization rack.

The System Controller CRT can be switched between the System Controller and Monty Computer. Thus the CRT can be used to communicate with the computer system in the same manner as other CRT's in the VLA. A CRT output of Monty Computer can also communicate directly with the SC. This connection is made whenever bit 2^2 (C) of the first word sent by Boss Computer to SC is a 1. This mode allows the on-line computer system to control the SC tests in the same manner that the SC's CRT terminal controls tests. The data input to the SC's CRT terminal controls tests. The data input to the SC's CRT input required for each test is listed in Table 6. Table 5 shows how Monty Computer could receive data back through its CRT input; however, this mode is not required by the on-line computer system since the same data is available to Core Computer via its connection to the SC. Table 7 is the format for Table 5.

To operate the SC in test mode, Boss Computer should send two complete sets of data as shown in Tables 2 and 4. In addition to delay data, the two sets should contain the following:

First Set of Data:

Word 0: A=1, B=1, C=1

Words 55 ····: Multiplier Sets Desired During Test

Second Set of Data:

Word 0: A=0, B=0, C=1

DO NOT SEND WORDS 55 THRU 405. (55 thru 60 in case of prototype).

Each of the communication networks to the Core computers and from the Boss computer consists of three signals:

1. Clock - maximum of 5 MHz
2. Data
3. Ready Line

The inputs to Core Computers are double buffered and when one buffer is full and the second begins receiving data the Ready Line changes state to "Not Ready". The sending block continues to send to the end of the present word, then stops and waits for the line to go "Ready" again.

Each of the three lines are twisted pair coaxial cable (RG-22) which is driven and received differentially with ECL logic. The transmission system has been tested with 500 ft. of cable and operation was excellent with considerable safety margin.

Tables 1 through 4 list all data transmitted to and from the System Controller, excluding the CRT, as follows:

Table 1 - Final System	-SC to VLAC
Table 2 - Final System	-VLAC to SC
Table 3 - Two Antenna System	-SC to VLAC
Table 4 - Two Antenna System	-VLAC to SC

The following rules are to be observed:

1. No transmission of data from VLAC to SC is to occur during blanking time. Therefore during blanking time the ready line from SC to VLAC is held "not ready".
2. Data transmission from VLAC to SC can be absorbed at the maximum rate (5 MHz clock rate) by the SC.

3. The block of data (VLAC to SC) shown in Tables 2 and 4 must be sent complete between two adjacent blanking times. This includes the first block sent before an observation is begun.
4. After a dump time, data from SC to VLAC may be taken at any rate and may extend across blanking times, but must be completed at least 2 microseconds prior to the beginning of the next dump time. Dump Time refers to the blanking time following completion of an integration period by the multipliers. Blanking time is referred to in the VLA system as "data invalid time" (1.603 ms).
5. Format of data in both directions:

   $000000, P, D_{23}, D_{22} \cdots\cdots\cdots D_1, D_0, 1$

   P = parity D_n = data D_o = LSB D_{23} = MSB 1 = start bit

   Transmission is serial, starting at "1". A minimum of one clock time will exist between words. The clock from SC to VLAC will be continuous (5 MHz, 80 ns positive, 120 ns negative - negative going edge centered on data bit at transmitter). The clock from VLAC to SC same as above except discontinuous - 32 clock pulses per 32 bit data word. The data word length and number of clock pulses may be as short as 30, leaving off the last two zeros.
6. For each observation the VLAC will send a block of data between every set of blanking times, the first being before the blanking time which precedes the start of an observation (integration) and the last being before the blanking time which follows the end of the observation (integration).
7. The relationships between when the different sets of data sent to the VLAC are obtained and to what they apply is shown in Figure 2.
8. The delay data should never contain a delay value of less than 70 ns.
9. Data in the tables which indicate errors - such as parity, overflow, etc. - are indicated thus:

   NO ERROR = 0 ERROR = 1

FINAL SYSTEM

SYSTEM CONTROLLER ⟶ VLAC (CORE A & B)

CORE INPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION	SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
0	0 0 0 G H_4 L_4 H_3 L_3 H_2 L_2 H_1 L_1 S_7 S_5 S_4 P_2 P_1 P_0 F E D C B A	A=0 UPDATE DATA-EVERY 50 ms. A=1 INITIATION DATA-AT START OF OBSERVATION B=0 STOP OBSERVATION ON NEXT BT. B=1 START OR CONTINUE OBS. ON NEXT BT. C=1 COMPUTER TEST-CONTROLLED BY MONITY COMPUTER THROUGH CRT TERMINAL INPUT. D=1 PARITY ERRORS RECEIVED BY VLAC E=1 OBSERVATION STOPPED BECAUSE OF TOO MANY PARITY ERRORS F=1 DELAY-MULTIPLIER SYSTEM LOCAL TEST P_2, P_1, P_0 = DUMP PERIOD - BINARY NUMBER 1=50; 2=100; 3=150; 4=200; 5=250; 6=300 ms. S_4=1 DISABLE NEGATIVE SAMPLER S_5=1 DISABLE POSITIVE SAMPLER S_7 - SPARE SAMPLER BIT - ALWAYS = 0 G=0 SET 1 V_S's USED G=1 SET 2 V_S's USED	0	0
	L OR H=0 DENOTES V_S COUNTER IN TOLERANCE. L=1 COUNTER BELOW LOW TOLERANCE H=1 COUNTER ABOVE HIGH TOLERANCE L_1, H_1 REFER TO 1 V_S L_2, H_2 " " 2 V_S ETC.			
	NOTE: IF V_S IS WITHIN TOLERANCE, G ALTERNATES BETWEEN 0 & 1 BETWEEN OBSERVATIONS.			
1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	SPARE WORD	1	1
2	0 0 0 C 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	SPARE WORD	2	2
3	0 0 0 0 0 D_{18} D_{17} D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	THEORETICAL VALUE OF V_S.	3	3
4	0 0 P ϕ S D_{18} — — — — — — — — — — — — — — — — — — D_0	SET 1-(LS×LS) V_S SET 2-(LC×RS) V_S	4	4
5	0 0 P ϕ S D_{18} — — — — — — — — — — — — — — — — — — D_0	SET 1-(LC×RC) V_S SET 2-(LS×LC) V_S	5	5
6	0 0 P ϕ S D_{18} — — — — — — — — — — — — — — — — — — D_0	SET 1-(RS×RS) V_S SET 2-(RC×LC) V_S	6	6
7	0 0 P ϕ S D_{18} — — — — — — — — — — — — — — — — — — D_0	SET-1-(RC×LS) V_S SET 2-(RS-RC) V_S	7	7
8	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 A_4 A_3 A_2 A_1 A_0	ANTENNA USED IN S×C MULTIPLICATION - BINARY	10	8
9	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	SPARE WORD	11	9
10	0 0 0 0 0 0 — — — — — — — — — — — — — — — — — — 0	SPARE WORD	12	10
11	0 0 0 0 0 0 — — — — — — — — — — — — — — — — — — 0	SPARE WORD	13	11
12	0 0 P ϕ S D_{18} D_{17} D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	MULTIPLIER 1 L NLS×NLC	14	12
13	0 0 P ϕ S D_{18} — — — — — — — — — — — — — — — — — — D_0	MULTIPLIER 2 L NLS×NLC	15	13
14	0 0 P ϕ S D_{18} — — — — — — — — — — — — — — — — — — D_0	MULTIPLIER 1 R NRS×NRC	16	14
15	0 0 P ϕ S D_{18} — — — — — — — — — — — — — — — — — — D_0	MULTIPLIER 2 R NRS×NRC	17	15

SIN × COSINE MULTIPLIERS

NOTE ⟶ IN all computer words from 12 through 3039 the D_{18} bit is obtained by using the overflow bit to form a 19 bit Vn word before subtracting V_0. ϕ = OVERFLOW P = PARITY (OBTAINED DURING TEMPORARY STORAGE TO SYSTEM CONTROLLER — TRANSMISSION)

S = SIGN

REV. B 5-7-75 amc A.M. SHALLOWAY

REV. A 11-12-74 [illegible] 6-11-74

TABLE 1

SYSTEM CONTROLLER → VLAC (CORE A & B)

CORE INPUT COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION		SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
16	0 1 P Ø S D_{18} D_{17} D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	1RS x 1RS	SELF MULTIPLIERS	20	16
17	0 1 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_1	1RS x 1RS		21	17
18	0 1 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	1LS x 1LS		22	18
19	0 1 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_1	1LS x 1LS		23	19
20	0 1 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	1RC x 1RC		24	20
21	0 1 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_1	1RC x 1RC		25	21
22	0 1 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	1LC x 1LC		26	22
23	0 1 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_1	1LC x 1LC		27	23
24	0 1 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	2RS x 2RS		30	24
				⋮	⋮
231	0 1 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	27LC x 27LC		347	231
232	1 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	1RS x 2RS	MULTIPLIER SET 32	400	256
233	1 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_1	1RS x 2RC		401	257
234	1 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	1LS x 2LS		402	258
235	1 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_1	1LS x 2LC		403	259
236	1 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	1RC x 2LC		404	260
237	1 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_1	1RC x 2LS		405	261
238	1 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	1LC x 2RC		406	262
239	1 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_1	1LC x 2RS		407	263
240	1 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	1RS x 3RS	MULTIPLIER SETS 33 THRU 382 CROSS MULTIPLIERS	410	264
				⋮	⋮
3039	1 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	26LC x 27RS		5767	3063
3040	1 1 0 0 S_6 A D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 S_3 S_2 S_1 S_0	D_{13}-D_0 = DELAY-10ns RESOLUTION-BINARY		6000	3072
	NOTE: Word No. 3040 = LEFT ANT. 1	S_3-S_0 = DELAY-625ps RESOLUTION-BINARY		⋮	⋮
	Word No. 3041 = RIGHT ANT. 1	S_6=0 NON-INVERT } { SAMPLER INVERT SIGNAL			
	Word No. 3042 = LEFT ANT. 2	S_6=1 INVERT }			
	Word No. 3043 = RIGHT ANT. 2 & ETC.	A=0 ENABLE DELAY LINE OUTPUT			
3093	1 1 0 0 S_6 A D_{13} — — — — — — — — — — — — — D_0 S_3 S_0	A=1 DISABLE DELAY LINE OUTPUT		6065	3125
3094	1 1 0 0 0 A D_{13} — — — — — — — — — — — — — D_0 T T T T	D_{13}-D_0 = LEFT TEST DELAY LINE DELAY		6066	3126
3095	1 1 0 0 0 A D_{13} — — — — — — — — — — — — — D_0 T T T T	D_{13}-D_0 = RIGHT TEST DELAY LINE DELAY		6067	3127

TABLE 1

REV. B 5/7/75 amc A.M. SHALLOWAY
REV. A 11/12/74 amc 6-11-74

FINAL SYSTEM

SYSTEM CONTROLLER → VLAC (CORE A & B)

CORE INPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION	SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
3096	1 1 0 0 0 0 0 0 0 0 0 0 $X_M^C X_L^C X_M^S X_L^S$ 0 0 0 $M_4 M_3 M_2 M_1 M_0$	M_4-M_0 = LEFT S/N INPUT MULTIPLEXER ADDRESS	6070	3128
	NOTE: IF T (IN WORD NOS. 3094 & 3095) = 1 ALL EXCHANGE DATA BITS = 1. X's ARE EXCHANGE DATA BITS FOR ANTENNA ASSOCIATED WITH INPUT MUX. ADDRESS. $X_M^C X_L^C X_M^S X_L^S$: 0 0 0 0 / 0 0 0 0 / 0 0 0 0 / 0 0 0 0 / 0 0 0 0	NOTE: S = SIN C = COS L = LSB M = MSB		
		M_4-M_0 = RIGHT S/N INPUT MULTIPLEXER ADDRESS		
		M_4-M_0 = LEFT COS INPUT MULTIPLEXER ADDRESS		
		M_4-M_0 = RIGHT COS INPUT MULTIPLEXER ADDRESS		
		M_4-M_0 = LEFT S/N OUTPUT MULTIPLEXER ADDRESS		
		M_4-M_0 = RIGHT S/N OUTPUT MULTIPLEXER ADDRESS		
		M_4-M_0 = LEFT COS OUTPUT MULTIPLEXER ADDRESS		
3103	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 M_4 — — M_0	M_4-M_0 = RIGHT COS OUTPUT MULTIPLEXER ADDRESS	6077	3135
3104	1 1 0 0 0 0 0 0 G F_1 F_0 E D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	SYSTEM MONITOR DATA	6100	3136
	G = 0 POWER ON; G = 1 POWER OFF (DOWN) } DELAY MULTIPLIER RACK	D = 12 BIT BINARY ABSOLUTE VALUE DATA		
		E = 0 WITHIN LIMITS E = 1 OUT OF LIMITS		
3167	1 1 0 0 0 0 0 0 G F_1 F_0 E D_{11} — — — — — — — — — — — D_0	F_0 F_1 BINARY NUMBER INDICATES WHICH LIMIT HAS BEEN EXCEEDED	6177	3199
3168	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 C_1 C_0 S_1 S_0	GO/NO-GO RESULTS FROM DELAY COMPARATOR	6200	3200
		S = SIN - L & MSB C = COS - L & MSB		
		S OR C = 0 = GO S OR C = 1 = NO-GO		
		EVEN COMPUTER WORDS = LEFT ODD = RIGHT		
3221	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 C_1 C_0 S_1 S_0		6265	3253
3222	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	SPARE WORDS	6266	3254
3231	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		6277	3263
3232	1 1 0 0 0 0 0 0 0 0 0 0 B_2 B_1 B_0 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	A_8-A_0 = COMPUTER WORD NO. (STARTING AT 0) OF WORD(S) VLAC → SC WITH PARITY ERRORS	6300	3264
	NOTE: A MAXIMUM OF 64 ERRORS CAN BE INDICATED.	B_2, B_1, B_0 = BLANKING TIME IN WHICH ERROR OCCURRED - BINARY 1 THRU 6.		
3295	1 1 0 0 0 0 0 0 0 0 0 0 B_2 B_1 B_0 A_8 — — — — — — — — A_0		6377	3327
3296	1 1 0 1 0 0 0 0 0 0 0 0 0 0 L C_8 C_7 C_6 C_5 C_4 C_3 C_2 C_1 C_0	C_8-C_0 = MULTIPLIER SETS DESIRED BY VLAC. EACH NUMBER = 8 MULTIPLIERS	6400	3328
MAX ↓		NOTE: 32 = 1×2 33 = 1×3 34 = 1×4 ETC.	MAX ↓	MAX ↓
3646	1 1 0 1 0 0 0 0 0 0 0 0 0 0 L C_8 — — — — — — — — C_0	MAXIMUM OF 351 SETS OF CHANNELS	7136	3678
		L = 1 IN LAST WORD.		
LAST WORD	1 1 1 1 0 0 0 0 0 0 0 0 0 0 T_8 T_7 T_6 T_5 T_4 T_3 T_2 T_1 T_0	T_8-T_0 = TIME IN TENS OF SECONDS TO END OF OBSERVATION - BINARY	7137	3679
	NOTE: Four 1's in bit positions 20, 21, 22 & 23 indicate the last word of transmission.			

REV. B 5/7/75 ams A.M. SHALLOWAY

REV. A 11/12/74 ams

TABLE 1

[redacted] FINAL [redacted] SYSTEM

VLAC (BOSS) ⟶ SYSTEM CONTROLLER

BOSS OUTPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION
0	0 0 0 1 0 0 0 0 0 0 0 0 S_7 S_5 S_4 P_2 P_1 P_0 F E D C B A	A=0 UPDATA DATA — EVERY 50mis. A=1 INITIATION DATA — AT START OF OBSERVATION. B=0 STOP OBSERVATION ON NEXT BT. B=1 START OR CONTINUE OBS. ON NEXT BT. C=1 COMPUTER TEST-CONTROLLED BY MONTY COMPUTER THROUGH CRT TERMINAL INPUT. P_2, P_1, P_0 = DUMP PERIOD - BINARY NUMBER 1=50; 2=100; 3=150; 4=200; 5=250; 6=300 ms. S_7 - SPARE SAMPLER BIT - ALWAYS=0 S_5, S_4 = SAMPLER TEST CODE S_4=DISABLE NEGATIVE SAMPLER S_5=DISABLE POSITIVE SAMPLER
1	0 0 1 0 S_6 A D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 S_3 S_2 S_1 S_0	D_{13} - D_0 = DELAY - 10ns RESOLUTION - BINARY S_3 - S_0 = DELAY - 625ps RESOLUTION - BINARY S_6=0 NON-INVERT, S_6=1 INVERT } SAMPLER INVERT SIGNAL A=0 ENABLE DELAY LINE OUTPUT A=1 DISABLE DELAY LINE OUTPUT
	NOTE: WORD NO. 1 = LEFT | ANT. 1 WORD NO. 2 = RIGHT | ANT. 1 WORD NO. 3 = LEFT | ANT. 2 WORD NO. 4 = RIGHT | ANT. 2 & ETC.	
54	0 0 1 0 S_6 A D_{13} — — — — — — — — — — — — — — D_0 S_3 — S_0	
55	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 L C_8 C_7 C_6 C_5 C_4 C_3 C_2 C_1 C_0	C_8 - C_0 = MULTIPLIER SETS DESIRED BY VLAC EACH NUMBER = 8 MULTIPLIERS. NOTE: 32=1×2 33=1×3 34=1×4 ETC. MAXIMUM OF 351 SETS OF CHANNELS.
MAX 405	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 L C_8 — — — — — — — — C_0	L=1 IN LAST WORD
LAST WORD	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 T_8 T_7 T_6 T_5 T_4 T_3 T_2 T_1 T_0	T_8 - T_0 = TIME IN TENS OF SECONDS TO END OF OBSERVATION - BINARY.

NOTE: COMPUTER WORDS 55 THRU 405 WILL BE TRANSMITTED ONLY ON THE FIRST TRANSMISSION BEFORE AN OBSERVATION BEGINS.

TABLE 2

REV. B 5/7/75 amc A.M. SHALLOWAY
REV. A 11/12/74 amc 6-11-74

PROTOTYPE (2 ANTENNA) SYSTEM

SYSTEM CONTROLLER ⟶ VLAC (CORE A)

CORE INPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION	SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
0	0 0 0 0 G H_4 L_4 H_3 L_3 H_2 L_2 H_1 L_1 S_7 S_5 S_4 P_2 P_1 P_0 F E D C B A	IGNORE G-WILL ALTERNATE UNLESS Vs BAD	0	0
1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	NC- SPARE WORD	1	1
2	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	NC- SPARE WORD	2	2
3	0 0 0 0 0 D_{18} D_{17} D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	NC- THEORETICAL VALUE OF Vs.	3	3
4	0 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	THERE IS ONLY ONE Vs COUNTER IN	4	4
5	0 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	THE SYSTEM. THE OUTPUT OF THE COUNTER	5	5
6	0 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	IS SENT TO 4 INTEGRATORS, ALL OF WHICH	6	6
7	0 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	SHOULD HAVE THE SAME VALUE.	7	7
8	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 A_4 A_3 A_2 A_1 A_0	ANTENNA USED IN S×C MULTIPLICATIONS (BINARY) ACCORDING TO FOLLOWING TABLE:	10	8

NOTE: A_4-A_0 PROGRESSES ONE STEP EVERY DUMP TIME FROM 1 TO 27. HOWEVER, 1 THRU 18 & 27 DO NOT PROVIDE ANY USEABLE DATA.

A_4-A_0	ANT. No.	50MHz SYSTEM
19	1R	A
20	1R	B
21	2R	A
22	2R	B
23	1L	A
24	1L	B
25	2L	A
26	2L	B

9	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	NC- SPARE WORD	11	9
10	0 0 0 0 0 0 — — — — — — — — — — — — — — — — — — 0	NC- SPARE WORD	12	10
11	0 0 0 0 0 0 — — — — — — — — — — — — — — — — — — 0	NC- SPARE WORD	13	11
12	0 0 P Ø S D_{18} D_{17} D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	MULTIPLIER 1 — ACTUAL MULTIPLICATION OBTAINED FROM TABLE ABOVE.	14	12
13	0 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	MULTIPLIER 1	15	13
14	0 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	MULTIPLIER 2	16	14
15	0 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	MULTIPLIER 2	17	15

SIN X COSINE MULTIPLIERS

NOTE: NC = NO CHANGE FROM FINAL SYSTEM.
R = RIGHT L = LEFT

TABLE 3

REV. B 5/7/75 ame A.M. SHALLOWAY
REV. A [redacted] 12/74 ame [redacted] 6-19-74

[redacted] PROTOTYPE (2 [redacted] ANTENNA) [redacted] SYSTEM

SYSTEM CONTROLLER → VLAC (CORE A)

CORE INPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION		SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
16	0 1 P Ø S D_{18} D_{17} D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	1RS × 1RS	A 50 MHz. SYSTEM — SELF MULTIPLIERS	20	16
		1LS × 1LS		21	
		1RC × 1RC		22	
		1LC × 1LC		23	
		2RS × 2RS		24	
		2LS × 2LS		25	
		2RC × 2RC		26	
		2LC × 2LC		27	
		1RS × 1RS	B 50 MHz. SYSTEM — SELF MULTIPLIERS	30	
		1LS × 1LS		31	
		1RC × 1RC		32	
		1LC × 1LC		33	
		2RS × 2RS		34	
		2LS × 2LS		35	
		2RC × 2RC		36	
31	0 1 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	2LC × 2LC		37	31
32	1 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	1RS × 2RS	A 50 MHz. SYSTEM — MULTIPLIER SET 32 — CROSS MULTIPLIERS	400	256
		1RS × 2RC		401	
		1LS × 2LS		402	
		1LS × 2LC		403	
		1RC × 2LC		404	
		1RC × 2LS		405	
		1LC × 2RC		406	
		1LC × 2RS		407	
		1RS × 2RS	B 50 MHz. SYSTEM — MULTIPLIER SET 33 — CROSS MULTIPLIERS	410	
		1RS × 2RC		411	
		1LS × 2LS		412	
		1LS × 2LC		413	
		1RC × 2LC		414	
		1RC × 2LS		415	
		1LC × 2RC		416	
47	1 0 P Ø S D_{18} — — — — — — — — — — — — — — — — — — D_0	1LC × 2RS		417	271

TABLE 3

REV. B 5/7/75 [redacted]
REV. A 11/12/74 [redacted]

A. M. SHALLOWAY
6-19-74

PROTOTYPE (2 ANTENNA) SYSTEM

SYSTEM CONTROLLER → VLAC (CORE A)

CORE INPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION	SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
48	1 0 P ϕ S D_{18} D_{17} D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	1LS × 1LC 1LS × 1LC 2LS × 2LC 2LS × 2LC 1RS × 1RC 1RS × 1RC 1LS × 1LC 1LS × 1LC 2RS × 2RC 2RS × 2RC 2LS × 2LC	A 50 MHz SYSTEM B 50 MHz SYSTEM MULTIPLIER SET 34 MULTIPLIER SET 35 REDUNDANT SIN × COS MULTIPLIERS	420 421 422 423 424 425 426 427 430 431 432	272
59	1 0 P ϕ S D_{18} — — — — — — — — — — — — — — — — — — D_0	2LS × 2LC	433	283
60	1 0 P ϕ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1LC × 1LC 2LS × 2LS 1LS × 1LS 1RC × 1RC 2LS × 2LS 2RC × 2RC	A 50 MHz SYSTEM B 50 MHz SYSTEM MULTIPLIER SET REDUNDANT SELF MULTIPLIERS	434 435 436 437 440 441	284 289
65	1 0 P ϕ S D_{18} — — — — — — — — — — — — — — — — — — D_0				
66	1 0 P ϕ S D_{18} — — — — — — — — — — — — — — — — — — D_0	1RC × 2RS 1LC × 2LS 1RS × 2LC 1LS × 2RC 2RC × 1LS 2RS × 1RC 2LS × 1LC 1RS × 2LC 1LS × 2RC	MULTIPLICATIONS BEFORE INVERSIONS 1RC × 2RS 1LC × 2LS 1RS × 2LC 1LS × 2RC 2RC × 1LS 2RS × 1RC 2LS × 1LC 1RS × 2LC 1LS × 2RC	1RS × 2RC 1LS × 2LC 1RC × 2LS 1LC × 2RC 1LC × 2RS 1LC × 2RS 1RS × 2RS 1RS × 2RC 1LS × 2LC 1RC × 2LS 1LC × 2RS	A 50 MHz SYSTEM B 50 MHz SYSTEM MULTIPLIER SET 36 MULTIPLIER SET 37 REDUNDANT CROSS MULTIPLIERS	442 443 444 445 446 447 450 451 452 453 454	290 300
76	1 0 P ϕ S D_{18} — — — — — — — — — — — — — — — — — — D_0					
77	1 0 P ϕ S D_{18} — — — — — — — — — — — — — — — — — — D_0	A1LC × A2LC A1LC × B2LS A1LS × B2LS A1LS × B2LC	ILLEGAL MULTIPLICATIONS MULTIPLIER SET 38 ILLEGAL MULTIPLIERS	455 456 457 460	301 304
80	1 0 P ϕ S D_{18} — — — — — — — — — — — — — — — — — — D_0				

← NOTE: THIS MAY BE A "0" IN WORDS 81 THRU 87.

TABLE 3

A. M. SHALLOWAY

REV. 5/7[illegible] 6-19-74

PROTOTYPE (2 ANTENNA) SYSTEM

SYSTEM CONTROLLER → VLAC (CORE A)

CORE INPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION	SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
88	1 1 0 0 S_6 A D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 S_3 S_2 S_1 S_0	NC - DELAY LINE DATA	6000	3072
	NOTE: ORDER OF DELAYS IS AS FOLLOWS:			
	WORD NO. | ANT. NO. | 50MHz. SYSTEM			
	124 | 1R | A			
	126 | 1R | B			
	128 | 2R | A			
	130 | 2R | B			
	132 | 1L | A			
	134 | 1L | B			
	136 | 2L | A			
	138 | 2L | B		6016	3086
	NOTE: ALL WORDS NOT LISTED ARE SPARE WORDS.		6017	3087
141	1 1 0 —		6065	3125
142	1 1 0 0 0 A D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 T T T T	TEST DELAY LINE	6066	3126
143	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	SPARE DELAY WORD	6067	3127
144	1 1 0 0 0 0 0 0 0 0 0 0 Y_C Y_M Y_L Y_S X_M X_L 0 0 0 M_4 M_3 M_2 M_1 M_0	M_4-M_0 = SIN INPUT MULTIPLEXER ADDRESS	6070	3128
	NOTE: IF T (IN WORD NO. 281) = 1, ALL EXCHANGE DATA BITS = 1. X's ARE EXCHANGE DATA BITS FOR ANT. ASSOCIATED WITH INPUT MUX. ADDRESS. NOTE: S=SIN C=COS L=LSB M=MSB	0 0 0 0 0 0 0 0 0 0 0	SRARE MULTIPLEXER WORD		
		0 0 0 0 M_4 — — M_0	M_4-M_0 = COS INPUT MULTIPLEXER ADDRESS		
		0 0 0 0 0 0 0 0 0 0 0	SPARE MULTIPLEXER WORD		
		0 0 0 0 M_4 — — M_0	M_4-M_0 = SIN OUTPUT MULTIPLEXER ADDRESS		
		0 0 0 0 0 0 0 0 0 0 0	SPARE MULTIPLEXER WORD		
		0 0 0 0 M_4 — — M_0	M_4-M_0 = COS OUTPUT MULTIPLEXER ADDRESS		
151	1 1 0 — — — — 0 0 0 0 — 0 0 0 0 0	SPARE MULTIPLEXER WORD	6077	3135
152	1 1 0 0 0 0 0 0 G F_1 F_0 E D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	NC - SYSTEM MONITOR DATA	6100	3136
215	1 1 0 — D_0		6177	3199

TABLE 3

REV. B 5/7/75 ams
REV. A 11/12/74 ams

A.M. SHALLOWAY
6-19-74

PROTOTYPE (2 ANTENNA) SYSTEM

SYSTEM CONTROLLER → VLAC (CORE A)

CORE INPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION	SC-RAM ADDRESS OCTAL	SC-RAM ADDRESS DECIMAL
216	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	GO/NO-GO RESULTS FROM DELAY COMPARATOR S=SIN-L&MSB C=COS-L&MSB S OR C=0=GO S OR C=1=NO-GO CONSIDER THESE WORDS NUMBERED FROM 1 TO 54. THE GO/NO-GO'S ARE ASSOCIATED WITH ANT. AS FOLLOWS:	6200	3200

COMPUTER WORD NO.	WORD NO.	ANT. NO.	50 MILE SYSTEM
252	37	1R	A
254	39	1R	B
256	41	2R	A
258	43	2R	B
260	45	1L	A
262	47	1L	B
264	49	2L	A
266	51	2L	B

262	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 C_1 C_0 S_1 S_0	ALL OTHER WORDS PROVIDE NO USEFUL DATA, AND NORMALLY ARE ZERO	6265	3253
263	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		6266	3254
279	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		6277	3263
280	1 1 0 0 0 0 0 0 0 0 0 0 B_2 B_1 B_0 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	N.C. — PARITY ERROR ADDRESSES.	6300	3264
343	1 1 0 0 0 0 0 0 0 0 0 0 B_2 B_1 B_0 A_8 — — — — A_0		6377	3327
344	1 1 0 1 0 0 0 0 0 0 0 0 0 0 L 0 0 0 C_5 C_4 C_3 C_2 C_1 C_0	C_5-C_0 = MULTIPLIER SET DESIRED BY VLAC. EACH NUMBER = 8 MULTIPLIERS. SEE COMPUTER WORD NOS. 32 THRU 87 FOR SET NUMBERS. L=1 IN LAST WORD.	6400	3328
MAX ↓ 350	1 1 0 1 0 0 0 0 0 0 0 0 0 0 L 0 0 0 C_5 C_4 C_3 C_2 C_1 C_0		MAX ↓ 6406	MAX ↓ 3334
LAST WORD	1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 T_8 T_7 T_6 T_5 T_4 T_3 T_2 T_1 T_0	N.C. — TIME TO END OF OBSERVATION.	7137	3679

NOTE: Four 1's in bit positions 20, 21, 22, & 23 indicate the last word of transmission.

REV. B 5/7/75 A.M. SHALLOWAY

TABLE 3 REV. A 10/[illegible] 9-74

[redacted] VLAC (BOSS) ⟶ SYSTEM CONTROLLER

BOSS OUTPUT

COMPUTER WORD NO.	BIT NUMBER 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	DESCRIPTION
0	0 0 0 1 0 0 0 0 0 0 0 0 0 S_7 S_5 S_4 P_2 P_1 P_0 F E D C B A	N.C. – CONTROL WORD
1	0 0 1 0 S_6 A D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 S_3 S_2 S_1 S_0	N.C. – DELAY LINE DELAY
	NOTE: ORDER OF DELAYS IS AS FOLLOWS:	
	WORD No. / ANT. NO. / 50 MHz SYSTEM 37 / 1R / A 39 / 1R / B 41 / 2R / A 43 / 2R / B 45 / 1L / A 47 / 1L / B 49 / 2L / A 51 / 2L / B	
	NOTE: ALL WORDS NOT LISTED ARE SPARE WORDS	
54	0 0 1 0 – – – –	
55	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 L C_8 C_7 C_6 C_5 C_4 C_3 C_2 C_1 C_0	C_8-C_0 = MULTIPLIER SETS DESIRED BY VLAC. EACH NUMBER = 8 MULTIPLIERS. SEE COMPUTER WORD NOS. 32 THRU 87 IN TABLE 3 FOR SET NUMBERS. L = 1 IN LAST WORD.
MAX ↓ 60	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 L C_8 – – – – C_0	
LAST WORD	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 T_8 T_7 T_6 T_5 T_4 T_3 T_2 T_1 T_0	N.C. – TIME TO END OF OBSERVATION

NOTE: COMPUTER WORDS 55 THRU 60 WILL BE TRANSMITTED ONLY ON THE FIRST TRANSMISSION BEFORE AN OBSERVATION BEGINS.

TABLE 4

REV. B 5/7/75 and A.M. SHALLOWAY
REV. A 11/12/74 and 6-19-74

TABLE 5

INSTRUCTIONS FOR CRT TERMINAL DATA DISPLAY

NOTES:

A. In each instruction below, the first heading (e.g. DB 0000.7137) is used to display the desired information in octal and the second heading (e.g. DC 0000.7137) is used to display the information in decimal. If only one heading is shown, the information is available only in octal.

B. At the end of each display instruction, the ENTER key must be depressed to transfer the instruction from the CRT to the SC. This function will appear on the CRT screen as a backwards letter L (e.g. DB 0000.7137⌟).

C. Spaces within an instruction have no effect and may be used as desired for clarity (e.g. DB0000.7137 or DB 0000.7137).

D. To continually update the data display, prefix the desired instruction by one of the following letters:

LETTER	UPDATE PERIOD
R	0.8 sec
S	1.6 sec
T	3.2 sec
U	6.4 sec
V	12.8 sec
W	25.6 sec
X	51.2 sec
Y	102.4 sec

For faster update periods, some displays will not have time to complete between updates depending on the length of the display and the baud rate.

E. To stop an updating display (necessary before entering new instructions) use the DA instruction.

F. Each instruction for displaying multiplier results (instructions 3 thru 6) contains one or more octal number XXXX which is a starting address for a group of 8 multiplier results. These may be interpreted in two ways:

XXXX = Octal number of starting RAM address

or if the least significant digit is taken as zero:

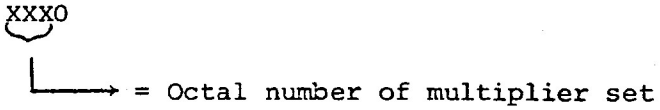


TABLE 5 (continued)

INSTRUCTION	DATA TO BE DISPLAYED
1. DA	STOP UPDATE and RESET DISPLAY LOGIC (No data will be displayed by this instruction)
2. DB DC 0000.7137	CONTROL and TIME WORDS
3. DD DE XXXX ↑—See Note F	MULTIPLIER RESULTS, SEQUENTIAL BEFORE Vs SUBTRACTION (128 sequential multiplier results starting at SC Ram address XXXX)
4. DF DG XXXX. ··· XXXX.1000	MULTIPLIER RESULTS, GROUPS OF 8 BEFORE Vs SUBTRACTION (Maximum of 16 groups, each group consisting of 8 sequential multiplier results starting at SC Ram address XXXX)
5. DH XXXX	MULTIPLIER RESULTS, SEQUENTIAL AFTER Vs SUBTRACTION
6. DI XXXX. ··· XXXX.10000	MULTIPLIER RESULTS, GROUPS OF 8 AFTER Vs SUBTRACTION
7. DL DM 6000	DELAY and DISABLE DATA EXCHANGE DATA AND MUX ADDRESSES (54 delay words; 2 test delay words; left and right exchange data in the order CM, CL, SM, SL; input and output mux addresses)
8. DN DO 6100	SYSTEM MONITOR DATA (64 words)
9. DP 6200	GO/NO GO DATA (Delay Line Self Test Results 54 words = 216 delay lines)
10. DQ XXXX	RAM DATA SET (8 sequential words starting at Ram octal address XXXX, bits 0 thru 21 displayed in octal)
11. DR DS 6300	PARITY ERROR ADDRESSES (64 words, contains computer word number for parity error and the BT in which it occurred BOSS computer to SC)
12. DT DU 6400	ADDRESSES OF MULTIPLIERS REQUESTED (Maximum of 351 words, each representing one multiplier set requested by VLAC)

TABLE 6

INSTRUCTIONS FOR CRT TERMINAL DATA ENTRY

NOTES:

A. All numbers indicated by X are in octal.

B. At the end of each entry instruction, the ENTER key must be depressed to transfer the instruction from the CRT to the SC. This function will appear on the CRT screen as a backwards letter L (e.g. EE XX⌟).

C. Spaces within an instruction have no effect and may be used as desired for clarity (e.g. EXX or EE XX).

D. The following table gives the delay word number for each of the eight prototype delay words and the corresponding multiplexer address that tests the associated delay lines:

DELAY WORD NUMBER		DELAY		MULTIPLEXER ADDRESS	
Decimal	Octal	Ant. No.	50 MHz System	Decimal	Octal
37	45	1R	A	19	23
39	47	1R	B	20	24
41	51	2R	A	21	25
43	53	2R	B	22	26
45	55	1L	A	23	27
47	57	1L	B	24	30
49	61	2L	A	25	31
51	63	2L	B	26	32

E. The following table gives the GO/NO GO logic tests for mux addresses 0 and 28-31.

MUX ADR	INPUT MUX DATA	OUTPUT MUX DATA	GO/NO GO RESULTS
0	0	0	GO
28	1	1	GO
29	0	1	NO GO
30	1	0	NO GO
31	Random Data	Random Data	NO GO

TABLE 6 (continued)

1. EA XXXX — CONTROL WORD

- Observation/Test Status: Bits CBA (see Table 2)
- Parity Error Status = Bits FED (see Table 2)
- 1 thru 6 = 50ms thru 300ms Dump Period = Bits P_2 P_1 P_0 (see Table 2)
- 1 = Disable Neg Sampler 2 = Disable Pos Sampler 3 = Both: Bits S_7 S_5 S_4 (see Table 2)

---

2. EB X XXXXX XX — DELAY DATA, SAME TO ALL DELAY CONTROLS

- Sampler delay in 625 picosecond steps
- Delay Line Delay in 10 nanosecond steps
- 0 = Normal 1 = Delay Line Disable 2 = Sampler Invert 3 = Both

---

3. EC X XXXXX XX. ····X XXXXX XX — DELAY DATA DIFFERENT TO EACH DELAY CONTROL

54 delay words each as in EB

---

4. ED XX.X XXXXX XX — DELAY DATA TO ONE DELAY CONTROL

- Same as in EB
- Octal delay word number (In decimal 1 = 1L ···· 53 = 27L, 2 = 1R ···· 54 = 27R) See Note D for prototype)

---

5. EE XX — HOLD MUX ADDRESSES

- Octal mux address to hold (In decimal 1 = Ant 1 27 = Ant 27, 0 and 28-31 = Tests of GO/NO GO Logic) See Note E.

---

6. EF XXXX — EXCHANGE DELAY LINE(S) AT ONE MUX ADR

- Octal mux adr to hold
- Exchange data 1 = SL 2 = SM 3 = Both
- Exchange data 1 = CL 2 = CM 3 = Both

7a. EG 3317 — MULTIPLIER TEST-RANDOM NOISE GENERATOR

(All multiplier terminated inputs receive the same data pattern and all bridging inputs receive the same data pattern but different from the terminated inputs)

7b. EG XXXX7317 — MULTIPLIER TEST-STATIC PATTERN

(As above except the inputs receive static data determined by XXXX.)

- Bridging LSB Input
- Bridging MSB Input
- Terminated LSB Input
- Terminated MSB Input

TABLE 6 (continued)

8.	EH XX ↑— Octal mux address to hold	DELAY LINE TEST-HOLD MUX ADR SHORT PATTERN
9.	EI XX ↑— Octal mux address at which test starts	DELAY LINE TEST-ROTATE MUX ADR SHORT PATTERN (One complete cycle = 20 seconds for DT = 50ms)
10.	EJ XX ↑— Octal mux address to hold	DELAY LINE TEST-HOLD MUX ADR LONG PATTERN
11.	EK XX ↑— Octal mux address at which test starts	DELAY LINE TEST-ROTATE MUX ADR LONG PATTERN (One complete cycle = 5.7 min. for DT = 50ms)
12.	EL	RESET FROM COMPUTER (Left GO/NO GO and Exchange Data)
13.	EM	RESET FROM COMPUTER (Right GO/NO GO and Exchange Data)
14.	EQ	RESET TEST INSTRUCTIONS 5 THRU 11 (Resets storage flip flops F13 thru F17 on L31 but does not reset the TEST indicator)
15.	ER	RESET ALL TESTS (Same as EQ but also resets the TEST indicator)

TABLE 7

CRT DISPLAY FORMATS

NOTES:

1. The following table is intended to aid the user of the System Controller CRT to interpret the displayed information. This table is intended to be used along with Tables 1-6 to provide a complete users description of the display functions available.
2. For each type display instruction an example display or partial display is shown, and where appropriate, the associated 24 bit computer word is shown to indicate which bits of the word are represented by each character displayed on the CRT screen.
3. If certain conditions are present in the displayed information, the associated character is displayed on the CRT screen as a reverse flashing character. In the display examples these characters are shown with an underline. For certain test conditions that are not errors, the associated display character appears on the screen as a reverse character but without flashing.

   EXAMPLES: 2 indicates error condition
   2* indicates test condition

DISPLAY EXAMPLES

1. CONTROL and TIME WORDS

Octal

DB 0000.7137

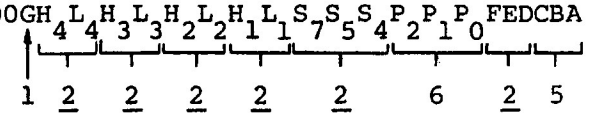
1 2 2 2 2 2* 6 2 5 7777 (tens of seconds)

Decimal

DC 0000.7137

1 2 2 2 2 2* 6 2 5 5110 SEC

Control Word Only



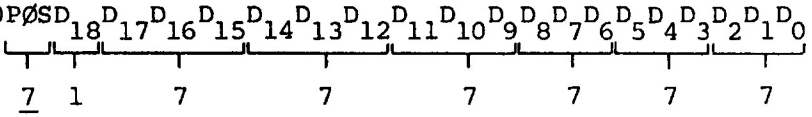
2. MULTIPLIER RESULTS

Octal

DD XXXX (seq. before V_S)
DH XXXX (seq. after V_S)
DF XXXX.10000 (non-seq. before V_S)
DI XXXX.10000 (non seq. after V_S)

7 1777777 ←8 per line→ 7 1777777

Multiplier Result

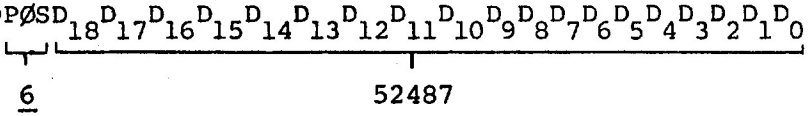


Decimal

DE XXXX (seq. before V_S)
DG XXXX.10000 (non-seq. before V_S)

6 524287 ←8 per line→ 6 524287

Multiplier Result



NOTE: The sign bit should always be 0 before V_S.

3. DELAY VALUES and EXCHANGE DATA

Octal

DL 6000

LEFT - RIGHT

1 1 3 377 3 3 17 ←4 per line→ 1 1 3 377 3 3 17

14 Lines Total: Line 1 = 1 left 1 right 2 left 2 right

Line 14 =27 left 27 right Left Test Delay Right Test Delay

LEFT	RIGHT
1 1 1 1 37	1 1 1 1 37
37	37
37	37
37	37

Decimal

DM 6000

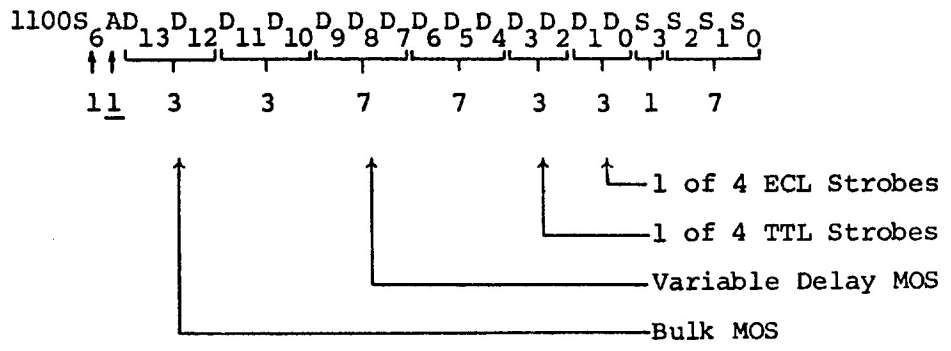
LEFT - RIGHT

1 1 16383 15 ←4 per line→ 1 1 16383 15

14 lines total in same order as above

LEFT	RIGHT
1 1 1 1 31	1 1 1 1 31
31	31
31	31
31	31

Delay Word

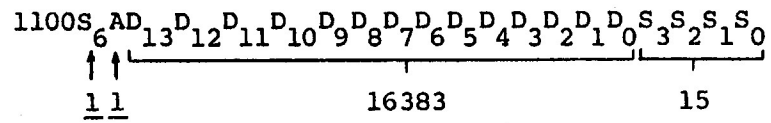


Exchange Data

CM CL SM SL

Sin Input Mux Adr
Cos Input Mux Adr
Sin Output Mux Adr
Cos Output Mux Adr

Delay Word



Exchange Data

Same as for octal

4. SYSTEM MONITOR MEASUREMENTS (2 ANT PROTOTYPE)

DN 6100 (octal)

DO 6100 (decimal)

	1	2	3	4	5	6	7	8	Out of Spec Code:
1.	0 2500* (+5 SC)	0 2500* (+5 D/M)	0 XXXX	0 2600* (-5.2 D/M)	0 2600* (-5.2 SC)	0 1200 (-12 D/M)	0 1200 (-12 SC)	0 2800 (+28 D/M)	0 = In spec 3 = Emergency Low
2.	0 1500 (+15 SC)	0 1500 (-15 SC)	0 900 (-9 SC)	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	5 = High 7 = Low
3.	0 1000* (02V D/M)	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	For an Emergency High condition in either the SC or D/M rack, the
4.	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	D/M rack will be automatically powered down
5.	0 750* (Mult Clk)	0 750* (Dly Clk)	0 750* (Cont A Clk)	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	and all error codes will contain either an 8 or 9 or a punctuation character.
6.	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	
7.	0 1100* (SC Temp)	0 1100* (SC Temp)	0 1100* (D/M Temp)	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	
8.	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	0 XXXX	

NOTES:

1. The nominal measurement is shown above in decimal. For octal display, only the measurement is in octal.
2. Measurements marked * must be doubled to obtain the value.
3. The user must enter the decimal point mentally.
4. Clock measurements are of the peak value of the sinewave 100 MHz clock.
5. SC = System Controller Rack D/M = Delay-Multiplier Rack.
6. XXXX = Inputs not used in 2 Ant Prototype and spare inputs. These are not all zero on the display.
7. Full range temperature = 81.90°C.

5. GO/NO GO RESULTS

DP 6200 (octal only)

LEFT - RIGHT

	COS		SIN			COS		SIN	
	M	L	M	L		M	L	M	L
1	1	1	1	1	←4 sets per line→	1	1	1	1

9 Lines Total: Line 1 = 1 left 1 right 2 left 2 right 3 left 3 right

Line 9 = 25 left 25 right 26 left 26 right 27 left 27 right

6. RAM DATA SET

DQ XXXX (octal only)

17777777

↓ Total of 8 words

17777777

Computer Word Bit:

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		1	7			7			7			7			7			7			7		

7. PARITY ERROR ADDRESSES

DR 6300 (octal)

DS 6300 (decimal)

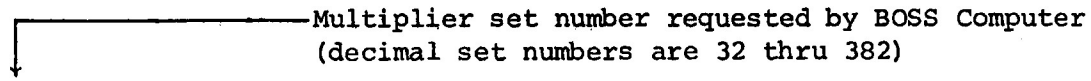
6 677 ←8 per line→ 6 677

↑ ↑ Computer Word No. Boss → SC

└ Blanking Time in which error occurred (1 thru 6)

8. ADDRESSES OF MULTIPLIERS REQUESTED

DT 6400 (octal)
DU 6400 (decimal)



677 ←16 per line max→ 677

22 lines total maximum
351 total addresses maximum

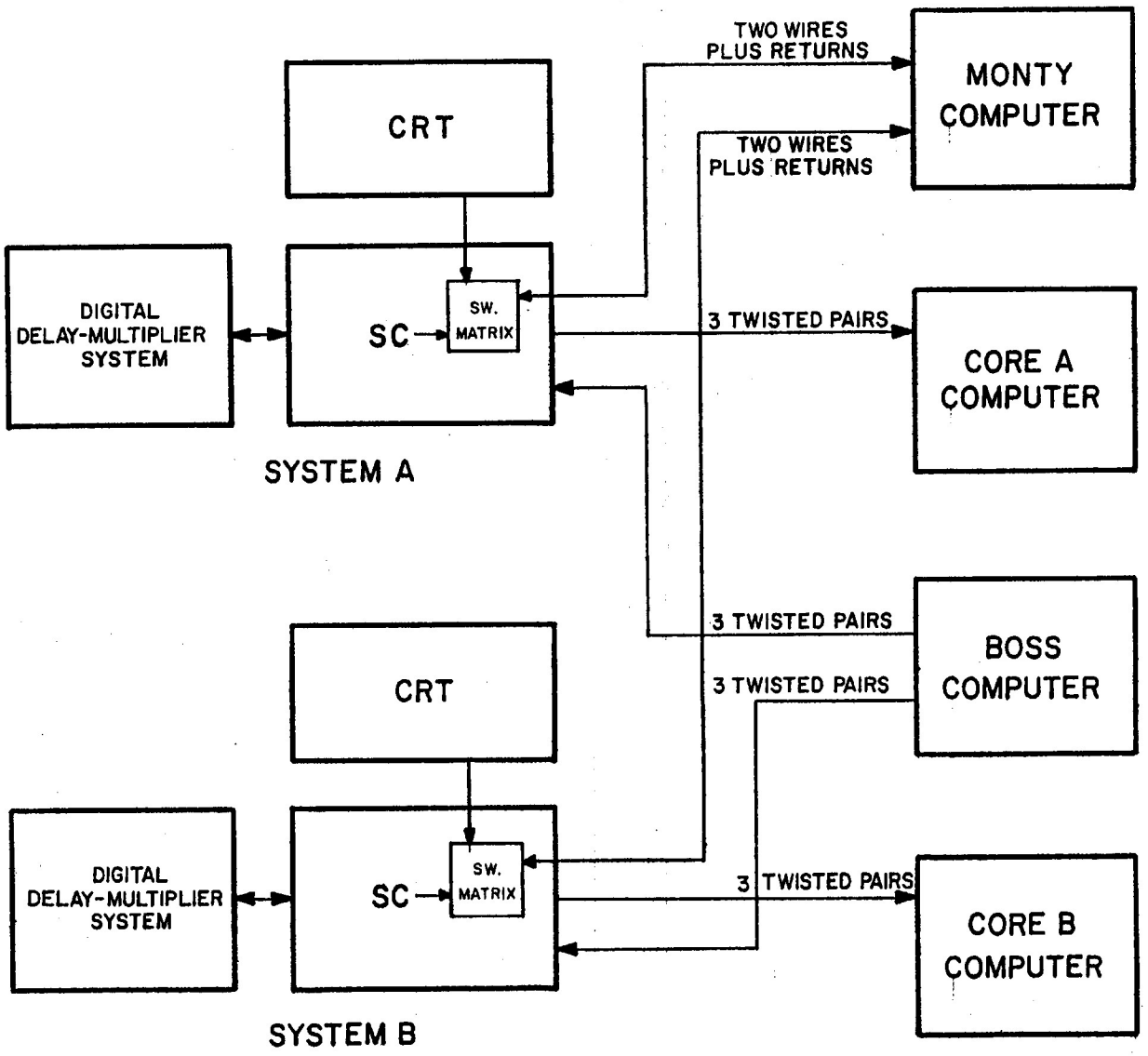
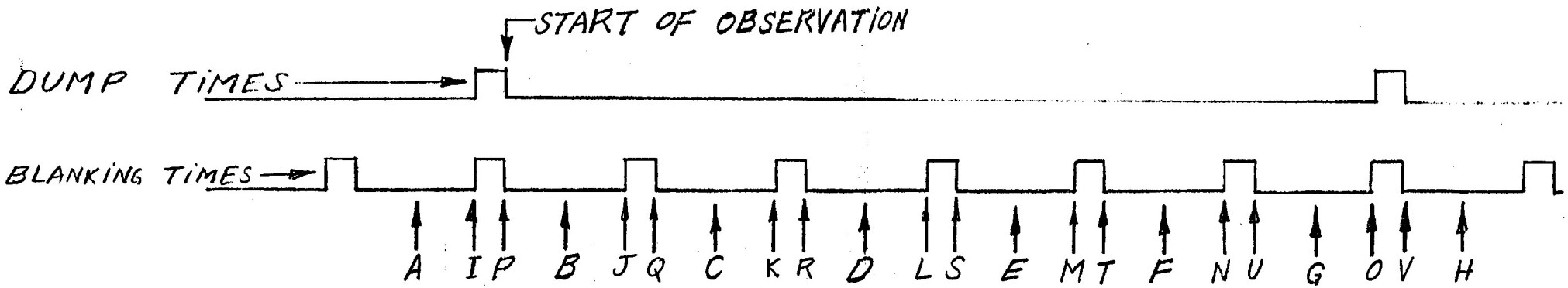


FIGURE I

COMMUNICATIONS SYSTEM BETWEEN SYSTEM CONTROLLER AND VLA SYNCHRONOUS COMPUTERS



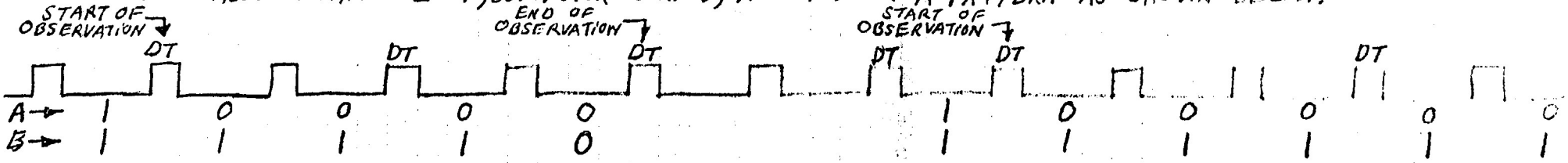
DATA OBTAINED BY SC AT THIS TIME

DATA APPLIES TO THIS TIME

DATA SET SENT TO VLAC AT H	1	2	NOTES
DELAY	G	H	
SYSTEM MONITOR	G	G	IF AN "OUT OF SPEC" CONDITION IS DETECTED AT B, C, D, E OR F THE FIRST ONE DETECTED WILL REPLACE G IN BOTH COLUMNS AT LEFT.
GO/NO-GO	J→O	B→G	ALL GO/NO GO's ARE OR'ED INTO MEMORY UNTIL RESET.
PARITY, VLAC→SC	B→G	B→G	ALL BAD PARITY ADDRESSES (UP TO 64) ARE STORED IN MEMORY & RESET EVERY DT.
MULTIPLIERS DESIRED	A	→	APPLIES TO ALL DATA FROM B TO END OF OBSERVATION
TIME	G	O	
MUX. ADDRESS	O	B→G	
MULTIPLIERS	B→G	O	
EXCHANGE DATA	O	H→	DELAY LINE(S) CONTINUE TO BE EXCHANGED UNTIL RESET.

NOTE: ABOVE COVERS DATA FROM SC TO CORE COMPUTER – SEE TABLES 1&3. COLUMN 1 INDICATES WHEN THE SC's STORAGE RECEIVES THE DATA – FROM EITHER CORE COMPUTER, DELAY MULTIPLIER OR SC's INTERNAL CONTROL. COLUMN 2 INDICATES WHEN THIS DATA WAS USED OR GENERATED.

BITS A&B IN TABLES 2&4, COMPUTER WORD 0, WILL FOLLOW A PATTERN AS SHOWN BELOW:



SC TO VLAC DATA RELATIONSHIPS

FIGURE 2

A.M. SHALLOWAY
[redacted] REV. B [redacted]/75