VLA TECHNICAL REPORT #17

MODULE F6

RF SPLITTER

Sander Weinreb

July 1975

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II. FUNCTION

The RF Splitter Module couples two front-end dewar outputs, AB and CD, into four Frequency Converter inputs, A, B, C, and D. Each dewar-output is at 4.5 to 5.0 GHz and has passed thru the cooled paramp (+30 dB), transistor amplifier (+35 dB), isolator (-0.5 dB), and ∿1.5m of 3mm-coaxial cable (-1.5 dB). This 63 dB of gain produces a Splitter input level of -22 dBm with 300° system temperature and 800 MHz of RF bandwidth. Specifications and data sheets for the transistor amplifier and isolator are included in Section IV of this manual.

Photographs of the module are shown in Figures 1 and 2 and a block-diagram is presented in Figure 3. The functions of the Splitter are as follows:

a) Log Detector Monitoring - Each input is coupled to a detector and logarithmic amplifier to provide a DC output as shown in Figure 4. This output is within a few percent of 10 dB per volt for input levels of -33 dBm to -3 dBm (output level of -3 volts to 0 volts). This signal is for swept frequency testing of the front-end; the sweep generator output level should be adjusted so the peak Log Detector output level is ∿0 volts.

b) RF Monitoring - RF samples approximately 8 dB below the input signal levels are available on front-panel SMA connectors for the purpose of spectrum analyzer RFI Analysis or for phase stability testing.

c) Level Adjustment - A voltage-controlled attenuator is provided in each signal path to allow front-panel adjustment of output signal level. The attenuators can be switched between two settings, NORMAL GAIN and LOW GAIN, under computer control. The total loss of the splitter can be adjusted from ∿9 to ∿20 dB with the NORMAL GAIN range pots (initial adjustment, 13 dB) and ∿9 to ∿30 dB with the LOW GAIN pots (initial adjustment, 23 dB). The switchable gain is needed to allow solar observations.

d) Transfer Switch - In NORMAL mode the AB input is connected to A and B outputs whereas in TRANSFER mode it is connected to C and D outputs; the complementary statement applies to the CD input. The purpose of this switch is to facilitate calibration of polarization measurements and to aid in isolation of malfunctions.

e) Power Division - Each front-end channel must feed two Frequency Converters; the Splitter contains isolated power dividers to accomplish this task.

Input and output connections are given in Figure 4.1.

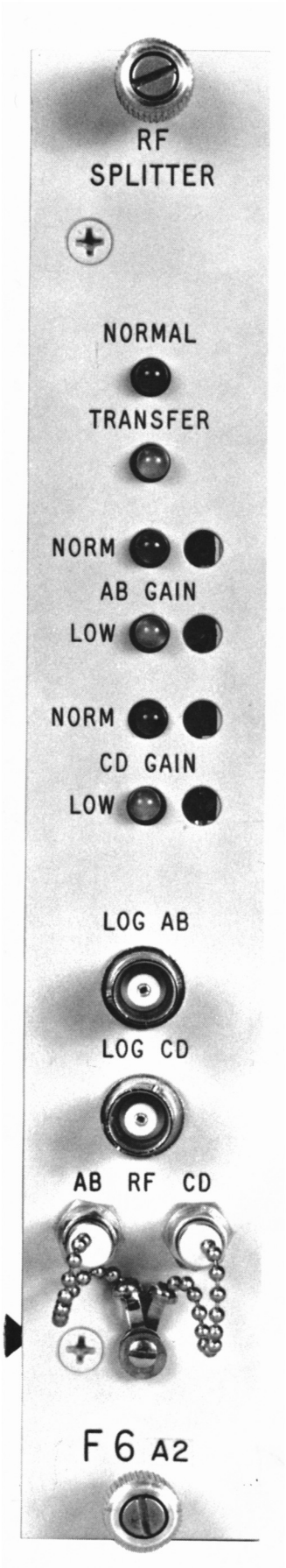


FIGURE 1 RF SPLITTER FRONT PANEL

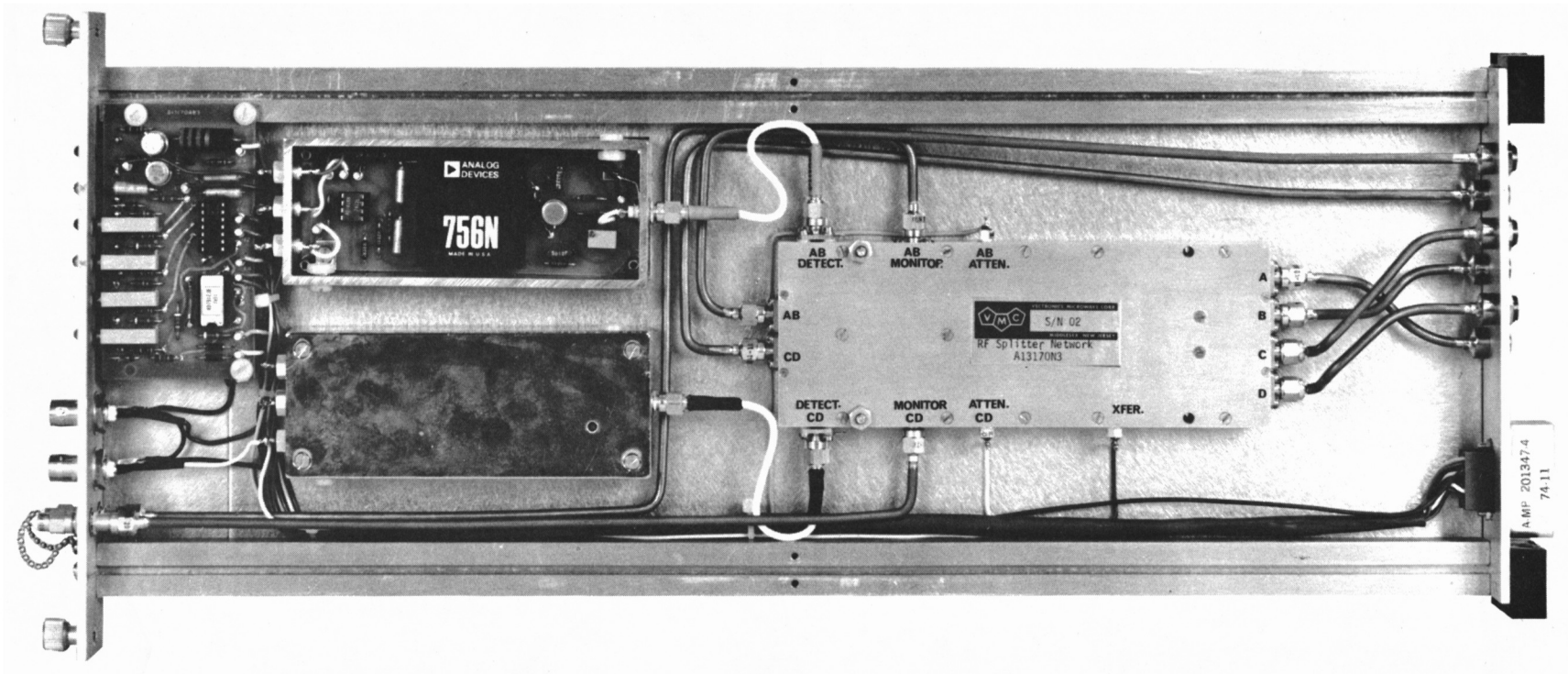
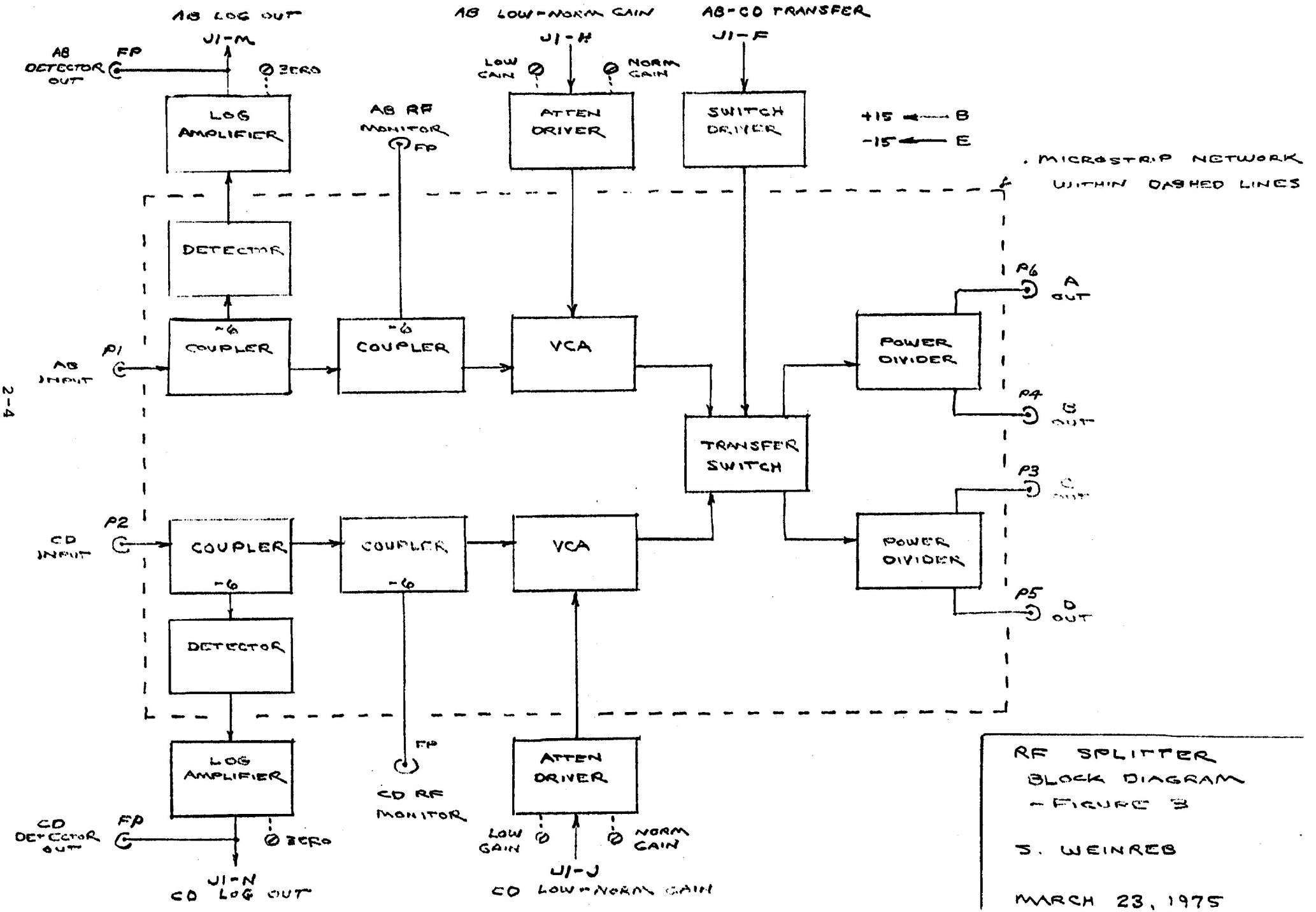


FIGURE 2 RF SPLITTER SIDE VIEW



RF SPLITTER
BLOCK DIAGRAM
- FIGURE 3

S. WEINREB

MARCH 23, 1975

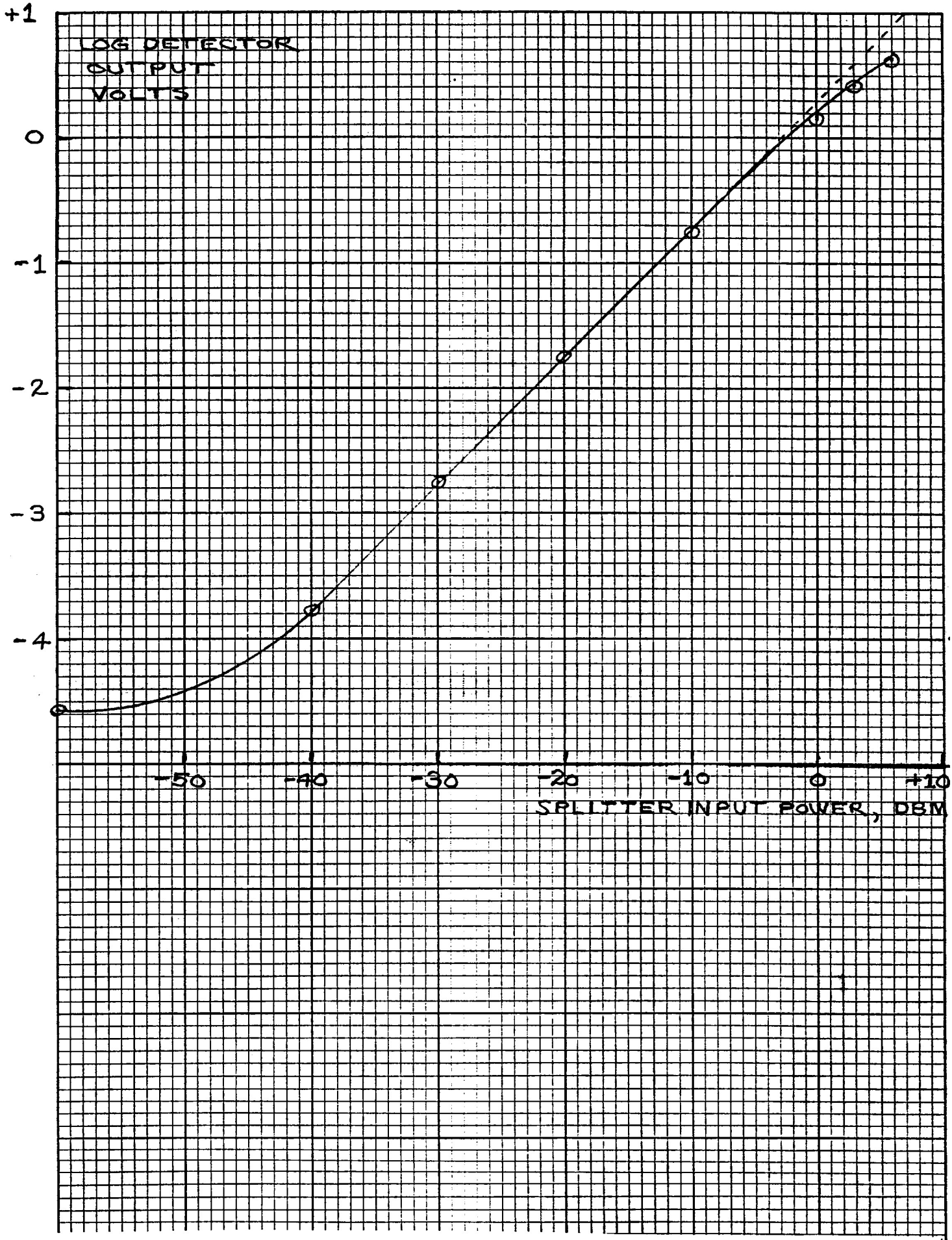


FIGURE 4 - Log Detector output voltage as a function of Splitter input power level.

14 PIN CONNECTOR WIRE LIST

RACK:	BIN: G	SLOT: 7	MODULE: RF Splitter	TYPE: F6
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 14 PIN		CONNECTOR PAGE: 1 of 1		

PIN	FUNCTION	WIRE TYPE	External Connection	Internal Connection
A				
B	+15	Red		Driver - E5
C	+5	Orange		Driver - E8
D	GND	Black		
E	-15	Yellow		Driver - E9
F	Transfer Control	Brown	G10J1-z	Driver - E1
H	AB Attenuator Control	Red	G10J1-a	Driver - E2
J	CD Attenuator Control	Orange	G10J1-b	Driver - E2
K				
L				
M	AB Log Out	Blue	G10J2-AA	Log amp - out
N	CD Log Out	White	G10J2-BB	Log amp - out
P				
R				
P1	AB Input	.141	ZDP1	
P2	CD Input	.141	ZDP2	
P3	C Output	.141	G8P2	
P4	B Output	.141	G6P2	
P5	D Output	.141	G9P2	
P6	A Output	.141	G5P2	

FIGURE 4.1 - Input and output connections.

III. IMPLEMENTATION AND ADJUSTMENT

The heart of the RF Splitter Module is an integrated microstrip network which performs all of the required RF functions in an economical, compact manner. A photograph of the interior of the network is shown in Figure 5. Specifications (A13170N3) of the network and manufacturers data are included in Section IV. If there is a malfunction in the network it should be examined under a lower-power microscope for loose connections (especially at SMA connector interface) and diodes should be checked with an ohmmeter. If this does not reveal the fault the unit should be returned to the manufacturer.

The network transfer switch and attenuators are driven by driver circuits shown in Figures 6 and 7. The transfer-switch driver translates a TTL input ("1" = NORMAL, "0" = TRANSFER) into +3 volts (NORMAL) and -3 volts (TRANSFER) into a 50 ohm switch-control input. The attenuator driver allows either a NORMAL GAIN pot or a LOW GAIN pot to control the current thru PIN diodes in the network; the current is varied from 0 to 4 mA for 0 to 20 dB of attenuation.

A schematic of the Log Detector Amplifier is shown in Figure 8. Tests of square-law detector error vs detector load resistance revealed that a load resistance of 1K gave least error as shown in Figure 9. The first-stage of the Log Detector Amplifier presents this load resistance and provides a gain of -30 in a low drift (1μV/°C) operational amplifier. The amplifier output is applied to a plug-in logarithmic conversion module (AD756N) which is described in the manufacturers data sheet included in Section IV. The log module output is inverted and offset by an output op amp, A3. A log module output of +4 to +1 volts produces -3 to 0 volts output of A3. A maximum output of 0 volts for good square-law accuracy has been chosen so the top of a response curve can be expanded by increasing oscilloscope gain without getting a large offset; i.e. 0.1 volt per division gives 1 dB per division.

Tests of the RF Splitter Module are performed by connecting DC power and +3 or 0V control signals for transfer and gain control. A 4.5 to 5.0 GHz generator is connected to AB or CD input and the appropriate otuputs are measured with a power meter as controls signals are switched and gain pots are varied. For initial adjustment the NORMAL GAIN and LOW GAIN pots are adjusted for 13 dB and 23 dB total insertion loss, respectively. The front-panel indicator LED's should follow the applied control signal; improper initial operation is usually caused by a reversed LED or incorrect rear panel to circuit board wiring.

The only internal adjustment in the RF Splitter Module is the Log Amplifier zero, R10. This should be adjusted to give a one volt output change as input level is changed from -30 dBm to -20 dBm; the absolute level need not be accurate but the 10 dB change should be accurate to $\pm$1 dB. If RF equipment is not available an approximate zero adjustment can be made by adjusting R10 to give -4.3 volts log output with no network input signal. The adjustment is accessible through a small hole in the side of the log amplifier module.

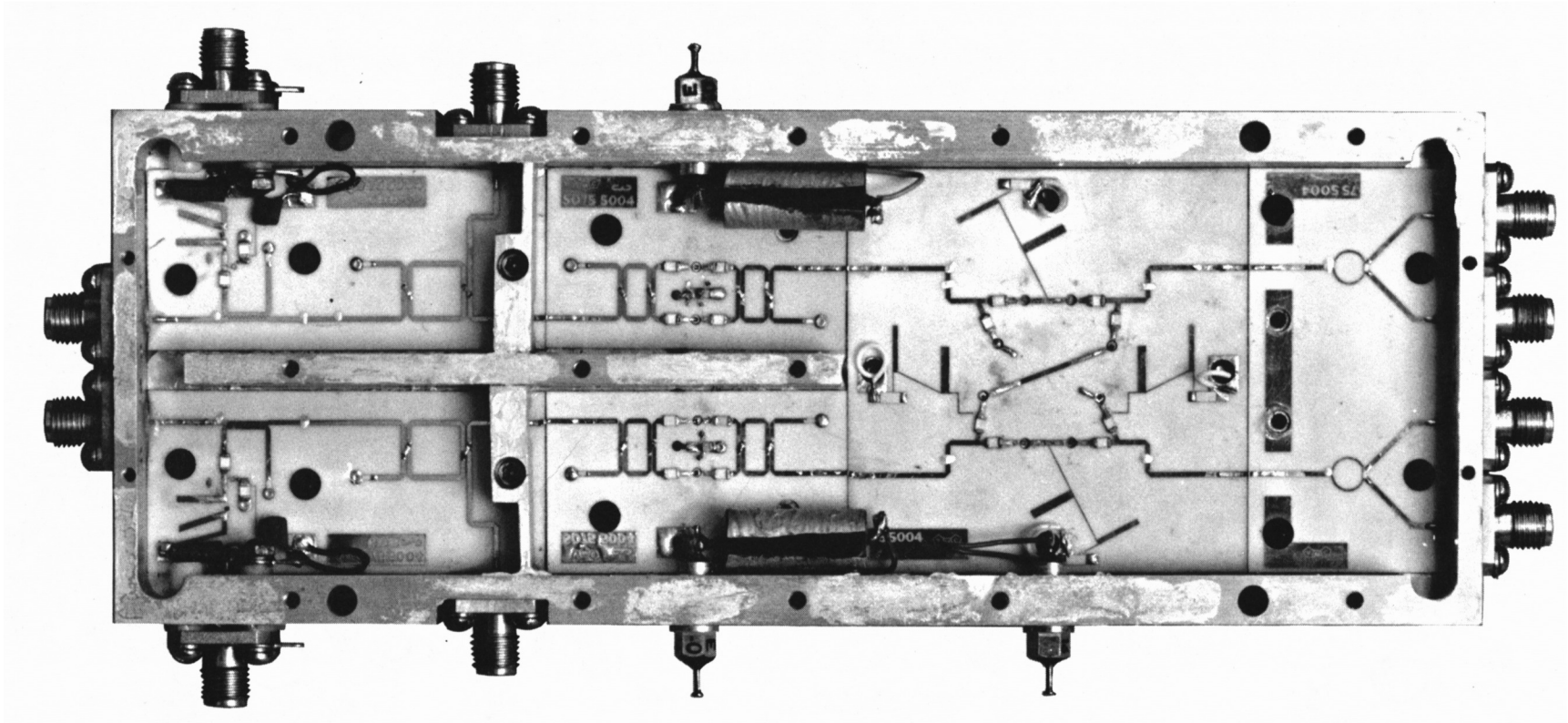


FIGURE 5 SPLITTER NETWORK INTERIOR VIEW

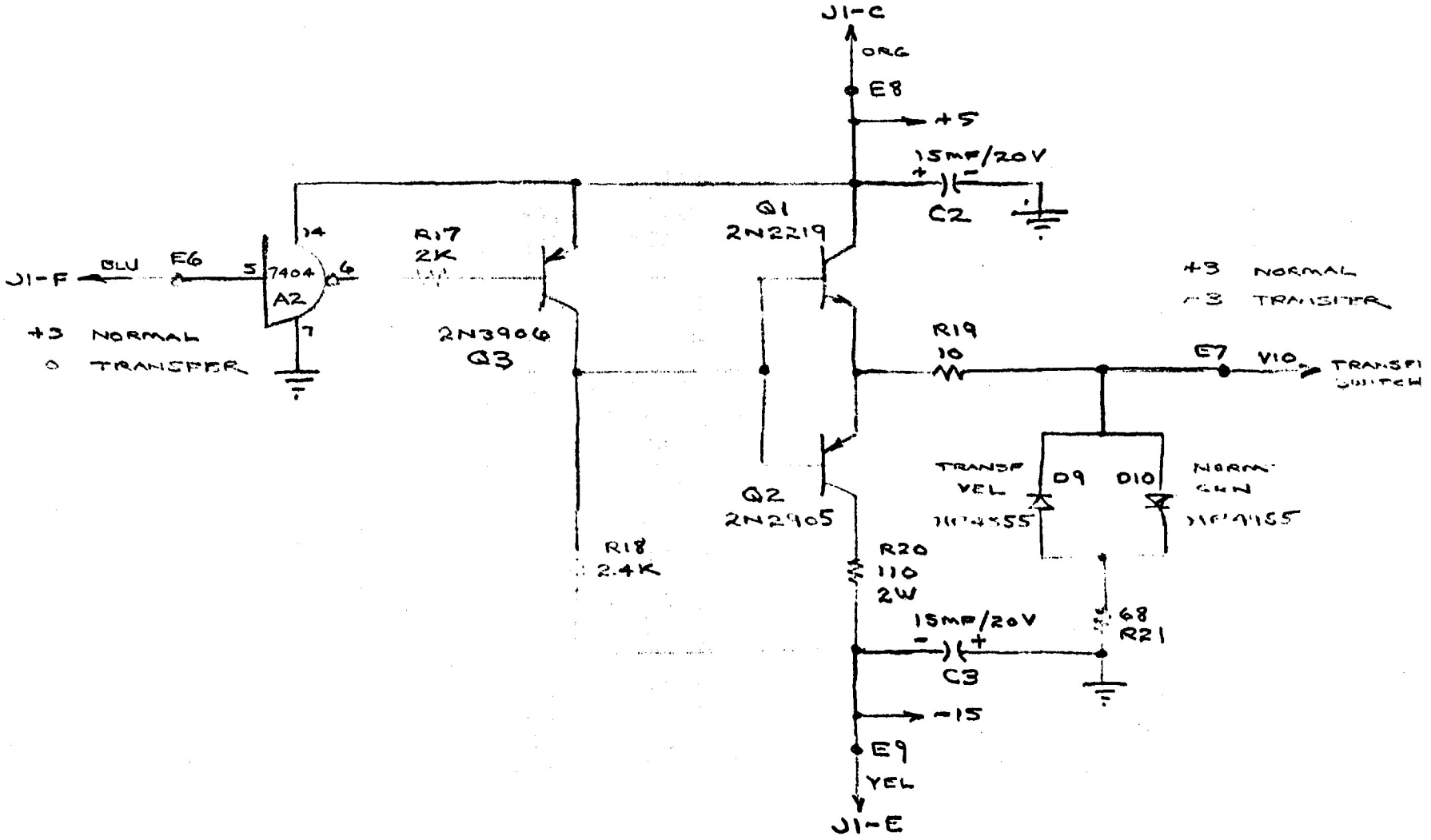


FIGURE 6
RF SPLITTER
- SWITCH DRIVER

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MAY 5, 1975

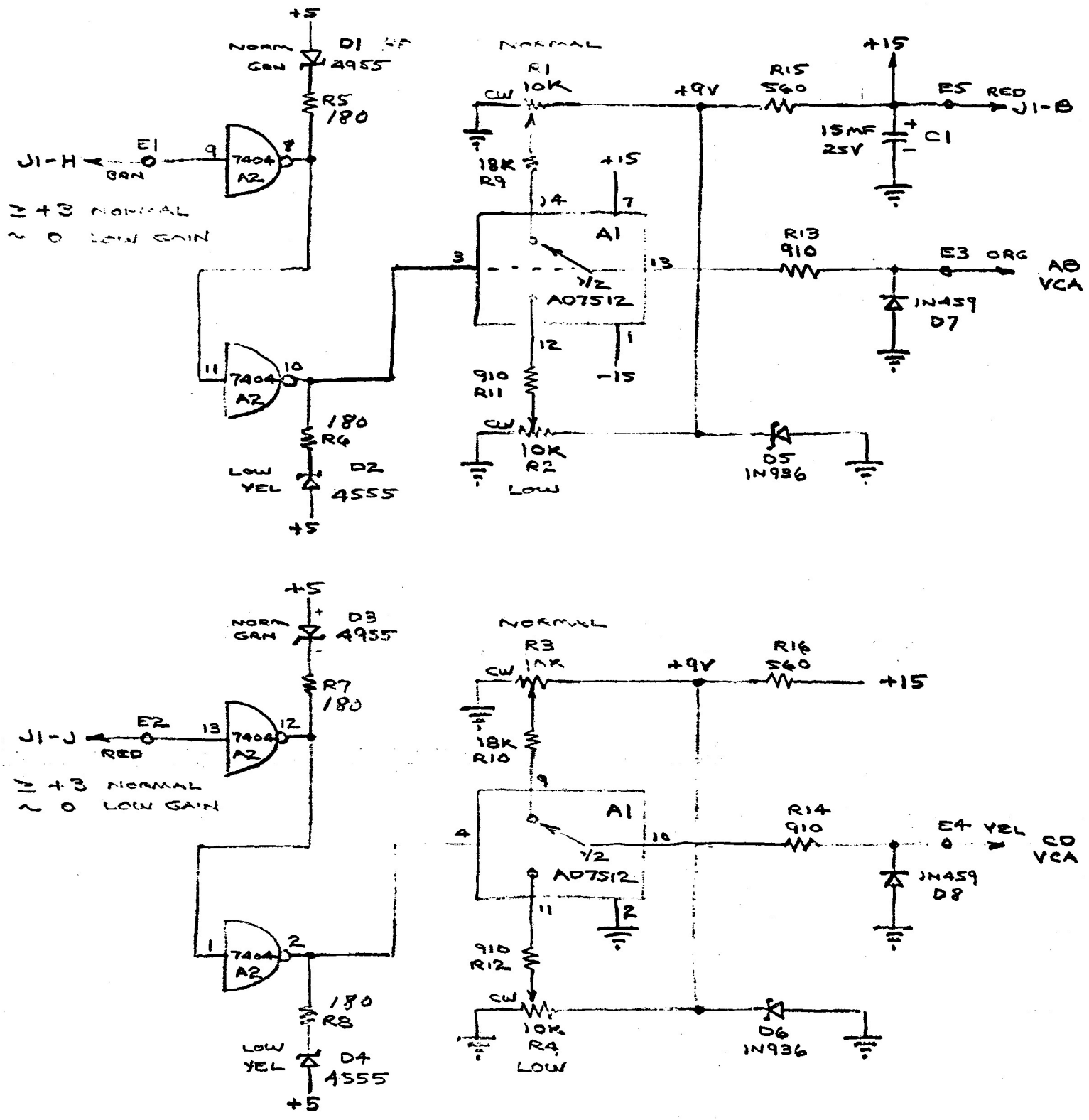
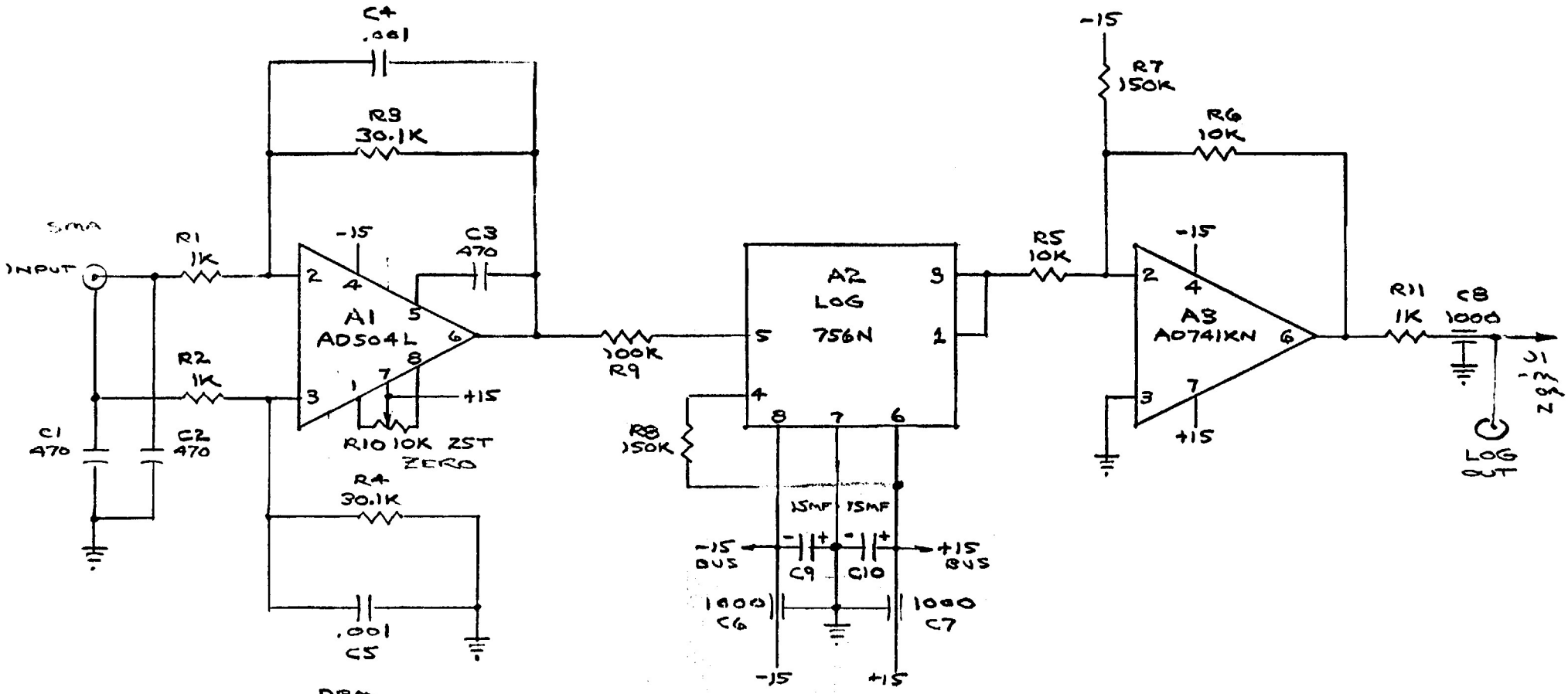


FIGURE 7
RF SPLITTER - ATTENUATOR DRIVER

S. WEINREB

APRIL 1, 1975



IN	OUT	DBM P_{IN}
-33 μV	-3V	-33
-330 μV	-2V	-23
-3.3 mV	-1V	-13
-33 mV	0V	-3
-330 mV	+1V	+7

ALL RESISTORS 1% RNS55D

FIGURE 8
LOG DETECTOR AMP
FOR RF SPLITTER

S. WEINREB

[redacted] MA[redacted] 7, [redacted] 7[redacted]

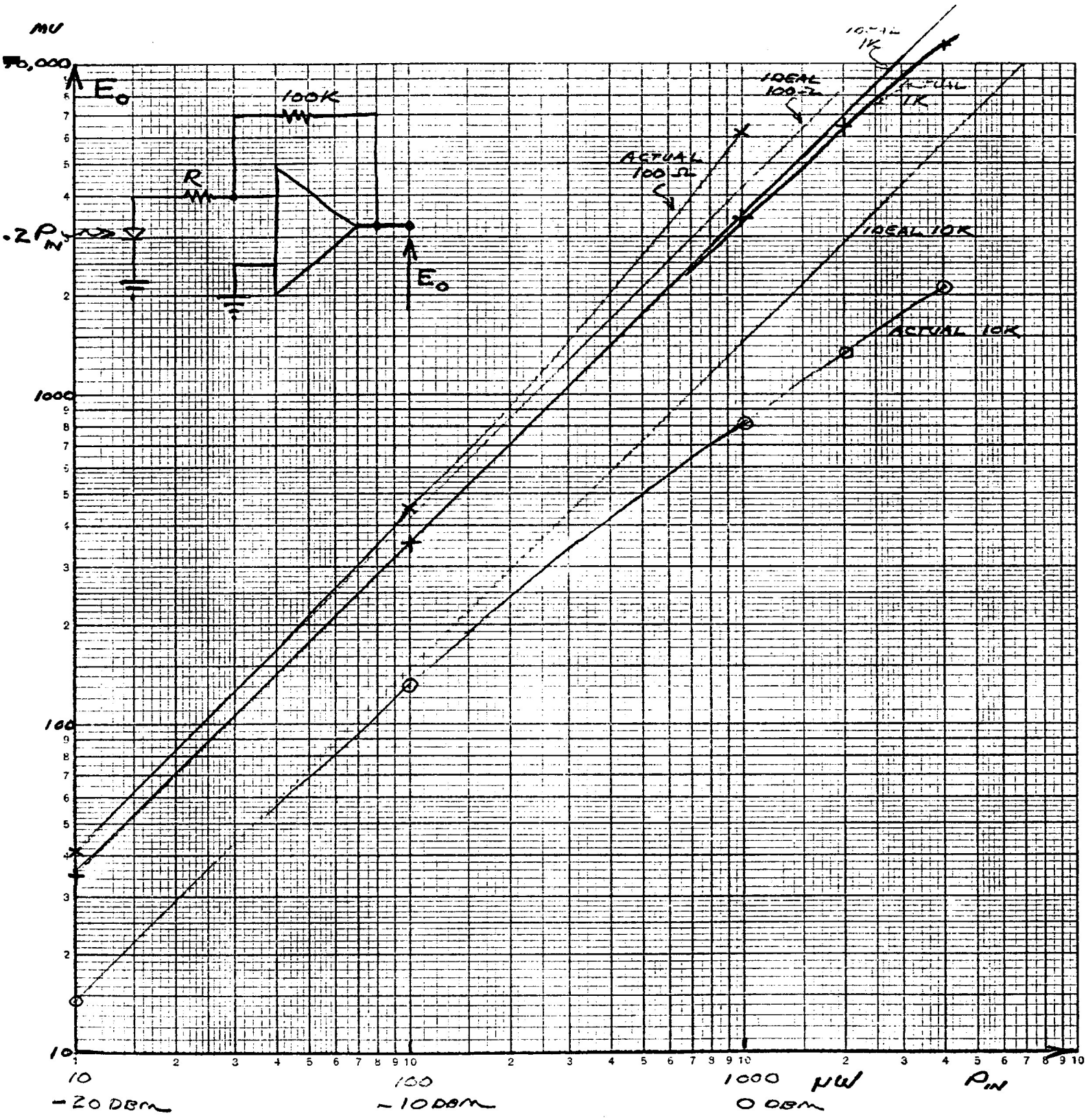


FIGURE 9 - Detector output as function of load resistance, R for Aertech zero-bias Schottky-diode.

IV. BILL OF MATERIALS, SPECIFICATIONS, AND MANUFACTURERS' DATA

BILL OF MATERIAL

☐ ELECTRICAL ☑ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 1 OF 1

MODULE # F6 NAME RF SPLITTER DWG # _____ SUB ASMB MAIN DWG # _____

SCHEMATIC DWG # _____ LOCATION _____ QUA/SYSTEM _____ PREPARED BY _____ APPROVED _____

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
	–	VECTRONICS	A13170N3	RF SPLITTER NETWORK	1	
	–	ANY	B13170AB3	DRIVER PC BOARD	1	
	–	ANY	A13170AB4	LOG AMP PC BOARD	2	
	–	MODPAK	708-100-0000	BOX	2	
		AMPHENOL	74868	UG-625/U BNC JACK	2	
		OMNI SPECTRA	209	OSM FEEDTHRU	2	
		OMNI SPECTRA	20020 P/C	TERMINATION WITH CHAIN	2	

BILL OF MATERIAL

☑ ELECTRICAL ☐ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 1 OF 2

MODULE # F6 NAME RF SPLITTER DWG # _____ SUB ASMB. DRIVER DWG # _____

SCHEMATIC DWG # _____ LOCATION _____ QUA/SYSTEM 1 PREPARED BY _____ APPROVED _____

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1	A1	ANY	7404N	IC	1	7
2	A2	ANALOG DEVICES	AD7512 KN	IC	1	7
3	Q1	ANY	2N2219	TRANSISTOR	1	7
4	Q2	ANY	2N2905	TRANSISTOR	1	7
5	Q3	ANY	2N3906	TRANSISTOR	1	7
6	D1, D3 D10	HEW PAC	5082-4955	GREEN LED	3	18
7	D2, D4 D9	" "	5082-4555	YELLOW LED	3	18
8	D5, D6	ANY	IN936	ZENER 0100E	2	
9	D7, D8	ANY	IN459	0100E	2	14
10	—	ROBINSON - NUGENT	ICN143-S3	14 PIN D'L SOCKET	2	14
11	C1, C2 C3	KEMET	CSR13E156KL	15 MF / 20V TANTALUM CAP	3	PR 4469
12	—	KEYSTONE	1562-2	TERMINAL	10	
13	R1, R2 R3, R4	BECKMAN	89PR10K	10K POT	4	
14	R5, R6 R7, R8	A-B		180 OHM, 1/4W, 5%	4	STOCK
15	R9, R10	A-B		18K, 1/4W, 5%	2	STOCK

BILL OF MATERIAL

☑ ELECTRICAL ☐ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 2 OF 2

MODULE # F6 NAME RF SPLITTER DWG # _____ SUB ASMB DRIVER DWG # _____

SCHEMATIC DWG # _____ LOCATION _____ QUA/SYSTEM 1 PREPARED BY _____ APPROVED _____

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
16	R11, R12 R13, R14	A-B		910 OHM, 1/4W, 5%	4	STOCK
17	R15, R16	A-B		560 OHM, 1/4W, 5%	2	
18	R17	A-B		2K, 1/4W, 5%	1	
19	R18	A-B		2.4K, 1/4W, 5%	1	
20	R19	A-B		10 OHM, 1/4W, 5%	1	
21	R20	A-B		110 OHM, 2W, 5%	1	
22	R21	A-B		68 OHM, 1/4W, 5%	1	

BILL OF MATERIAL

☑ ELECTRICAL ☐ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 1 OF 1

MODULE # F6 NAME RF SPLITTER DWG # _____ SUB ASMB. LOG DETECTOR DWG # _____

SCHEMATIC DWG # _____ LOCATION _____ QUA/SYSTEM 2 PREPARED BY _____ APPROVED _____

ITEM #	REF. DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1	A1	ANALOG DEVICES	AD504L	OP AMP	1	14
2	A2	ANALOG DEVICES	756N	OP AMP	1	15
3	A3	ANALOG DEVICES	AD741KN	OP AMP	1	7
4	—	ROBINSON-NUGENT	DP-5178-T	8 PIN TO-5 SOCKET	1	9
5	—	" "	ICN083-S3	8 PIN DIL SOCKET	1	9
6	—	CAMBION	450-3388-01-03	SOCKET PINS	9	
7	—	OMNI-SPECTRA	OSM 211	OSM BULKHEAD JACK	1	
8	C1, C2 C3	ERIE	8101-100-651-471M	470 PF/100V CAPACITOR	3	12
9	C4, C5	ERIE	8101-050-651-102M	1000 PF/50V "	2	20
10	C6, C7 C8	SPECTRUM CONTROL	FB-38-102W	1000 PF FEED-THRU CAPACITOR	3	30
11	C9, C10	KEMET	CSR13E156KL	15 MF/20V TANTALUM	2	
12	R1, R2 R5, R6	ANY	RN550	10K 1%	4	PR 4469
13	R3, R4 R9	ANY	RN550	100K 1%	3	"
14	R7, R8	ANY	RN550	150K 1%	2	"
15	R10	BECKMAN	63WR10K	10K 22 TURN POT	1	
16	R11	ANY	RN550	1K 1%	1	25
[redacted]17		[redacted]NE[redacted]		[redacted]L[redacted] [redacted]K[redacted]	4	

NATIONAL RADIO ASTRONOMY OBSERVATORY
Charlottesville, Virginia
VERY LARGE ARRAY PROJECT

SPECIFICATION NO: A13170N1, Rev. B

NAME: 4.4 - 5.1 GHz Transistor Amplifier

DATE: March 4, 1975

PREPARED BY: _____ APPROVED BY: _____

1. FREQUENCY RANGE AND GAIN

Within the 4.4 to 5.1 GHz range the gain must be 35 ±1 dB. The gain must be less than 37 dB at any frequency outside of this band.

2. NOISE FIGURE

Less than 7 dB.

3. POWER OUTPUT

+10 dBm at 1 dB compression.

4. INPUT AND OUTPUT VSWR

Less than 2:1.

5. DC POWER

+15 volts.

6. TEMPERATURE

15°C to 35°C

7. CONNECTORS

Type SMA female.

8. MOUNTING PROVISION

Tapped holes on one surface.

9. GAIN TEMPERATURE COEFFICIENT

The temperature coefficient of gain shall be less than 0.1 dB/°C from 20°C to 35°C.

MEASURED DATA

LOCUS Model RF-623A

Frequency (GHz)	Gain (dB)	Noise Figure (dB)	Input VSWR	Output VSWR	Output Power at 1.0dB Gain Compression (dBm)
4.4	35.1	5.8	<1.5:1	<1.48	+12.9
4.5	35.3	5.8			+13.4
4.6	35.6	5.9			+12.8
4.7	35.6	6.0			+12.3
4.8	35.2	6.2			+11.9
4.9	34.9	6.4			+12.0
5.0	35.3	6.8			+11.1
5.1	34.9	6.9			+10.3

Test Performed By: RM Jackman

Approved By: R.L Dunkle

Date: May 15, 1975

Serial # 4

+15 Vdc @ 154 ma

NATIONAL RADIO ASTRONOMY OBSERVATORY
Charlottesville, Virginia
VERY LARGE ARRAY PROJECT

SPECIFICATION NO: A13170N3, Rev. A

NAME: RF Splitter Network

DATE: July 14, 1975

PREPARED BY: _____ APPROVED BY: _____

1. General Description

A microwave integrated circuit containing four directional couplers, two PIN diode attenuators, two detectors, a diode transfer switch, and two power dividers is required; the desired configuration is shown in Figure 1. A deviation from this configuration in which monitor and detector couplers are exchanged in position is allowed. The unit will be used at power levels $\leq +20$ dBm, at a temperature of 25 $\pm$5°C, and must meet all specifications in the 4.3 to 5.2 GHz range.

2. Attenuation and Return Loss

The maximum loss from either input to a desired output is 10 dB with PIN diode attenuators at minimum attenutation. The minimum return loss at any RF input or output shall be 15 dB.

3. Detectors

The detector sensitivity into a 1K load shall be 20 to 40 μV per μw of network input power. The detector shall be unbiased, have negative output, and shall have a DC to 1 MHz frequency response. The detector shall be square-law within $\pm$1 dB for network input powers of up to -3 dBm and for a detector load resistor of 1K.

4. PIN Attenuator

The PIN attenuator shall be controllable from a single control terminal and shall have a 20 dB attenuation range. The frequency variation of loss at any attenuator setting shall be $\leq \pm 0.5$ dB and the return loss specification must be met at any attenuation. The switching speed shall be $\leq$100 μs. An input current of 4 mA shall produce $\geq$15 dB of attenuation.

5. Transfer Switch

The diode transfer switch must provide a minimum of 35 dB isolation and a switching speed of $\leq$ 100 µs. The control voltage shall be +3 volts for normal and -3 volts for transfer into a load resistance $\geq$ 50 ohms.

6. Monitor Couplers

The monitor couplers shall have coupling of 8 $\pm$2 dB referred to input and isolation $\geq$15 dB.

7. Output Power Dividers

The output power dividers shall have an isolation $\geq$20 dB and produce equal power within $\pm$0.5 dB.

8. Construction

The unit must be housed in an RFI-tight aluminum case having dimensions 0.69"x2.5"x6.75" excluding connectors. The printed circuit must be of rigid construction with high quality solder joints.

9. Connectors

All RF connections and detector outputs shall be type SMA female. Control lines shall be feed-thru capacitor solder terminals.

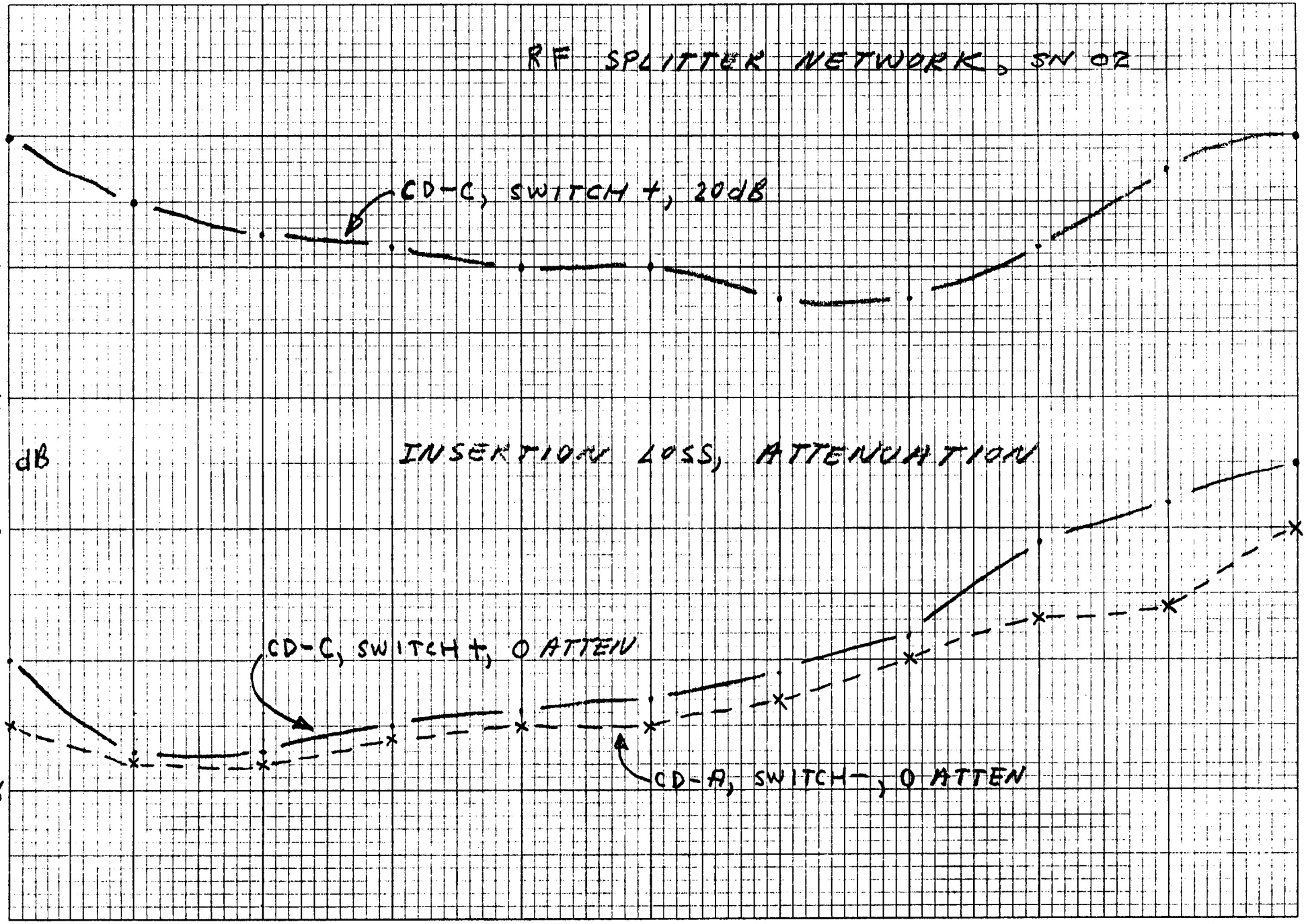
10. Drawings

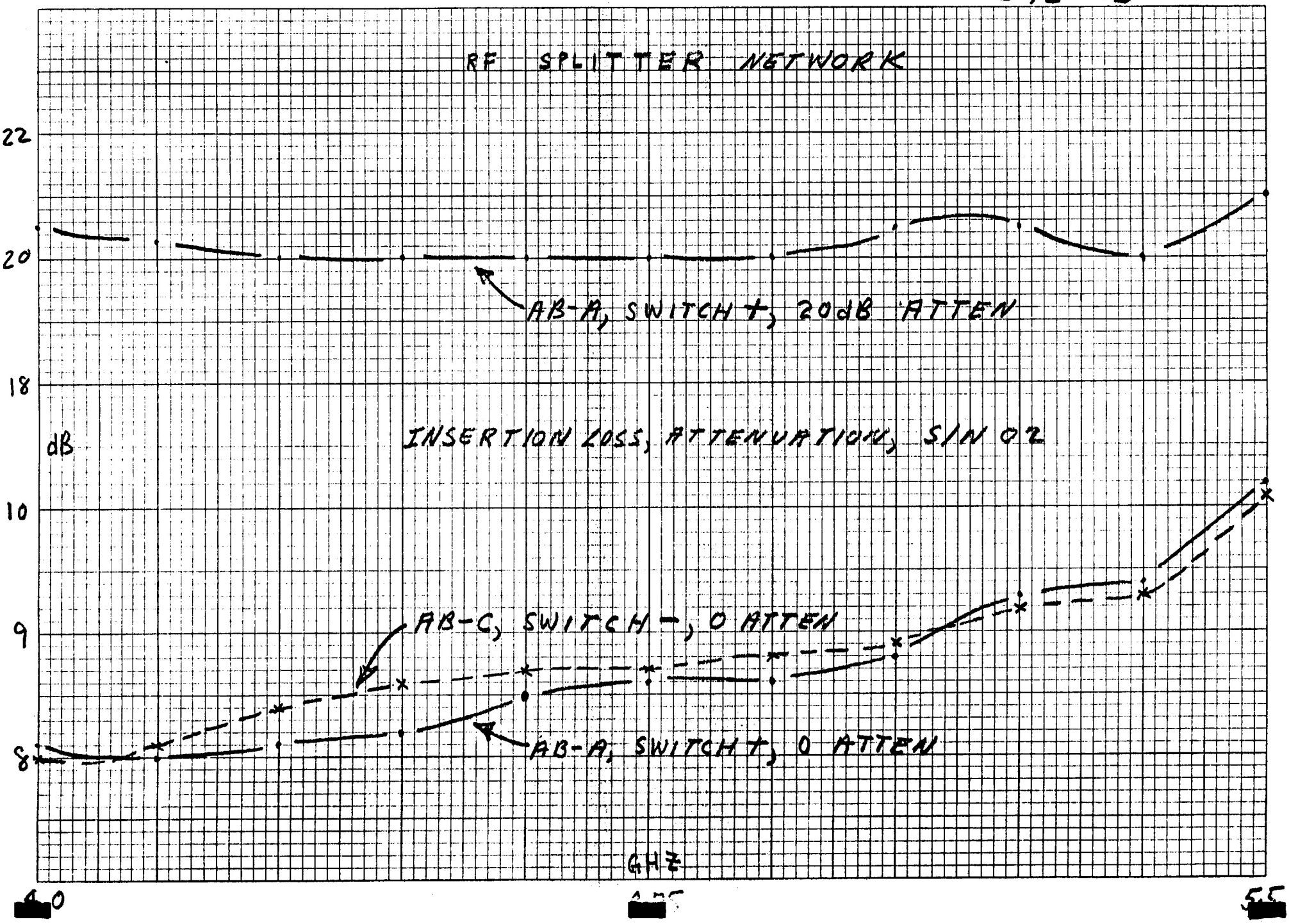
All artwork and reproducible copies of all drawings generated in manufacture shall be delivered with hardware.

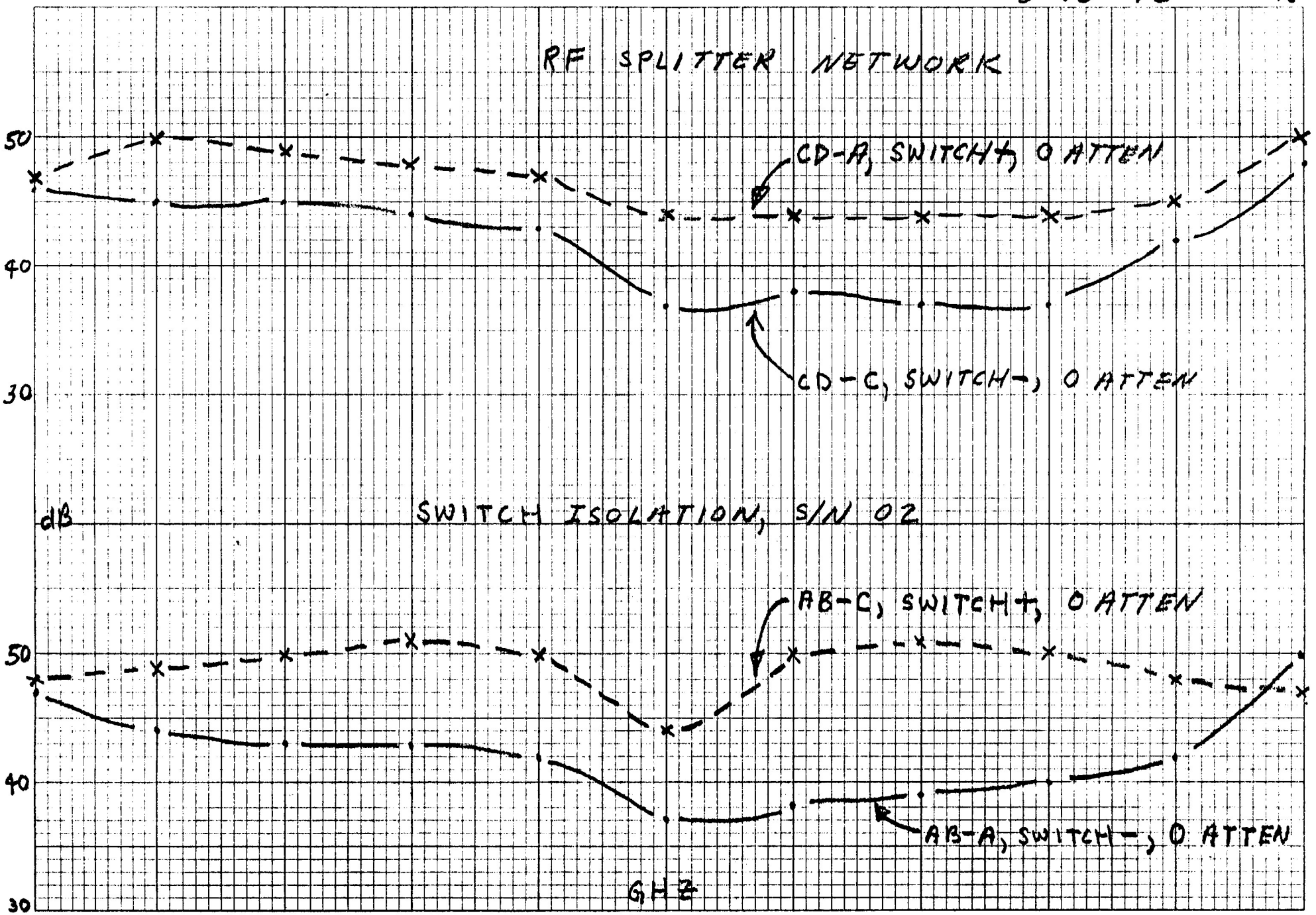
11. Test Data

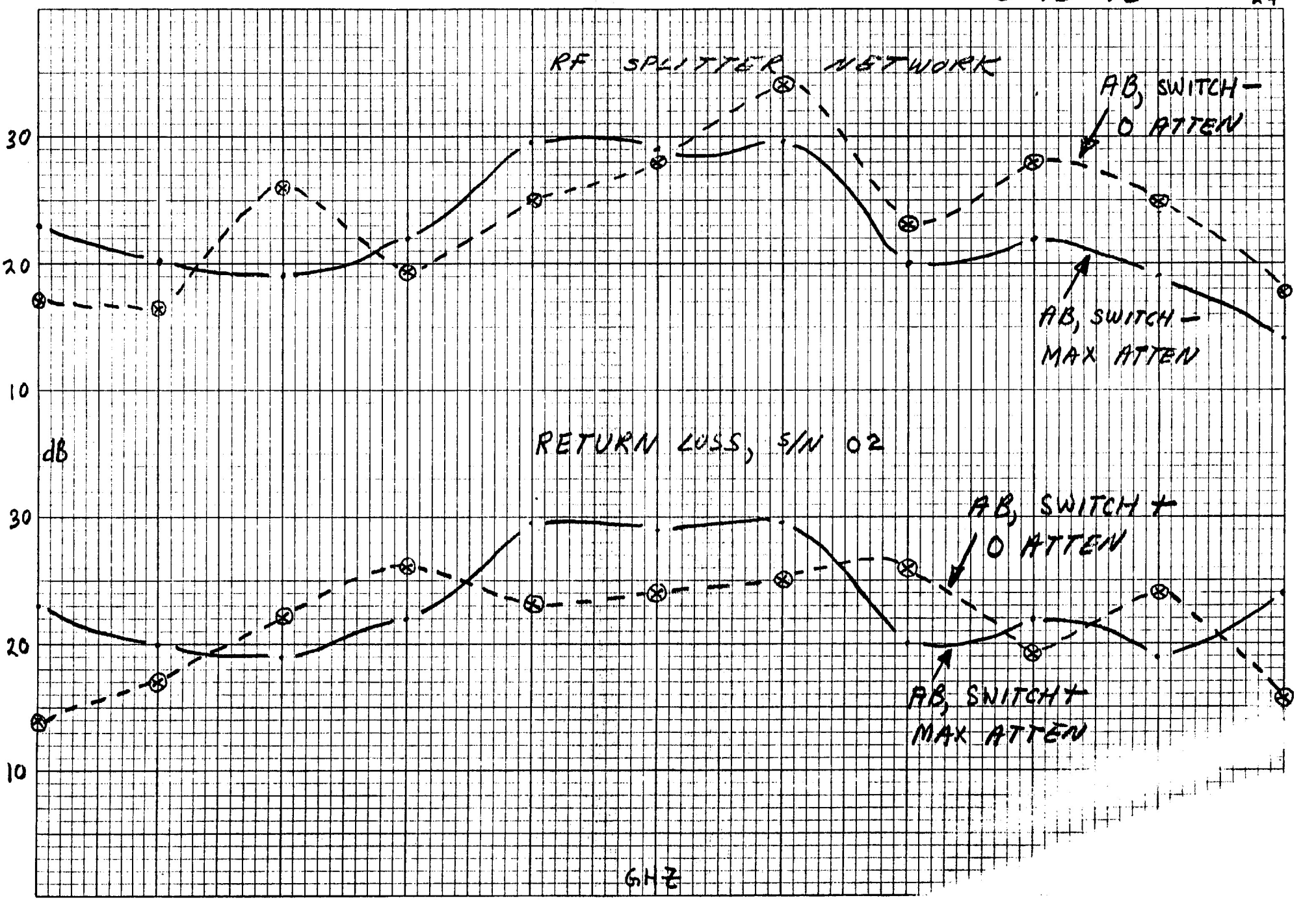
The following data must be provided for each unit in the 4.0 to 5.5 GHz range.

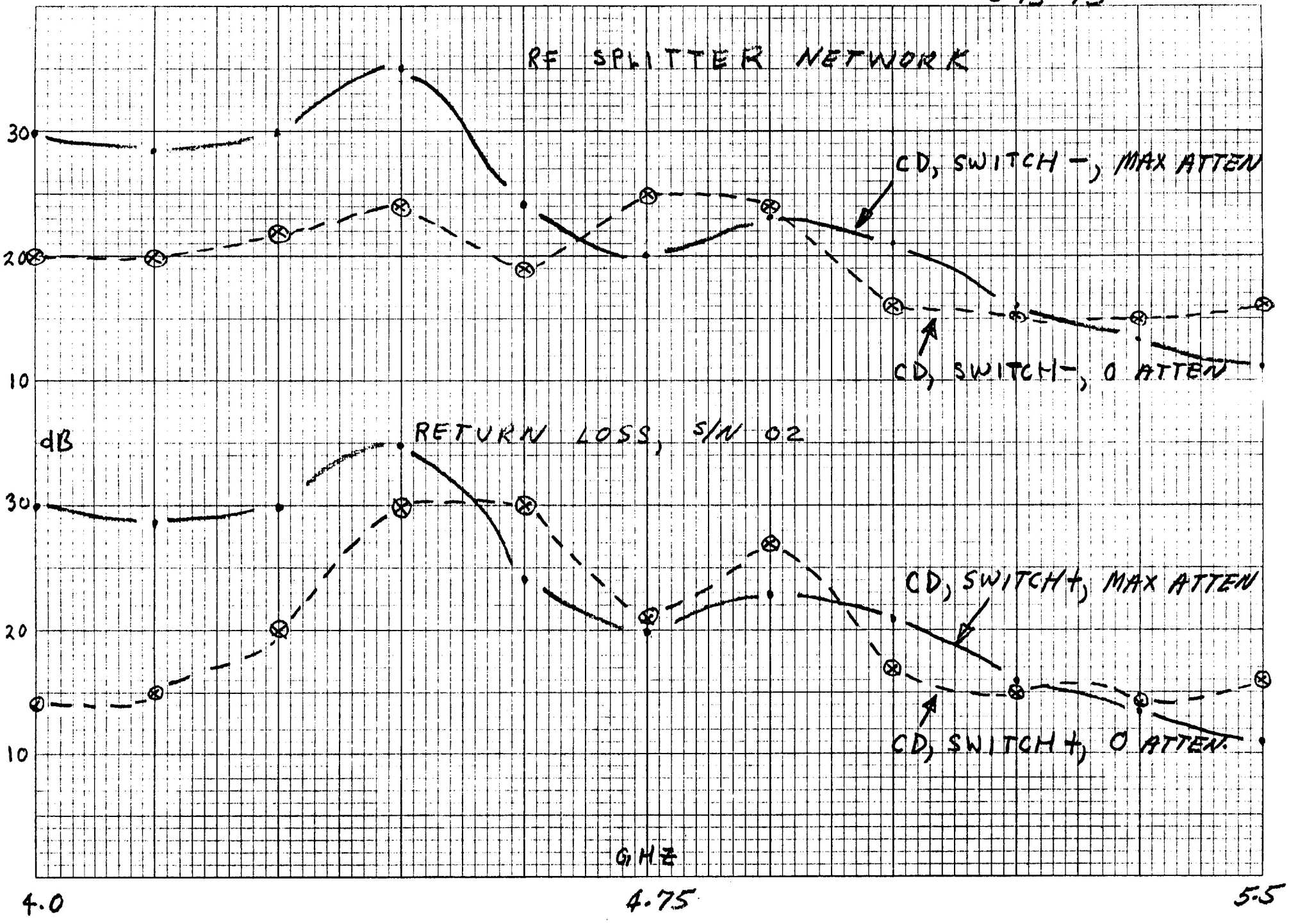
1) AB and CD return loss in normal and transfer mode with 0 dB and 20 dB PIN attenuator settings (8 curves).
2) AB to A and CD to C insertion loss in normal and transfer mode with 0 dB and 20 dB PIN attenuator settings (8 curves).
3) AB and CD detector output voltage at input levels of -20 dBm (2 curves).

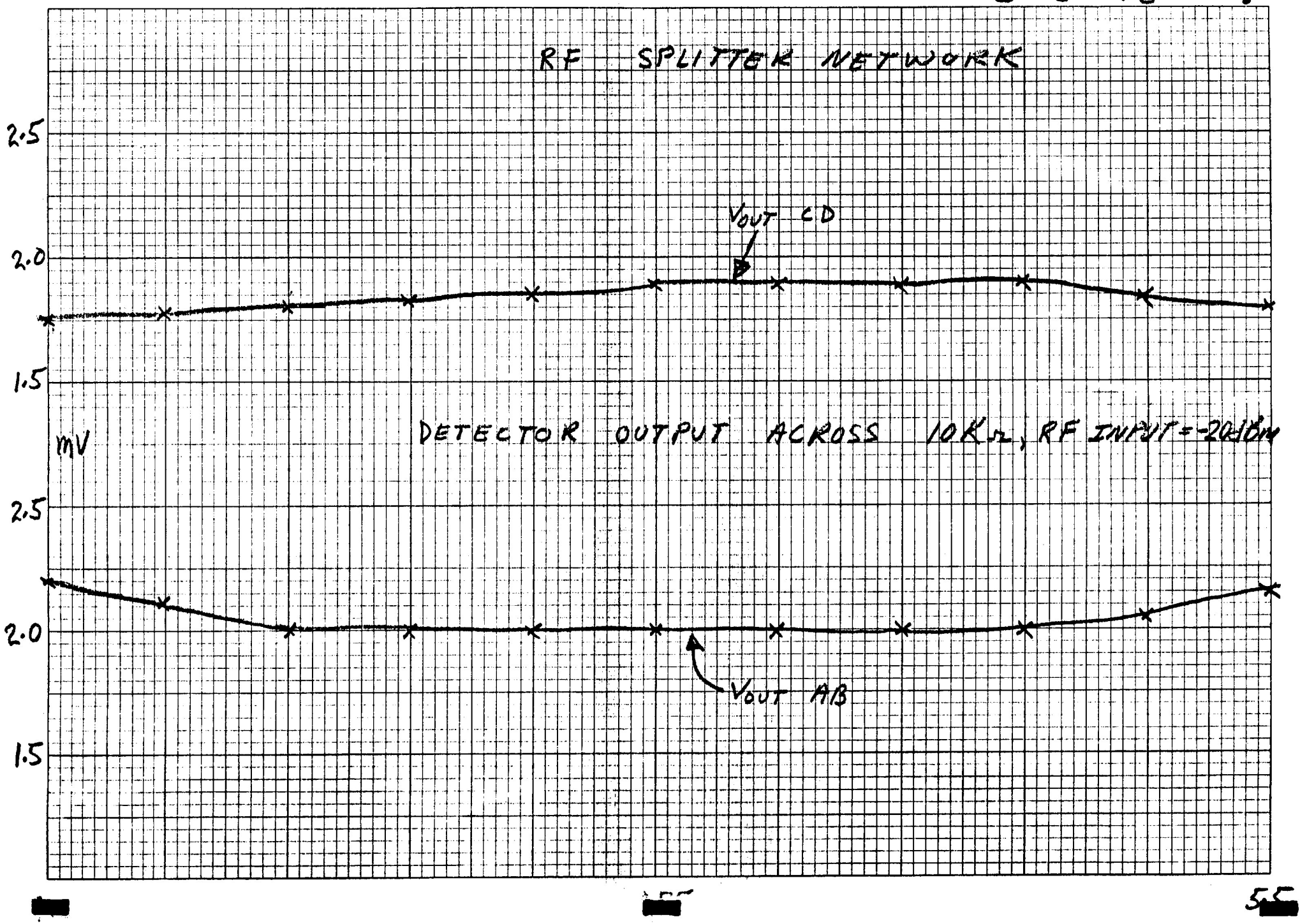

RF SPLITTER NETWORK, SN 02
CD-C, SWITCH +, 20dB
INSERTION LOSS, ATTENUATION
dB
22
20
18
10
9
8
CD-C, SWITCH +, 0 ATTEN
CD-A, SWITCH −, 0 ATTEN
4.0
4.75
5.5


RF SPLITTER NETWORK
22
20
18
dB
10
9
8
AB-A, SWITCH +, 20dB ATTEN
INSERTION LOSS, ATTENUATION, SIN 02
AB-C, SWITCH −, 0 ATTEN
AB-A, SWITCH +, 0 ATTEN
GHz
4.0
5.5


RF SPLITTER NETWORK
CD-A, SWITCH+, 0 ATTEN
CD-C, SWITCH-, 0 ATTEN
dB
SWITCH ISOLATION, S/N 02
AB-C, SWITCH+, 0 ATTEN
AB-A, SWITCH-, 0 ATTEN
GHz
50
40
30
50
40
30
4.0
4.75
5.5


RF SPLITTER NETWORK
AB, SWITCH – 0 ATTEN
AB, SWITCH – MAX ATTEN
RETURN LOSS, S/N 02
AB, SWITCH + 0 ATTEN
AB, SWITCH + MAX ATTEN
dB
30
20
10
30
20
10
GHZ


RF SPLITTER NETWORK
CD, SWITCH −, MAX ATTEN
CD, SWITCH −, 0 ATTEN
RETURN LOSS, S/N 02
dB
CD, SWITCH +, MAX ATTEN
CD, SWITCH +, 0 ATTEN.
30
20
10
30
20
10
GHz
4.0
4.75
5.5


RF SPLITTER NETWORK
2.5
2.0
1.5
mV
V_{OUT} CD
DETECTOR OUTPUT ACROSS 10KΩ, RF INPUT = -20dBm
2.5
2.0
1.5
V_{OUT} AB

ANALOG DEVICES

CMOS Dual SPDT Analog Switch

PRELIMINARY DATA SHEET

AD7512

FEATURES

- Two Independent SPDT Switches
- TTL/DTL/CMOS Direct Interface
- Power Dissipation: 30μW
- "ON" Resistance: 75Ω
- Silicon Nitride Passivation

GENERAL DESCRIPTION

The AD7512 consists of two independent analog SPDT switches switches on a monolithic CMOS chip. Packaging is a 14-pin ceramic or plastic DIP. All digital inputs are TTL/DTL and CMOS compatible with at least $10^9\Omega$ input impedance.

The extremely low power dissipation of 30μW is achieved by combining unique circuit design with state-of-the-art CMOS technology.

ABSOLUTE MAXIMUM RATINGS

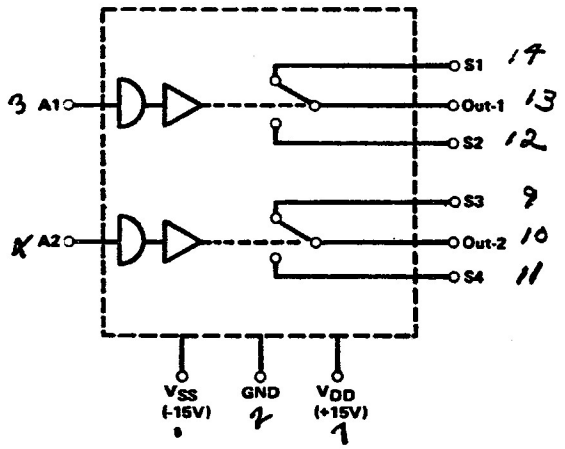
(T_A = +25°C unless otherwise noted)

V_{DD} (to GND)	+17V
V_{SS} (to GND)	-17V
Switch Voltage (to V_{SS})	+27V
Switch Voltage (to V_{DD})	-30V
Switch Current ($I_{D\text{-}out}$, Continuous)	30mA
Switch Current ($I_{D\text{-}out}$, Surge)	
1ms duration, 10% duty cycle	150mA
Digital Input Voltage Range	V_{SS} to V_{DD}
Power Dissipation (Package)	
14-pin Plastic DIP	
Up to +70°C	670mW
Derates above +70°C by	8.3mW/°C
14-pin Ceramic DIP	
Up to +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C

CAUTION:

1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when V_{SS} = V_{DD} = 0V all other pins should be at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

FUNCTIONAL DIAGRAM



Address "High" makes S2 to Out-1 and S3 to Out-2.

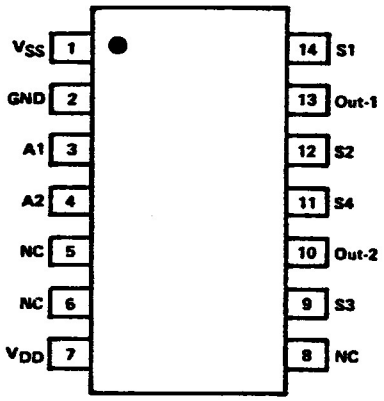
ORDERING INFORMATION

AD7512J:	0°C to +75°C
AD7512K:	0°C to +75°C
AD7512S:	-55°C to +125°C
AD7512T:	-55°C to +125°C

PACKAGE VERSIONS

Suffix "N"	Plastic DIP
Suffix "D"	Ceramic DIP
Suffix "F"	Flatpack (Special Request)

PIN CONFIGURATION (Top View)



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West Coast Tel: 213/595-1783
Mid-West Tel: 312/297-8710

SPECIFICATIONS (V_{DD} = +15 V, V_{SS} = −15 V, T_A = +25°C unless otherwise noted)

PARAMETER	VERSION	SWITCH	@ 25°C			OVER SPECIFIED TEMP. RANGE		UNITS	TEST CONDITIONS
			MIN	TYP	MAX	MIN	MAX		
ANALOG SWITCH									
R_{ON}	All	ON		70	100			Ω	−10 V ≤ V_S ≤ +10 V, I_S = 1.0 mA
R_{ON} vs. V_S	All	ON		20				%	
$\frac{\Delta R_{ON}}{\Delta T}$	All	ON		+0.5				%/°C	V_S = 0, I_S = 1.0 mA
R_{ON} Mismatch Between Switches	All	ON		1				%	
R_{ON} Mismatch Between Switches vs. Temperature	All	ON		0.01				%/°C	
I_S	J, K	OFF		0.5	5		500	nA	−10 V ≤ V_S ≤ +10 V and −10 V ≤ V_{OUT} ≤ +10 V
	S, T	OFF		0.2	3		200	nA	
I_{OUT}	J, K			1.5	15		1500	nA	
	S, T			0.6	9		600	nA	
$I_{OUT} - I_S$	All				20			nA	V_D = 0
DIGITAL CONTROL									
V_{INL}	All						0.8	V	
	J, S					3.0		V	
V_{INH} Note 1	K, T					2.4		V	
I_{INL} or I_{INH}	All			10				nA	
	J, K						100 typ	nA	
	S, T						1 typ	μA	
C_{IN}	All			5				pF	
DYNAMIC CHARACTERISTICS									
$t_{Transition}$	All			1.2				μs	
C_S	All	ON		28				pF	
C_S	All	OFF		8				pF	
C_{OUT}	All	–		28				pF	
C_S–OUT	All	OFF		0.5				pF	
C_{SS} Between Switches	All	–		0.5				pF	
C_{OUT}–OUT Between Switches	All	–		0.5				pF	
POWER SUPPLY									
I_{DD}				1	100			μA	All Digital Inputs Low
I_{SS}				1	100			μA	
I_{DD}				0.15	0.5			mA	All Digital Inputs High
I_{SS}				1	100			μA	
PRICE (1-49)									
	AD7512JN			8.00				$	
	AD7512JD			13.00				$	
	AD7512KN			9.00				$	
	AD7512KD			15.00				$	
	AD7512SD			22.00				$	
	AD7512TD			24.00				$	

NOTES:
1. A pullup resistor, typically 1-2 kΩ, is required to make the AD7512J and AD7512S compatible with TTL/DTL levels. The maximum value is determined by the output leakage current of the driver gate when in the high state.
2. Specifications subject to change without notice.

ANALOG DEVICES

Complete Log Ratio Module

PRELIMINARY TECHNICAL DATA

FEATURES
- Complete Log Ratio Module
- Provides Log Ratio of Current
- Provides Log Ratio of Voltage
- Dynamic Range of 7 Decades of Ratio

APPLICATIONS
- Log Ratio or Antilog Ratio of Voltages
- Log Ratio or Antilog Ratio of Currents
- Absorbance Measurements (see Figure 2)

GENERAL DESCRIPTION

Model 756 is a complete temperature compensated DC log ratio module, containing two channels for processing input variables. Channel 1 features a high quality FET amplifier with bias current of only 10pA. Using this input, signals spanning 4 decades can be processed with less than 1% error. By applying signals spanning up to 3 decades to channel 2, overall performance of 1% can be achieved for ratios covering a dynamic range of 10 million to 1 (7 decades).

Designed primarily for photometer applications, model 756 replaces two log modules, a subtractor, and associated circuitry. The signal sources for these applications are usually photo diodes which should be operated in the zero-volt mode (short circuit current). When connected as shown in Figure 2, the summing junctions provide virtual grounds, thereby forcing the input currents to be the short circuit current of the photo diodes.

PRINCIPLES OF OPERATION

CURRENT LOG RATIO

Current log ratio is accomplished by model 756 when two currents, I_{sig} and I_{ref}, are applied directly to the input terminals (see Figure 1). The two log amps process these signals providing voltages which are proportional to the log of their respective inputs. These voltages are then subtracted and applied to an output amplifier. The scale factor, when connected as shown, is 1V/dec. However, other scale factors may be achieved by using an external/feedback resistor for A_3 instead of the internal 15kΩ. The governing equation for this optional adjustment is:

$$R \approx \left(\frac{15k\Omega}{V}\right) K_{DES}$$

where R represents the total feedback resistance of A_3, and K_{DES} is the desired scale factor.

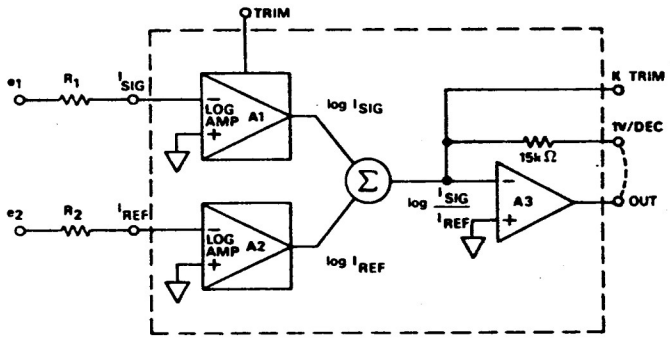

Figure 1. Functional Block Diagram of Model 756

VOLTAGE LOG RATIO

The principle of operation for voltage log ratio is identical to that of current log ratio after the voltage signal has been converted to a current. To accomplish this conversion, an external resistor is attached from the voltage signal to the appropriate input current terminal of the 756. Input currents are then determined by:

$$I_{sig} = \frac{e_1}{R_1}, \; I_{ref} = \frac{e_2}{R_2}$$

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SPECIFICATIONS (typical at +25°C and ±15V unless otherwise noted)

Current Log Ratio Transfer Equation

$$e_0 = -K \log \frac{i_1}{i_2}, \; i_1 = \text{sig}, \; i_2 = \text{ref}$$

Transfer Equation including Error Terms

$$e_0 = -K \left[\log \left(\frac{i_1 - I_{b1}}{i_2 - I_{b2}} \right) + E_{os3} \right]$$

Voltage Log Ratio Transfer Equation

$$e_0 = -K \log \left[\frac{e_1}{e_2} \times \frac{R_2}{R_1} \right]$$

Transfer Equation including Error Terms

$$e_0 = -K \left[\log \left(\frac{\frac{e_1 - E_{os1}}{R_1} - I_{b1}}{\frac{e_2 - E_{os2}}{R_2} - I_{b2}} \right) + E_{os3} \right]$$

Parameter	Value
Signal Current, i_1 [1]	10nA to 100μA (4 decades)
Reference Current, i_2 [1]	100nA to 100μA (3 decades)
Log Conformity[2]	±0.5% (2 decades, i_2 constant) ±1.0% (4 decades, i_2 constant)
Scale Factor, K[1,3]	1V ±1% ±0.04%/°C
Bias Current, I_{b1}	10pA, doubles/10°C
Bias Current, I_{b2}	10nA, max, ±1%/°C
Offset Voltage, E_{os1} [3]	±1mV, max, 25μV/°C
Offset Voltage, E_{os2}	0.5mV, max, 30μV/°C max
Output Offset, E_{os3} [3]	±10mV, max, 85μV/°C

Small Signal Response

i_{in}	f_t
1nA	1kHz
1μA	8kHz
100μA	25kHz

Slew Rate

i_{in} (increasing) time		i_{in} (decreasing) time	
1nA to 10nA	70μs	10nA to 1nA	200μs
10nA to 100nA	25μs	100nA to 10nA	50μs
100nA to 1μA	25μs	1μA to 100nA	25μs
1μA to 100μA	20μs	100μA to 1μA	20μs

Noise in 10kHz B.W.

V_n, INPUT 1	3μV rms
V_n, INPUT 2	3μV rms
I_n, INPUT 1	0.1pA rms
I_n, INPUT 2	20pA rms

Rated Output

Log Mode	±10V at 5mA
Antilog Mode	±10V at 4mA

Power

Quiescent Current	3mA at ±15V
Recommended Supply	Model 915[4]
PSRR	54dB
Package Size	1.5" x 1.5" x 0.4"
Price (1-9)	$75
(10-24)	$65

[1] Positive for positive inputs (N type), negative for negative inputs (P type).

[2] The log conformity specification is referred to input (R.T.I.). Note: 1% error R.T.I. is equivalent to 4.3mV of error at output for K = 1V.

[3] Externally trimmable.

[4] Model 915 is a 0.1% regulated dual 15V supply at 25mA. 1-9 price is $23. For higher current capability consider models 904 (50mA), 902 (100mA) or 920 at 200mA.

Specifications subject to change without notice.

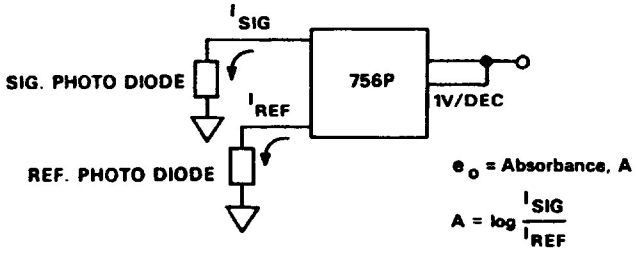
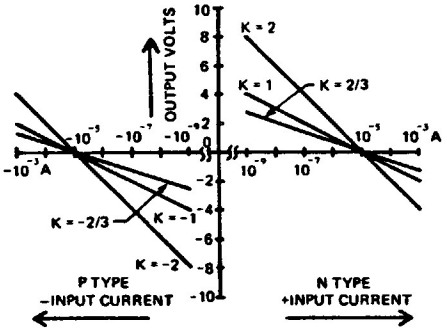


Figure 2. Photometry Application of Model 756

TRANSFER CURVES



Plot of output voltage vs. input current for Model 756 connected in log mode and I_{ref} = 10μA. To use the same curve for input voltage, calculate i_{in} as e_1/R_1 (see Figure 1).

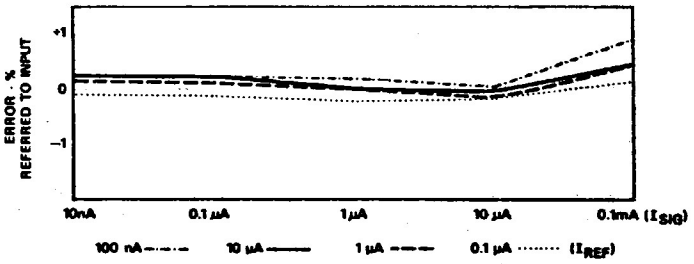
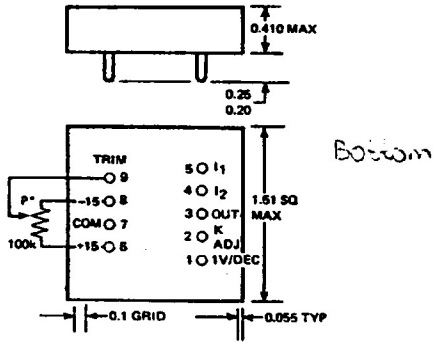


Figure 3. Typical % Error (R.T.I.) vs I_{sig} Over 7 Decades of $\frac{I_{sig}}{I_{ref}}$

OUTLINE DIMENSIONS (In Inches)



PIN VIEW

Pins: 0.040 $^{+0.002}_{-0.000}$ dia. spherical radius on ends, half-hard brass, gold plated per QQ-B-626.

Mating Socket AC1039 @ $3.00
*Ext 100k pot available from ADI Model #79PR100K at $3.00

LOW DRIFT, LOW NOISE OP AMP

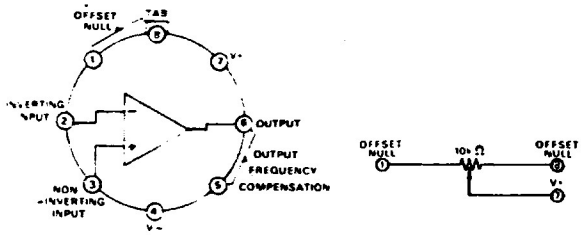
AD504

new product: AD504M

GENERAL DESCRIPTION

The AD504J, AD504K, AD504L, and AD504M are moderately priced operational amplifiers which combine ultra-low drift and noise and extremely high gain with the frequency response and slew rate of general purpose I.C. op amps. A new double integrator circuit concept combined with a precise thermally-balanced layout achieves maximum nulled offset drift below 0.5μV/°C, max input noise voltage of 0.6μV (p-p), and minimum gain of 10^6. Unity gain small signal bandwidth is 300kHz and the slew rate is 1.2V/μsec at a gain of 10. The amplifier is externally compensated for unity gain with a single 390pF capacitor; no compensation is required for gains above 500. The AD504 has fully protected inputs, which permit differential input voltages of up to $\pm V_S$ without voltage gain or bias current degradation due to reverse breakdown. The output is also protected from short circuits to ground and/or either supply voltage, and is capable of driving 1000pF of load capacitance. All models are specified for operation over the 0 to +70°C temperature range, and are supplied in the TO-99 can package.

PIN CONFIGURATION
Top View



TO-99

ELECTRICAL SPECIFICATIONS (Typical @ +25°C and ±15VDC, unless otherwise noted)

MODEL	AD504J	AD504K	AD504L	AD504M
OPEN LOOP GAIN				
V_{OS} = ±10V, $R_L \geq 2k\Omega$	250,000 min	500,000 min	10^6 min	10^6 min
@ T_A = 0°C to +70°C	125,000 min	250,000 min	500,000 min	500,000 min
OUTPUT CHARACTERISTICS				
Voltage @ $R_L \geq 2k\Omega$, T_A = 0°C to +70°C	±10V min (±13V typ)	•	•	•
Load Capacitance	1000pF	•	•	•
Output Current	10mA min	•	•	•
Short Circuit Current	25mA	•	•	•
FREQUENCY RESPONSE				
Unity Gain, Small Signal, C_c = 390pF	300kHz	•	•	•
Full Power Response, C_c = 390pF	1.5kHz	•	•	•
Slew Rate, Unity Gain, C_c = 390pF	0.12V/μsec	•	•	•
INPUT OFFSET VOLTAGE				
Initial Offset, $R_S \leq 10k\Omega$	2.5mV max	1.5mV max	0.5mV max	0.5mV max
vs. Temp., T_A = 0°C to +70°C, V_{OS} nulled	5.0μV/°C max	3.0μV/°C max	1.0μV/°C max	0.5μV/°C max
T_A = 0°C to +70°C, V_{OS} unnulled (Note 1)	10μV/°C max	5.0μV/°C max	2.0μV/°C max	1.0μV/°C max
vs. Supply	25μV/V max	15μV/V max	10μV/V max	10μV/V max
@ T_A = 0°C to +70°C	40μV/V	25μV/V max	15μV/V max	15μV/V max
vs. Time	20μV/mo	15μV/mo	10μV/mo	10μV/mo
INPUT OFFSET CURRENT				
@ T_A = +25°C	40nA max	15nA max	10nA max	10nA max
INPUT BIAS CURRENT				
Initial	200nA max	100nA max	80nA max	80nA max
@ T_A = 0°C to +70°C	300nA max	150nA max	100nA max	100nA max
vs. Temp., T_A = 0°C to +70°C	300pA/°C	250pA/°C	200pA/°C	200pA/°C
INPUT IMPEDANCE				
Differential	0.5MΩ	1.0MΩ	1.3MΩ	1.3MΩ
Common Mode	100MΩ‖4pF	•	•	•
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	1.0μV (p-p)	•	•	0.6μV (p-p) max
f = 100Hz	10nV/√Hz (rms)	•	•	10nV/√Hz (rms) max
f = 1kHz	8nV/√Hz (rms)	•	•	9nV/√Hz (rms) max
Current, f = 10Hz	1.0pA/√Hz (rms)	•	•	1.3pA/√Hz (rms) max
f = 100Hz	0.6pA/√Hz (rms)	•	•	0.6pA/√Hz (rms) max
f = 1kHz	0.5pA/√Hz (rms)	•	•	0.3pA/√Hz (rms) max
INPUT VOLTAGE RANGE				
Differential or Common Mode, max safe	$\pm V_S$	•	•	•
Common Mode Rejection, V_{in} = ±10V	94dB min	100dB min	110dB min	110dB min
POWER SUPPLY				
Rated Performance	±15V	•	•	•
Operating	±(5 to 18)V	•	•	•
Current, Quiescent	±4.0mA max	±3.0mA max	±3.0mA max	±3.0mA max
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	•	•	•
Storage	-65°C to +150°C	•	•	•
PRICE				
(1–24)	$11.20	$19.80	$28.00	$30.00
(25–99)	9.55	16.80	21.80	23.80
(100–999)	8.40	15.30	20.40	22.00

NOTES:
[1] This parameter is not 100% tested. Typically, 90% of the units meet this limit.
*Specifications same as for AD504J.

ANALOG DEVICES

Lowest Cost High Accuracy IC Op Amps

AD741J,K,L,S

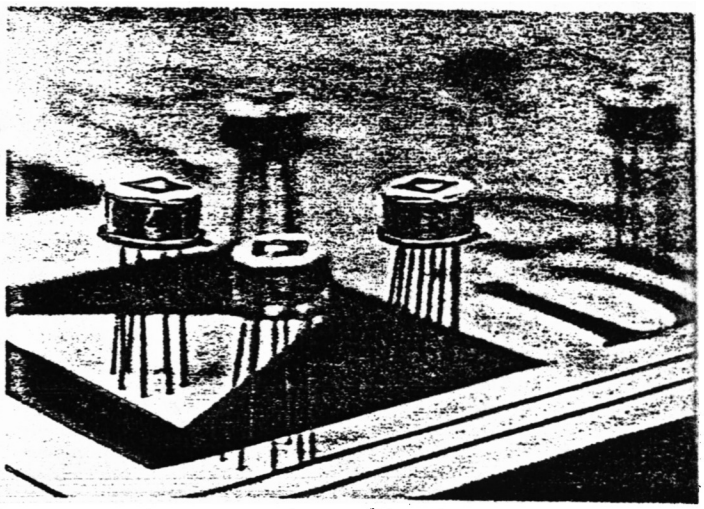
FEATURES

Precision Input Characteristics
- Low V_{OS}: 0.5mV max (L)
- Low V_{OS} Drift: 5μV/°C max (L)
- Low I_b: 50nA max (L)
- Low I_{OS}: 5nA max (L)
- High CMRR: 90dB min (K, L)

High Output Capability
- A_{OL} = 25,000 min, 1kΩ load (J, S)
  T_{min} to T_{max}
- V_O = ±10V min, 1kΩ load (J, S)

Low Cost (100 pieces)

AD741J	$1.25
AD741K	$2.25
AD741L	$6.00
AD741S	$3.30



GENERAL DESCRIPTION

The Analog Devices AD741J, AD741K, AD741L and AD741S are specially tested and selected versions of the popular AD741 operational amplifier. Improved processing and additional electrical testing guarantee the user precision performance at a very low cost. The AD741J, K and L substantially increase overall accuracy over the standard AD741C by providing maximum limits on offset voltage drift, and significantly reducing the errors due to offset voltage, bias current, offset current, voltage gain, power supply rejection, and common mode rejection (see Error Analysis). For example, the AD741L features maximum offset voltage drift of 5μV/°C, offset voltage of 0.5mV max, offset current of 5nA max, bias current of 50nA max, and a CMRR of 90dB min. The AD741S offers guaranteed performance over the extended temperature range of −55°C to +125°C, with max offset voltage drift of 15μV/°C, max offset voltage of 4mV, max offset current of 25nA, and a minimum CMRR of 80dB.

HIGH OUTPUT CAPABILITY

Both the AD741J and AD741S offer the user the additional advantages of high guaranteed output current and gain at low values of load impedance. The AD741J guarantees a minimum gain of 25,000, swinging ±10V into a 1kΩ load from 0°C to +70°C. The AD741S guarantees a minimum gain of 25,000, swinging ±10V into a 1kΩ load from −55°C to +125°C.

All devices feature full short circuit protection, high gain, high common mode range, and internal compensation. The AD741J, K and L are specified for operation from 0°C to +70°C, and are available in both the TO-99 and mini-DIP packages. The AD741S is specified for operation from −55°C to +125°C, and is available in the TO-99 package.

GUARANTEED ACCURACY

The vastly improved performance of the AD741J, AD741K, AD741L and AD741S provides the user with an ideal choice when precision is needed and economy is a necessity. An error budget is calculated for all versions of the AD741 (see page 3); it is obvious that these selected versions offer substantial improvements over the industry-standard AD741C and AD741. A typical circuit configuration (see Figure 1) is assumed, and the various errors are computed using maximum values over the full operating temperature range of the devices. *The results indicate a factor of 8 improvement in accuracy of the AD741L over the AD741C, a factor of 5 improvement using the AD741K, and a factor of 2.5 improvement using the AD741J. The AD741S, similarly, achieves a factor of 3.5 improvement over the standard AD741.* Note that the total error has been determined as a sum of component errors, while in actuality, the total error will be much less. Also, while the circuit used for the error analysis is only one of a multitude of possible applications, it effectively demonstrates the great improvement in overall 741 accuracy achievable at relatively low cost with the AD741J, K, L or S.

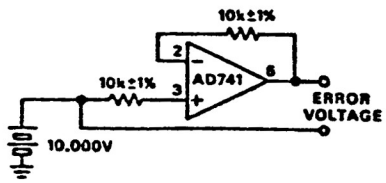


Figure 1. Error Budget Analysis Circuit

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Tel: 617/329-4700 TWX: 710/394-6577

SPECIFICATIONS (typical @ +25°C and ±15VDC, unless otherwise specified)

MODEL	AD741J	AD741K	AD741L	AD741S
OPEN LOOP GAIN				
R_L = 1kΩ, V_O = ±10V	50,000 min (200,000 typ)			*
R_L = 2kΩ, V_O = ±10V		50,000 min (200,000 typ)	50,000 min (200,000 typ)	
Over Temp Range, T_{min} to T_{max}, same loads as above	25,000 min	*	*	*
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 1kΩ, T_{min} to T_{max}	±10V min (±13V typ)			*
Voltage @ R_L = 2kΩ, T_{min} to T_{max}		±10V min (±13V typ)	±10V min (±13V typ)	
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1MHz	*	*	*
Full Power Response	10kHz	*	*	*
Slew Rate, Unity Gain	0.5V/μsec	*	*	*
INPUT OFFSET VOLTAGE				
Initial, $R_S \leq$ 10kΩ (adjustable to zero)	3mV max (1mV typ)	2mV max (0.5mV typ)	0.5mV max (0.2mV typ)	2mV max (1mV typ)
T_{min} to T_{max}	4mV max	3mV max	1mV max	*
Avg vs Temperature (untrimmed)	20μV/°C max	15μV/°C max (6μV/°C typ)	5μV/°C max (2μV/°C typ)	15μV/°C max (6μV/°C typ)
vs Supply, T_{min} to T_{max}	100μV/V max (30μV/V typ)	15μV/V max (5μV/V typ)	15μV/V max (5μV/V typ)	*
INPUT OFFSET CURRENT				
Initial	50nA max (5nA typ)	10nA max (2nA typ)	5nA max (2nA typ)	10nA max (2nA typ)
T_{min} to T_{max}	100nA max	15nA max	10nA max	25nA max
Avg vs Temperature	0.1nA/°C	0.2nA/°C max (0.02nA/°C typ)	0.1nA/°C max (0.02nA/°C typ)	0.25nA/°C max (0.1nA/°C typ)
INPUT BIAS CURRENT				
Initial	200nA max (40nA typ)	75nA max (30nA typ)	50nA max (30nA typ)	75nA max (30nA typ)
T_{min} to T_{max}	400nA max	120nA max	100nA max	250nA max
Avg vs Temperature	0.6nA/°C	1.5nA/°C max (0.6nA/°C typ)	1nA/°C max (0.6nA/°C typ)	2nA/°C max (0.6nA/°C typ)
INPUT IMPEDANCE				
Differential	1MΩ	2MΩ	2MΩ	2MΩ
INPUT VOLTAGE RANGE (Note 1)				
Differential, max safe	±30V	*	*	*
Common Mode, max safe	±15V	*	*	*
Common Mode Rejection, $R_S \leq$ 10kΩ, T_{min} to T_{max}, V_{in} = ±12V	80dB min (90dB typ)	90dB min (100dB typ)	90dB min (100dB typ)	*
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	±(5 to 22)V	±(5 to 22)V	±(5 to 22)V
Current, Quiescent	3.3mA max (2.0mA typ)	2.8mA max (1.7mA typ)	2.8mA max (1.7mA typ)	2.8mA max (2.0mA typ)
TEMPERATURE RANGE				
Operating, Rated Performance	0°C to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

*Specifications same as AD741J.

Specifications subject to change without notice.

OUTPUT CHARACTERISTICS

The AD741J and AD741S are specially selected for high output current capability. High efficiency output transistors, thermally balanced chip design and precise short circuit current control insure against gain degradation at high current levels and temperature extremes. The AD741J guarantees a minimum gain of 25,000, swinging ±10V into a 1kΩ load from 0°C to +70°C. The AD741S guarantees minimum gain of 25,000, swinging ±10V into a 1kΩ load from −55°C to +125°C. The AD741K and AD741L are guaranteed with the standard 2kΩ load.

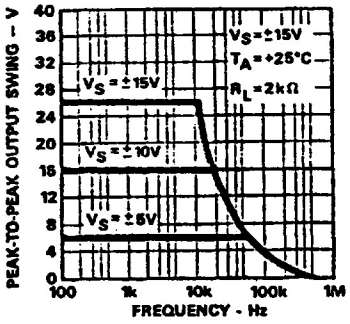


Figure 8. Output Voltage Swing vs. Frequency

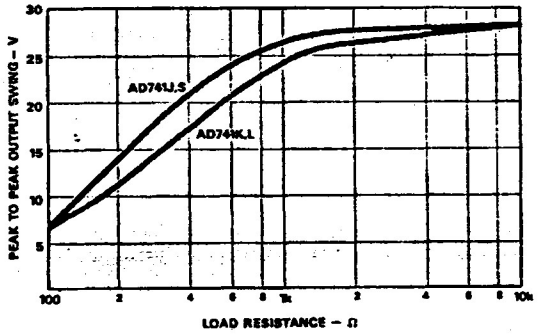


Figure 9. Output Voltage Swing vs. Load Resistance

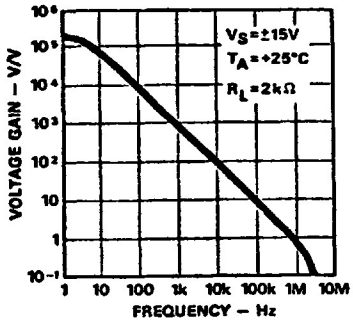
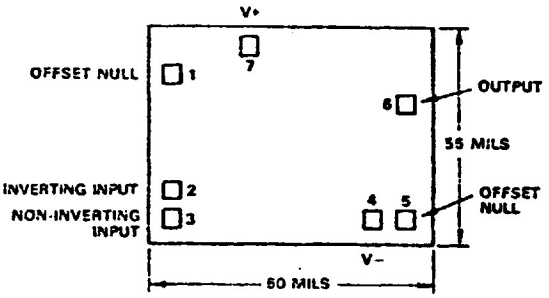


Figure 10. Open Loop Gain vs. Frequency

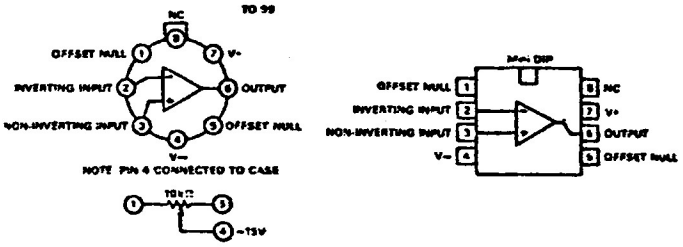
BONDING DIAGRAM

All versions of the AD741 are available in chip or wafer form, fully tested at +25°C. Because of the critical nature of using unpackaged devices, it is suggested that the factory be contacted for specific information regarding price, delivery and testing.



CONNECTION DIAGRAMS

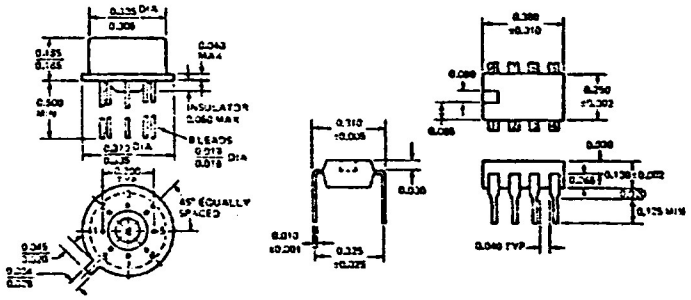
(Top View)



(H package) (N package)

PHYSICAL DIMENSIONS

(In Inches)



MIL-STANDARD-883

The AD741S is available with 100% screening to MIL-STD-883, Method 5004, Class A, B, or C. Consult the factory for pricing and delivery.

ORDERING GUIDE

MODEL	TEMP. RANGE	ORDER NUMBER	PRICE (1–24)	PRICE (25–99)	PRICE (100–999)
AD741J	0°C to +70°C	AD741J*	$1.85	$1.50	$1.25
AD741K	0°C to +70°C	AD741K*	$3.40	$2.70	$2.25
AD741L	0°C to +70°C	AD741L*	$9.00	$7.20	$6.00
AD741S	−55°C to +125°C	AD741SH	$4.95	$4.00	$3.30

*Add Package Type Letter; H = TO-99, N = Mini-DIP.

ERROR BUDGET ANALYSIS

PARAMETER	AD741C SPEC (0°C to +70°C)	AD741C ERROR	AD741J SPEC (0°C to +70°C)	AD741J ERROR	AD741K SPEC (0°C to +70°C)	AD741K ERROR	AD741L SPEC (0°C to +70°C)	AD741L ERROR	AD741 SPEC (−55°C to +125°C)	AD741 ERROR	AD741S SPEC (−55°C to +125°C)	AD741S ERR
Gain (*Error = $10V_{in}/G$*)	15,000	660μV	25,000[1]	400μV	25,000	400μV	25,000	400μV	25,000	400μV	25,000[1]	400μV
I_b (*Error = I_b x resistor mismatch*)	800nA	160μV	400nA	80μV	120nA	24μV	100nA	20μV	1500nA	300μV	250nA	50μV
I_{os} (*Error = I_{os} x 10kΩ*)	300nA	3000μV	100nA	1000μV	15nA	150μV	10nA	100μV	500nA	5000μV	25nA	250μV
$\Delta V_{os}/\Delta T$ (*Error = $\Delta V_{os}/\Delta T \times \Delta T$*)	25μV/°C[2]	1125μV	20μV/°C	900μV	15μV/°C	675μV	5μV/°C	225μV	25μV/°C[2]	2500μV	15μV/°C	1500μV
CMRR (*Error = 10V/CMRR*)	70dB	3300μV	80dB	1000μV	90dB	330μV	90dB	330μV	70dB	3300μV	80dB	1000μV
PSRR (*assume a ±5% power supply variation*)	150μV/V	450μV	100μV/V	300μV	15μV/V	45μV	15μV/V	45μV	150μV/V	450μV	100μV/V	300μV
TOTAL		8.7mV		3.7mV		1.6mV		1.1mV		12.0mV		3.5mV
PRICE (*100 pieces*)	$1.00		$1.25		$2.25		$6.00		$2.00		$3.30	

[1] AD741J and AD741S...Open Loop Gain is guaranteed with a 1kΩ load.
[2] AD741C and AD741..$\Delta V_{OS}/\Delta_T$ is not guaranteed (for complete specifications, contact the factory for data sheet).

INPUT CHARACTERISTICS

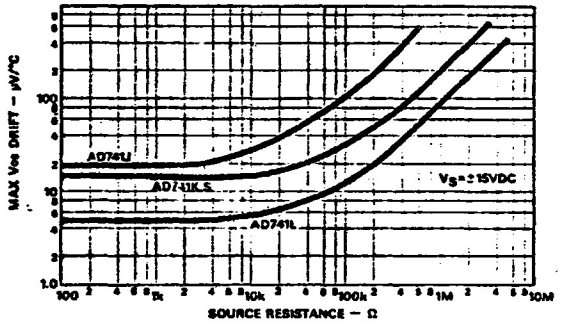


Figure 2. Max Equivalent Input Offset Drift vs. Source Resistance

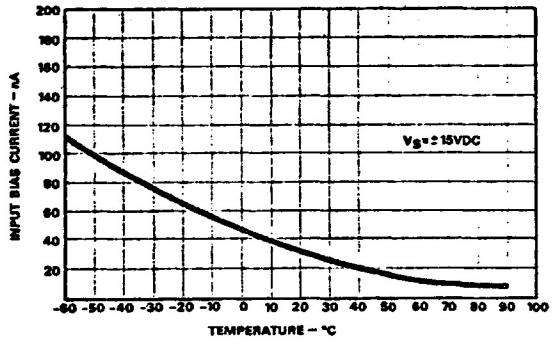


Figure 3. Input Bias Current vs. Temperature

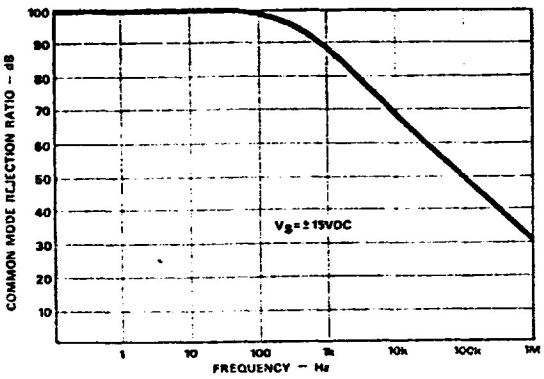


Figure 4. Common Mode Rejection vs. Frequency

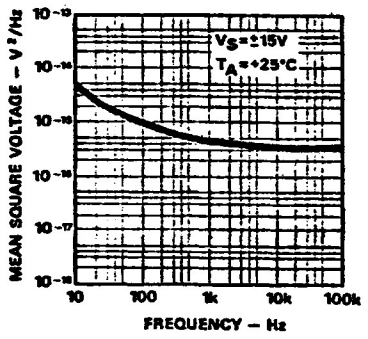


Figure 5. Input Noise Voltage vs. Frequency

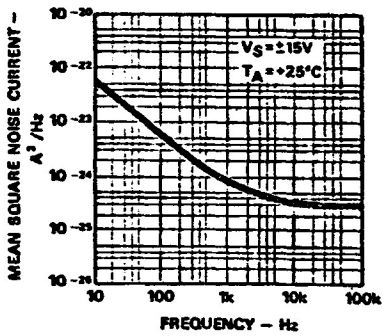


Figure 6. Input Noise Current vs. Frequency

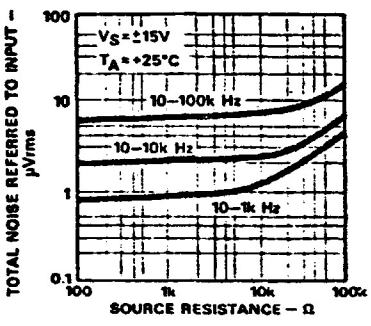


Figure 7. Broadband Noise vs. Source Resistance