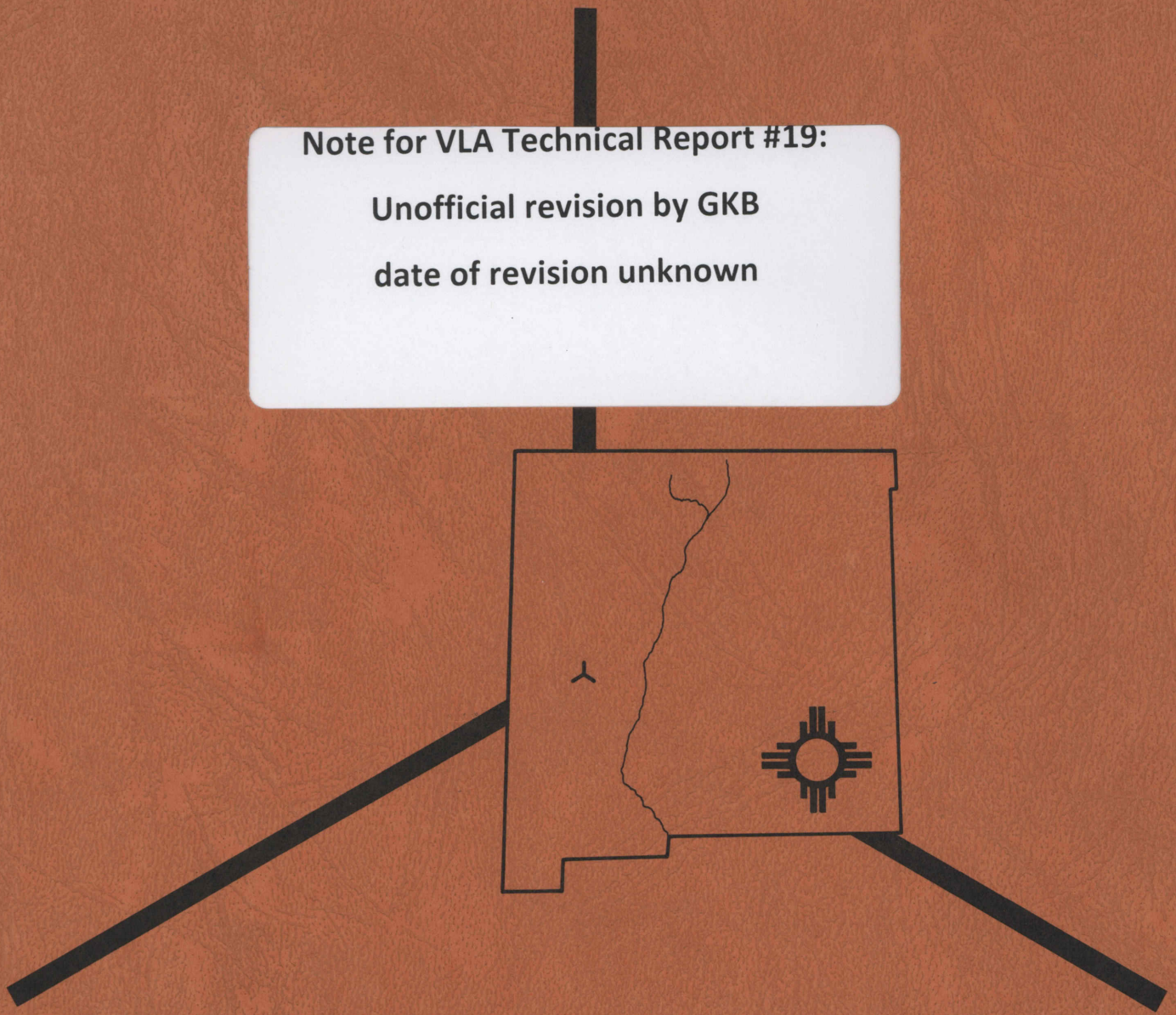
GKB

VERY LARGE ARRAY TECHNICAL REPORT

Note for VLA Technical Report #19:

Unofficial revision by GKB

date of revision unknown



NATIONAL RADIO ASTRONOMY OBSERVATORY
P.O. Box O, Socorro, New Mexico 87801

OPERATED BY ASSOCIATED UNIVERSITIES, INC.
UNDER CONTRACT WITH THE NATIONAL SCIENCE FOUNDATION

Note for VLA Technical Report #19:

Unofficial revision by GKB

date of revision unknown

VLA TECHNICAL REPORT #19

MODULE F5
CONTROL INTERFACE MODULE MANUAL

Garey Barrell

September 1975

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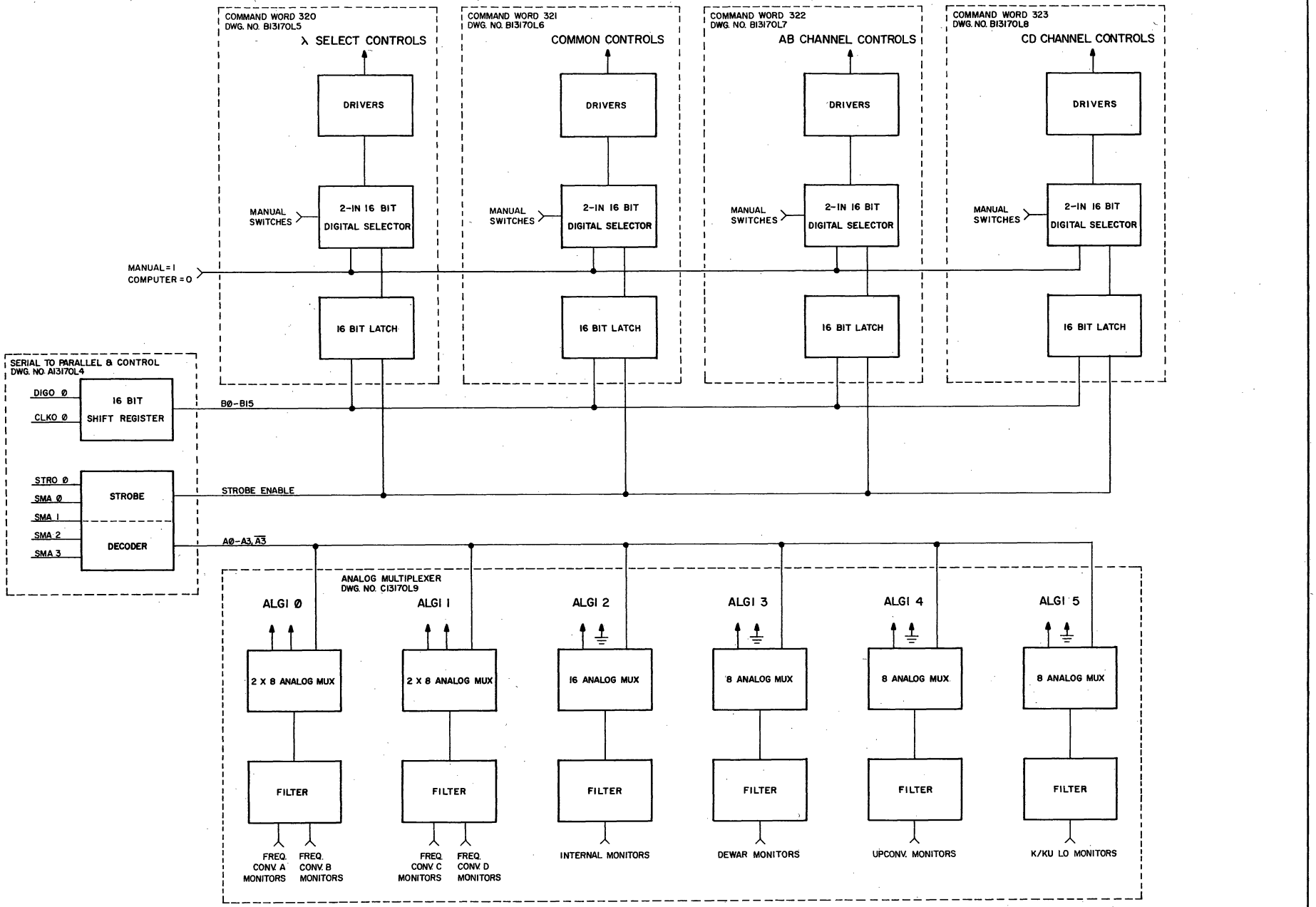


REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

VLA PROJECT: FRONT END

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

TITLE: CONTROL INTERFACE F5
BLOCK DIAGRAM

DRAWN BY E.J. Mufson	DATE 5-14-75	
DESIGNED BY G.K. Bansell	DATE 6-19-75	
APPROVED BY G.K. Bansell	DATE 6-18-75	
SHEET NUMBER	DRAWING NUMBER C13170L10	REV. / SCALE

III. THEORY OF OPERATION

The Control Interface module, F5, provides for both local (at the front end rack) and remote (at the central computer) control of the operation of the front end. Additionally, a series of analog AND DIGITAL monitor points within the front end may be remotely selected and displayed by the central computer. This module contains the circuitry to interface between the front end and the VLA monitor and control system.

Description of the monitor and control system, for the purposes of this manual, will be limited to the input/output interface between the Data Set and Control Interface module installed in the individual front end rack.

The data set module includes a variety of digital and analog circuitry to allow both digital and analog monitoring as well as digital control of the associated electronics. ~~There are currently no requirements in this rack for digital monitoring capabilities, therefore only the analog monitor and digital control facilities are employed.~~

Computer data for the controls is presented to the Control Interface module in the form of a serial string of 24 bit digital words. Two control bits, CLKO Ø and STRO Ø are also provided. The remaining outputs from the data set are the four sub multiplex address bits, SMA Ø, SMA 1, SMA 2, and SMA 3. The SMA bits perform a dual function, enabling selection of a specific 24 bit digital control word as well as selecting a particular analog monitor point.

1. Serial to Parallel Converter and Control (DWG #A13170L4)

   Control data from the data set is applied to this circuit and operated upon as follows. The digital input string (DIGO Ø) is inverted, buffered, and applied to the serial input of a 16 bit shift register. The data is clocked into the register via the CLKO Ø signal from the data set. Since only 16 of the 24 available bits are employed in this particular module, bit Ø (LSB) appears at parallel output B Ø and bit 16 appears at B15. Bits 17 through 24 (MSB) are shifted through and lost.

The sub multiplex address signals, SMA Ø - SMA3, are inverted and buffered and applied directly to the analog multiplexers. A fifth control is developed, $\overline{\text{SMA 3}}$, and is used to inhibit unselected analog multiplexers. This data is also converted to a one-of-four word enable by a decoder and buffer under control of strobe signal STRO Ø. The enable signal is a 2.5μ sec. wide logic 1 coincident with the strobe pulse.

2. Command Word Latches and Controls (DWGS #A13170L5, L6, L7 & L8)

There are four essentially identical word latches in this module. The description that follows will be limited primarily to word 321 which contains a representative sample of circuitry contained in all four words.

Parallel data bits B Ø through B 15 are continuously applied to the inputs of a 16 bit latch consisting of four 7475 LS IC's. The command word enable line is at a logic Ø normally until the SMA code for word 321 is received coincident with a STRO Ø pulse. When the command word enable line goes to a logic 1, the latch "looks" at the 16 input lines, and on the falling edge of this pulse, "holds" the data present at that time. This data is then held by the latch until the next command word enable is received. The timing relationships of these signals are shown in ~~Figure 1.~~ THE DATA SET MANUAL, VLA TECHNICAL REPORT NO. 30, TIMING DIAGRAM 8

The 16 bits of latched data are then presented to the inputs of a 2-in 16 bit digital selector consisting of four 74157 IC's. Inversion of data can be accomplished at this point by selection of either the inverting or non-inverting data outputs from the 7475 LS chips. The other set of inputs are connected to front panel switches to provide for manual control of all functions. Selection of manual (module front panel switches) or computer control is determined by the computer-manual switch on the module front panel (DWG. A13170L2). The mode selected is displayed by two LED indicators on either side of this switch. Indication of the mode selected is also fed to the monitor system to allow the computer operator to determine that the switch has not been inadvertantly left in the manual position by service personnel.

The 16 outputs of the digital selectors are then connected to appropriate interface circuits for the function to be controlled. In some cases no special signal conditioning is required and the TTL line is used directly. The 75461 is a dual open-collector output capable of sinking up to 300 MA and has a VCBO of 40V. The 75326 used as a coax switch driver is a quad open collector driver capable of sinking up to 600 MA and has a VCEO of 25V. Internal clamping diodes are included on this chip. The 75450 is a dual power driver capable of sinking 300 MA and has a VCEO of 30V. In this chip all three of the leads for each power transistor are brought out of the package. This feature is used to drive an external power transistor to sink the 1.0 amp current required to operate the LO waveguide swtich.

3. Calibration/Reference Control (DWG #A13170L1)

The CAL/REF control is a special driver circuit designed to select between either an internally generated 9.6 Hz reference signal or an external reference of 1 Hz to 100 kHz. The desired reference source is selected by either grounding or floating pin J1-36. The internal reference is generated by a 555 IC with the period determined by the R-C network contained in dip header C5. Exact rate is trimmed by the 10K potentiometer. The rectangular waveform is then divided by four and made symmetrical by the 7474 IC, and applied to one input of digital selector IC 74157. The output of this selector connects to the input of a second digital selector which is controlled by the computer-manual bus and provides the selected reference or the computer reference to the reference bus, J1-J, and to the calibration control gates in the 7410 IC. The calibration control gates enable the operator to select either CAL. ON, CAL. OFF, or CAL. AUTO from the front panel or from the computer. The internal/external reference may only be selected while operating under manual control. The CAL signal is converted to a 0-15 volt square wave in dip header D2. This voltage then drives the noise diodes directly.

6. DIGITAL MONITOR (DWG. #C131701L11)

THIS CIRCUIT CONSISTS OF FOUR 16-BIT DIGITAL LATCHES AND THEIR ASSOCIATED CONTROL LOGIC. # EACH SIGNAL TO BE MONITORED IS APPLIED TO A LATCH INPUT IN ONE OF FOUR DIGITAL WORD GROUPS. A WORD CONSISTS OF TWO 74165 PARALLEL-LOAD 8-BIT SHIFT REGISTER IC'S. THE MONITOR WORD ENABLE LINE IS AT A LOGIC '1' LEVEL UNTIL THE SMA CODE FOR WORD 220, 221, 222, OR 223 IS RECEIVED COINCIDENT WITH A STRI-1 PULSE. WHEN THIS OCCURS, THE DATA PRESENT AT THE MONITOR POINTS IS LATCHED INTO THE SHIFT REGISTER AND A 24 PULSE CLKI-1 PULSE TRAIN SHIFTS THE DATA OUT IN SERIAL FORM VIA DIGI-1 THE TIMING RELATIONSHIPS OF THESE SIGNALS ARE SHOWN IN THE DATA SET MANUAL, VLA TECHNICAL REPORT NO. 30, TIMING DIAGRAM 9.

4. Analog Monitor Multiplexers (DWG #C13170L9)

The analog multiplexers are switched statically by the sub multiplexer address lines. The data set sequentially samples ALGI Ø through ALGI 5 and digitizes the voltage being monitored. Dip headers are included to provide for RC filtering of each input line. The input limitations are Ø to ± 10 vdc.

5. Noise Temperature Monitor (DWG #A13170L3)

The noise temperature monitor circuit is comprised of an Analog Devices multifunction module AD433J and ~~an~~ external scaling resistor. Frequency converter A outputs TOTAL POWER and SYNCHRONOUS DETECTOR are sampled and converted to a voltage related to system noise temperature. This voltage is MONITORED THROUGH THE DCS AND IS ALSO THIS VOLTAGE MAY ~~made~~ available at a front panel test point "NTM". ~~and can~~ be converted to noise temperature by the following equation:

$$Tsys = 10 \times E_o \times Tcal$$

IV. TEST AND TROUBLESHOOTING

The majority of the Control Interface module circuitry may be tested on the bench without computer facilities, by operating the module in the manual control mode and manipulating the front panel switches. Most of the output drivers are open collector pull-downs which may be used to control a simple LED - 150 ohm series resistor combination from the +5 volt supply. Outputs which require special testing conditions are described below.

1. LO Waveguide Switch Driver

   This driver may be tested by connecting a 10 ohm 10 watt resistor between pins J4-BB and J4-AA. When the digiswitch labeled "AB-λ" is moved to position "3", the voltage measured from J4-AA to chassis must be less than 0.8 volts DC.

2. Cal Switch Drivers

   The cal switch drivers are open collector pull-ups to the +15 volt supply. Both drivers are controlled by a common signal line. They may be tested by connecting a 680Ω resistor in series with an LED to ground from pins J3-27 and J3-28. Both LED's should then be on, off, or flashing depending upon the position of the front panel switch.

3. LO Frequency Set

   The LO frequency set drivers are TTL outputs controlled by the front panel digiswitches. If four LED-resistor combinations are connected simultaneously, position "Ø" of each switch will turn on all four LED's. Position "1" will cause LED "1" to go off, position "2" will turn off LED "2" and so on in a BINARY fashion.

4. Upconverter Control Drivers

   The upconverter control drivers are essentially the same as the LO frequency set drivers but are only operative for the first four positions of each switch.

The analog monitor portion of the module circuitry may be tested statically by applying TTL level control signals to the four "SMA" lines. The "SMA" inputs are wired for negative, (low true), logic. Therefore TTL "1's" on all four inputs select switch position 1 on each of the six analog multiplexers. The checkout procedure, then, consists of applying a known

voltage in the range of 0 to ±10V dC to an individual monitor input, setting in the proper SMA binary code, and measuring the output voltage appearing at the appropriate multiplexer output.

The internal reference signal period is controlled by potentiometer R2, located on dip header C5. The period should be set for 100 ms, as monitored at Pin J1-J.

NOTE

A special pin numbering scheme is employed in this module. The analog monitor card, Group A, consists of 9 vertical rows marked A through J. Each row is then numbered 1 through 50 from top to bottom. On this card, each device will have its Pin 1 location described by that matrix. For example, analog IC AAØ1 is located with Pin 1 on Card A, Row A, and Socket 1. The other pin numbers of this IC are then counted in normal fashion around the package. All Group A pin number references in schematics and text are made to package pin numbers.

The other cards in this module consist of a series of 16 pin groups numbered 1 through 30. All IC's are identified by their location on the card, i.e., IC C10 is located on Card C, position 10. Pin 1 of each IC is always plugged into pin 1 of each socket. The 16 pin IC package and card numbers are identical but 8 and 14 pin packages require a modified numbering system. For a 14 pin package, pins 1 through 7 are as marked but pin 8 of the IC mates with pin 10 on the card. All Group B, C, ~~and~~ D AND E pin number references in schematics and text are made to the CARD numbers rather than the package numbers.

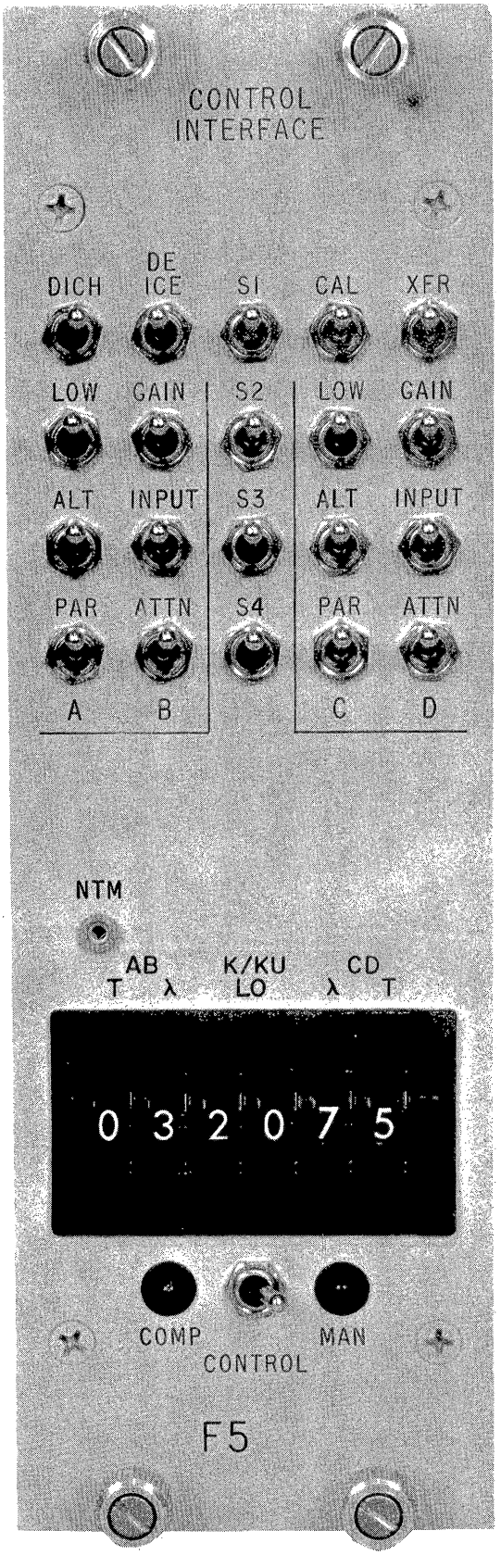

CONTROL
INTERFACE
DICH
DE
ICE
SI
CAL
XFR
LOW
GAIN
S2
LOW
GAIN
ALT
INPUT
S3
ALT
INPUT
PAR
ATTN
S4
PAR
ATTN
A
B
C
D
NTM
AB
T λ
K/KU
LO
CD
λ T
0 3 2 0 7 5
COMP
MAN
CONTROL
F5

FIGURE 2

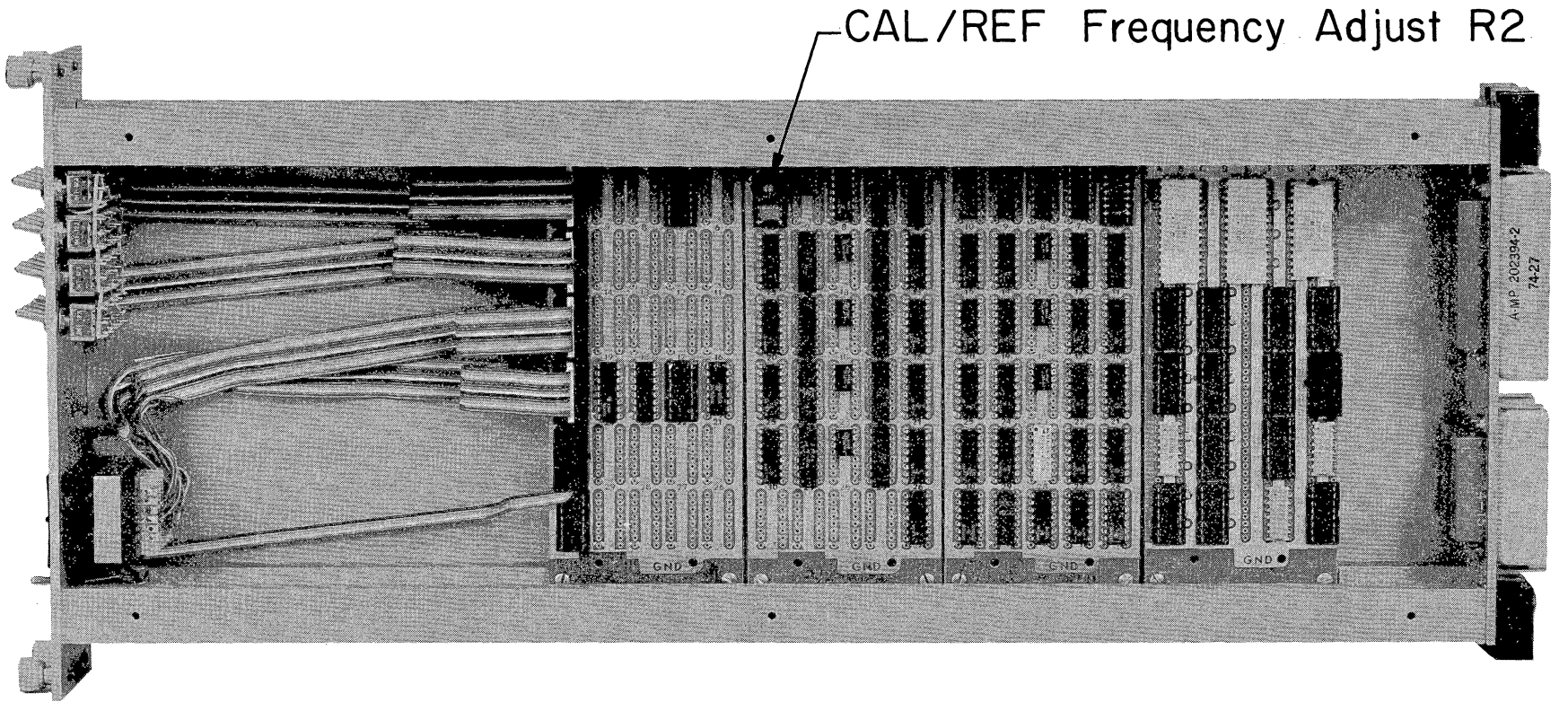
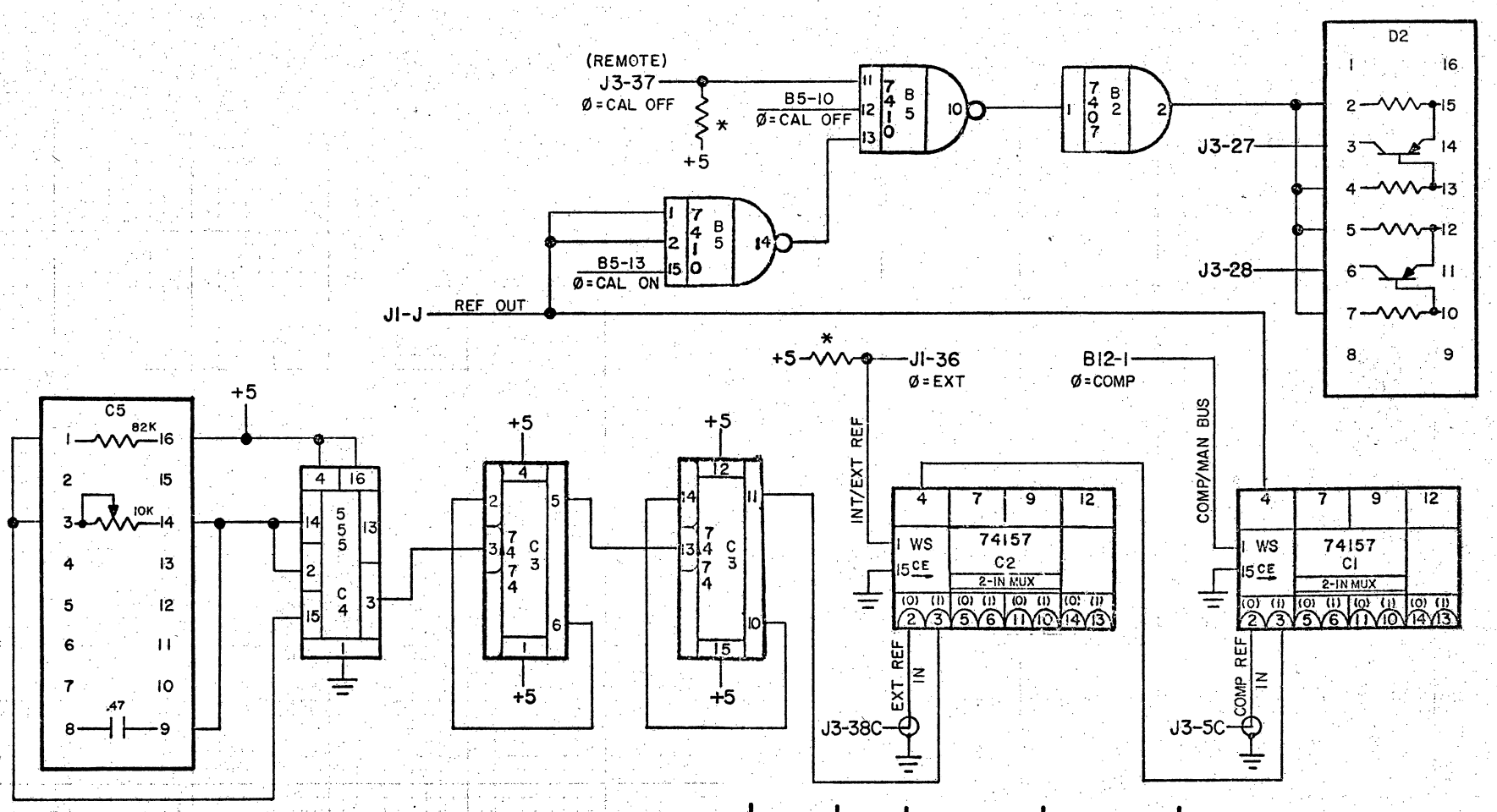


FIGURE 3



* RESISTORS LOCATED IN B-23

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

VLA PROJECT

FRONT END

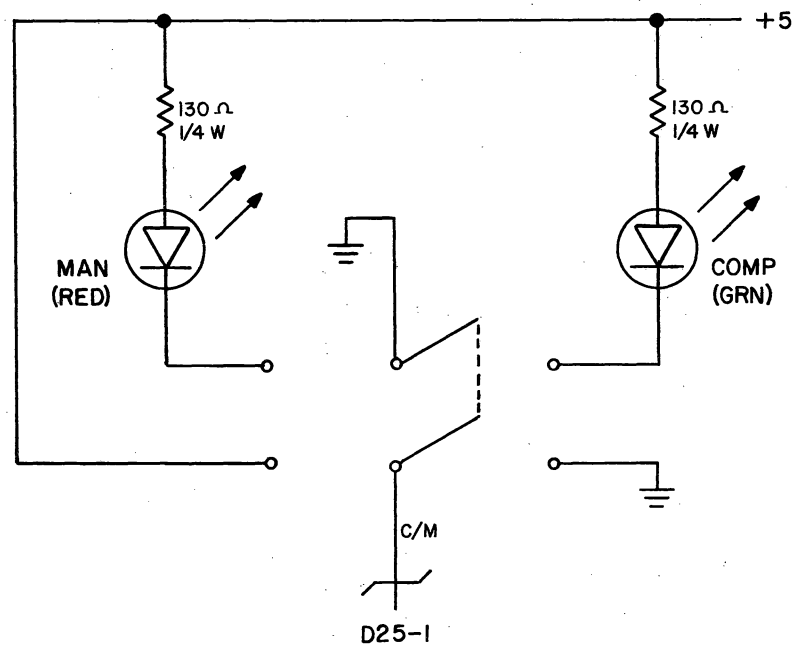
TITLE

CONTROL INTERFACE F5

CAL/REF CONTROL

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

DRAWN BY E.J. Mufson	DATE 4-17-75		
DESIGNED BY G.K. Gamell	DATE 4-28-75		
APPROVED BY G.K. Gamell	DATE 4-28-75		
SHEET NUMBER	DRAWING NUMBER A13170L1	REV.	SCALE



REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

VLA PROJECT: FRONT END

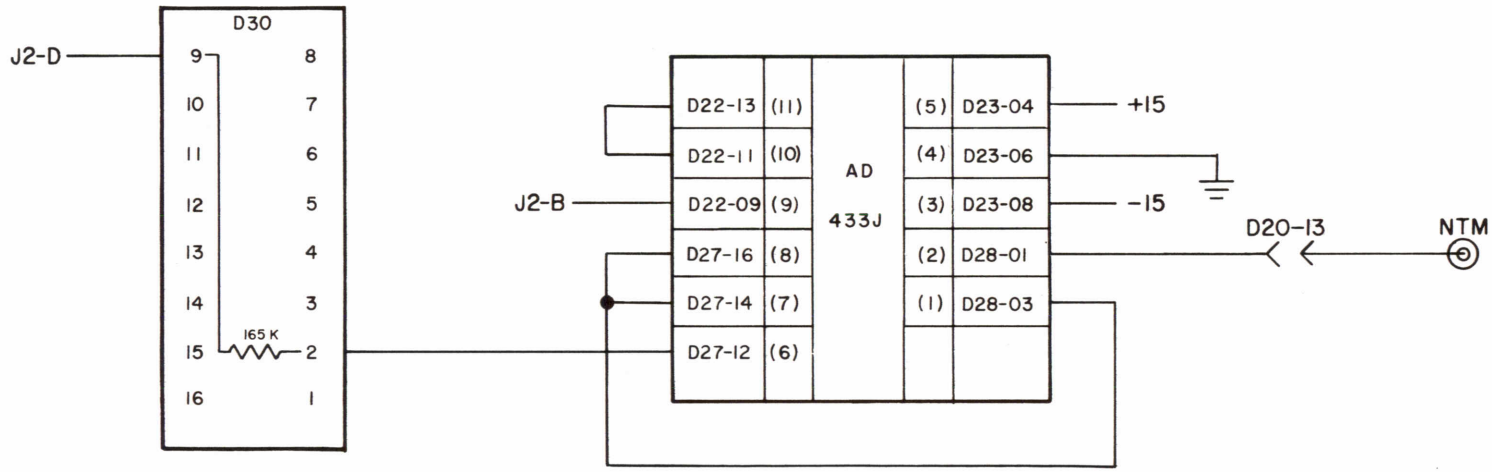
TITLE: CONTROL INTERFACE F5

COMPUTER-MANUAL CONTROL

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

DRAWN BY E. J. Mufson	DATE 4-29-75
DESIGNED BY GKB	DATE 4-28-78
APPROVED BY GK Bansell	DATE 4-28-78

SHEET NUMBER	DRAWING NUMBER	REV.	SCALE
	A13170L2		



REV

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

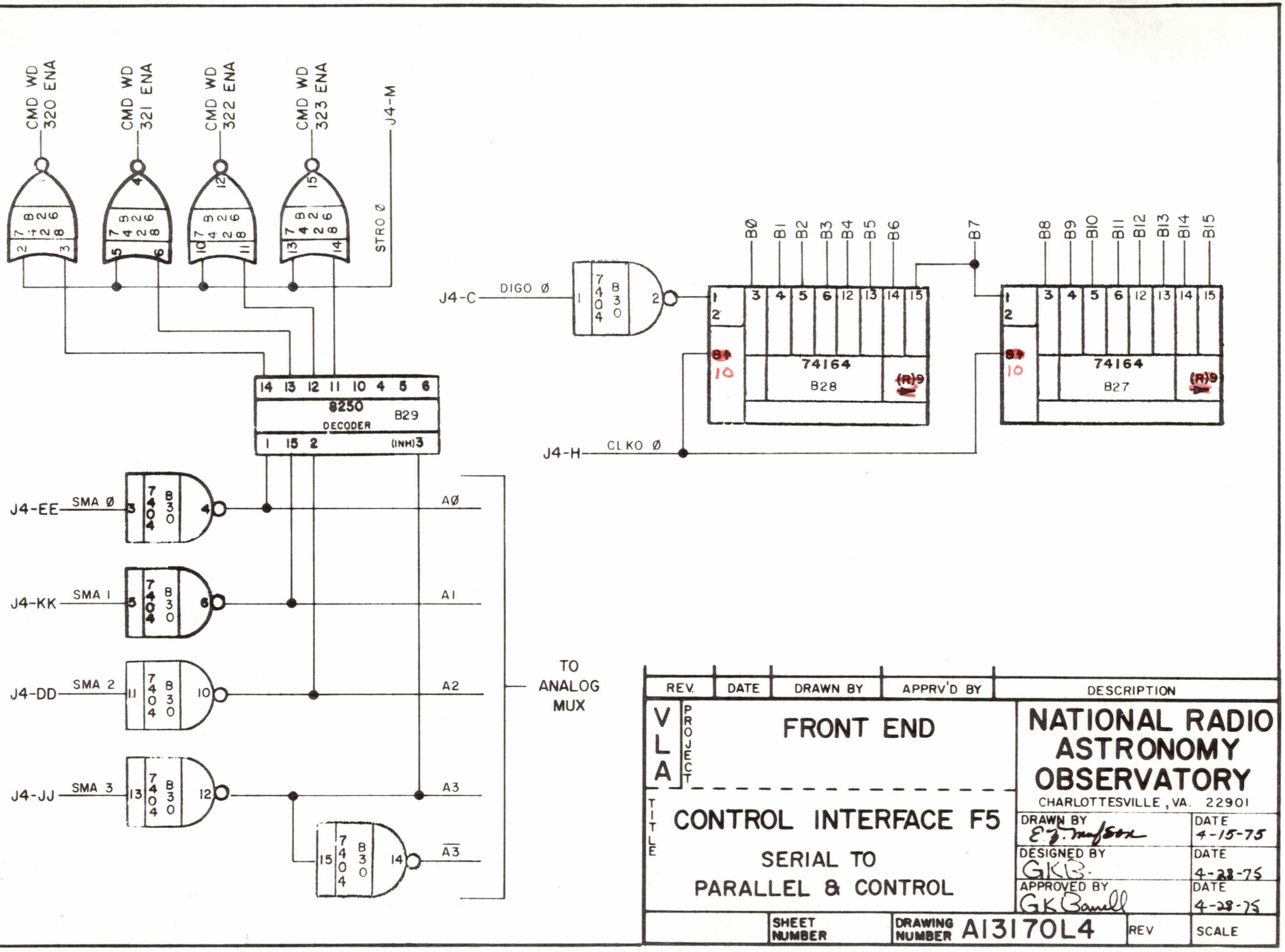
VLA PROJECT: FRONT END

TITLE: CONTROL INTERFACE F5
NOISE TEMPERATURE
MONITOR

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

DRAWN BY E.J. Mayfield	DATE 4-24-75
DESIGNED BY GKB	DATE 4-28-75
APPROVED BY GK Bansell	DATE 4-28-75

SHEET NUMBER	DRAWING NUMBER	REV.	SCALE
	A13170L3		



REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

VLA PROJECT

FRONT END

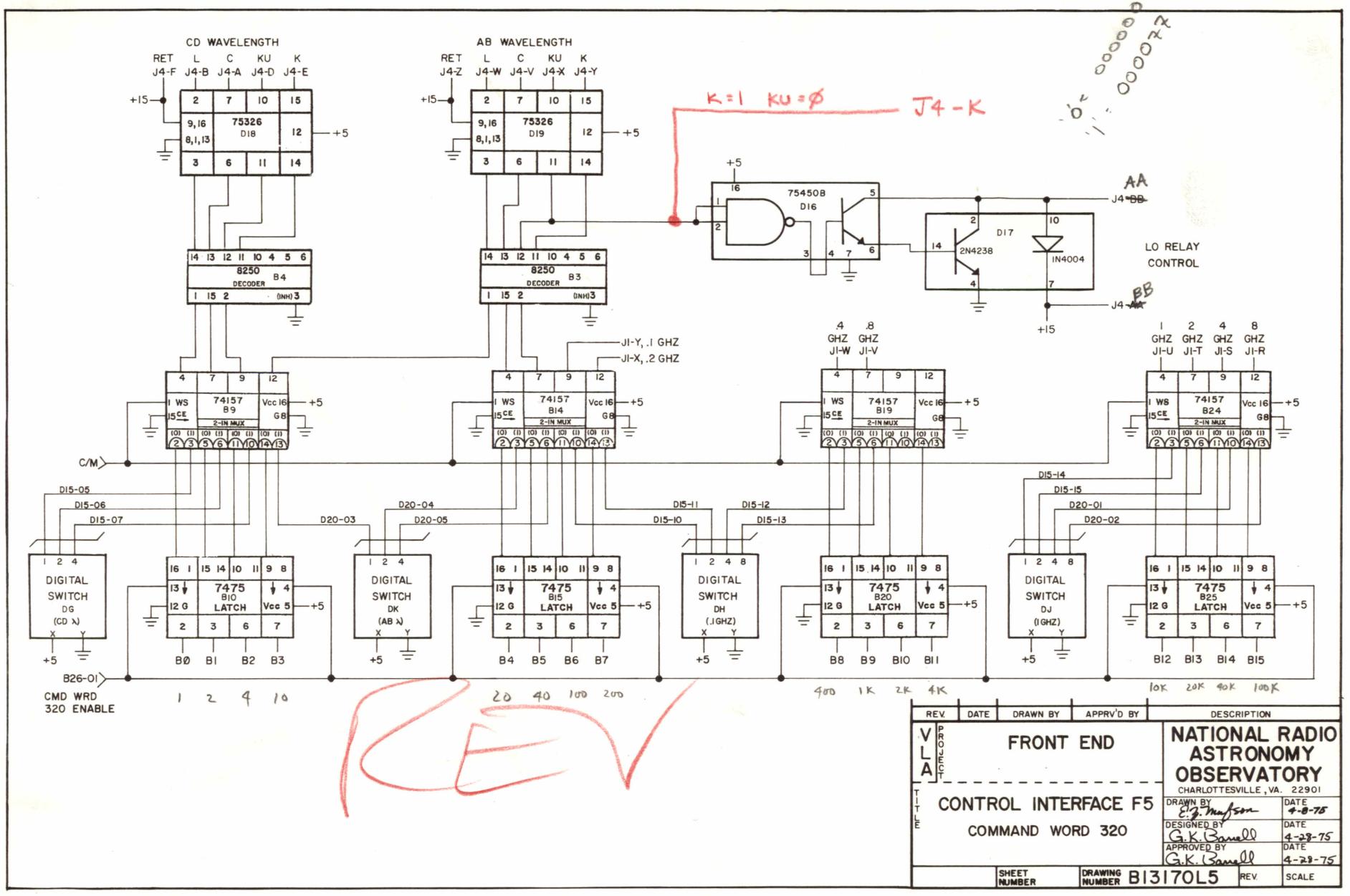
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

TITLE

CONTROL INTERFACE F5

SERIAL TO PARALLEL & CONTROL

DRAWN BY E.J. Mattox	DATE 4-15-75		
DESIGNED BY GKB.	DATE 4-28-75		
APPROVED BY GK Bamell	DATE 4-28-75		
SHEET NUMBER	DRAWING NUMBER A13170L4	REV	SCALE



REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

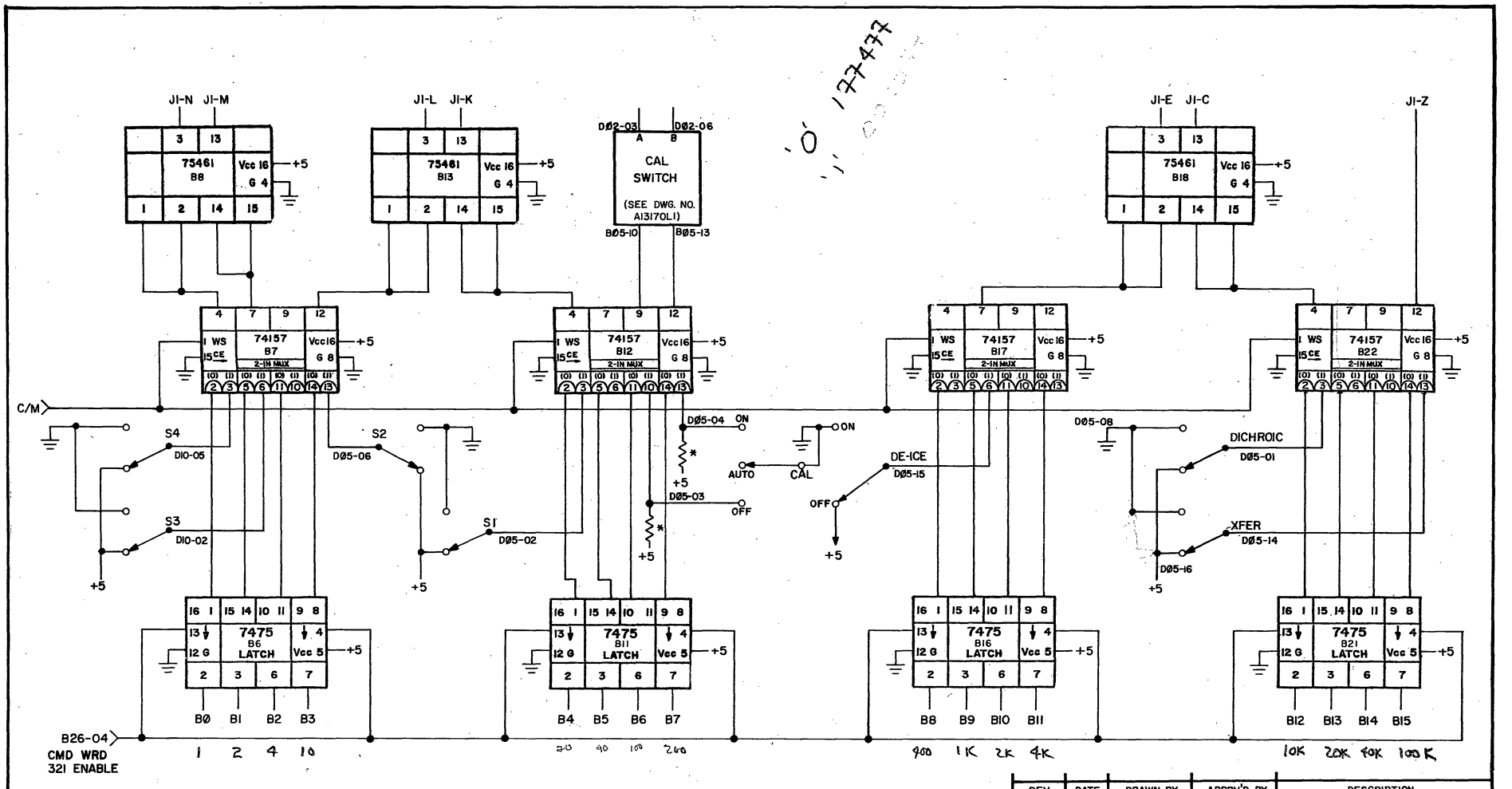
VLA PROJECT: FRONT END

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

TITLE: CONTROL INTERFACE F5
COMMAND WORD 320

DRAWN BY E.J. Mayson	DATE 4-8-75	
DESIGNED BY G.K. Bansell	DATE 4-28-75	
APPROVED BY G.K. Bansell	DATE 4-29-75	

SHEET NUMBER | DRAWING NUMBER B13170L5 | REV. | SCALE



NOTE: ALL SWITCHES SHOWN IN NORMAL OPERATING POSITION

* RESISTORS LOCATED IN B-23

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

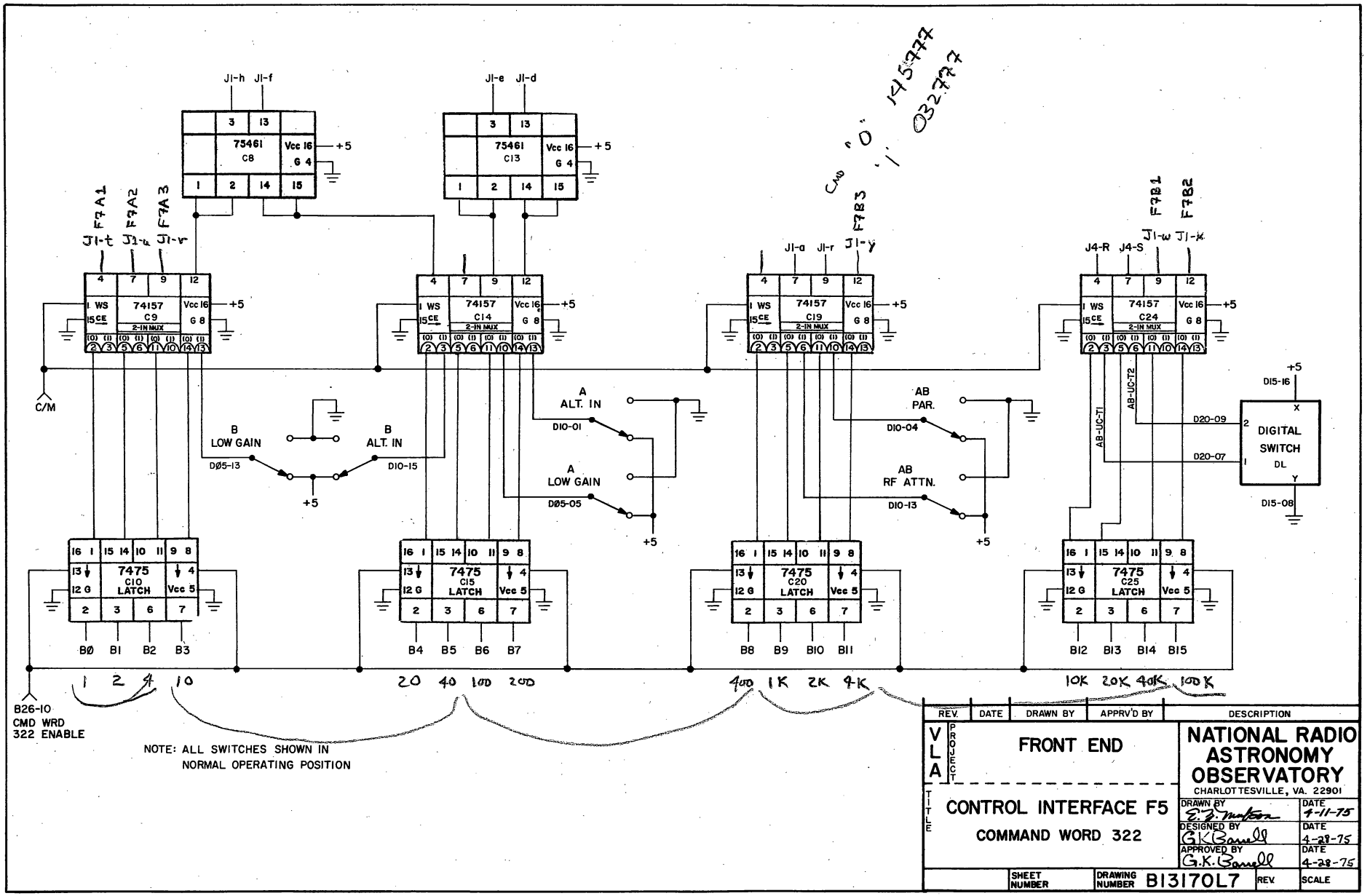
VLA PROJECT: FRONT END

TITLE: CONTROL INTERFACE F5
COMMAND WORD 321

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

DRAWN BY E.J. Mayer	DATE	4-10-75
DESIGNED BY G.K. Gamell	DATE	4-29-75
APPROVED BY G.K. Gamell	DATE	4-29-75

SHEET NUMBER | DRAWING NUMBER B13170L6 | REV. | SCALE



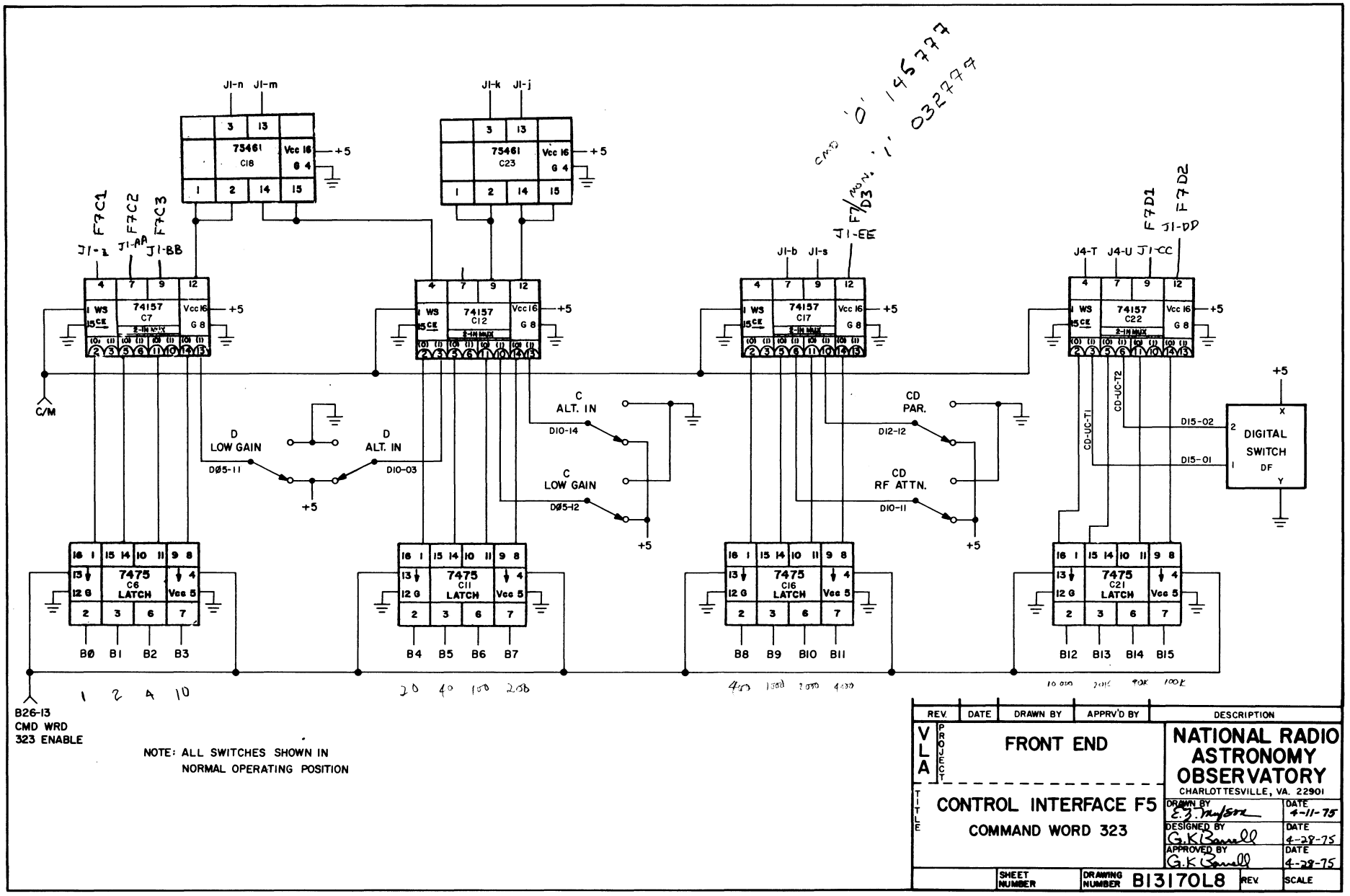
REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

VLA PROJECT: FRONT END

TITLE: CONTROL INTERFACE F5
COMMAND WORD 322

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

DRAWN BY E.B. Mattson	DATE 4-11-75		
DESIGNED BY G.K. Bansell	DATE 4-28-75		
APPROVED BY G.K. Bansell	DATE 4-28-75		
SHEET NUMBER	DRAWING NUMBER B13170L7	REV.	SCALE



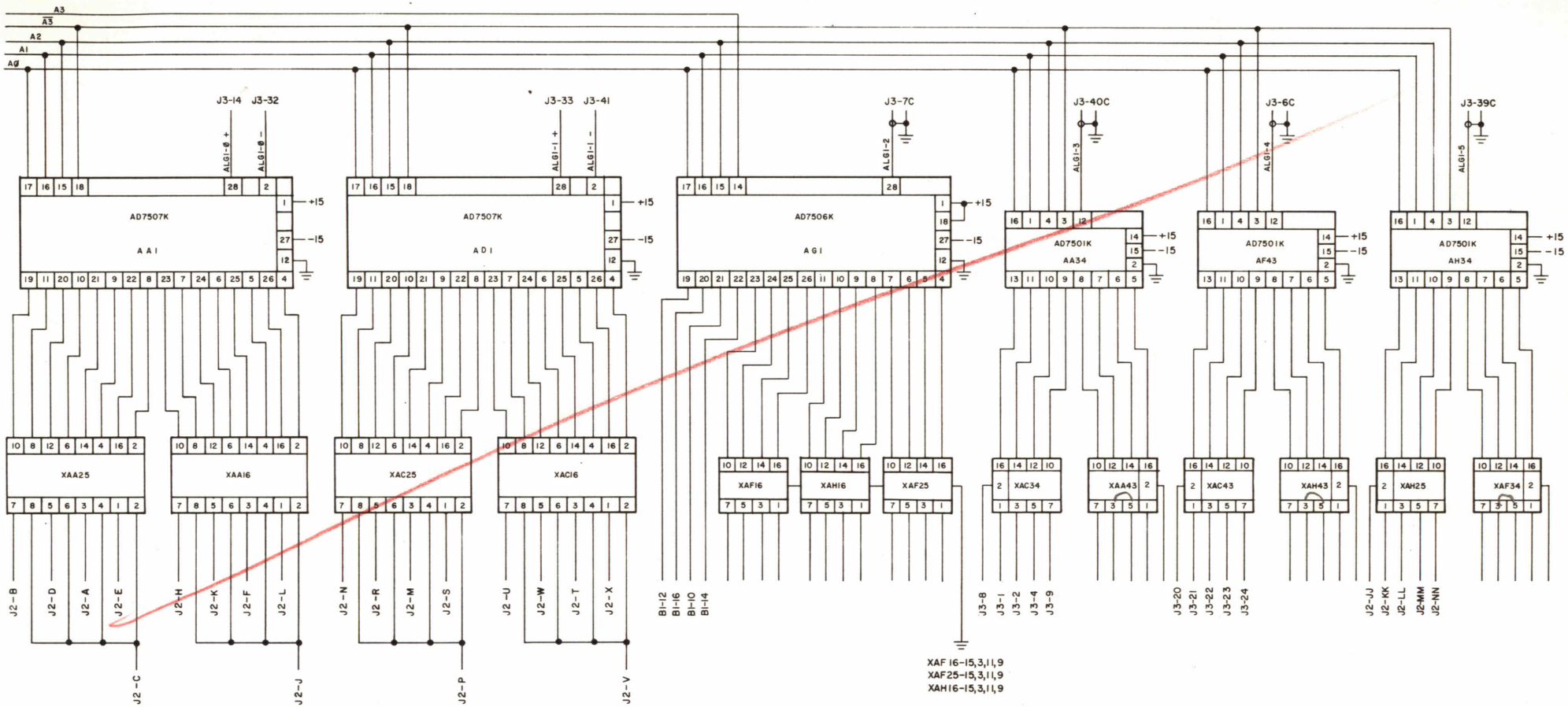
REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

VLA PROJECT: FRONT END

TITLE: CONTROL INTERFACE F5
COMMAND WORD 323

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

DRAWN BY E.J. Mayfarth	DATE 4-11-75	
DESIGNED BY G.K. Gunnell	DATE 4-28-75	
APPROVED BY G.K. Gunnell	DATE 4-28-75	
SHEET NUMBER	DRAWING NUMBER B13170L8	REV.
		SCALE



REV

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

VLA

FRONT END

CONTROL INTERFACE F5

ANALOG MULTIPLEXER

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

DRAWN BY E.J. Danielson	DATE	4-29-75
DESIGNED BY G.K. Gaull	DATE	4-29-75
APPROVED BY G.K. Gaull	DATE	4-29-75

SHEET NUMBER	DRAWING NUMBER	REV.	SCALE
	C13170L9		

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 1 OF 1

MODULE # F5 NAME CONTROL INTERFACE DWG # _____ SUB ASMB _____ DWG # _____

SCHEMATIC DWG # _____ LOCATION FRONT END QUA/SYSTEM 1 PREPARED BY GKB. APPROVED _____

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		NRAO		FRONT PANEL ASSEMBLY	1	
2		NRAO		CARD ASSEMBLY	1	
3		NRAO		REAR PANEL ASSEMBLY	1	
4		NRAO	B13050M18	RIGHT & LEFT SIDE PLATES	2	
5		NRAO	C13050M22-1	COVER, PERFORATED	2	
6		NRAO	B13050M4	GUIDES	4	

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☐ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 1 OF 1

MODULE # F5 NAME CONTROL INTERFACE DWG # _____ SUB ASMB FRONT PANEL DWG # _____

SCHEMATIC DWG # _____ LOCATION FRONT END QUA/SYSTEM 1 PREPARED BY GKB APPROVED _____

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		NRAO	C13170M63	FRONT PANEL 8 hrs shop	1	5.00
2		J3T	JMT 123	SWITCH, TOGGLE	19	.90
3		"	JMT 121	SWITCH, TOGGLE	1	1.85
4		"	JMT 223	SWITCH, TOGGLE	1	2.10
5		DIGITRAN	23011	SWITCH, DIGITAL (6X)	1	22.00
6		H-P	5082-4860	DIODE, LED RED	1	.80
7		H P	5082-4955	DIODE, LED GRN	1	.80
8		E.F. JOHNSON	105-1050-001	TEST JACK (BLUE)	1	.30
9		E-N	WJC-163D-29T	RIBBON CABLES	3	5.00
10		SOUTHCO	47-10-209-10	CAPTIVE FASTENER	4	

60.00

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NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☐ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 1 OF 3

MODULE # F5 NAME CONTROL INTERFACE DWG # _____ SUB ASMB WIRE WRAP CARDS DWG # _____

SCHEMATIC DWG # _____ LOCATION _____ QUA/SYSTEM 1 PREPARED BY GKB APPROVED _____

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		NRAO		SUPPORT BAR, MODIFIED	2	
2		NRAO		SPACER RAIL	2	

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☐ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 3 OF 3

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
16		TI	75450	IC	1	1.03
17		TI	75461		7	.89
18		R-N	MPB-163	16 PIN PLATFORM	18	.22
19		BECKMAN	899-1-R-2.0K	2K ~ RESISTOR PACKAGE	1	2.00
20		MOTOROLA	2N4238	TRANSISTOR, SILICON, NPN	1	1.55
21		"	1N4004	DIODE, SILICON	1	.60
22		"	2N3906	TRANSISTOR, SILICON, PNP	2	.29
23		AB	RC07GF202J	RESISTOR, 2K, 1/4 W, 5%	4	.04
24		DALE		RESISTOR, 165K, 1%	1	.60
25		TI	7407	IC	1	.60
26		AD	432J	MULTIFUNCTION MODULE	1	75
27		R-N	PS-5026-119-6	W/U SOCKETS	11	

9231

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☐ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 2 OF 3

MODULE # FC NAME CONTROL INTERFACE DWG # _____ SUB ASMB WIRE WRAP CARDS DWG # _____

SCHEMATIC DWG # _____ LOCATION _____ QUA/SYSTEM 1 PREPARED BY GKB APPROVED _____

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		GARRY		16 PIN WIRE WRAP CARD	~~3~~ 4	37.00
2		GARRY		UNIVERSAL WIRE WRAP CARD	1	45.00
3		AD	AD7501	ANALOG MUX	3	20.00
4		AD	AD7506	ANALOG MUX	1	28.00
5		AD	AD7507	ANALOG MUX	2	28.00
6		SIGNETICS	NE 555	TIMER	1	.75
7		TI	7404	IC	1	.24
8			7410		1	.20
9			7428		1	.40
10			74LS74		1	.29
11			7475		16	.48
12			74157		18	.83
13		TI	74164		2	1.20
14		SIGNETICS	8250A		3	2.26
15		TI	75326		2	2.75

339.18

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NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☐ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 1 OF 1

MODULE # F5 NAME CONTROL INTERFACE DWG # _____ SUB ASMB REAR PANEL DWG # _____

SCHEMATIC DWG # _____ LOCATION FRONT END QUA/SYSTEM 1 PREPARED BY GKB APPROVED _____

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		NRAO	C13170M66	MODULE REAR PANEL	1	
2		AMP	204186-5	42 PIN CONNECTOR BLOCK	1	
3		"	201358-3	50 PIN CONNECTOR BLOCK	1	
4		"	202394-2	42/50 PIN MODULE CONNECTOR HOOD	2	
5		"	201357-3	34 PIN CONNECTOR BLOCK	2	
6		"	202434-4	34 PIN MODULE CONNECTOR HOOD	2	
7		"	66460-6	WIRE WRAP CONNECTOR PINS	154	
8		"	201143-5	COAXIAL CONNECTOR PINS	6	
9		"	202514-1	GOLD GROUND PINS	4	
10		"	200833-4	SILVER GUIDE PINS	4	
11		AMP	203964-6	SILVER GUIDE SOCKETS	8	

signetics

TIMER | 555

LINEAR INTEGRATED CIRCUITS

DESCRIPTION

The NE/SE 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA or drive TTL circuits.

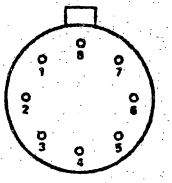
FEATURES

- TIMING FROM MICROSECONDS THROUGH HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- ADJUSTABLE DUTY CYCLE
- HIGH CURRENT OUTPUT CAN SOURCE OR SINK 200mA
- OUTPUT CAN DRIVE TTL
- TEMPERATURE STABILITY OF 0.005% PER °C
- NORMALLY ON AND NORMALLY OFF OUTPUT

APPLICATIONS

PRECISION TIMING
PULSE GENERATION
SEQUENTIAL TIMING
TIME DELAY GENERATION
PULSE WIDTH MODULATION
PULSE POSITION MODULATION
MISSING PULSE DETECTOR

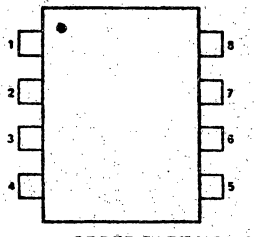
PIN CONFIGURATIONS



T PACKAGE
(Top View)

1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

ORDER PART NOS. SE555T/NE555T



V PACKAGE
(Top View)

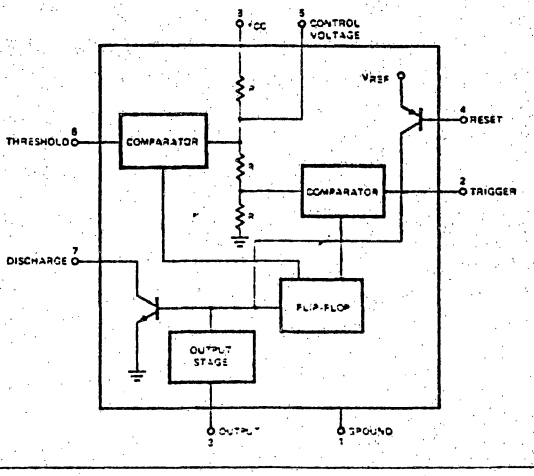
1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

ORDER PART NOS. SE555V/NE555V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18V
Power Dissipation	600 mW
Operating Temperature Range	
NE555	0°C to +70°C
SE555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

BLOCK DIAGRAM



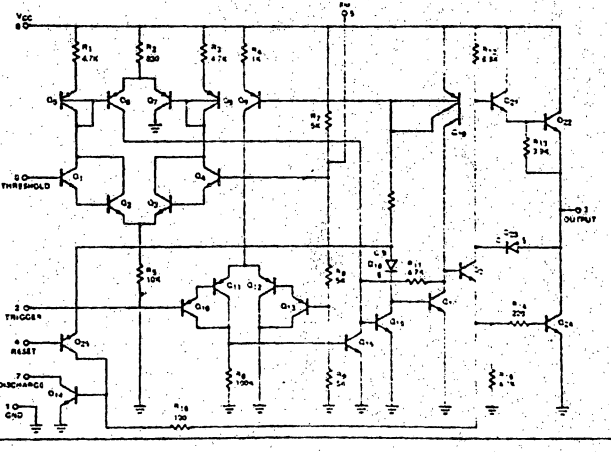
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified)

PARAMETER	TEST CONDITIONS	SE 555			NE 555			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V R_L = ∞		10	12		10	15	mA
	Low State, Note 1							
Timing Error	R_A, R_B = 1KΩ to 100KΩ							
Initial Accuracy	C = 0.1 µF Note 2		0.5	2		1		%
Drift with Temperature			30	100		50		ppm/°C
Drift with Supply Voltage			0.005	0.02		0.01		%/Volt
Threshold Voltage			2/3			2/3		X V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		µA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current	Note 3		0.1	.25		0.1	.25	µA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage Drop (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	.75	V
	I_{SINK} = 100mA		2.0	2.2		2.0	2.5	V
	I_{SINK} = 200mA		2.5			2.5		
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.25				V
	I_{SINK} = 5mA					.25	.35	
Output Voltage Drop (high)								
	I_{SOURCE} = 200mA V_{CC} = 15V		12.5			12.5		
	I_{SOURCE} = 100mA							
	V_{CC} = 15V	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		nsec
Fall Time of Output			100			100		nsec

NOTES:

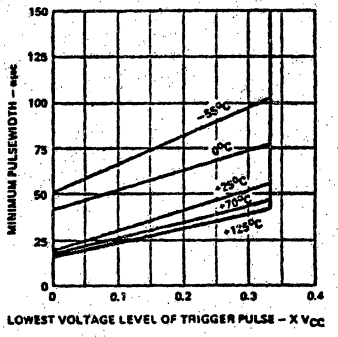
1. Supply Current when output high typically 1mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V
3. This will determine the maximum value of R_A + R_B For 15V operation, the max total R = 20 megohm.

EQUIVALENT CIRCUIT

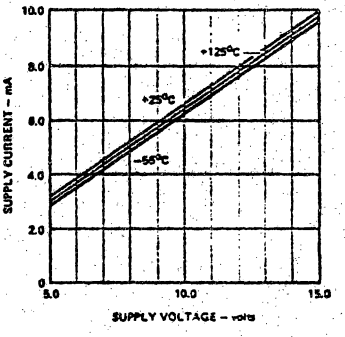


CAL CHARACTERISTICS

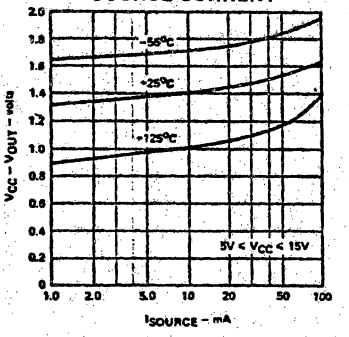
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



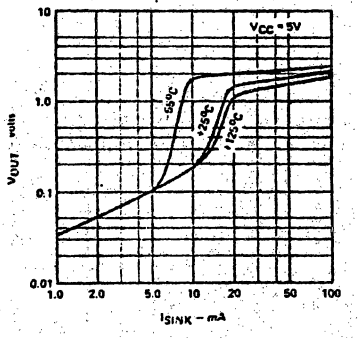
SUPPLY CURRENT vs SUPPLY VOLTAGE



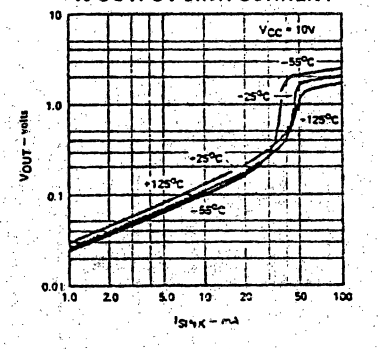
HIGH OUTPUT VOLTAGE vs OUTPUT SOURCE CURRENT



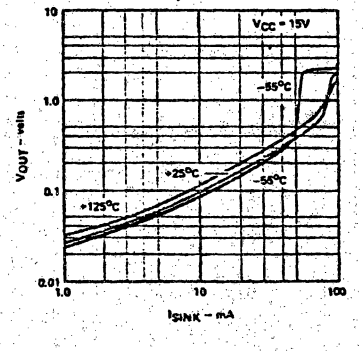
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



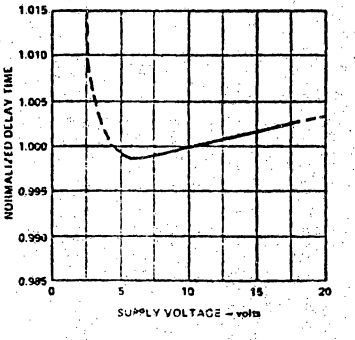
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



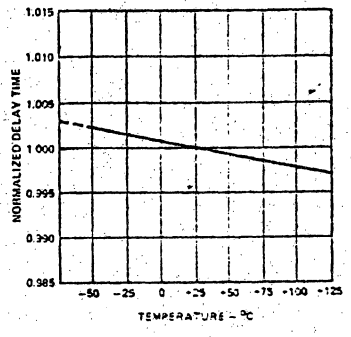
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



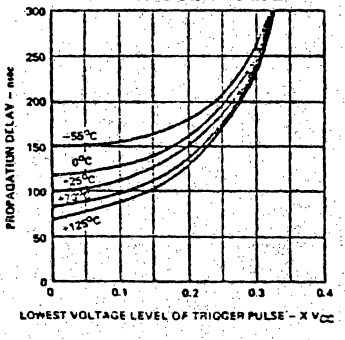
DELAY TIME vs SUPPLY VOLTAGE



DELAY TIME vs TEMPERATURE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



TYPES SN55326, SN55327, SN75326, SN75327
MEMORY DRIVERS

BULLETIN NO. DL-S 7312063, SEPTEMBER 1973

SERIES 55/75 MEMORY DRIVERS
featuring

SN55326, SN75326 PERFORMANCE

- Quad Positive-OR Sink Memory Drivers
- 600-mA Output Current Sink Capability
- 24-V Output Capability
- Clamp Voltage Variable to 24 V

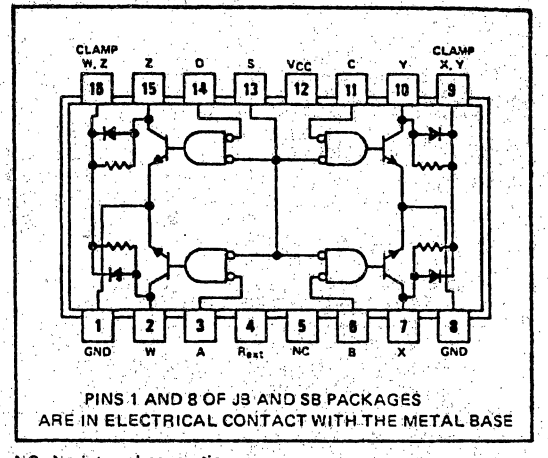
SN55327, SN75327 PERFORMANCE

- Quad Memory Switches
- 600-mA Output Current Capability
- V_{CC2} Drive Voltage Variable to 24 V
- Output Capable of Swinging Between V_{CC2} and Ground

EASE OF DESIGN

- High-Repetition-Rate Driver Compatible with High-Speed Magnetic Memories
- Inputs Compatible with TTL Decoders
- Minimum Time Skew between Strobe and Output-Current Rise
- Pulse-Transformer Coupling Eliminated
- Drive-Line Lengths Reduced

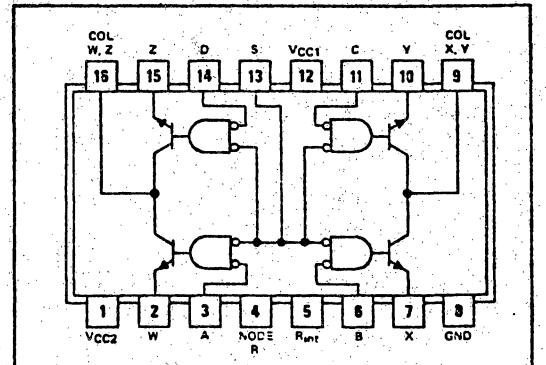
SN55326, SN75326
J, JB, OR N DUAL-IN-LINE OR
SB FLAT PACKAGE (TOP VIEW)



PINS 1 AND 8 OF JB AND SB PACKAGES
ARE IN ELECTRICAL CONTACT WITH THE METAL BASE

NC—No internal connection

SB55327, SN75327
J, JB, OR N DUAL-IN-LINE OR
SB FLAT PACKAGE (TOP VIEW)



PIN 8 OF JB AND SB PACKAGES IS IN
ELECTRICAL CONTACT WITH THE METAL BASE

description

The SN55326, SN55327, SN75326, and SN75327 are monolithic integrated circuit quadruple memory drivers. These devices accept standard TTL decoder input signals and provide high-current and high-voltage output levels suitable for driving magnetic memory elements. Output transistor selection is determined by using one of the four address inputs and the common timing strobe.

The SN55326 and SN75326 memory drivers can sink up to 600 milliamperes and operate from a single 5-volt supply. Each driver is similar to the sink drivers of the SN55325/SN75325. The four output transistors share a common base-drive resistor and it is recommended that only one of the four driver gates be selected at a time. Output-transistor base current may be increased by connecting an external resistor between R_{ext} (pin 4) and V_{CC}. Each output collector is protected from voltage surges during inductive switching by a clamp diode in parallel with its internal pull-up resistor. The two clamp pins may be returned to a power supply of from 4.5 volts to 24 volts.

The SN55327 and SN75327 memory switches can source or sink up to 600 milliamperes and operate from two supplies; one of five volts and the other from 4.5 volts to 24 volts. Each switch is similar to the source drivers of the SN55325/SN75325. They can function as either sink drivers or source drivers since the voltages at the output transistor terminals are capable of swinging between V_{CC2} and ground. The four output transistors share a common base-drive resistor and it is recommended that only one of the four outputs be selected at a time. An internal base-drive resistor is available on the chip and can be

TENTATIVE DATA SHEET

TEXAS INSTRUMENTS
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description (continued)

used by connecting Node R (pin 4) to R_{int} (pin 5). This resistor provides adequate base current to the output transistors for output sink currents up to 375 milliamperes with V_{CC2} at 15 volts or 600 milliamperes with V_{CC2} at 24 volts. Base current can be regulated to within ±5 percent by substituting for this resistor an external resistor connected between Node R (pin 4) and V_{CC2} with R_{int} (pin 5) remaining open. This method is preferable in high-duty-cycle, high-power applications since the power dissipated in this resistor is outside the package. When a source current and V_{CC2} voltage other than the above values are required, it is recommended that the base drive be supplied through an external resistor of the appropriate value calculated using Equation 1 shown in the SN55325, SN75325 data sheet.

FUNCTION TABLE

INPUTS					OUTPUTS			
ADDRESS				STROBE				
A	B	C	D	S	W	X	Y	Z
L	H	H	H	L	ON	OFF	OFF	OFF
H	L	H	H	L	OFF	ON	OFF	OFF
H	H	L	H	L	OFF	OFF	ON	OFF
H	H	H	L	L	OFF	OFF	OFF	ON
H	H	H	H	X	OFF	OFF	OFF	OFF
X	X	X	X	H	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant
NOTE: Not more than one output is to be on at any one time.

The SN55326 and SN55327 circuits are characterized for operation over the full military temperature range of –55°C to 125°C; the SN75326 and SN75327 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55326	SN75326	SN55327	SN75327	UNIT
Supply voltage, V_{CC} or V_{CC1} (see Note 1)	7	7	7	7	V
Supply voltage, V_{CC2}			25	25	V
Input voltage, any address or strobe	5.5	5.5	5.5	5.5	V
Output collector voltage	25	25	25	25	V
Output clamp voltage	25	25			V
Output collector current	750	750	750	750	mA
Continuous total dissipation at (or below) 100°C case temperature (see Note 2)	1	1	1	1	W
Operating free-air temperature range	–55 to 125	0 to 70	–55 to 125	0 to 70	°C
Storage temperature range	–65 to 150	–65 to 150	–65 to 150	–65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds: J, JB, or SB package	300	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260	260	260	260	°C

recommended operating conditions

	SN55326			SN75326			SN55327			SN75327			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} or V_{CC1}	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
Supply voltage, V_{CC2}							4.5		24	4.5		24	V
Output collector voltage			24			24			24			24	V
Output-clamp voltage, $V_{(clamp)}$	4.5		24	4.5		24							V
Output collector current			600			600			600			600	mA
Operating free-air temperature, T_A	–55		125	0		70	–55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal(s).
2. For operation above 100°C case temperature, refer to Dissipation Derating Curve, Figure 1. For dissipation ratings in free-air, see Figure 2.

SN55326, SN75326 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN55326 MIN	SN55326 TYP‡	SN55326 MAX	SN75326 MIN	SN75326 TYP‡	SN75326 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = 4.5 V, T_A = 25°C	I_I = −10 mA,		−1	−1.7		−1	−1.7	V
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	I_O = 0	19	23		19	23		V
$V_{(sat)}$	Saturation voltage		V_{CC} = 4.5 V, $I_{(sink)}$ = 600 mA§, See Note 3	Full range			0.9			0.9	V
				T_A = 25°C		0.43	0.7		0.43	0.75	
$V_{F(clamp)}$	Output-clamp-diode forward voltage		$V_{(clamp)}$ = 0, T_A = 25°C	$I_{(clamp)}$ = −10 mA,			1.5			1.5	V
$I_{(clamp)}$	Output-clamp current, one output on		$I_{(sink)}$ = 50 mA, T_A = 25°C			5	7		5	7	mA
I_I	Input current at maximum input voltage	Address	V_I = 5.5 V				1			1	mA
		Strobe					4			4	
I_{IH}	High-level input current	Address	V_I = 2.4 V				40			40	μA
		Strobe					160			160	
I_{IL}	Low-level input current	Address	V_I = 0.4 V			−1	−1.6		−1	−1.6	mA
		Strobe				−4	−6.4		−4	−6.4	
$I_{CC(off)}$	Supply current, all outputs off		All inputs at 5 V, T_A = 25°C			18	25		18	25	mA
$I_{CC(on)}$	Supply current, one output on		$I_{(sink)}$ = 50 mA, T_A = 25°C			58	75		58	75	mA

SN55326, SN75326 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST CONDITIONS§	MIN	TYP	MAX	UNIT
t_{PLH}	W, X, Y, or Z	$V_S = V_{(clamp)}$ = 15 V, R_L = 24 Ω, C_L = 25 pF, See Figure 5		30	50	ns
t_{PHL}				25	50	
t_{TLH}	W, X, Y, or Z			7	15	ns
t_{THL}				10	20	
t_s	W, X, Y, or Z			24	35	ns
V_{OH}	W, X, Y, or Z	$V_S = V_{(clamp)}$ = 24 V, R_L = 47 Ω, C_L = 25 pF, $I_{(sink)}$ ≈ 500 mA, See Figure 5	V_S−25			mV

†Unless otherwise noted, V_{CC} = 5.5 V, $V_{(clamp)}$ = 24 V. See Figure 3.
‡All typical values are at T_A = 25°C.
§Under these conditions, not more than one output is to be on at any one time.
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{TLH} ≡ transition time, low-to-high-level output
t_{THL} ≡ transition time, high-to-low-level output
t_s ≡ Storage time
V_{OH} ≡ High-level output voltage (after switching)
NOTE 3: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 2%.

For typical characteristic curves, Figures 11 through 14 of the SN55325/SN75325 data sheet apply for these circuits.

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SN55327, SN75327 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN55327 MIN	SN55327 TYP‡	SN55327 MAX	SN75327 MIN	SN75327 TYP‡	SN75327 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = 4.5 V, T_A = 25°C	I_I = −10 mA		−1	−1.7		−1	−1.7	V
$I_{(off)}$	Collectors terminal off-state current		V_{CC1} = 4.5 V, $V_{(col)}$ = 24 V	Full range			500			200	μA
				T_A = 25°C			150			200	
$V_{(sat)}$	Saturation voltage		V_{CC1} = 4.5 V, V_O = 0, $I_{(source)}$ = −600 mA§, See Notes 3 and 4	Full range			0.9			0.9	V
				T_A = 25°C		0.43	0.7		0.43	0.75	
I_I	Input current at maximum input voltage	Address	V_I = 5.5 V				1			1	mA
		Strobe					4			4	
I_{IH}	High-level input current	Address	V_I = 2.4 V				40			40	μA
		Strobe					160			160	
I_{IL}	Low-level input current	Address	V_I = 0.4 V			−1	−1.6		−1	−1.6	mA
		Strobe				−4	−6.4		−4	−6.4	
$I_{CC(off)}$	Supply current, all outputs off	From V_{CC1}	All inputs at 5 V,	T_A = 25°C		7	10		7	10	mA
		From V_{CC2}				13	20		13	20	
$I_{CC(on)}$	Supply current, one output on	From V_{CC1}	$V_{(col)}$ = 6 V, T_A = 25°C,	$I_{(source)}$ = −50 mA, See Note 3		8	12		8	12	mA
		From V_{CC2}				36	55		36	55	

SN55327, SN75327 switching characteristics, V_{CC1} = 5 V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST CONDITIONS§	MIN	TYP	MAX	UNIT
t_{PLH}	Collectors W, Z or X, Y	V_S = V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF, See Figure 5 and Note 4		35	55	ns
t_{PHL}				30	55	
t_{TLH}	W, X, Y, or Z	$V_{(col)}$ = V_{CC2} = 20 V, R_L = 100 Ω, C_L = 25 pF, See Figure 6 and Note 4		30		ns
t_{THL}				10		
V_{OH}	Collectors W, Z or X, Y	V_S = V_{CC2} = 24 V, R_L = 47 Ω, C_L = 25 pF, $I_{(sink)}$ ≈ 500 mA, See Figure 5 and Note 4	V_S−25			mV

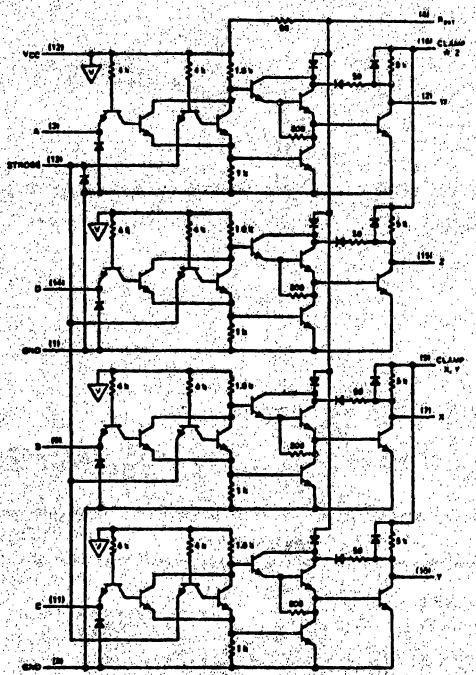
†Unless otherwise noted, V_{CC1} = 5.5 V, V_{CC2} = 24 V. See Figure 3.
‡All typical values are at T_A = 25°C.
§Under these conditions, not more than one output is to be on at any one time.
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{TLH} ≡ transition time, low-to-high-level output
t_{THL} ≡ transition time, high-to-low-level output
V_{OH} ≡ High-level output voltage (after switching)

NOTES: 3. These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 2%.
4. A 350-Ω resistor is connected between node R (pin 4) and V_{CC2} (pin 1) with R_{int} (pin 5) open.

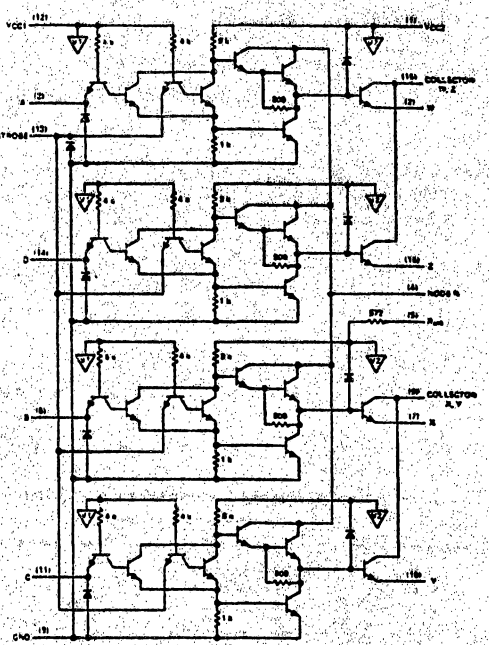
For typical characteristic curves, Figures 11 through 14 of the SN55325/SN75325 data sheet apply for these circuits.

schematics

SN55326, SN75326



SN55327, SN75327

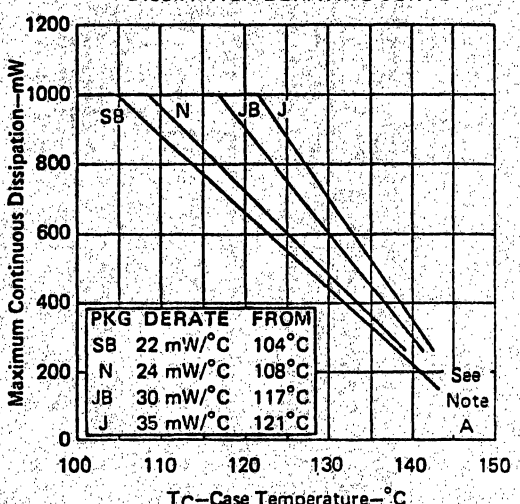


▽ ▽ ▽ . . . V_{CC}, V_{CC1}, or V_{CC2} bus, respectively.

Resistor values shown are nominal and in ohms.

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE



NOTE A: Rated operating free-air temperature ranges must be observed regardless of heat-sinking.

FIGURE 1

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

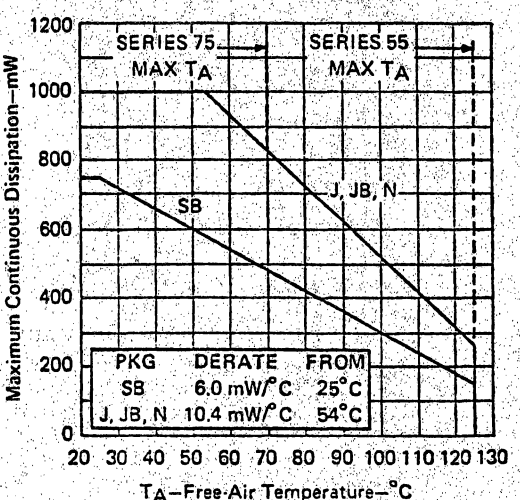


FIGURE 2

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES 55450B/75450B
DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 7311798, SEPTEMBER 1973

PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT HIGH SPEEDS

performance

- 300-mA Output Current Capability
- High-Voltage Outputs
- No Output Latch-Up at 20 V
- High-Speed Switching

ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL or DTL Compatible Diode-Clamped Inputs
- Standard Supply Voltages

SUMMARY OF SERIES 55450B/75450B

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55450B	Positive-AND†	J, JB
SN55451B	Positive-AND	JP, L
SN55452B	Positive-NAND	JP, L
SN55453B	Positive-OR	JP, L
SN55454B	Positive-NOR	JP, L
SN75450B	Positive-AND†	J, N
SN75451B	Positive-AND	L, P
SN75452B	Positive-NAND	L, P
SN75453B	Positive-OR	L, P
SN75454B	Positive-NOR	L, P

†With output transistor base connected externally to output of gate.

description

Series 55450B/75450B dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. The 55450B/75450B family is functionally interchangeable with and replaces the 75450 family and the 75450A family devices manufactured previously. The speed of the 55450B/75450B family is equal to that of the 75450 family and a test to ensure freedom from latch-up has been added. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55450B drivers are characterized for operation over the full military temperature range of −55°C to 125°C; Series 75450B drivers are characterized for operation from 0°C to 70°C.

The SN55450B and SN75450B are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage n-p-n transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The SN55451B/SN75451B, SN55452B/SN75452B, SN55453B/SN75453B, and SN55454B/SN75454B are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

This data sheet replaces the Series 75450 data sheet, DL-S 7111444, dated March 1971

TEXAS INSTRUMENTS
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POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55450B	SN55451B SN55452B SN55453B SN55454B	SN75450B	SN75451B SN75452B SN75453B SN75454B	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	7	7	V
Input voltage		5.5	5.5	5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	5.5	5.5	V
V_{CC}-to-substrate voltage		35		35		V
Collector-to-substrate voltage		35		35		V
Collector-base voltage		35		35		V
Collector-emitter voltage (see Note 3)		30		30		V
Emitter-base voltage		5		5		V
Output voltage (see Note 4)			30		30	V
Collector current (see Note 5)		300		300		mA
Output current (see Note 5)			300		300	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6)		800	800	800	800	mW
Operating free-air temperature range		−55 to 125	−55 to 125	0 to 70	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, JB, JP, or L package	300	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	260	260	°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
6. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 20. This rating for the L package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 95°C/W.

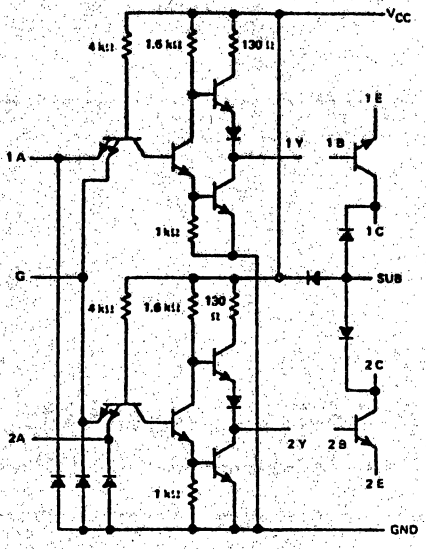
recommended operating conditions (see Note 7)

	SERIES 55450B			SERIES 75450B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 7: For the SN55450B and SN75450B only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

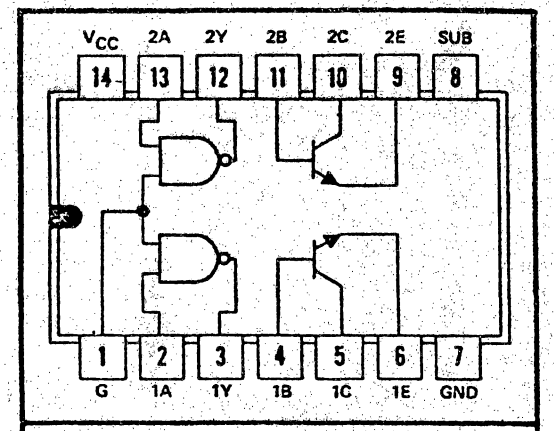
TYPE SN75450B
DUAL PERIPHERAL POSITIVE-AND DRIVER

schematic



Resistor values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL gates

PARAMETER			TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage		1		2			V
V_{IL}	Low-level input voltage		2				0.8	V
V_I	Input clamp voltage		3	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		2	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.3		V
V_{OL}	Low-level output voltage		1	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 16 mA		0.22	0.4	V
I_I	Input current at maximum input voltage	input A	4	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
		input G					2	
I_{IH}	High-level input current	input A	4	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
		input G					80	
I_{IL}	Low-level input current	input A	3	V_{CC} = 5.25 V, V_I = 0.4 V			−1.6	mA
		input G					−3.2	
I_{OS}	Short-circuit output current‡		5	V_{CC} = 5.25 V	−18		−55	mA
I_{CCH}	Supply current, outputs high		6	V_{CC} = 5.25 V, V_I = 0		2	4	mA
I_{CCL}	Supply current, outputs low		6	V_{CC} = 5.25 V, V_I = 5 V		6	11	mA

†All typical values at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

output transistors

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0		35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C	See Note 8	25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			
		V_{CE} = 3 V, I_C = 100 mA, T_A = 0°C		20			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 0°C		25			
V_{BE}	Base-Emitter Voltage	I_B = 10 mA, I_C = 100 mA	See Note 8		0.85	1	V
		I_B = 30 mA, I_C = 300 mA			1.05	1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 10 mA, I_C = 100 mA	See Note 8		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA			0.5	0.7	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 8: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TTL gates

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	12	C_L = 15 pF, R_L = 400 Ω		12	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output				8	15	ns

output transistors

PARAMETER		TEST FIGURE	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t_d	Delay time	13	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1 V, C_L = 15 pF, R_L = 50 Ω		8	15	ns
t_r	Rise time				12	20	ns
t_s	Storage time				7	15	ns
t_f	Fall time				6	15	ns

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

gates and transistors combined

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	I_C ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output				20	30	ns
t_{TLH}	Transition time, low-to-high-level output				7	12	ns
t_{THL}	Transition time, high-to-low-level output				9	15	ns
V_{OH}	High-level output voltage after switching	15	V_S = 20 V, I_C ≈ 300 mA, R_{BE} = 500 Ω	V_S−6.5			mV

SERIES 55460/75460
DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 7312055, SEPTEMBER 1973

PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

performance

- 300-mA Output Current Capability
- High-Voltage Outputs
- No Output Latch-Up at 30 V
- Medium-Speed Switching

ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL or DTL Compatible Diode-Clamped Inputs
- Standard Supply Voltages

SUMMARY OF SERIES 55460/75460

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55460	AND†	J, JB
SN55461	AND	JP, L
SN55462	NAND	JP, L
SN55463	OR	JP, L
SN55464	NOR	JP, L
SN75460	AND†	J, N
SN75461	AND	L, P
SN75462	NAND	L, P
SN75463	OR	L, P
SN75464	NOR	L, P

†With output transistor base connected externally to output of gate

description

Series 55460/75460 dual peripheral drivers are functionally interchangeable with Series 55450B/75450B peripheral drivers, but are designed for use in systems that require higher breakdown voltages than Series 55450B/75450B can provide at the expense of slightly slower switching speeds. Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55460 drivers are characterized for operation over the full military temperature range of −55°C to 125°C; Series 75460 drivers are characterized for operation from 0°C to 70°C.

The SN55460 and SN75460 are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage, n-p-n transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The SN55461/SN75461, SN55462/SN75462, SN55463/SN75463, and SN55464/SN75464 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

CONTENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55460	SN55461 SN55462 SN55463 SN55464	SN75460	SN75461 SN75462 SN75463 SN75464	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	7	7	V
Input voltage		5.5	5.5	5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	5.5	5.5	V
V_{CC}-to-substrate voltage		40		40		V
Collector-to-substrate voltage		40		40		V
Collector-base voltage		40		40		V
Collector-emitter voltage (see Note 3)		40		40		V
Collector-emitter voltage (see Note 4)		25		25		V
Emitter-base voltage		5		5		V
Output voltage (see Note 5)			35		35	V
Collector current (see Note 6)		300		300		mA
Output current (see Note 6)			300		300	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 7)		800	800	800	800	mW
Operating free-air temperature range		−55 to 125	−55 to 125	0 to 70	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, JB, JP, or L package	300	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	260	260	°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This value applies between 0 and 10 mA collector current when the base-emitter diode is open-circuited.
5. This is the maximum voltage which should be applied to any output when it is in the off state.
6. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
7. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 16. This rating for the L package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 95 °C/W.

recommended operating conditions (see Note 8)

	SERIES 55460			SERIES 75460			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 8: For the SN55450B and SN75450B only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

TEXAS INSTRUMENTS
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TYPE SN75461
DUAL PERIPHERAL POSITIVE-AND DRIVER

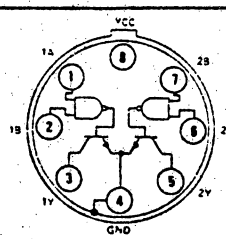
logic

FUNCTION TABLE

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

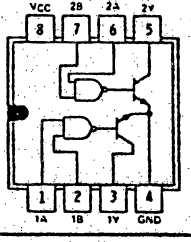
H = high level, L = low level

L
PLUG-IN PACKAGE (TOP VIEW)



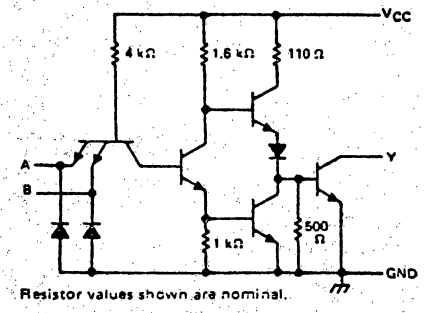
PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = AB

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA		−1.2	−1.5	V
I_{OH}	High-level output current	7	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 35 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.15	0.4	V
			V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.36	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	10	V_{CC} = 5.25 V, V_I = 5 V		8	11	mA
I_{CCL}	Supply current, outputs low		V_{CC} = 5.25 V, V_I = 0		61	76	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω		45	55	ns
t_{PHL}	Propgation delay time, high-to-low-level output				30	40	ns
t_{TLH}	Transition time, low-to-high-level output				8	20	ns
t_{THL}	Transition time, high-to-low-level output				10	20	ns
V_{OH}	High-level output voltage after switching	15	V_S = 30 V, I_O ≈ 300 mA	V_S−10			mV

TEXAS INSTRUMENTS
INCORPORATED
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ANALOG DEVICES

Programmable Multifunction Module

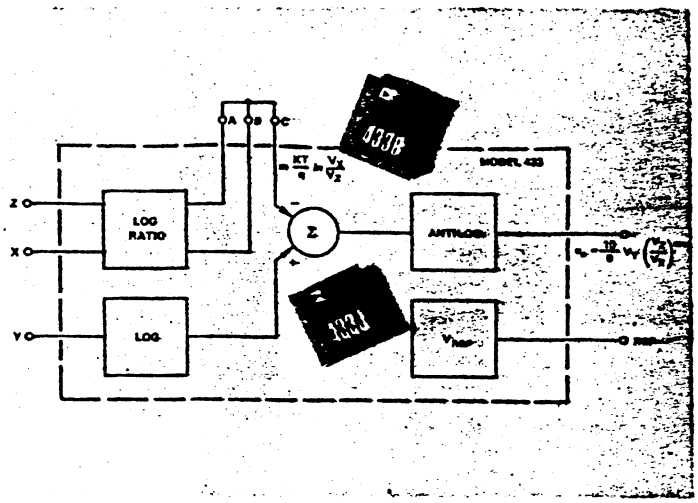
MODEL 433J/B

FEATURES

- **Versatility: Provides Transfer Characteristics of Several Function Modules**
- **Divides Over a 100:1 Range With a Max Error of 0.25% (433B)**
- **Internal Voltage Reference**
- **Hermetically Sealed Semiconductors**
- **No External Trims Required**
- **Low Noise**
- **Low Cost: $75 (1-9) 433J**

APPLICATIONS

- **Transducer Linearization**
- **Signal Processing**
- **Raising to Arbitrary Powers**
- **Vector Functions**
- **Trigonometric Functions (Sine, Cosine, Arctangent)**



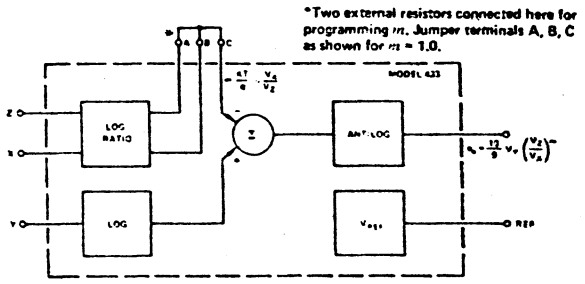


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The model 433 is an extremely versatile function module which implements the transfer function:

$$e_o = \frac{10}{9} V_y \left(\frac{V_z}{V_x}\right)^m, \quad 0.2 \leq m \leq 5.0$$

By either jumper connections on the pins, or selection of two external resistors the user can program the 433 to: multiply, divide, square, square root, root of a ratio, square of a ratio, or raise voltage ratios to an arbitrary power, m.

When used with a low cost op amp, such as AD741, the model 433 may be used to compute the true rms value of a varying signal. With two such op amps, the 433 can be used to perform accurate vector computations over wide ranges of the vector sum.

Due to its log/antilog circuit approach, signal levels of 100mV to 10V may be processed with a maximum output error of 0.25% F.S. (433B). The allowable input range for the three input variables is 0.01 to +10V, for which there is a typical error of ±5mV ±0.3% of the theoretical output voltage for model 433J, and ±1mV ±0.15% for 433B.

Because of its small size, accuracy, versatility, and speed (and all at low cost), the model 433 will prove to be an essential component in equipment requring on-the-spot computations in real time, or for linearizing a wide range of transducer characteristics in medical, industrial, and process control equipment. Designed with the OEM's needs in mind, the model 433 is attractively priced for new equipment designs.

PRINCIPLE OF OPERATION

The model 433 is comprised of log and antilog circuits interconnected as shown in Figure 1. The log ratio circuit provides the log of V_x/V_z to terminals A, B, C where, for exponents other than unity, it is scaled by two external programming resistors (see hook-up diagrams for connection and values of these two resistors). The scaled log ratio from terminal C is subtracted from a signal proportional to the log of V_y. The resulting expression is operated on by the antilog circuit, yielding an output of

$$e_o = \frac{10}{9} V_y \left(\frac{V_z}{V_x}\right)^m$$

The voltage reference circuit is a high stability (0.005%/°C) voltage source which is generated internally. It is provided as an output terminal for user convenience, and may be used as a constant at any of the input terminals.

ONE-QUADRANT DIVIDER

When connected as a divider, the model 433B has less than ¼% output error over an input signal range of 100:1. This performance is obtained with no external trims, and is nearly twenty times better than that attainable with a 0.1% multiplier/divider connected in a feedback loop.

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast Tel: 213/595-1783
Mid-West Tel: 312/297-8710

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

Model	433J	433B
Transfer Function	$e_o = + \frac{10}{9} V_y \left(\frac{V_z}{V_x}\right)^m$	*
Rated Output[1]	+10.5V @ 5mA, min	*
Input		
Signal Range	$0 \leqslant V_x, V_y, V_z \leqslant +10V$,	*
Max Safe Input	$V_x, V_y, V_z \leqslant \pm 18V$	*
Resistance		
X Terminal	100kΩ ±1%	*
Y Terminal	90kΩ ±10%	*
Z Terminal	100kΩ ±1%	*
External Adjustment of the Exponent, m		
Range for m <1 (Root)	$1/5 \leqslant m < 1$, $m = \frac{R_2}{R_1 + R_2}$	*
Range for m > 1 (Power)	$1 \leqslant m < 5$, $m = \frac{R_1 + R_2}{R_2}$	*
	$(R_1 + R_2) \leqslant 200\Omega$	*
Accuracy (Divide Mode)[2,3]		
Total Output Error @ +25°C (for specified input range)		
Typical (RTO)	±5mV ±0.3% of output	±1mV ±0.15% of output
Max Error (RTO)	±50mV	±25mV
Input Range ($V_z \leqslant V_x$)	0.01V to 10V, V_z	*
	0.1V to 10V, V_x	*
Over Specified Temp. Range	±1%	±1% max
Output Offset Voltage (Not Adjustable)		
Initial @ +25°C	±5mV	±2mV max
Offset vs Temp.	±1mV/°C	±1mV/°C max
Noise, 10Hz to 1kHz		
V_x = +10V	100μV rms	*
V_x = +0.1V	300μV rms	*
Bandwidth, V_y, V_z		
Small Signal (-3dB), 10% of DC Level	V_y or V_z	*
$V_y = V_z = V_x$ = 10V	100kHz	*
$V_y = V_z = V_x$ = 1V	50kHz	*
$V_y = V_z = V_x$ = 0.1V	5kHz	*
$V_y = V_z = V_x$ = 0.01V	400Hz	*
Full Output (V_y or V_z = 5VDC ±5VAC)	(V_x) x (5kHz)	*
Reference Terminal Voltage[1]		
V_{ref} (Internal Source)	+9.0V ±5% @ 1mA	*
vs Temp (0 to +70°C)	±0.005%/°C	*
Power Supply Range		
Rated Performance	±15VDC @ 10mA	*
Operating	±(12 to 18)VDC	*
Temperature Range		
Rated Performance	0 to +70°C	-25°C to +85°C
Storage	-55°C to +125°C	-55°C to +125°C
Mechanical		
Case Size	1.5" x 1.5" x 0.62"	*
Mating Socket	AC1038	*
Price		
(1–9)	$75	$87
(10–24)	$69	$77

*Same specifications as 433J.

[1] Terminals short circuit protected to ground.

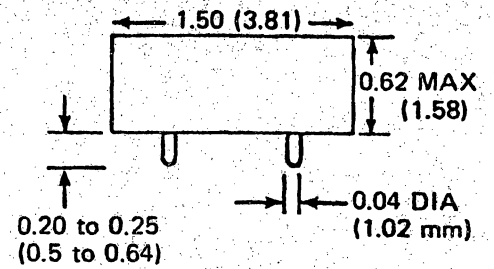
[2] Accuracy is specified in divide mode which is a worst case condition. Input range is 10mV to 10V for specified accuracy when connected as a multiplier.

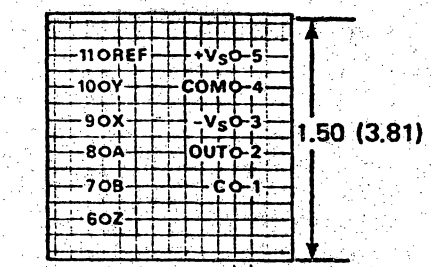
[3] Error is defined as the difference between the measured output and the theoretical output for any given pair of specified input voltages.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (cm).



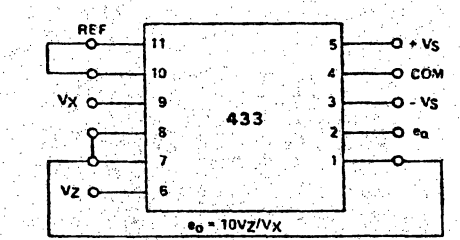


Mating Socket AC 1038
$3.00 (1–9)

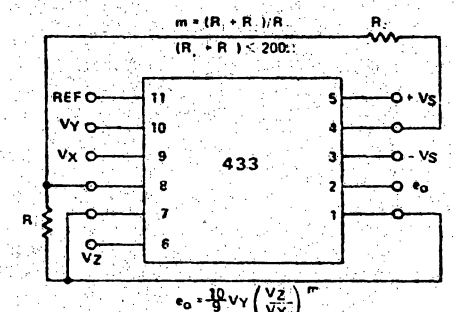
WIRING CONNECTIONS

Bottom View Shown in All Cases

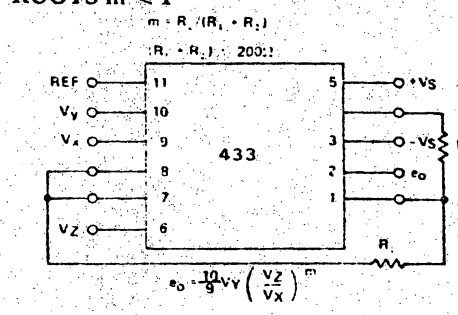
DIVIDE MODE m = 1



POWERS m ⩾ 1



ROOTS m ⩽ 1



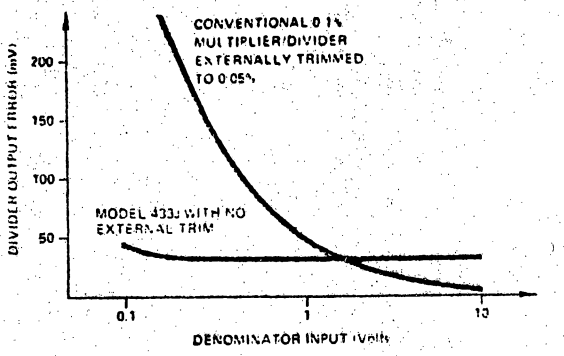


Figure 2. Comparison of Divider Error vs. Denominator Level for Model 433J and a Conventional Mult./Div.

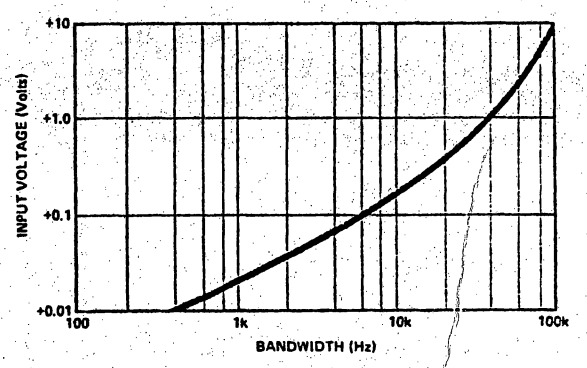


Figure 3. 433 Small Signal Bandwidth vs. Input Voltage

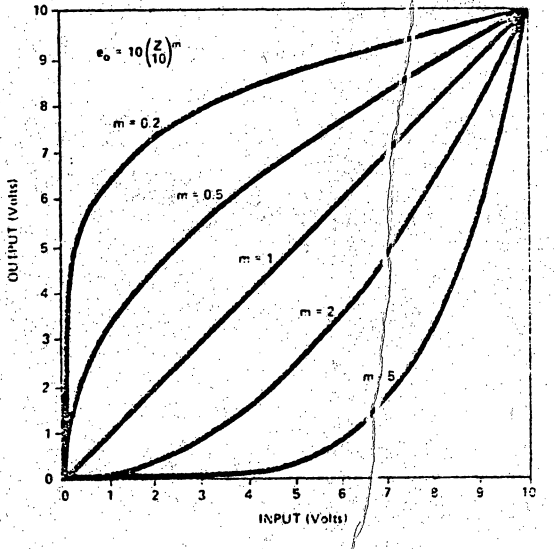


Figure 4. Varying the Exponent, m

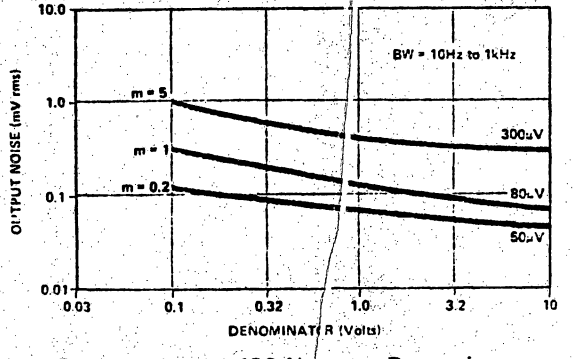


Figure 6. Model 433 Noise vs. Denominator for Various Exponents, m

MODEL 433B – 0.25% DIVIDER, WIDE DYNAMIC RANGE

Probably the most impressive performance improvement owing to model 433's log/antilog circuit approach, is its ability to hold high divider accuracies over a wide 100:1 input signal range.

When using a conventional multiplier/divider as a divider, accuracy, offset drift, and noise performance are all degraded as the denominator is decreased.

For model 433, accuracy, offset drift, and noise performance are all virtually independent of denominator level as illustrated in Figure 2 and this performance is obtained with no external trims.

FREQUENCY RESPONSE

A curve of amplitude vs. bandwidth for model 433 is shown in Figure 3. For all input terminals, the small signal frequency response (-3dB point) is signal level dependent, decreasing from 100kHz for a 10V input to 400Hz for a 10mV input. These small signal measurements are made by superimposing a 10% small signal amplitude on the DC level being characterized.

Full output for a ±5 volt signal superimposed on a 5VDC level is 50kHz for the multiplier, and V_X x 5kHz for the divider.

VARYING THE EXPONENT, m

Presented in Figure 4 is a family of curves which illustrates the effect of varying the exponent, *m*. All curves have been scaled for the full scale output of 10V by reducing the 433's transfer equation to $e_O = 10\ (V_Z/V_X)^m$. For applications where a continuous variation in *m* is desired, connections should be made as shown in Figure 5C. Model 433 features very small accuracy changes (≈0.1%) as *m* is adjusted over the entire range from 0.2 to 5.

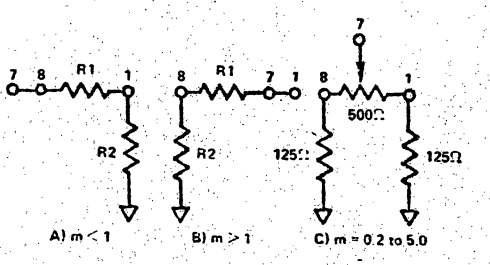


Figure 5. Resistor Programming for the Exponent, m.

Various values of *m* are programmed by two external resistors, R_1 and R_2. For values of $m < 1$ resistor connections are made to terminals, 1, 7, 8 as shown in Figure 5A. For values of $m > 1$, see Figure 5B. For $m = 1$, connect terminals 1, 7 and 8 together.

NOISE PERFORMANCE

The curves shown in Figure 6 are for output noise vs. signal level in a 1kHz BW for worst case conditions. These conditions exist when V_X is equal to V_Z and is varied over the specified range. It should be noted that for 0.1V inputs the effective gain is 100. To retain the full performance capability of model 433, all external noise sources should be isolated from the input terminals.

An exceptional advantage of the 433 over other means of dividing is revealed by these curves. That feature being that noise is virtually independent of signal level. For a 100:1 signal level change of the denominator, the output noise is changed only 3:1. Division by using a multiplier in the feedback loop exhibits a 100:1 increase in output noise for a denominator signal level change of 100:1.

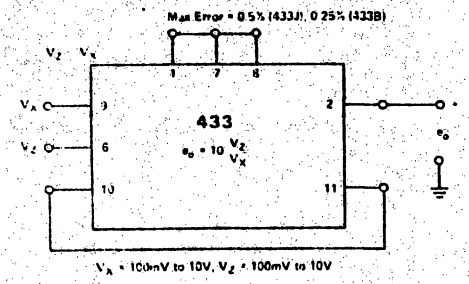


Figure 7. Divider

When connected as a divider as shown above, the 433 has less than ½% error (50mV) for input signals from 100mV to 10V. Output noise, offset drift and accuracy are all virtually independent of signal level and no trims are required.

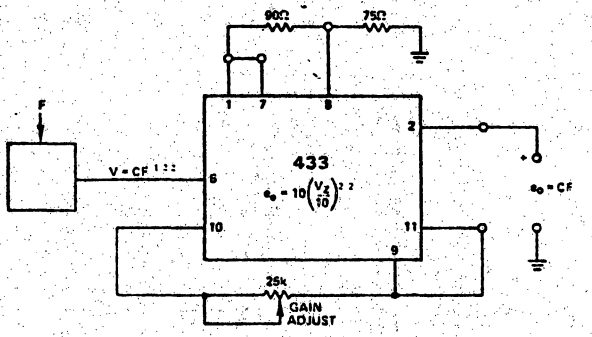


Figure 8. Transducer Linearization

A transducer's output may be linearized by utilizing the 433 as an exponentiator. In the example above, a transducer is used to convert a force, F, to a voltage, V. The desired relationship being V directly proportional to F; i.e., V = CF where C is constant.

The actual output for this example is proportional to F, but is a nonlinear relation which can be approximated by $CF^{1/2.2}$. Connecting the 433 as shown with $m = 2.2$ provides the desired relation of $e_O = CF$.

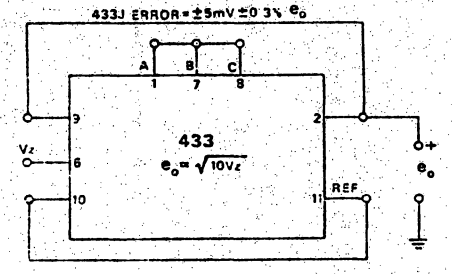


Figure 9. Square Root

The square root of a single variable may be obtained with no external components when connected as shown above. Noise performance is even better than that for the multiply or divide mode.

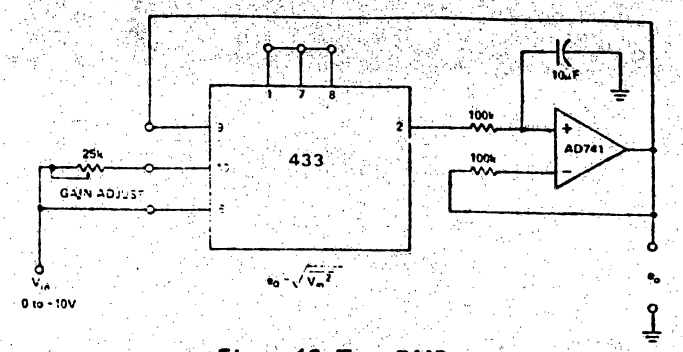
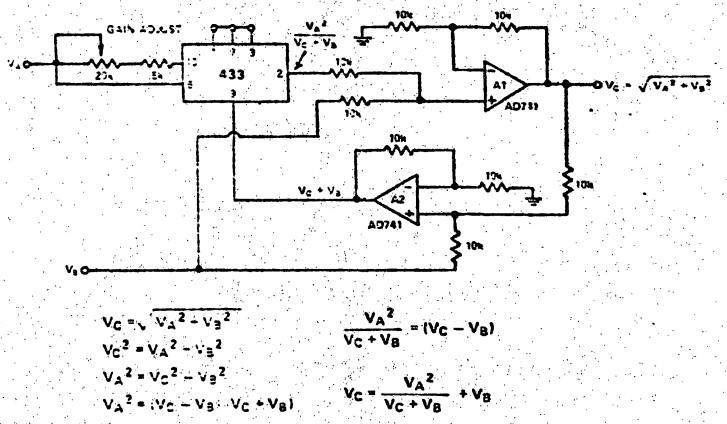


Figure 10. True RMS

By combining the 433 with a simple filter, using an external op amp as shown above, the true RMS value of a one quadrant input signal may be computed. Accuracy is not degraded by crest factor, provided the maximum input is 10V or less.

The 433 output is applied to an integrator to average the signal and is then fed back to the X input to obtain the square root of the mean square of the input.

Accuracy of 5mV + 0.1% of reading may be achieved over an input range of 500:1.



$$V_C = \sqrt{V_A^2 + V_B^2}$$

$$V_C^2 = V_A^2 - V_B^2$$

$$V_A^2 = V_C^2 - V_B^2$$

$$V_A^2 = (V_C - V_B)(V_C + V_B)$$

$$\frac{V_A^2}{V_C + V_B} = (V_C - V_B)$$

$$V_C = \frac{V_A^2}{V_C + V_B} + V_B$$

Figure 11. Vector Computation $V_C = \sqrt{V_A^2 + V_B^2}$

The vector computation circuit shown in Figure 11 illustrates the extreme versatility of model 433. Used with two inexpensive op amps the 433 is used as a basic building block, which in this case, provides the square root of the sum of the squares.

This application is based on the identity for the difference of squares. The derivation is shown by the equations above and the final equation for V_C is implemented.

Due to the excellent inherent accuracy of the above circuit (error = 0.1% of reading), matched resistors with a low T.C. should be used. Errors of only 0.1% of the theoretical output may be achieved over signal levels of +100mV to +10V.

The usefulness of model 433 extends beyond the illustrative examples shown above. Model 433 may also be used to generate basic trigonometric functions (sine, cosine, arctangent). Further detailed applications information on model 433 is provided in the Nonlinear Circuits Handbook, published by Analog Devices.

ANALOG DEVICES

CMOS 8 and 4 Channel Analog Multiplexers

GENERAL DESCRIPTION

The AD7501 is an 8 channel analog multiplexer which switches one output to one of 8 inputs depending on the state of 3 binary inputs. An "enable" control allows for disconnecting the output regardless of the digital input states. The AD7502 is identical to the AD7501 except it has 2 outputs switched to two of 8 inputs depending on 2 binary inputs.

ORDERING INFORMATION

AD7501J:	0 – +75°C	AD7502J:	0 – +75°C
AD7501K:	0 – +75°C	AD7502K:	0 – +75°C
AD7501S:	-55°C – +125°C	AD7502S:	-55°C – +125°C

PACKAGE VERSIONS

Suffix "D": Ceramic Dip
Suffix "N": Plastic Dip

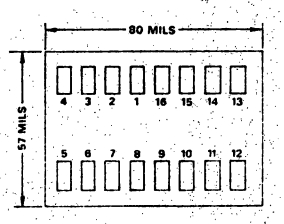
ABSOLUTE MAXIMUM RATINGS

V_{DD} – (to Gnd)	+17V
V_{SS} – (to Gnd)	-17V
Switch Voltage (to V_{SS})	+27V
Switch Current	10mA
Digital Input Voltage Range	V_{DD} to GND
Power Dissipation (package)	
up to +75°C	450mW
derates above +75°C at	6mW/°C
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C

CAUTION:

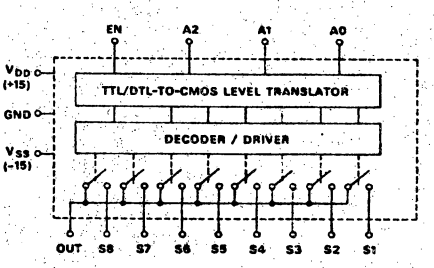
1. Do not apply voltages higher than V_{DD} and V_{SS} on any other terminal, especially when $V_{SS} = V_{DD} = 0V$ all other pins should be at 0V.
2. The digital control inputs are zener protected. However, permanent damage can occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

BONDING DIAGRAM

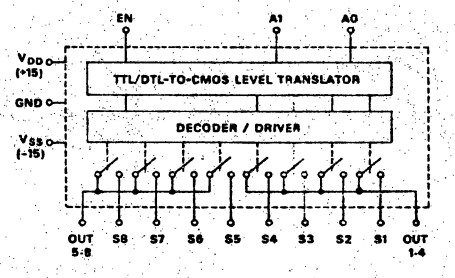


FUNCTIONAL DIAGRAMS

AD7501



AD7502



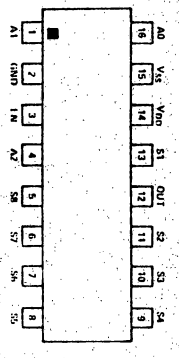
TRUTH TABLES

AD7501				
A_2	A_1	A_0	E_N	ON
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8
X	X	X	L	NONE

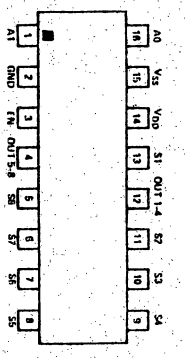
AD7502			
A_1	A_0	E_N	ON
L	L	H	1 & 5
L	H	H	2 & 6
H	L	H	3 & 7
H	H	H	4 & 8
X	X	L	NONE

PIN CONFIGURATION (TOP VIEW)

AD7501



AD7502



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Tel: 617/329-4700 TWX: 710/394-6577
West Coast Tel: 213/595-1783
Mid-West Tel: 312/297-8710

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = -15V unless otherwise noted)

PARAMETER			SWITCH	T_A (°C)	MIN	TYP	MAX	UNIT	TEST CONDITIONS
ANALOG SWITCH									
R_{ON}			ON	+25		170	300	Ω	-10V ≤ V_S ≤ +10V I_S = 1mA
R_{ON} vs. V_S			ON	+25		20		%	V_S = -10V to +10V I_S = 1mA
R_{ON} vs. Temperature			ON			0.5		%/°C	
R_{ON} between Switches			ON	+25		4		%	V_S = 0V I_S = 1mA
R_{ON} vs. Temperature between Switches			ON			±0.01		%/°C	
I_S		Commercial	OFF	+25		0.2	2	nA	V_S = -10V, V_{OUT} = +10V and V_S = +10V, V_{OUT} = -10V
			OFF	0 to +75			50	nA	
		Military	OFF	+25			0.5	nA	
			OFF	-55 to +125			50	nA	
I_{OUT}	AD7501	Commercial	OFF	+25		1.0	10	nA	V_S = -10V, V_{OUT} = +10V and V_S = +10V, V_{OUT} = -10V "enable" low
			OFF	0 to +75			250	nA	
		Military	OFF	+25			5	nA	
			OFF	-55 to +125			250	nA	
	AD7502	Commercial	OFF	+25		0.6	5	nA	
			OFF	0 to +75			125	nA	
		Military	OFF	+25			3	nA	
			OFF	-55 to +125			125	nA	
$\|I_{OUT} - I_S\|$			ON	+25			5	nA	V_S = 0
DIGITAL CONTROL									
V_{INL}				+25			0.8	V	
V_{INH}	AD7501J AD7502J			+25	4			V	SEE NOTE
	AD7501K AD7501S AD7502K AD7502S			+25	2.4			V	
I_{INL} or I_{INH}		Commercial		+25		10		nA	
				0 to +75		100		nA	
		Military		-55 to +125		1		µA	
C_{IN}				+25		3		pF	
DYNAMIC CHARACTERISTICS									
T_{ON}				+25		0.8		µs	
T_{OFF}				+25		0.8		µs	
C_S			OFF	+25		5		pF	
C_{OUT}			OFF	+25		30		pF	
$C_{S\text{-}OUT}$			OFF	+25		0.5		pF	
C_{SS} between any two switches			OFF	+25		0.5		pF	
POWER SUPPLY									
I_{DD} (Quiescent)			OFF	+25		1	100	µA	ALL DIGITAL
I_{SS} (Quiescent)			OFF	+25		1	100	µA	INPUTS LOW
I_{DD}			ON	+25		0.2	0.5	mA	ALL DIGITAL
I_{SS}			ON	+25		1	100	µA	INPUTS HIGH
PRICE (1-49)									
AD7501JD/AD7502JD						28.00		$	
AD7501JN/AD7502JN						18.00		$	
AD7501KD/AD7502KD						30.00		$	
AD7501KN/AD7502KN						20.00		$	
AD7501SD/AD7502SD						44.00		$	

NOTE: A pull-up resistor, typically 1-2kΩ, is required to make the AD7501J and AD7502J compatible with TTL/DTL levels. The maximum value is determined by the output leakage current of the driver gate when in the high state.

Specifications subject to change without notice.

C174a–5–4/74

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ANALOG DEVICES

CMOS 8 and 16 Channel Analog Multiplexers

PRELIMINARY DATA SHEET

AD7506/AD7507

FEATURES

R_{ON}	300Ω
Power Dissipation	1.5 mW

- TTL/DTL/CMOS Compatible
- Break Before Make Switching
- Silicon Nitride Passivation
- Replaces DG506/DG507

GENERAL DESCRIPTION

The AD7506 is a monolithic CMOS 16-channel analog multiplexer packaged in a 28-pin DIP. It switches a common output to one of 16 inputs, depending on the state of four address lines and an "enable". The AD7507 is identical to the AD7506 except it has two outputs switched to two of 16 inputs depending on three binary address states and an "enable".

The AD7506 and AD7507 are excellent examples of a high breakdown CMOS process combined with a double layer interconnect for high density. Both units are silicon/nitride passivated featuring increased stability and reliability.

ORDERING INFORMATION

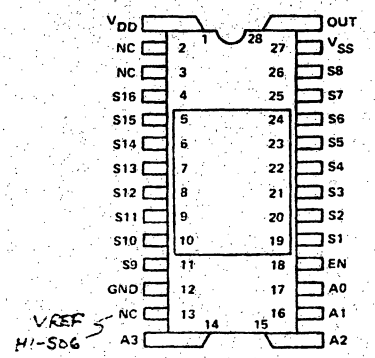
AD7506J	:	0°C to +75°C
AD7506K	:	0°C to +75°C
AD7506S	:	−55°C to +125°C
AD7506T	:	−55°C to +125°C
AD7507J	:	0°C to +75°C
AD7507K	:	0°C to +75°C
AD7507S	:	−55°C to +125°C
AD7507T	:	−55°C to +125°C

PACKAGE VERSIONS

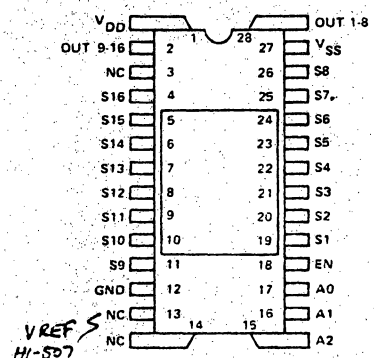
Suffix "D": 28-pin Ceramic DIP

PIN CONFIGURATION (TOP VIEW)

AD7506

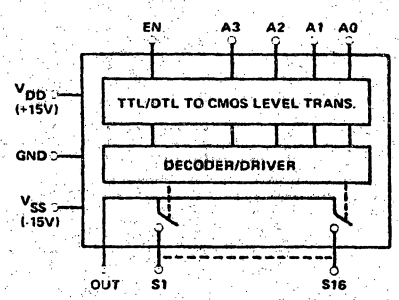


AD7507



FUNCTIONAL DIAGRAMS

AD7506



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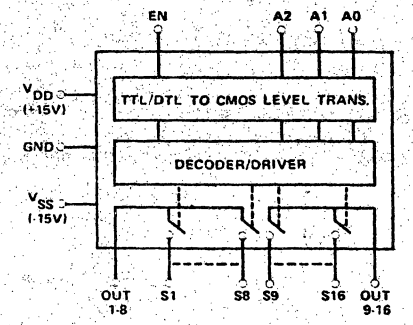
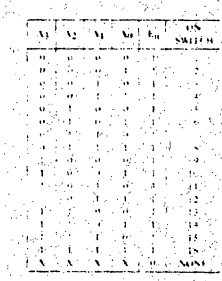


TRUTHTABLE

AD7506



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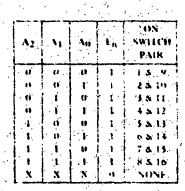

ABSOLUTE MAXIMUM RATINGS

V_{DD} (to GND)	+17 V
V_{SS} (to GND)	−17 V
Switch Voltage (to V_{SS})	+27 V
Digital Input Voltage Range	V_{DD} to GND
Switch Current	10 mA
Power Dissipation (Package)	
To +70°C	1200 mW
Derate Above +70°C by	10 mW/°C
Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6777

SPECIFICATIONS (V_{DD} = +15 V, V_{SS} = −15 V unless otherwise noted)

PARAMETER		VERSION	SWITCH CONDITION	@ 25°C			Over Specified Temp. Range		UNITS	TEST CONDITIONS
				MIN	TYP	MAX	MIN	MAX		
ANALOG SWITCH										
R_{ON}		J, K	ON		300	450		550		V_S = −10 V to +10 V, I_S = 1 mA
		S, T	ON			400		500		
R_{ON} vs. V_S		All	ON		15				%	
R_{ON} vs. Temperature		All	ON		0.5				%/°C	
R_{ON} Between Switches		All	ON		4				%	V_S = 0 V, I_S = 1 mA
R_{ON} Between Switches vs. Temperature		All	ON		0.05				%/°C	
I_S		J, K	OFF		0.05	5		50	nA	
		S, T	OFF		0.05	1		50	nA	V_S = −10 V, V_{OUT} = +10 V
I_{OUT}	AD7506	J, K	OFF		0.3	20		500	nA	and
		S, T	OFF		0.3	10		500	nA	V_S = +10 V, V_{OUT} = −10 V
	AD7507	J, K	OFF		0.3	10		250	nA	"Enable" Low
		S, T	OFF		0.3	5		250	nA	
$I_{OUT} - I_S$	AD7506	J, K	ON		0.3	20		500	nA	
		S, T	ON		0.3	10		500	nA	V_S = 0
	AD7507	J, K	ON		0.3	10		250	nA	
		S, T	ON		0.3	5		250	nA	
DIGITAL CONTROL										
V_{INL}								0.8	V	
V_{INH}		J, S					3.0		V	Note 2
		K, T					2.4		V	
I_{INL} or I_{INH}		All				10		30	μA	
C_{IN}		All			3				pF	
DYNAMIC CHARACTERISTICS										
$t_{transition}$		J, S			700				ns	
		K, T			700	1000			ns	V_{IN}: 0 to 3.0 V
t_{open}		All			100				ns	
$t_{on(En)}$		J, S			0.8				μs	
		K, T				1.5			μs	V_{EN}: 0 to 3.0 V
$t_{off(En)}$		J, S			0.8				μs	
		K, T				1			μs	
"OFF" Isolation		All			70				dB	V_{EN} = 0, R_L = 200 Ω, C_L = 3.0 pF, V_S = 3.0 VRMS, f = 500 kHz
C_S		All	OFF		5				pF	
C_{OUT}		All	OFF		40				pF	
C_{S-OUT}		All	OFF		0.5				pF	
C_{SS} Between Any Two Switches		All	OFF		0.5				pF	
POWER SUPPLY										
I_{DD} (Standby)		J, K	OFF		0.05	1			mA	
		S, T	OFF		0.05	1		2	mA	All Digital Inputs Low
I_{SS} (Standby)		J, K	OFF		0.05	1			mA	
		S, T	OFF		0.05	1		2	mA	
I_{DD}		J, K	ON		0.3	1			mA	
		S, T	ON		0.3	1		2	mA	All Digital Inputs High
I_{SS}		J, K	ON		0.05	1			mA	
		S, T	ON		0.05	1		2	mA	
PRICE (1-49)	AD7506	J			38.00				$	
		K			40.00				$	
		S			76.00				$	
		T			80.00				$	
	AD7507	J			38.00				$	
		K			40.00				$	
		S			76.00				$	
		T			80.00				$	

NOTES:
1. Specifications subject to change without notice.
2. A pull-up resistor, typically 1–2 kΩ is required to make the J and S versions compatible with TTL/DTL. The maximum value is determined by the output leakage current of the driver gate when in the high state.