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DIGITAL DELAY AND MULTIPLIER SYSTEM MULTIPLIER AND SYSTEM CONTROLLER SECTIONS MAINTENANCE MANUAL
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## SPECIFICATIONS

Al3500N3 Communications Between Digital Delay-Multiplier System S-l and VLA Synchronous Computers

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## LOGIC DRAWINGS

| D13500L1 | High Speed Integrators |
| :---: | :---: |
| D13500L4 | Low Speed Integrators |
| D13500L5 | Multipliers |
| C13500L6 | Vs Counter, BT and Reset Card |
| D13500L7 | Multiplier Control A |
| D13500L8 | Multiplier Control B |
| D13500L9 | Temporary Storage for Multipliers |
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| D13500L19 | Boss $\rightarrow$ SC, Requested Mult. Address and Control Register |
| D13500L20 | Delay Word Storage, Delay Test Generator, Delay/Sampler Output Shift Registers |
| D13500L21 | Data Control, Boss $\rightarrow$ SC and SC $\rightarrow$ Delays |
| D13500L22 | Exchange Data Generator, Go/No Go Storage |
| D13500L2 3 | Boss $\rightarrow$ SC Parity Storage and Delay Mux. Registers |
| D13500L24 | System Control, Rom 2 |
| D13500L25 | Ram Address Memory, Rom 1 |
| Dl3500L26 | Ram Bits $2^{0}$ to $2^{7}$, Address Register |
| D13500L27 | Ram Bits $2^{8}$ to 215 |
| Dl3500L28 | Ram Bits $2^{16}$ to 223, VLAC Output |
| D13500L29 | Vs Subtractor, Rom 5 and Rom 6 |
| D13500L30 | CRT $\leftrightarrow$ SC, CRT Output and Input, Update Control |
| D13500L31 | CRT $\rightarrow$ SC, Control and Storage, Rom 3 |

LOGIC DRAWINGS (cont.)

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D13500L32 SC->CRT Control, Rom 4
D13500L33 SC->CRT Storage and Binary to BCD Converter
Dl3500L34 Alarm and Reset Control
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Dl3500L36 System Monitor Analog Multiplexers
Dl3500L37 System Monitor Alarm and Storage, Rom 7
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## I. RELATED MATERIAL

## Memoranda

'Digital Delay System for the VLA', VLA Electronics \#103
'Digital Delay and Multiplier', VLA Electronics \#ll3
'Reliability Study of VLA Digital Delay and Multiplier', VIA Electronics \#121

## Reports

'Digital Delay and Multiplier System Two Antenna PrototypeObserver's Manual', VLA Technical Report \#16

## Specifications

Digital Delay and Multiplier P.C. Mother Boards Al3500Nl, Rev. A
Digital Delay and Multiplier-Signal Transmission Cable
Communication Between Digital Delay-Multiplier System and VLA Synchronous Computers

VLA Delay and Multiplier System Prototype P.C. Card Assemble and Test Specification

Al3510N1
NRAO VLA Digital Delay and Multiplier MultiLayer Printed Circuit Cards

A13510N2
Test Specifications for the Multiplier P.C. Board

Al3500N2

Al3500N3, Rev. B

Al 3540NI


The Two Antenna Prototype System.


## II. INTRODUCTION

This report will cover the theory of operation for the Multiplier and System Controller Sections of the Digital Delay-Multiplier System which is made up of a total of four sections - Samplers, Delays, Multipliers, and System Controller. The theory of operation for the Sampler and the Delay Sections are described separately in different reports. The Digital Delay-Multiplier System consists of two identical 50 MHz sections each operating independently from one another and without any interconnections; thus for simplification, this report will consider only one of the 50 MHz sections unless otherwise noted. This report describes the full system although all antennas are not in operation at this time. The main difference between the final system and the present prototype is the number of multiple cards required in the Multiplier Section; and in the System Controller section, ROM1 and ROM2 will need to be expanded to handle more antennas.

This report is not intended to give a person an overall view; but instead, this report deals mainly with the detailed logic description of the Multiplier and System Controller. To gain an overall picture of the Digital Delay System, one should refer to VLA Technical Report \#16 'Digital Delay and Multiplier System-Two Antenna Prototype Observer's Manual'.

Table 1 lists all memoranda, specifications, drawings, reports, and any other information relating to the Digital Delay System.

Before proceeding to the theory of operation one should have an understanding of the system layout, location terminology, and logic drawing nomenclature. Drawings D13500P18 and C13500P19 illustrate the layout of the racks and the System Controller chassis layout along with the nomenclature used on the logic drawings and also the IC layout of the wire wrap cards. As illustrated in the drawings and figures, all components can be located by an alphanumeric coding system which alternates between alphabetical and numerical characters. The following are some samples and notes:

1. Multiplier mother board, see Drawing Dl3500pl8
2. Jack on System Controller, see :Drawing Dl3500pl8

3. Plugs on the end of a cable are always referred to with the letter P. Jacks on a panel surface are always referred to with the letter J.
4. In many instances the complete designation number is not used; however, this is done in such a manner that an ambiguity should not exist.
5. IC locations and pin number, see Figure 1.
$\prod_{\rightarrow \rightarrow \rightarrow \rightarrow}^{2} \stackrel{B}{\longrightarrow}$ IC pin no.

Each logic drawing represents all the logic on one printed circuit or wire wrap card. Figure 1 illustrates the nomenclature found inside the logic symbols and also signal descriptions. All flip-flops are given an $F$ number. If a flip-flop is part of a counter, register, or closely associated with other flip-flops in logic operation, then
they are given dash numbers, e.g. F2-10, which would be referred to as the $2^{10}$ bit of the F 2 counter. Gate outputs, which cannot be drawn with a continuous line to the input point(s), are given an identification number, e.g. G6 or C5. The $C$ number indicates that the gate output is a free running clock in megahertz at the frequency indicated by the number; e.g. C 5 is a 5 MHz clock. Examples of these and others are as follows:

1. F5 The $Q$ output from a flip-flop
2. $\overline{F 5}$ The $\bar{Q}$ output from a flip-flop
3. F5A Same signal as F5 but from different drive point
4. G6 A gate output
5. G6A Same signal as $G 6$ but from a different drive point
6. C5" The same logical signal -5 MHz clock, but with a
7. C5' $\}$ gate delay difference between each.
8. C5
9. C5.55 ${ }^{\circ}$ The dot indicates that the clock frequency is not exactly 5.55 MHz
10. CI. 85 1.85 MHz clock
11. CAl. 85 1.85 clock but phase shifted from C1. 85 clock.
12. C-B Clock pulse "B" - see Drawing Dl3500B5
13. M2-10 Similar to $G$ number but the output device is a rom or a ram
14. 19F4-0 Output of a flip-flop which is located on logic drawing Dl3500L19. Notice that the last 2 digits of the logic drawing is used to prefix the number so that one will know where the signal originates.
15. Prefix to any of the above examples (1-13) will have the same meaning as the prefix illustrated in No. 14 above.
16. R5 Resistor number 5
17. L5 The last digits of the logic drawing
18. 

$\left.\right|_{\rightarrow \rightarrow \rightarrow \rightarrow} ^{A L}$ Least significant bit
19.


On each logic drawing along the right hand edge is listed the input/output pins on the logic card. The number-letter at the top is the edge connector designation that the card plugs into. On the outside of this block is the list of the input/output signals on each pin along with an arrow which indicates whether the signal is an input or an output on the card. The numbers inside the block make up the back plane wiring list. On many of the logic drawings for the multiplier section the connector block is not filled in because there are several cards of each type thus making it impossible to fill in the information on one drawing that would be representative for all the back plane wiring.

Also on each logic drawing in the System Controller section there are two additional tables. The table titled "Card Locations" list each logic number and its corresponding card slot location. The other table, which is called "Signal Origin" is located, in most cases; in the upper left hand corner. The Signal Origin table lists all the $F$ and $G$ numbers that originate on the drawing and give the quadrant of the drawing in which they originate. The quadrants of the drawing are as follows:

| $A$ | $B$ |
| :---: | :---: |
| $C$ | $D$ |

The logic drawings also contain a lot of additional information in the form of notes, truth tables, and partial timing diagrams. A list of abbreviations used on the drawings along with the abbreviations used in figures and this report are listed in Table 6.

The entire Digital Delay System is operated synchronously. The Multiplier section is operated in synchronism with the 100 MHz clock from the Local Oscillator while the System Controller section is operated in synchronism with a 5 MHz clock which is crystal controlled on the System Controller Clock card. If a signal passes from one logic
element controlled by one clock to a logic element controlled by another it is done thru an asynchronous to synchronous element.
III. MULTIPLIER SECTION

The Multiplier Section is contained in two racks and is made up of the following logic cards:

| LOGIC CARD TYPE | DRAWING NO. | NO. CARDS REQUIRED |
| :---: | :---: | :---: |
| Multipliers | D13500L5 | 216 |
| High Speed Integrators | Dl3500L1 | 36 |
| Low Speed Integrators | D13500L4 | 3 |
| Temporary Storage for Multipliers | D13500L9 | 3 |
| Vs Counter, BT \& Rest Card | D13500L6 | 8 |
| Multiplier Control A | D13500L7 | 1 |
| Multiplier Control B | D13500L8 | 1 |
| Integrators \& Storage for Vs \& SxC | D13500Ll0 | 1 |
| Delay Program Word Buffers | D13500L15 | 1 |

Drawing Dl3500Bl is a detailed block diagram of the Multiplier section which also shows the data flow in and out of the System Controller and to the computers.

The Multiplier section requires only a few external signals in addition to the Delay Data inputs. These external signals are:

1. 100 MHz clock
2. BT input
3. DT input
4. Three select lines (24G11-0 to 24G11-2) to control tristate gates on the Temporary Storage output.
5. Temporary Storage shift out clock, 24G10.

The output signals are as follows:

1. 20 bit parallel word from Temporary Storage cards 3032 words
2. 8Fl-3A which indicates that Temporary Storage is filled with data.

The data from the delay lines is transmitted over ribbon cable to the various 4-layer PC Multiplier mother boards. Then the data signals are distributed to the 27 Multiplier cards plugged into each mother board by microstrip lines on the mother board.

The data inputs from the delay lines to the multipliers are a two bit, three level digital signal produced by the samplers. For details on this type of signal, reference should be made to:

Australian Journal of Physics; Correlators with Two-Bit Quantization, B.F.C. Cooper; 1970, 23, p.521-7.

The output code of the samplers is as follows:


The output code is chosen arbitrarily to simplify the logic. A multiplication table for the above would be:

| ANT. A <br> ANT. B | -1 | 0 | +1 |
| :---: | :---: | :---: | :---: |
| -1 | +1 | 0 | -1 |
| 0 | 0 | 0 | 0 |
| +1 | -1 | 0 | +1 |

To perform this multiplication and integrate the results would require reversible counters. To simplify the system, an altered multiplication table is used in which +1 is added to each multiplication result:
$\left.\begin{array}{|c|c|c|c|}\hline \text { ANT. A } \rightarrow & -1 & 0 & +1 \\ \hline \text { ANT. B }+ & -1 & 2 & 1\end{array}\right] 0$

The System Controller can correct for this change simply:

$$
v_{n}^{\prime}-v_{s}=v_{n}
$$

where $V_{n}^{\prime}=$ results of integration of multiplier $N$ after a period $T$, $V_{s}=$ number of multiplications during $T$ and $V_{n}=$ results desired; that is, the results that would have been obtained with the unmodified multiplication table.

A block diagram showing how the modified multiplication is done as shown in Figure 5. Figure 6 shows one integration channel.

The required number of cross multipliers is 2808 and the required number of self multipliers is 108. From the required number of cross and self multipliers the most efficient number per board is 13 cross multipliers and 1 self multiplier which works out to be 216 cards. This leaves 108 extra self multipliers; but since the loss of a self multiplier is greater than that of a cross multiplier and because of simpler overall layout, these 108 multipliers are used as redundant self multipliers.

The following table shows how the signals are distributed to achieve all the necessary multiplications.

Abbreviations: $\quad$| R | $=$ right circular polarization |
| ---: | :--- |
| L | $=$ left circular polarization |
| S | $=$ sine |
| C | $=$ cosine |

Example:
RS2 represents the right circular polarization, sine component of antenna \#2.

For each 50 MHz BW there will be eight arrays with 27 printed circuit cards per array, arranged as follows:

| MOTHER BOARD LOCATION |  | SELF-MULTI PLIED ANTENNA OUTPUT | CROSS MULTIPLIED  <br> A X | ANTENNA OUTPUT B |
| :---: | :---: | :---: | :---: | :---: |
| D3 | ARRAY \#1 | RS | RS | RS |
| C3 | " \#2 | LS | LS | LS |
| D4 | " \#3 | RC | RC | LC |
| C5 | " \#4 | LC | LC | RC |
| D6 | " \#5 | RS | RS | RC |
| C6 | " \#6 | LS | LS | LC |
| D5 | " \#7 | RC | RC | LS |
| C4 | " \#8 | LC | LC | RS |
| MULTIPLIER CARD LOCATION ON MOTHER BOARD | ```MULT. CARD SERIAL NO.``` | $\downarrow$ | TERMINATED <br> ON EACH <br> MULT. CARD | TERMINATED <br> ON MOTHER BOARD |
| PS | 1 | 2 x | $\begin{array}{ll}1 & \mathbf{x} \\ \mathbf{2} & \mathbf{x}\end{array}$ | $\begin{aligned} & 2-8 \\ & 3-8 \end{aligned}$ |
| PA | 2 | 1 x | $\begin{array}{ll}2 & \\ 1 & \\ \end{array}$ | $\begin{aligned} & 9-15 \\ & 9-14 \end{aligned}$ |
| PT | 3 | 4 x | $\begin{array}{ll}3 & x \\ 4 & x\end{array}$ | $\begin{aligned} & 4-10 \\ & 5-10 \end{aligned}$ |
| PB | 4 | 3 x | $\begin{array}{ll}4 & \mathbf{x} \\ 3 & \mathbf{x}\end{array}$ | $\begin{aligned} & 11-17 \\ & 11-16 \end{aligned}$ |


| $\downarrow$ | $\downarrow$ | $\downarrow$ |  | $\downarrow$ |  | $\downarrow$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PU | 5 |  |  | 5 | x | 6-12 |
|  |  | 6 | x | 6 | X | 7-12 |
| PC | 6 |  |  | 6 | x | 13-19 |
|  |  | 5 | x | 5 | X | 13-18 |
| PV | 7 |  |  | 7 | $x$ | 8-14 |
|  |  | 8 | X | 8 | x | 9-14 |
| PD | 8 |  |  | 8 | x | 15-21 |
|  |  | 7 | x | 7 | x | 15-20 |
| PW | 9 |  |  | 9 | x | 10-16 |
|  |  | 10 | X | 10 | X | 11-16 |
| PE | 10 |  |  | 10 | x | 17-23 |
|  |  | 9 | x | 9 | x | 17-22 |
| PX | 11 |  |  | 11 | x | 12-18 |
|  |  | 12 | x | 12 | x | 13-18 |
| PF | 12 |  |  | 12 | x | 19-25 |
|  |  | 11 | x | 11. | X | 19-24 |
| PY | 13 |  |  | 13 | x | 14-20 |
|  |  | 14 | x | 14 | x | 15-20 |
| PG | 14 |  |  | 14 | x | 21-27 |
|  |  | 13 | $\mathbf{x}$ | 13 | x | 21-26 |
| PZ | 15 |  |  | 15 | x | 16-22 |
|  |  | 16 | $\mathbf{x}$ | 16 | $\mathbf{x}$ | 17-22 |
| PH | 16 |  |  | 16 | x | 23-27,1-2 |
|  |  | 15 | X | 15 | X | 23-27.1 |
| PAA | 17 |  |  | 17 | x | 18-24 |
|  |  | 18 | x | 18 | x | 19-24 |
| PJ | 18 |  |  | 18 | x | 25-27,1-4 |
|  |  | 17 | x | 17 | x | 25-27,1-3 |
| PBB | 19 |  |  | 19 | $x$ | 20-26 |
|  |  | 20 | x | 20 | X | 21-26 |
| PK | 20 |  |  | 20 | $x$ | 27,1-6 |
|  |  | 19 | X | 19 | X | 27,1-5 |
| PCC | 21 |  |  | 21 | x | 22-27,1 |
|  |  | 22 | $\mathbf{x}$ | 22 | x | 23-27,1 |


| $\downarrow$ | $\downarrow$ |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |

Multiplier Card sequence number 27 does not fit as smoothly in the array - although it is physically identical to the other cards. Therefore, multiplier card sequence number 27 for each array is listed separately below:


The large mother board is a four layer printed circuit card. One of the inner layers is a ground plane. The other inner layer is divided into +5 V and -5.2 V power planes. The two outer layers are used to distribute the signals and also the -2 V and the -12 V required by the multiplier cards.

All the ECL signal lines from the delay lines, and the 100 MHz clock lines are 50 ohm microstrip transmission lines. All the signal lines from the bridging cables are terminated with 51 ohm resistors on the mother board. The clock and the signals from the terminated connectors are terminated on the Multiplier Card.

The four voltages are decoupled on the mother board with $.019 \mu \mathrm{~F}$ and $10 \mu \mathrm{~F}$ capacitors.

The description of the $-2 V$ regulator and the description of the clock paddle board is found in the report on the Delay Section.

The following is a list of testers for the cards in the Multiplier Section:

1. Multiplier Card Test Fixture.

This test fixture will test the Multiplier Cards below and above 100 MHz with both static and dynamic data.
2. HS1-LSI Card Test Fixture.

This one test fixture will test either the HSl or the LSl Card.
3. Multiplier Section Test Chassis.

This test chassis will test all the cards in the Multiplier section except the Multiplier Card.

In this test the cards all operate together similar to their actual operation in the system.

The following consists of a description of the nine different logic cards found in the Multiplier Section.

1. Multiplier Card Dl3500L5

The multiplier is a five layer PC board on which the two outer layers carry the signals and the inner three layers make up the power planes $-+5 \mathrm{~V},-5.2 \mathrm{~V},-2 \mathrm{~V},-12 \mathrm{~V}$, and GND. The 100 MHz sine wave clock input is AC coupled to the input of four differential amplifiers which then drive an emitter follower amplifier. Each of these clock amplifiers shape the sine wave, set the swing, and has enough output
to drive 8 flip-flops. The output of $Q 2$ is loaded with only 6 ECL flip-flops instead of 8 like the other three are.

From the modified multiplication table on page 3 one can see that a multiplier must be able to count 1,2 or not count at all. This is accomplished by the gating in front of the first and second stages of each multiplier. The 10118 gate allows the first stage to only count the ones in the multiplication table. The 10119 gate allows the secondstage to count the twos in the multiplication table and also allow the carry from the first stage to count into the second stage. The first two stages, which are ECL, of each multiplier operate as a synchronous counter, counting as per the modified multiplication table.

The maximum output frequency of the second ECL multiplier stage is 50 MHz which would be the case if the multiplier were to count two every time. The output of the second multiplier stage is passed through a 10125 gate which translates the ECL logic levels to TTL logic levels. The output of the 10125 is then counted by the 82591 high speed four bit binary counter which can easily count the maximum 50 MHz signal. The MSB of the 82591 is then fed into a 74283 four bit binary counter.

The MSB of each of the 14 multipliers is fed off the card through a 74150 multiplexer to a High speed Integrator (HSI) card where each multiplier is integrated further. The NMSB of each multiplier is fed through the other 74150 multiplexer to a HSI card where it is latched and tri-stated to be picked up by temporary storage. The multiplexer select lines cycle around in step with the HSI address and will be further explained in the HSI section.

During blanking time (BT) it is mandatory that the multipliers do not continue counting. Normally this would be accomplished by stopping the 100 MHz clock; however, the discrete clock driver cannot be easily gated off and the 10135 flip-flops do not have an inhibit input. So instead of stopping the clock the first tow stages of each multiplier is held to reset during $B T$ and $D T$. The possible error that is caused by resetting these two stages averages out, therefore, the integration results are not affected by resetting the first two stages every BT.

At dump (DT) and after the multiplier results have been read into Temporary Storage the TTL counters are reset to zero. The ECL multiplier stages are held reset during the whole DT as they are during BT. The data buffer flip-flops (the 10231 's) are not reset so that they will contain preset data when DT and/or BT is over.

One discouraging discovery that was made on the prototype of the multiplier card was that the rising edge of the reset to the 82591 counters must be fairly fast. Although nothing is stated in the specification sheet, if the rising edge of the reset pulse is to sloppy then a strobe pulse is internally generated in the 82591 causing the counter to be preset, to all ones in this case since the parallel inputs were left floating. This is what was happening when the reset driver for the 82591 was a 7404. There were three solutions to this problem. One was to ground the parallel inputs, two was to increase the number of reset drivers in order to improve the wave shape and the third alternative was to use a high speed gate with faster rise and fall times. Since the first two solutions would have required reworking the PC layout, a 74504 gate was used in position llG.
2. High Speed Integrators (HSI) Dl3500Ll

The multiplexed MSB and the multiplexed LSB outputs of the Multiplier cards are fed to one of six integrators on a High Speed Integrator wire wrap card. Each of the 36 HSI cards contain six separate integrators, each of which integrates the output of the 14 multipliers from one Multiplier card. This is a total of 84 individual integrators each being seven bits long on one card.

For the High Speed Integrators and also the Low Speed Integrators a technique of using rams, latches and addresses was implemented in such a way as to operate like a ripple counter, but with a package count of only a fraction of what would have been required for straight ripple counters. Drawing Dl3500Bl illustrates how the required number of cards have been reduced by using this technique, i.e. there are 216 Mult. cards, 36 HSI cards, and only 3 LSI cards.

Before getting into the actual operation of the HSI look at a couple of requirements. One requirement is knowing what the output of the Multiplier card is doing. The maximum frequency of a multiplier output (MSB) is $195.3125 \mathrm{kHz}-5.12 \mu \mathrm{~s}$ period - which means that each multiplier output cannot change states more often than $2.56 \mu s$. Now since each multiplier is in a particular state for at least $2.56 \mu s$,
a HSI can then cycle around and look at each of the 14 multipliers on a Multiplier card as long as the integrator cycles back around to the first multiplier before $2.56 \mu s$ is up.

Another requirement for the HSI is that their inputs be synchronized with the ram cycle. This synchronization is accomplished by clocking the output of the multiplier into the 74H74's located on the HSI cards. In addition to providing synchronization, the flip-flops also provide the true and compliment data that is also required by the HSI.

Keeping the above requirements in mind look at the actual operation of one of the HSI. The two 74283 adders in each of the integrator units does the integration for 14 multipliers. The two 3101A open collector rams, store the results of the 14 integrations and the 3404 latches hold the results of the old integration data while the new integration is taking place.

The same address that addresses one of the 14 locations in the 3101A rams also addresses the multiplexers on the Multiplier cards. The multiplier being integrated and the multiplier being addressed by the multiplexer is one removed from one another because of the 74H74 flip-flop. This difference does not matter in operation, but it must be kept in mind when tracing a particular multiplier.

A $180 \mathrm{~ns}(\mathrm{C} 5.55)$ clock is used to clock all the logic on the HSI card. The C 5.55 clock used for the read/write signal is such that for 120 ns it is in the read state and for 60 ns it is in the write state. For each of the 14 addresses (there are two addresses not used) the ram does a read/write cycle in 180 ns ; thus requiring a total of $2.52 \mu \mathrm{f}$ for 14 addresses. This $2.52 \mu \mathrm{~s}$ cycle time more than meets the $2.56 \mu s$ requirement stated earlier.

The LSB in the ram is redundant to the MSB on the multiplier card or what is in the 74 H 74 flip-flop; however, the LSB stored in the ram is necessary as will be seen as the operation of the integrator is explained. A particular address is read out of the ram which complements and is then strobed into the latch which also complements. The number now in the latch is what this particular multiplier integration result was when last addressed $2.52 \mu \mathrm{~s}$ ago. The output of the latch is applied to the adder which is going to do the integration. The only other input that the adder requires is the complement of what this
particular multiplier output is at present. What we now have presented to the LSB of the adder is the complement of the present state of a multiplier and the previous state of the multiplier. From this the adder will then generate an internal carry only if the output of the multiplier was a logic 1 but is now a logic 0. This carry, if generated, will then add a one to the number being held by the latch. Next the result of this addition is written back into the same ram location. So functionally the adder is acting as one ripple counter for 14 multipliers and the ram is storing the results.

The LSB output of the adder is not used - only the internal carry. What is written back into the LSB of the ram is what the multiplier is at present.

The HSI continuously cycles around as described, during which time the Low Speed Integrator looks at the MSB of the HSI in the same manner as the HSI looks at the output of the multipliers. The Low speed Integrator further integrates the multiplier results. When BT comes this same HSI cycle continues, but the multiplier results are prevented from changing because the first two ECL stages of the multipliers are held at reset which prevents the output of the multipliers from changing. As long as the input to the HSI is not changing, the multiplier results will not change as the HSI goes thru its cycle.

Then at DT the cycle is the same except that the contents of the rams are picked up by the Temporary Storage logic. The Temporary Storage picks up the data thru the tri-state gating on the HSI card. The selection of the tri-state gating is controlled by the output of the 7442A decoder also located in the HSI card. The first three decoder input signals - 8G7-0, 8G7-1 and 8G7-2 - select one of the six integrators on a HSI; while the last decoder input - 8G8-X selects one of the six HSI cards that are tri-stated together.

After the transfer to Temporary Storage is complete but still during DT, the HSI cards are easily reset by taking the chip select on the rams high while the cycle continues. A reset signal need not
be applied to the $74 H 74$ flip-flops because all the multipliers have been reset by this time which means that " 0 's" will be clocked into the flipflops.

The timing diagram drawing Dl3500B2 shows the clock, address, reset, and tri-state control waveforms, and the explanation of their generation is covered under Multiplier Control A and B.
3. Low Speed Integrators (LSI) D13500L4

The basic operation of the Low Speed Integrators is the same as that of the HSI; therefore, the explanation of how the ram, latch, adder combination is used as a counter will not be repeated here. One very slight difference is that an AND gate (1A3 and 1A6) was used to determine the carry; where as on the HSI this was done in the LSB of the adder.

There are two integrators - 10 bits each - on one wire wrap card. Again block diagram drawing Dl3500Bl should be referred to. Each one of the two integrators integrates 504 multipliers which is a total of 1008 on one card. Two 256 bit rams are tri-stated together in order to get 512 ram locations of which only 504 are addressed. The tristate selection of the rams is controlled by the signal $\overline{7 G 5-8}$. The gates, 6Cll and 6D8, are so connected to insure that the tri-state selection input (CS) on the rams are not both selected at the same time which can cause chip failure.

A 540 ns (Cl.85) clock is used to clock all the logic on the LSI card. The $C l .85$ clock used for the read/write signal to the rams is such that for 480 ns it is in the read state and for 60 ns it is in the write state. For each of the 504 addresses (there are eight addresses not used) the ram does a read/write cycle in 540 ns ; thus requiring a total of $272.16 \mu s$ for 504 addresses. The carry output (MSB) of the HSI is in particular state for a minimum of $322.56 \mu \mathrm{~s}$ which is longer than the time required for the LSI to make-one complete address cycle.

The MSB of the LSI is used for the overflow bit. An OR gate is used to look at the carry of the NMSB and what the overflow bit was the last time. If either is a one, then a one is written into the ram, and at DT this one is sent to the computer indicating that an overflow condition occurred for this particular multiplier.

Like the HSI the LSI continuously cycles around. When BT comes the same cycle continues, the results in the LSI are kept from changing because the HSI results are not changing.

Then at DT the LSI will complete the address cycle it is in and then the contents of the LSI are read directly into Temporary Storage and in the same cycle the rams are reset thru the 7408 gates on the input to the rams.

The timing diagram drawing Dl3500B2 shows the clock, address, reset, and tri-state control waveforms, and the explanation of their generation is covered under Multiplier Control A and B.
4. Temporary Storage for Multipliers (TS) D13500L9

One Temporary Storage for Multipliers wire wrap card contains two separate storage units each of which is capable of storing 512 20-bit words. Dual 256-bit MOS shift registers are used for the storage. Although there are 512 words of storage only 504 words of storage are used. All of the inputs and outputs on the 2527 MOS static shift register are TTL compatible. The one specific requirement of the 2527 shift is that the clock must be stopped in the "l" state in order to retain data.

At Dr every 540 ns a word is clocked into storage by a 1.85 MHz square wave clock. Eleven bits of each word come directly from the LSI, seven bits from the HSI thru tri-state gates, and one bit from the Multipliers via HSI thru tri-state gates. The twentieth bit is generated by the parity generator on the $T S$ card. All six TS units are loaded simultaneously ( 504 words $\times 540 \mathrm{~ns}=272.16 \mu \mathrm{~s}$ ) giving ample time to reset the Multipliers and integrators before the end of DT.

The 8275 latches are used to hold the 8 bits from the HSI because the data from the HSI is changing every 180 ns versus 540 ns from the LSI. The LSI requires $7.56 \mu \mathrm{~s}(540 \mathrm{~ns} \times 14$ words $=7.56 \mu \mathrm{~s}$ ) to address the 14 multiplier results (MS bits) in which the LS bits are contained in the 14 addresses of one of the HSI. During this $7.56 \mu s$ the HSI will cycle thru each of the 14 addresses three times ( $7.56 \mu \mathrm{~s} \div 14$ words $\div$ $180 \mathrm{~ns}=3$ ). In this $7.56 \mu \mathrm{~s}$ period of time, TS picks off every third HSI address that corresponds to each of the LSI addresses, and since the HSI goes thru each of its 14 addresses three times all of them are picked up by TS. The following is an example of how the TS picks up all the HSI words:


The two storage units on each TS card are multiplexed together and then tri-stated with the outputs of the other two Temporary Storage for multiplier cards and also the storage card for the Vs and SxC multipliers. The System Controller controls - thru the Multiplier Control B card the multiplexer, the tri-state selection and the clock for transferring the 20 bit words in parallel to the System Controller at a rate of $1.6 \mu \mathrm{~s}$ per word. The transfer of the multiplier results to the System Controller starts during BT but will continue into observation time.

## 5. Vs Counter BT and Reset Card Cl3500L6

This card is a two sided PC board of the same dimensions as the multiplier boards. There is one of these cards located on each Multiplier Mother Board - the locations of these boards are shown in drawing Dl3500P18. As shown in the drawing this card is either located in card slot location PP or PR depending upon which of the two slots was required by multiplier card sequence no. 27. All the necessary input/output signal paths for the Vs counter BT and Reset Card are brought to both PP and PR connectors on the mother board.

The Vs counter counts the total number of samples taken in one integration period. The 100 MHz clock sampling rate is divided down to 390.625 kHz on this card which is then further divided down by the Integrators and Storage for $V s$ and $S x C$ card. The eight LSB of the Vs counter which are thrown away are not reset each BT because a slight error would be introduced.

The 100 MHz discrete clock circuit is the same as that found on the multiplier cards except for the addition of the clock monitor output The clock monitor output is a DC voltage which is sampled by the system monitor logic located in the System Controller. If the 100 MHz clock is found to be in error the System Controller will give an alarm.

Also on this card, BT is synchronized and buffered to drive the 27 multiplier cards on the mother board and also drive the Output

Mux Card in the Delay Section. The only other logic on this card is the TTL reset buffers which drive the TTL reset logic on the multiplier cards.
6. Integrators and Storage for Vs and SxC Dl3500LIO

This wire wrap card consists of an input multiplexer for Vs, a parity generator, eight twenty-bit integrators, and tri-state gating to tri-state output with the three Temporary Storage cards.

The first four counters - Fl thru F4 - serve as integrators for the eight Vs counters. The eight Vs counter outputs are fed to the 2-1 multiplexer the selection of which is controlled by the System Controller. The multiplexer is switched at the start of each observation or if the System Controller detects a bad Vs during an observation the System Controller will switch the multiplexer during DT.

F5 thru F8 counters integrate the results of the SxC multipliers which are located on the Self Test Output Mux. Card (D13500L1l) in the Delay Section. The result of this multiplication is used to adjust the sine-cosine phase angle in the Samplers.

At DT the contents of F1 thru F8 is transferred into the 9328 storage registers. This is accomplished by clocking on alternate 1-0 pattern into register $F 9$ whose outputs are connected to the strobe input of the counters. The 1-0 pattern alternately strobes the contents of one counter into another, so that after 16 clock pulses to $F 9$ the contents of what was in F8 will be in F1 so that it can then be clocked into 9328 storage register. See the timing diagram drawing D13500B2.

There are two separate clocks gated together to feed the clock input of the 9328 storage register. The shift in clock, 8G4, clocks the contents of Fl into the storage register. The shift out clock, 8 GlO , is generated and controlled by the System Controller thru Multiplier Control B card.

The overflow bit is generated by ORing two additional counter states together. It is assumed that these counters will not overflow to such an extent that two additional counter stages will not detect the overflow. The parity bit is generated as the data is clocked from $F 1$ into storage.

The output of the storage is tri-stated with the three Temporary Storage cards. Like the $T S$ tri-stating the tri-state gates on the card are controlled by the System Controller.
7. Delay Program Word Buffers Dl3500L15

This wire wrap board is used to buffer the clock and the delay program words sent from the System Controller to all the Delay Control cards and to all the Samplers. As can be seen from the logic drawing, the buffering of the data is very straight forward and does not need any exploration.

Instead of gating the delay words, the clock is gated to the Delay control cards and Samplers. A brief explanation of how the clock is gated follows. The counter on the board sets up the decoders except for the MSB which is controlled by the clock from the System Controller. When the clock to the decoder at position 3D is in the logic "l" state, one of its unused outputs is selected which in turn will select one of the unused outputs on all of the other decoders; thus making all the individual clock outputs - G5 thru G36 - a logic " 0 ". Then when the clock to the decoder at position 3D goes to a logic " 0 " the decoder output that is set up by the two MSB of the counter is selected, and then in turn one of the other decoder outputs is selected causing the selected clock output to go to a logical "l".
8. Multiplier Control A Dl3500L7

This wire wrap card along with Multiplier Control B contains all the necessary logic to control all the other cards in the Multiplier Section except the Delay Program Word Buffers card. Since there are 216 Multiplier, 36 HSI, 3 LSI, and 3 TS cards all operating in synchronism with one another, great care was taken so that the addresses and clocks to all these boards have the same delay. In order to achieve the same delay for all the various signals, extra gates were added in various signal paths.

The 100 MHz system clock is brought on and it is buffered and shaped by the same discrete clock drive that is found on the multiplier cards. The 100 MHz clock is divided down to a $5.55 \cdot \mathrm{MHz}$ and a $1.85 \cdot \mathrm{MHz}$ clock which are the two clock frequencies used to clock all the logic except the 100 MHz logic. The division of the 100 MHz clock is done such that the 5.55 and 1.850 MHz clocks are in exact synchronism with one another. The various clock waveforms are shown on the logic drawing and also on the timing diagram drawing Dl3500B2.

A TTL BT signal, $8 G 1$, is brought onto this card from Multiplier Control B. This BT signal is then translated to ECL logic levels, synchronized with the 100 MHz clock and then buffered to drive the eight Vs, Counter BT and Reset Cards.

The HSI Ram Address Register, the two tri-state selection address registers, and the associated control logic are all synchronized with the LSI Ram Address Register. This synchronization is done by G6A and G6B which detects when the LSI address is at address 0 .

The LSI Ram Address Register, F3, synchronously counts from 0 to 504. The F3 register is advanced every 540 ns . The output of F3 is delayed thru four gates before feeding off of this card to the three ISI cards.

The HSI Ram Address Register, F2, synchronously counts from 0 to 13 and the output is delayed thru gates and then buffered sufficiently to drive the 36 HSI cards. F2 is advanced every 180 ns which means that $F 2$ goes thru three addresses for each address of F3. F2 counts from 0 to 13108 times while $F 3$ counts from 0 to 503.

The HSI Select Address Register, F5, is advanced every $7.56 \mu s$ and synchronously counts from 0 to 5. The output of $F 5$ is sufficiently buffered on Multiplier Control B to drive the three LSB decoder inputs on the 36 HSI cards. This register selects the output of one of the six integrators on the HSI cards.

The HSI Card Select Address Register, F6, is advanced every $45.36 \mu s$ and synchronously counts from 0 to 5. The output of F6 feeds a decoder on Multiplier Control B. Each of these six decoder outputs feed the MSB decoder input on six of the HSI cards. This bit selects which of the six HSI cards that are tri-stated together.
9. Multiplier Control B Dl3500L8

This wire wrap card contains some buffering for various outputs from Multiplier Control A and the control logic for the $T S$ cards and also the reset control for the Multipliers, HSI and LSI cards.

The BT input signal comes from the SC along with 18Gl which indicates which BT is a DT. The timing diagram below shows the relationship of these signals.


For a 50 ms DT 18 Gl will stay in logic "l" state.
F1-0 to Fl-2 synchronizes DT with the $1.85 \cdot \mathrm{MHz}$ clock, and Fl-3 synchronizes the LSI cycle with DT. Fl-3 $\rightarrow 1$ when the LSI address register completes the cycle it was in when DT came. Fl-3 $\rightarrow 1$ at LSI address 0. The 272.16 us that Fl-3 is in the logical "l" state there are three things that happen. First the contents of the HSI and LSI are transferred to TS and the LSI are reset. Second but simultaneously with the first, the Vs and SxC Integrators are transferred into the TS. The third thing is Fl-3 is sent differentially to the SC.

In the first case Fl-3 enables F4 to generate a symmetrical 540 ns rep rate clock from the non-symmetrical free running, $540 \mathrm{~ns} \overline{7 \mathrm{Fl}-4}$ signal. The F4 clock then feeds thru the six 74 HOP gates to generate G6-0 to G6-5 which clocks the six TS units simultaneously. The other inputs to the six $74 \mathrm{HO8}$ gates are at a one during this time.

Fl-3 also allows the Vs and SxC Integrator and Storage Control to run thru its cycle at this time. F2 generates the 1-0 pattern input to 10F9, $\overline{G 3 C 1.85}$ is the clock for $10 \mathrm{F9}$ register, and G4 clocks the storage registers on $L 10$. The $F 3$ register, counts the number of G4 pulses and will stop G4 and F2 in the "0" state after 8.64 us; however, $\overline{\text { G3Cl. } 85}$ continues running to fill lof9 register with all " 1 's" so that the strobe inputs on the counters are set to allow the counters to count again.
$272.16 \mu s$ after $\mathrm{Fl}-3 \rightarrow 1$ Fl-4 $\rightarrow 1$ for $9.18 \mu \mathrm{~s}$ to reset all of the HSI and also reset the Vs and SxC Integrators. Reset to the ISI, although reset at this time, so also held at reset is that any carries from the HSI are not picked up by the LSI.

The four differential signals from the System Controller controls the inputs to the two decoders at 5 C and 5D, which in turn controls the shifting out and the tri-state gating on the TS cards. The truth table located on the drawing illustrates the various functions of the controls from the System Controller.

## IV. SYSTEM CONTROLLER (SC)

The SC rack consists of twenty wire wrap boards of logic packaged in an 8-3/4" Standard Chassis, a Beehive CRT terminal, a +5 V supply, a multiple supply and a power control chassis. This report will describe the operation of the SC chassis. The physical layout of the rack and chassis are shown in Figures 7 to 11 and drawing Cl3500P19.

In general, the $S C$ receives words from the Boss Computer; sends delay words to the Delay Lines and Samplers; receives and arranges all multiplier results; does the Vs subtraction; and sends the data that Boss computer requested to Core computer. The SC can also display and enter data thru the CRT terminal, and the SC can perform certain tests, that are programed into the $S C$ either from instructions from the CRT or from the Monty computer.

The block diagram drawing Dl3500B3 illustrates the complete logic flow of the SC. As can be seen from the block diagram, there are seven different roms. They are as follows:

|  | ROM | DRAWING NO. | FUNCTION |
| :---: | :---: | :---: | :---: |
| 1. | Rom 1 | Al3500Fl | Bits 0-1l contain the proper ram address for the multipler results <br> Bits 12 \& 13 used to indicate negation and provide code for ram bits $20 \& 21$ <br> Bits 14 \& 15 provide vs code for subtraction and code for ram bits $22 \& 23$ |
| 2. | Rom 2 | Al3500F2 | General control of the SC logic - the heart of the SC |
| 3. | Rom 3 | Al3500F3 | Controls the entry of words and tests that can be intiated from the CRT and also from Monty computer |
| 4. | Rom 4 | Al3500F4 | Controls the display of all ram words on the CRT terminal |
| 5. | Rom 5 | Al3500F5 | Contains the upper, lower, and theoretical values of Vs |
| 6. | Rom 5 | Al3500F6 | Controls the entry of zeroes in spare words and unused bit positions in the ram |
| 7. | Rom 7 | Al3500F7 | Contains the limits for the System Monitor logic |

For each of these roms there is a rom program which lists each word in the rom and a description of what each word does. Copies of these rom programs are not included in this report because of their size. Tables 2, 3, \& 4 do, however, list the functions of each bit for roms 2, 3, \& 4.

Specification No. Al3500N3, Rev. B starting on page 4-27 should be referred to at this time because it give the decription and format of the words between the computers and the SC, along with the rules to be followed. Also in this specification are the CRT entry and display formats. VLA Technical Report No. 16 may be referred to for more general operational information on the System Controller.

When Boss computer starts an observation the following events occur:

1. Rom 3 - CRT Entry Rom - is reset and further entry from the CRT is prevented.
2. The following error lights and associated logic are reset:
a. L\&R GO/NO GO
b. Vs Counter
c. Overflow
d. Parity $T S \rightarrow$ SC
e. Parity $S C \rightarrow$ VLAC
3. The "Boss:" display is lit indicating observation is in progress
4. The Requested Multiplier Addresses that are sent by Boss computer are stored
5. A DT is forced
6. The DT generator is set-up

During each DT during an observation the following events occur:

1. New delay words are sent out to the delay lines
2. The GO/NO GO results are checked
3. Rom 2 starts its cycle which controls the following that extend into integration time:
a. Write all words into the Ram
b. Check the limits of the Vs results
c. Vs - Mult. subtraction
4. (cont.)
d. Read all other words in Ram for display.
e. Send all requested words to the Core Computer.

Any word in the ram can be displayed on the CRT terminal. The instructions for displaying words are listed in Table 5 in Specification Al3500N3.

While an observation is in progress it is not possible to enter any words from the CRT terminal. The instructions for entering words from the CRT along with the words and the different tests that can be entered are listed in Table 6 in Specification Al3500N3.

Figure 8 shows the front panel of the SC and the Power Control chassis. A description of the few front panel switches and indicators are as follows:
A. Power Control Chassis

1. System On - applies power to all racks and equipment in the digital Delay System except the CRT terminal.
2. CRT On - turns power on/off to the CRT terminal.
3. CRT I/O Selection - selects whether the terminal is connected to the SC or to Monty computer. The display adjacent to the switch indicates the selection of the switch unless both "SC" and "Monty" are lit, which indicates that Monty computer is talking to the SC thru the CRT input. When this condition exists the switch has no influence. The CRT will monitor the data flow between the Monty computer and the SC.
B. System Controller Chassis
4. SC status indicator - If "Boss" is lit then the Boss computer is in control. If "Test" is lit then the SC is carrying out a test that the CRT or Monty computer instructed the SC to do. If neither part of the display is lit then the $S C$ is just sitting iale.
5. Sonalert buzzer - sounds if any error, as indicated by the column of lights, occurs.
6. Visual Alarm indicator - indicates one of the following abnormal operating conditions:
a. One or more error(s) as indicated by the column of lights.
b. The System Monitor Override switch (in the Delay Rack) is on; thus possible overriding a "power down" alarm condition detected by the System Monitor logic.
c. Switch one on the rear of the SC chassis is in
"Local Test" position; thus disabling the clock from Boss computer.
7. Function Reset Interlock - a pushbutton switch that operates in conjunction with the Function Reset switches.
8. Function Reset Light/Switch - Except for Start Up the lights indicate an error condition; and where appropriate the data should be displayed in order to find out exactly what is in error. The pushbutton switches reset the logic as designated. Because these switches reset logic that can affect the observation they cannot be operated without also pushing the Function Reset Interlock switch. A description of the Function Reset switches are as follows:
a. Start Up - is a master reset that is applied to all the logic in the SC that could possibly get out of synchronism.
b. L GO/NO GO - resets the left go/no go logic
c. R GO/NO GO - resets the right go/no go logic
d. Vs - reset Vs error logic
e. Clock Osc. - switches from the Standby Clock Osc. back to the regular oscillator.
9. Indicator Test - when pushed the Sonalert should sound and all the LED lamps should light except the three associated with the Test Point Selector.
10. Indicator Reset Light/Switch - the lights indicate an error condition. The pushbutton switches will reset only the error indicators if the error condition no longer exists; thus resetting these indicators will not have any effect on the observation. A description of each follows:
a. System Monitor - indicates that the System Monitor logic has detected some type of an alarm condition and the System Monitor data should be displayed to find out what is in error.
b. Overflow - an overflow has occurred in one or more of the Vs counters, SxC counters, and/or multiplier results. Displaying each of the above will indicate where the overflow is occurring.
c. Parity $T S \rightarrow$ SC - indicates that a parity error has occurred when the data in the Temporary Storage units when read into the ram. If an observation is not in progress then the parity can be displayed along with the Multiplier results. To display parity switch 1 on L28 must be closed and switch 1 on the rear of the $S C$ chassis must be thrown to the local test position.
d. Parity $S C \rightarrow$ VIAC - the Core computer has detected parity errors in data it received from the SC. The Boss computer then notifies the SC of the errors by one of two bits in the control word. Displaying the control word will indicate if the computer is going to continue the observation or stop it.
e. CRT - indicates a parity, ovex-run, and/or framing error has occurred in data transmission between the CRT $\rightarrow$ SC or Monty computer $\rightarrow$ SC.
f. Clock-BT Test - indicates that a switch on the clock board is thrown to a test position. The only way to reset this light is to return all switches on Ll8 to their normal operating positions. This light cannot be on during an observation.

8．Alarm Reset－will silence the Sonalert．
9．Test Point Selector A－selects one of eight signals to the LED，scope probe jack，and to the BNC connector on the side of the chassis．The eight signals are：

TEST POINT SELECTOR A

| $\begin{gathered} \hline \text { LOGIC } \\ \text { DWG } \end{gathered}$ | SIGNAL | DESCRIPTION | SW POS |
| :---: | :---: | :---: | :---: |
| L18 | $\overline{C-A} \cdot \underline{ }$ | $\overline{\text { CLOCK }}$ ， $1.52 \mu \mathrm{~s}$ ． | 0 |
|  | $\overline{C-B} \cdot \underline{ }$ | ＂${ }^{80.3}$ | 1 |
|  | $\overline{C-C}{ }^{\prime \prime}$ | ＂几 | 2 |
|  | $\overline{C-D " '}$ | ＂几 | 3 |
|  | $\overline{C-E " '}$ | ＂同 | 4 |
|  | $\overline{C-F}{ }^{\prime \prime}$ | ＂ | 5 |
|  | $\overline{C-G ' \prime}$ | ＂ | 6 |
|  | $\overline{\mathrm{C}-\mathrm{H}}{ }^{\prime}$ | $\cdots \longrightarrow$ | 7 |

10. Test point Selector B - selects one of eight signals to the LED, scope probe jack, and to the BNC connector on the side of the chassis. The eight signals are:

TEST POINT SELECTOR B

11. Test Point Selector C - selects one of eighty signals to the LED, scope probe jack, and to the BNC connector on the side of the chassis. The eighty signals are:

TEST POINT SELECTOR C

| LOGIC <br> DWG | SIGNAL | DESCRIPTION | SW <br> POS |
| :---: | :---: | :---: | :---: |
| L20 | G4* | Left serial delay data to Ll5 | 00 |
|  | G5* | Right serial delay data to Ll5 | 01 |
|  | G6 | Left serial delay data to ram | 00 |
|  | G7 | Right serial delay data to ram | 01 |
|  | F2-0A | Left serial sampler delay data to L15 | 02 |
|  | F3-0A | Right serial sampler delay data to Ll5 | 03 |
| L21 | G1 | Boss Computer or CRT clk. to ctrl. word register 19F4 | 20 |
|  | G2 | Clk. to Boss Computer $\rightarrow$ SC Parity Storage, $23 F 7$ (a clk. only if parity is bad) | 21 |
|  | G3 ${ }^{\prime}$ | Gated Boss Computer clk. to Computer Word Buffer, 19F2 | 22 |
|  | G4 ${ }^{\text {' }}$ | Clk. from Boss Computer | 23 |
|  | $\overline{\text { G5 }}$ | Gated Boss Computer clk. to Receiving Register, 19F1 | 24 |
|  | G6 | Reset to Receiving Register, 19Fl | 25 |
|  | G7* | Clk. ram receiving register $26,27,28 F 2$ \& F3 (for Delay data) | 26 |
|  | G9* | Clk. to Delay Program Word Buffer, 115 | 26 |
|  | Gl0 | Reset to Delay Program Word Buffer, L15 | 27 |
|  | Gl1 | Advance to Delay Program Word Buffer, Ll5 | 30 |
|  | G13 | Boss Computer or CRT clk. to Delay \& Sampler Storage Register 20F1 | 31 |
|  | G14 | Recirculate ctrl. to Delay \& Sampler Storage Register 20Fl | 32 |
|  | G24 | Rom 2 advance - at beginning $\&$ end of Delay \& Sampler Program Word transfer | 33 |
|  | F1-00A | LSB of computer receiving register 19 Fl | 34 |
|  | Fl-24 | MSB of computer receiving register $19 F 1$ | 35 |
|  | Fll | ```1 = Delay & Sampler Program Words being sent out``` | 36. |
|  | F12 | Load/shift ctrl. for transferring Delay \& Sampler Program Words | 37 |

TEST POINT SELECTOR C


TEST POINT SELECTOR C

| $\begin{gathered} \text { LOGIC } \\ \text { DNG } \\ \hline \end{gathered}$ | SIGNAL | DESCRIPTION | $\begin{aligned} & \text { SW } \\ & \text { POS } \end{aligned}$ |
| :---: | :---: | :---: | :---: |
| L24 | G2-4 | SHIFT OUT CLK to System Monitor Storage Register 37F3 | 50 |
|  | $\overline{\text { G4-4 }}$ | 3-ST SEL CTRL for System Monitor, 37F3 | 51 |
|  | $\overline{\text { G4-5 }}$ | 3-ST SEL CTRL for GO/NO GO Storage, 22 Fl 3 | 52 |
|  | G4-6 | 3-ST SEL CTRL for Boss Computer $\rightarrow$ SC Parity Error Storage, 23F7 | 53 |
|  | G4-7 | 3-ST SEL CTRL for Requested Mult. Addresses, 19F3 | 54 |
|  | G4-16 | 3-ST SEL CTRL for Time Word, 19F2 | 55 |
|  | G4-17 | 3-ST SEL CTRL for Mux Address for SxC, 23 Fl | 56 |
|  | G4-18 | 3-ST SEL CTRL for Ctrl Word, 19F4 | 57 |
|  | G4-19 | 3-ST SEL CTRL for TVs, 29M1 | 60 |
|  | G4-20 | 3-ST SEL CTRL for Vs subtraction results, 29 F 5 | 61 |
|  | G6 | Ram A.R. advance for entering Delay \& Sampler Program Words into ram | 62 |
|  | $\overline{\mathrm{G7}}$ | R/W Signal to rams | 63 |
|  | G10 | Clk to Temporary Storage, L9 \& Ll0 via L8 | 64 |
|  | G14 | Clk to Rom 2 Address Register, 24Fl | 65 |
|  | G15 | Clk/load ctrl to Rom 2 Address Register, 24Fl | 66 |
|  | Gl6 | Clk/reset ctrl to Rom 2 Address Register., 24Fl | 67 |
|  | G17 | Clk to Rom 2 Output Register, 24F3 | 70 |
|  | F3-0 | Clk/load ctrl to Ram Address Register, 26F4 | 71 |
|  | F3-1 | Clk ctrl to Ram Address Register, 26F4 | 72 |
|  | F3-2 | Word select ctrl on multiplexed input to Ram Address Register, 26F4 | 73 |
|  | F3-3 | Clk/reset ctrl to Rom 1 Address Register, 25Fl | 74 |
|  | F3-4 | Clk ctrl to Rom 1 Address Register, $25 F 1$ | 75 |
|  | F3-10 | Vs-RVs comparison test | 76 |
|  | F4-12 | Rom 2 Loop Counter output | 77 |
| L25 | G12-22 | Rom 1 output to ram input | 90 |
| L26 | F4-3 | Ram Address Register output | 91 |
|  | F4-7 | Ram Address Register output | 92 |
|  | F4-11 | Ram Address Register output | 93 |


| $\begin{gathered} \text { LOGIC } \\ \text { DWG } \end{gathered}$ | SIGNAL | DESCRIPTION | $\begin{aligned} & \text { SW } \\ & \text { POS } \end{aligned}$ |
| :---: | :---: | :---: | :---: |
| L28 | F1-00 | SC $\rightarrow$ Core Computer data | 11 |
|  | F5A | Shift/load ctrl for SC $\rightarrow$ Core Computer Data Register | 12 |
|  | G5 | Clk to SC $\rightarrow$ Core Computer Data Register | 13 |
|  | G7 | Advance Ram Address Register ctrl for next word to Core Computer | 14 |
| L29 | G5 | Advance Ram Address Register ctrl for next Vs check | 15 |
|  | G6 | (8F1-3A) integrator results being transferred into Temporary Storage | 16 |
| L30 | F7-1 | Reset 30F5 \& 31 Fll at beginning of CRT transmission | 94 |
|  | F8-2 | Loads starting address of Entry Program into Rom 3 A.R. | 95 |
|  | G7 | Loads starting address of Display Program into Rom 4 A.R | 80 |
| L 31 | G8 | Display Comparator output | 96 |
| L32 | F2-10 | Rom 4 ctrl to load Display Storage File | 81 |
|  | F2-14 | Rom 4 ctrl to load and advance Loop Counter A and reset Rom 4 O.R. | 82 |
|  | F2-15 | Rom 4 ctrl to load and advance Loop Counter $B$ and reset Rom 4 O.R. | 83 |
|  | F2-16 | Rom 4 ctrl to load and advance Loop Counter $C$ and reset Rom 4 O.R. | 84 |
| L35 | F1 | Rom 4 skip ctrl | 86 |
| L37 | $\overline{F 2-2 A}$ | System Monitor Control Register | 17 |
| CRT | CLOCK | CRT clock-baud rate | 85 |
| Spare |  | Multiplexer on L32 | 87 |
| Spare |  | Multiplexer on L34 | 97 |
| *Indicates that the signal at the test point is logically the same as the signal description; however, the test point signal is taken from a different point in the circuit. |  |  |  |

12. Sync Points - two scope probe jacks for sync.

The SC was designed so that it can be operated without the computer; thus allowing testing and troubleshooting when the computer is not available. This is accomplished by using the CRT terminal to enter the control word and delay values that the computer normally enters. The procedure for entering and displaying data thru the CRT terminal is outlined in Specification No. Al3500N3.

Drawing Dl3500B4 should be thoroughly studied because it shows the time relationship among most of the events that take place. Rom 2 is the main control element in the SC and is shown in this drawing.

The timing diagram drawing Bl3500B5 is also very important in the understanding of the SC. This timing diagram shows the general relationship of the main control elements in the system.

A brief description of the logic on each card is given. A detailed pulse by pulse decription is not given, but instead just a general operating description of the logic that is not straight forward. $\dot{A}$ person with a good logic background should be able to easily trace any signal with the help of the description given herein along with the timing diagram.

1. Clock Dl3500L18

The Start Up Generator produces a pulse when power is first turned on. This pulse (SU) then resets the $S C$ logic so that no hang up modes occur. A SU pulse can also be generated from the front panel control which may be necessary, e.g. if the computer fails to send words in the correct format.

All clocks in the system controller are derived from a dual-in-line 50 MHz crystal oscillator. There are two of these oscillators on the clock card. One of the oscillators acts as a standby in case the other fails. F3 and F4 act as missing pulse detectors while F5 selects which oscillator is used. An oscillator failure is indicated on the front panel.

F2 divides the 50 MHz down to 5 MHz . The 5 MHz clock is further divided down by $F 1$ which gates the 5 MHz clock. The timing diagram drawing Bl3500B5 shows the relationship of all the clocks. This clocking system of generating different clock pulses from C5 was used in order
to reduce the clock gating required on each card. Also in order to achieve complete synchronism of the $S C$ logic, all clocks pass thru the same number and type of gates before reaching the device to be clocked.

F8 generates a 9.615 kHz clock for the system monitor logic and G7 which is the clock for the UAR/T. The gating along with F9 in front of F8 prevents every 64 th pulse from being counted into F8. This is necessary in order that $G 7$ will meet the specs for the UAR/T.

Test B' Generator is used to generate a BT signal in the absence of the main BT input signal. The operation of this generator is indicated on the front panel.

The operation of the DT Generator is controlled by three bits in the computer control word. The output of the generator, G9, is then ANDed with BT to produce DT.
2. Boss $\rightarrow$ SC, Requested Mult. Addresses and Control Reg. Dl3500L19 All the words from the Boss computer are received by the Fl register. The control word is shifted into both F4 and F2. All other words are shifted into $F 2$ buffer register. The delay words are shifted from F2 into 20F1. The Requested Mult. Address words are shifted from F2 into F3. The time word is left in F2.

Bits 20 to 23 are control bits which determine the register into which the computer words are to be shifted.

Since the Requested Multiplier Addresses are received only at the start of an observation the contents of F 3 is recirculated twice each DT. The first time is when the contents of F3 is read into the ram and the second time is when F3 is used to preset the ram address register when sending multiplier results to the computer. In both cases the output is from the tri-state gates on the card.

A "l" in F3-9 is used to indicate that the last word is being read out. This is necessary since any number of words from 1 to 351 may be in the register. At start-up F5 ensures that a "l" gets into the register so that Rom 2 will get advanced properly.

F6 is necessary so that a change in the DT period will change at the proper time as not to cause a Vs subtraction error or a Vs error.
3. Delay Word Storage, Delay Test Generator, Delay/Sampler Output SR Dl3500L20 Fl contains the 54 Delay and Sampler words from Boss
computer. When the delays are sent out during BT they are also internally recirculated in Fl. This is done in case a parity error is received when the next group of delay words are received. If a parity error is detected then the old delay word in Fl is used.

The two tables on the drawing show the word formats sent to the Delay Lines and the ram. These tables should be studied in order to understand the logic. Timing diagram in Drawing Dl3500B6 should also be referred to.

The 54 delay words in Fl are sent out to the Delay Lines thru F4 and F5. The Test Delay Lines get one of the 54 delay values minus 5. Which one of the 54 delay words is determined by the Delay Input/ Output Mux on L23. This is done by the subtractor and clocking the output of the subtractor into F7 or F8. The words now in F7 and F8 are then held until the 54 words are transmitted from $F 4$ and $F 5$. The other inputs to F4, F5, F6, and F7 will be explained where they originate. Clock pulse $E$ loads the left output register then 3.2 us later clock pulse $E$ loads the right output register and then they are simultaneously shifted out in serial.at a 2.5 MHz rate.

The phase delay words for the Samplers are 8 bits each which are sent out to the samplers thru F2 and F3. In order to simplify the clocking to F2 and F3 the clocks to F4 and F5 are used. The serial shift out clock consists of 24 pulses, which is compensated for by recirculating that data in F2 and F3 so that each word is sent out three times to the same receiving register.

The shift out clock to F2 thru F7 is C-B, D, F, H while the clock to their respective receiving registers is C2.5 (C-A, C, E, G) which will center the receiving clock in the middle of the data.
4. Data Control VLAC $\rightarrow$ SC and SC $\rightarrow$ Delay Dl3500L21

The ECL logic level clock and data from Boss computer are received on this board where they are immediately translated to TTL logic levels. There are 32 clock pulses with each computer word the format of computer words is shown on the logic drawing. The clock must not be free running.

The data from the computer ends up in 19Fl and 21Fl-24 register, but the leading "1" continues to be shifted to F17-F18 - and finally to F19. 19Fl-00, F17, F18, and F19 along with the data bits $2^{20}-2^{23}$ are used to control the computer clock and to steer the different words into the proper registers.

The parity checker, F2, controls the recirculate input to 20Fl and the clock, F18, to $23 F 7$ which is parity storage.

The 10 Pulse Generator simply advances the 54 delay and sampler words in 20 Fl which is a 64 bit shift register.

The Observation Indicator and CRT Lockout Control lights the indicator - BOSS - on the front panel and prevents the CRT from entering words during an observation. The CRT is held lockout for two BT after the end of observation to ensure that all data has been transferred to Core computer.

The Observation Initiation Reset, F23, is used to reset Rom 3, any tests in progress, and the front panel indicator lights. This ensures that the computer has complete control during an observation.

The timing for the Delay Word Transfer Control logic is shown in drawing Dl3500B6. 22F11-2 starts the delay word transfer which takes place every BT. F14, F15, and Fl6 are for entering the delay words into the ram which only takes place at DT. With the aid of the timing diagram the logic should be straight-forward to understand.
5. Exchange Data Generator, GO/NO GO Storage D13500L22

Each BT the outputs of the GO/NO GO Comparator on the Lll cards in the Delay Section are clocked into F1 and F2 and are held there until the next $B T$. When $23 G 10 \rightarrow 1$ the contents of Fl is ORed with what was in Fl3 and the result is clocked into F13. When $23 \mathrm{Gll} \rightarrow 1$ the contents of F2 is Ored with what was in F13 and the result is clocked into Fl3. The GO/NO GO Storage, F13, stores the results from the 54 delay line comparisons until they are reset from the front panel or from Rom 3. At DT the contents of F13 is read into the ram and it is also preserved in Fl3 register by internally recirculating the data.

At DT the Exchange Data Generators look at the GO/NO GO results in F1 and F2 and decide whether or not to sound an alarm and if the Test Delay Line should be substituted. The truth table on the logic drawing lists the various possible conditions.

If an alarm condition arises in which the Test Delay Lines are to be substituted it is done by the X-Data bits G3 and F4. The G3 and G4 X-Data bits are part of the Delay Words sent to the delay lines.
6. Boss $\rightarrow$.SC Parity Storage and Delay Mux Registers Dl3500L23

The operation of the Boss computer $\rightarrow$ SC Parity Tracker is as follows: F6 register counts each computer word received and if parity checks bad for any word, then $21 G 2$ clocks that word number into $F 7$. F7 is capable of storing up to 64 computer word numbers with bad parity during one DT period. In addition to the computer word number the BT within the DT period is indicated by 18F15-0 thru 18F15-2. The 7408 gates on the output of F7 are needed because resetting $F 7$ does not remove the word setting on the output lines of F7.

The rest of the logic on this card has to do with the Delay Line Input and Output Mux. Addresses and controling the Delay Line words. The table in the lower left hand corner of the drawing illustrates the operation and function of F9 and F10. F10 is the main steering control register for controlling the transfer of all the delay words to the Delay Lines and also to the ram.

Fll, F12, F13 are the input and output multiplexer address registers for the Test Delay Lines comparisons. These registers are normally advanced by Gl4 after the Exchange Data Generators make their decisions on the GO/NO GO data. If a test delay line is to be substituted then 22F7
or/and $\overline{22 F 8}$ prevents the Delay Input Mux. Address Register(s) from advancing until the error is corrected and reset from the front panel. The Delay Output Mux Address Register is always advanced so that SxC Multiplications are continuously performed for all antennas. F8 keeps Fll and Fl2 in step with Fl3.

For test purposes the CRT thru Rom 3 can preset F11, F12, and F13 to any desired address. Also for when the Delay Line Test is being carried out by Rom 3, these registers are then advanced by the Delay Test Generators (20F8).

The two Test Delay Line Comparators determine when 20 F 6 and 20F7 registers should be loaded with the Test Delay program word. Two separate comparators are needed because one of the Input Mux. Address Registers may be stopped while the other continues circulating.

The two X-Data Comparators determine when the GO/NO GO data in 22 Fl and 22F2 should be clocked into 22 Fl 3.
7. System Control, Rom 2 Dl3500L24

The basic operation of Rom 2, Rom 3, and Rom 4 are all the same. The basic blocks of each are as follows:

1. A rom address register - advanced at a max. rate of 1.6 us.
2. The Rom itself - on each instruction for a minimum of $1.6 \mu \mathrm{~s}$.
3. A rom output register - on each instruction for a minimum of $1.6 \mu \mathrm{~s}$.
4. Loop counter(s)

Rom 2 is the main control of the SC. At each DT Rom 2 starts a cycle that controls the following three major events:

1. Entering all words into the rom.
2. A $R-M-W$ on all multiplier results and a read for all words so they can be displayed.
3. Transmitting data to Core computer.

Drawing Dl3500B4 illustrates these events in relationship to DT and other events. The actual program words and a description of what each rom bit controls is included in Al3500F2.

The loop counter when used, determines how many 1.6 us periods the rom should stay on one instruction; or in other words, how many times a certain instruction should be repeated. The operation of the loop counter is illustrated in the timing drawing Dl3500B5.

F5 and F6 control the two possible read/write pulses that are illustrated on the drawing.

The Rom 2 Control Comparator, output G8, is used as a 12 bit comparator and a three bit comparator. In both cases it is used only during the transmit to Core computer cycle. What is compared, in both cases, is the ram address and the output of Rom 2.
8. Ram Address Memory, Rom 1 D13500L25

Rom 1 performs the following functions starting at each DT:
A. During Load Fam Cycle

1. Bits G2-0 thru G2-11 sorts the 3024 multiplier results into sequential order into the ram. Also provides the Ram starting address for the other words entered into the ram.
2. Bits G2-13 is read into the ram along with each of the 3024 multiplier results to indicate which ones are to be negated during the Vs subtraction.
3. Bits G2-12 and G2-13 are used to provide a code for ram bits 20 and 21 for words other than the multiplier results.
4. Bits G12-22 and G12-23 are read into the ram to indicate which Vs to use during the subtraction cycle.
B. During the Vs Subtraction Cycle
5. Bits G2-0 thru G2-11 sets the ram to various starting addresses.
6. Bits G12-22 and G12-23 provide the proper computer word code for ram bits 22 and 23 for the multiplier results.
C. During SC $\rightarrow$ Computer Transmit Cycle
7. Bits G2-O thru G2-11 sets the ram to various addresses.

Rom 1 address register is completely controlled by Rom 2.
9. Ram Bits $2^{0}$ to $2^{7}$, Address Register D13500L26

This ram card is one of three which makes up the storage in the SC. The total storage capability is 4096 words - 24 bits each - of which 3647 word locations are used.

The ram address register (F4) can be stepped sequentially or preset either from Rom 1 or from the Requested Multiplier Address Storage Register (19F3). For the cases in which Rom 1 presets the ram address refer to page 4-18, Rom 1 description. The Requested Multiplier Address Storage Register contains the addresses and the order of the cross multipliers that are to be sent to Core computer each DT.

In general, the ram address register is preset and then it is stepped sequentially thru so many addresses as determined directly or indirectly by Rom 2.

All the inputs to the ram are tri-stated together. The tri-state gates are located on various boards in the SC so that the fewest input/ output pins are used on the cards. Although the output of Temporary Storage in the Multiplier Section is tri-state; it is not fed directly into the ram, but instead is fed thru another set of tri-state gates located in the ram cards.

Register F3 and F4 serially receive the LS Bits of the delay program words as they are sent out to the Delay Lines. The output of these registers are then entered into the ram thru tri-state gates. 10. Ram Bits $2^{8}$ to $2^{15}$ Dl3500L27

This ram board is pretty much like $L 26$ except for small amount of gating which is part of the tri-state gating control for entering Delay Words into the ram. The table on the drawing lists these tri-state control signals and lists the bits and/or word(s) that each selects to be entered into the ram.
11. Ram Bits $2^{16}$ to $2^{23}$. VLAC Output D13500L28

The ram part of this board is like that of 1.26 and L27. The Temporary Storage $\rightarrow$ SC Parity Checker and the transmit control are found on this card.

Parts of the parity checker is actually found on all three boards, but this board has the output result (G8) on it. G8 is fed to $L 34$ where it is checked at the proper time. If found to be in error an audible and visual alarm will be sounded on the front panel. For troubleshooting G8 can also be written into the ram along with the multiplier result that it is associated with, which will allow G8 to be displayed. In order for $G 8$ to be written into the ram, the dual-inline switch 1 on $L 28$ must be closed in addition with switch 4SWl located on the rear of the chassis - which must be thrown to the "Local Test" position.

The transmit control logic controls the parallel loading of ram words into Fl register (on $L 26, L 27$, and $L 28$ ) and then the serial transmission of the words to the computer. F5 controls the shift/load control of Fl along with gating the clock. F4 counts the number of serial bits transmitted.

The computer via the ready line can stop or hold up the transmission at any time; however, a complete word is always sent.

The word format is shown on the logic drawing.
12. Vs Subtractor, Rom 5 and Rom 6 D13500L29

The subtractor is used to check the limits of the four
Vs values and to do the Vs-Vn subtraction on all the multiplier results. The Vs check will be explained first.

The Vs Check Control logic is enabled by 24F3-10 which is an output of Rom 2 register. This control logic does the controlling of the four Vs checks and also the selection of the multiplexer on the Vs Integrator card, Ll0. The table on the drawing illustrates the various events that take place during the Vs check. What follows is a general description of what takes place during the Vs check. First a Vs is read from the ram and applied to one side of the subtractor and also to the 74158 multiplexer. The other input to the subtractor comes thru the 74158 multiplexer and the 74170 register from Rom 5 which contains the upper limits, lower limits, and the theoretical values for each of the six DT periods. The carry output of the subtractor as per table
determines if the $V s$ is within the proper limits. If the Vs value is within limits, then the 74158 multiplexer is switched and the Vs value is stored in the 74170 register; however, if the Vs value is out of limits then the theoretical value from Rom 5 is stored in the 74170 register.

F2 accumulates the result of each upper and lower limit check of the four Vs values. The contents of $F 2$ are then read into the ram word no. 1.

F3-0 $\rightarrow 1$ if any of the Vs checks are found to be in error. F3-0 via $\overline{G 7}$ wil give an audible and visual alarm indication on the front panel. F3-0 also controls the switch of the Vs input multiplexer on Llo during the observation.

During the Vs-Vn subtractions ram bits 28Gl-22 and 28Gl-23 select one of the four Vs values stored in the 74170 register. The results of each subtraction along with the proper code for ram bits 22 and 23 is written back into the ram.

The 74 H 87 IC's are used to negate certain Vs-Vn results because certain Vn results received, due to hardware considerations, are as follows:

MRS $\times$ NRC $=-$ NRS $\times$ MRC
MLS $\times$ NLC $=-$ NLS $\times$ MLC where $M$ and $N$ are 2 different antennas
MRC $\times$ NLS $=-$ NLS $\times$ MRS
MLC $\times$ NRS $=$ NRC $\times$ MLS
The result that is then sent to core computer is in one's complement instead of two's complement.

Rom 6 is also located on this card. Rom 6 bits 0-19 inserts zeroes into the unused bit position(s) of all ram words. Rom 6 bits 20 and 21 control the selection of what is written into ram bits 20 and 21.
13. CRT $\leftrightarrow S C, C R T$ - Output and Input, and Update Control D13500L30

This logic card contains various CRT display and enter control logic. Table 2 lists the various possible connections between the CRT, SC, and Monty computer. The selection is done by the CRT I/O selection switch on the front panel on the $S C$ rack and by bit $2^{2}$ of the control word sent from Boss computer. For word formats refer to specification no. Al3500N3, Rev. B.

The UAR/T IC does all the receiving and transmitting to and from the CRT or Monty computer. F10-0 generates the strobe pulse that loads the UAR/T with a character to be transmitted. Fl0-2 generates a pulse that indicates when the UAR/T can be loaded with another character that is to be transmitted. Table 1 on the drawing lists the UAR/T input sources.

The output of the UAR/T is controlled by F6 register. Each number or letter that appears on the UAR/T output is strobed into F4. From F4, letters are then clocked into $F 5$ while numbers are clocked into $31 F 10$.

F7-0 stores the ETX that the CRT or Monty computer sends at the end of each transmission. Then at the very beginning of the next transmission of data from the CRT a Monty computer F7-1 $\rightarrow 1$ for 800 ns to reset F 5 and 31 F 10 .
14. CRT $\rightarrow$ SC, Control and Storage, Rom 3 D13500L31 This logic card contains Rom 3 and other logic for entering words and running test from the CRT or Monty computer. The FlFO's (Fll) are used for CRT entry and display. The Display Comparator is used strictly for CRT display.

All numbers entered by the CRT or Monty computer are shifted into Fl0 from which they are then shifted into Fll. If the number(s) in Fll is to be entered into the SC logic (e.g. a control word or delay word(s)) then Rom 3 sets up the proper control signals to do so. On the other hand if the number(s) in Fll is an address (es) of word(s) to be displayed, then Rom 4 will enable $(\overline{24 G 4-20)}$ the Display Comparator which compares the output of Fll to the ram address. All numbers in Fll that are display addresses are recirculated in Fll thru the 74157 multiplexer (Gl); thus allowing the display to be updated.

Rom 3 basic components consist of address register F 2 , roms, a rom output register (F1) and a rom loop counter (F3). The loop counter, when used determines how many 1.6 us Rom 3 stays on a particular address. The operation of the loop counter is illustrated in the timing diagram drawing Dl3500B5. The actual program words in Rom 3 and a description of what each rom bit controls is included in Al3500F3.

For a listing of the word formats for entering various words along with a brief description of the tests that can be carried out, one should refer to specification no. Al3500N3.

In addition to the rom output register; registers F13 thru F18 are used to hold rom instructions that execute various tests until a reset command from the CRT is received or until an observation is started.
15. $\mathrm{SC} \rightarrow \mathrm{CRT}$ Control, Rom 4 D13500L32

This logic card contains Rom 4 along with its address register and output register. Rom 4 controls all the logic for taking words from the ram, converting the binary words to octal or decimal, formatting, and transmitting the words to the CRT screen.

The operation of the logic on this card should all be straight forward.
16. SC $\rightarrow$ CRT Storage and Binary to BCD Converter Dl3500L33 This card is part of the display logic which is controlled by Rom 4. The main blocks of logic on this card are as follows:

1. Display Storage Fifo - stores up to 128 words from the ram. From this fifo the words are formatted and displayed.
2. Binary to Octal Converter - converts the binary words from the Display Storage Fifo into octal format for display.
3. Binary to Decimal Converter - converts the binary words from the Display Storage Fifo into decimal format for display.
4. Control logic - is enabled by Rom 4.

Figure 13 shows the flow of data from the ram to the CRT.
All words are clocked into the $33 F 1$ and then into the Display Storage Fifo during the Display - Vs Subtraction cycle of the ram. The timing diagram drawing Bl3500B5 should be studied in order to gain an overall view of the time relationship among the main logic blocks in the SC.

Because non-sequential multipliers and Requested Multiplier Addresses vary in length, a "l" is clocked into Fl (bit position Fl-0) along with
the last word from the ram. From the output of the Display Storage Fifo this " 1 " is then clocked into $F 9$ which gives an indication (via skip control on L35) to Rom 4 that this is the last word in the fifo that is to be formated and then displayed. on the CRT terminal screen.

When a number in F2 is to be converted to BCD, the mode control of F4 (Binary to Decimal Converter) is set and held to parallel entry. The required number of bits are serially shifted from F2 into F4 (parallel entry a bit at a time). As soon as the last bit is parallel entered into $F 4$ the number is completely converted to $B C D$. The mode control on F4 is then changed to shift right and then the number (depending upon its magnitude) is shifted so that the MSB of the BCD is in F4-20 thru F4-23. From F4-20 to F4-23 it is transmitted to the CRT terminal a decade at a time.
17. Alarm and Reset Control D13500L34

This card contains the logic for driving the buzzer and most of the error indicating LED's. As a safeguard against accidentally hitting one of the Function Reset switches and possibly effecting an observation, the Function Reset Interlock switch must be pushed while the desired Function Reset switch is held until the Function Reset Interlock LED goes off.

To properly reset a Vs error, L GO/NO GO or a R GO/NO GO error the reset pulse must be synchronized with other logic in the system. This synchronism is done on this card. The reset pulse for the Vs error starts after all the words have been read into the ram and Vs values have been checked and the reset pulse ends when BT ends. The reset for the $R$ and $L G O / N O G O$ is synchronized so that the Left and Right Input Multiplexer Registers (23Fll and 23F12) will be in step with the Output Multiplexer Register (23F13).
18. $S C \rightarrow C R T$, Rom 4 Loop Counters and Display Control D13500L35

This card contains three loop counters for Rom 4; logic that enables Rom 4 address register to skip thru 1, 2, 3 or 4 addresses; and clock generators and control signals for the logic on L33.

The operation of the three loop counters are the same as the others in the system. Timing for the loop counters is shown in drawing Dl3500B5.

The Rom 4 Address Skip Control determines (when enabled) if Rom 4 address register will advance to the next address or skip thru the next $1,2,3$, or 4 addresses as determined by the number loaded into F2. Rom 4 selects one of the inputs to the multiplexer and if that selected input is a "l"; then Fl will make Rom 4 address register 32 Fl skip thru the number of addresses as determined by 22 . All the inputs to the multiplexer are sufficiently explained on the drawing except the Limit Comparator. The Limit Comparator is two four-bit word comparator in which each of the four-bits has a separate enable control. Rom outputs 32G2-4 thru 32G2-7 serve as the enable controls. Rom outputs 32G2-0 thru 32G2-3 are compared with the output of the Octal Converter 33F3-28 thru 33F3-31.
19. System Monitor Analog Muxs Dl3500L36
20. System Monitor Alarm and Storage, Rom 7 Dl3500L37

All the points in the Digital Delay System that are monitored for voltage, temperature, and 100 MHz clock are brought to L36 where certain ones are scaled and all are multiplexed together and then the single buffered output is fed to L37. On L37 this multiplexed output feeds an A/D converter.

The Measurement Comparison and Alarm Generator checks each measurement for the conditions shown in Table 1 on the drawing. A "0" on G1 indicates power to the Delay/Multiplier Sections has been turned off. G3 is the signal that turns power on/off to the Delay/Multiplier Sections.

The F 2 register is the measurement control and address register for both the analog multiplexers on $L 36$ and Rom 7. Rom 7 contains the limits in which the measurements are compared against.

The output of the $A / D$ is clocked into $F l$ which holds the measurement until it can be clocked into the System Monitor Alarm and Storage Fifo (F3). If an alarm condition is detected, then the type of an alarm is clocked into F8 as shown by Table 3 on the drawing. The type of alarm is then entered into F3 along with the measurement.

As long as there are no alarm conditions F3 is reset at the beginning of every 50 ms integration period and then updated with 63 new measurements. If, however, an alarm condition occurs then F9-1 prevents F 3 from being reset until the contents of F 3 is read into the ram thru the tri-state gates. This ensures that the measurement in error is recorded by the computer.


LOGIC SYMBOLS - EXAMPLE
FIGURE I




SEE NOTES ON SHEET 1 (FIGURE 3).

WIRE WRAP BOARD IC LAYOUT (SHEET 2 OF 2)
FIGURE 4

$$
C=\overline{A_{0} \cdot A_{1}}+\overline{B_{0} \cdot B_{1}}
$$



$$
E=\left(\overline{A_{0} \cdot A_{1}}+\overline{B_{0} \cdot B_{1}}\right) \cdot D+A_{0} \cdot B_{0}+A_{1} \cdot B_{1}
$$

note: := logic "And"; +=logic "Or"; A logic I lor true) on the counter countrol causes it to count when a clock occurs.
figure 5.


NOTE: IF $2^{\circ}: 1$ AT THE BEGINNING OF BT, THERE WILL BE A CARRY TO $2^{\prime}$ WHEN BT RESETS $2^{\circ}$.
FIGURE 6
MULTIPLIERS \& INTEGRATORS



Figure 7. Front View of System Controller Rack.


Figure 8. Front View of Power Control Chassis and System Controller Chassis.


Figure 9. Top View of System Controller Chassis.


Figure 10. Rear View of System Controller's Front Panel.


Figure 11. Power Control Chassis.


Figure 12. Rear View of Power Control Chassis and System Controller Chassis.

SPECIFICATION NO.: Al3500N3, Rev. B
NAME: Communications Between Digital Delay-Multiplier System and VLA Synchronous Computers

DATE: May 8, 1975


APPROVED BY:


## DESCRIPTION:

All data between the Digital Delay-Multiplier System and the VLA Synchronous Computer (VLAC) will be controlled by a unit referred to as the System Controller (SC), which is the interface into and out of the Delay-Multiplier System. The only exceptions are monitored from the Samplers and, in the two antenna systems, one analog signal which is a combined total power signal. The exceptions will not be covered by this specification.

A block diagram of the communication system is shown in Figure 1. Two System Controllers (SC) are shown -- one for each 50 MHz system. In the protontype -- two antenna system -- there is only one SC, and all delays and multipliers are handled as though they were in the left polarization rack.

The System Controller CRT can be switched between the System Controller and Monty Computer. Thus the CRT can be used to communicate with the computer system in the same manner as other CRT's in the VLA. A CRT output of Monty Computer can also communicate directly with the SC. This connection is made whenever bit $2^{2}(C)$ of the first word sent by Boss Computer to SC is a l. This mode allows the online computer system to control the SC tests in the same manner that the SC's CRT terminal controls tests. The data input to the SC's CRT terminal controls tests. The data input to the SC's CRT input required for each test is listed in Table 6. Table 5 shows how Monty Computer could receive data back through its CRT input; however, this mode is not required by the online computer system since the same data is available to core Computer via its connection to the SC. Table 7 is the format for Table 5.

To operate the SC in test mode, Boss Computer should send two complete sets of data as shown in Tables 2 and 4. In addition to delay data, the two sets should contain the following:

First Set of Data:
Word 0: $\quad A=1, B=1, C=1$
Words 55 ....: Multiplier Sets Desired During Test
Second Set of Data:
Word $0: \quad A=0, B=0, C=1$
DO NOT SEND WORDS 55 THRU 405. (55 thru 60 in case of prototype)
Each of the communication networks to the Core computers and from the Boss computer consists of three signals:

1. Clock - maximum of 5 MHz
2. Data
3. Ready Line

The inputs to Core Computers are double buffered and when one buffer is full and the second begins receiving data the Ready Line changes state to "Not Ready". The sending block continues to send to the end of the present word, then stops and waits for the line to go "Ready" again.

Each of the three lines are twisted pair coaxial cable (RG-22) which is driven and received differentially with ECL logic. The transmission system has been tested with 500 ft . of cable and operation was excellent with considerable safety margin.

Tables 1 through 4 list all data transmitted to and from the System Controller, excluding the CRT, as follows:

Table 1 - Final System
Table 2 - Final System
Table 3 - Two Antenna System
Table 4 - Two Antenna System
-SC to VIAC
-VLAC to SC
-SC to VIAC
-VLAC to SC

The following rules are to be observed:

1. No transmission of data from VLAC to SC is to occur during blanking time. Therefore during blanking time the ready line from SC to VLAC is held "not ready".
2. Data transmission from VLAC to SC can be absorbed at the maximum rate ( 5 MHz clock rate) by the SC .
3. The block of data (VIAC to SC) shown in Tables 2 and 4 must be sent complete between two adjacent blanking times. This includes the first block sent before an observation is begun.
4. After a dump time, data from SC to VLAC may be taken at any rate and may extend across blanking times, but must be completed at least 2 microseconds prior to the beginning of the next dump time. Dump Time refers to the blanking time following completion of an integration period by the multipliers. Blanking time is referred to in the VLA system as "data invalid time" ( 1.603 ms ).
5. Format of data in both directions:

$$
\begin{aligned}
& 000000, P, D_{23}, D_{22} \cdots \cdots \cdots D_{1}, D_{0}, 1 \\
& P=\text { parity } \quad D_{n}=\text { data } \quad D_{0}=L S B \quad D_{23}=M S B \quad 1=\text { start bit }
\end{aligned}
$$ Transmission is serial, starting at "1". A minimum of one clock time will exist between words. The clock from SC to VLAC will be continuous ( $5 \mathrm{MHz}, 80 \mathrm{~ns}$ positive, 120 ns negative - negative going edge centered on data bit at transmitter). The clock from VIAC to SC same as above except discontinuous 32 clock pulses per 32 bit data word. The data word length and number of clock pulses may be as short as 30 , leaving off the last two zeros.

6. For each observation the VIAC will send a block of data between every set of blanking times, the first being before the blanking time which precedes the start of an observation (integration) and the last being before the blanking time which follows the end of the observation (integration).
7. The relationships between when the different sets of data sent to the VLAC are obtained and to what they apply is shown in Figure 2.
8. The delay data should never contain a delay value of less than 70 ns .
9. Data in the tables which indicate errors - such as parity, overflow, etc. - are indicated thus:

$$
\text { NO ERROR }=0 \quad \text { ERROR }=1
$$

SYSTEM CONTFINALSYSTEMK $\quad$ VEL (CORE \& B)


NOTE $\rightarrow$ IN all computer words from 12 through 3039 the $D 18$ bit is obtained by using the oven flow bit to

SYSTEM CONTROLLER—VLAC (CORE A\&B)


DINAL SYSTEMK
SYSTEM CONTROLLER $\because V L A C(C O R E A \& B)$
 indicate the last word of fransmission.


REV, $B$
REV.A

5/7/75 ame A, M, Shalloway $6-11-74$

PROTOTYPE (2 ANTENMA) SYSTEMK
SYSTEM CONTROLLER $\rightarrow$ VLAC (CORE A)




YPROTOTYPE (2 ANTENNA) SYSTEMK

SYSTEM CONTROLLER $\longrightarrow$ VLAC (CORE A)


ROFOMYFE (2AHPEMA $A$ SOTETK
VLAC $B O S S) \longrightarrow S Y S T E M$ CONTROLLER


INSTRUCTIONS FOR CRT TERMINAL DATA DISPLAY

NOTES :
A. In each instruction below, the first heading (e.g. DB 0000.7137) is used to display the desired information in octal and the second heading (e.g. DC 0000.7137) is used to display the information in decimal. If only one heading is shown, the information is available only in octal.
B. At the end of each display instruction, the ENTER key must be depressed to transfer the instruction from the CRT to the SC. This function will appear on the CRT screen as a backwards letter L (e.g. DB 0000.7137」).
C. Spaces within an instruction have no effect and may be used as desired for clarity (e.g. DB0000.7137 or DB 0000.7137).
D. To continually update the data display, prefix the desired instruction by one of the following letters:

| LETMER | UPDATE PERIOD |
| :---: | :---: |
| R | 0.8 sec |
| S | 1.6 sec |
| T | 3.2 sec |
| U | 6.4 sec |
| V | 12.8 sec |
| W | 25.6 sec |
| X | 51.2 sec |
| Y | 102.4 sec |

For faster update periods, some displays will not have time to complete between updates depending on the length of the display and the baud rate.
E. To stop an updating display (necessary before entering new instructions) use the DA instruction.
F. Each instruction for displaying multiplier results (instructions 3 thru 6) contains one or more octal number XXXX which is a starting address for a group of 8 multiplier results. These may be interpreted in two ways:

```
XXXX \(=\) Octal number of starting RAM address
```

or if the least significant digit is taken as zero:


TABLE 5 (continued)
INSTRUCTION

1. DA

## DATA TO BE DISPLAYED

STOP UPDATE and RESET DISPLAY LOGIC
(No data will be displayed by this instruction)
2. DB

DC 0000.7137 CONTROL and TIME WORDS
3. DD

DE XXXX
MULTIPLIER RESULTS, SEQUENTIAL
BEFORE Vs SUBTRACTION
(128 sequential multiplier results starting at SC Ram address XXXX)
4. $D F$

DG XXXX. $\cdot$. $\operatorname{XXXX} .1000$
MULTIPLIER RESULTS, GROUPS OF 8 BEFORE VS SUBTRACTION
(Maximum of 16 groups, each group consisting of 8 sequential multiplier results starting at SC Ram address XXXX )
5. DH XXXX

MULTIPLIER RESULTS, SEQUENTIAL AFTER VS SUBTRACTION

- AF Ler

6. DI XXXX. . . XXXX. 10000

MULTIPLIER RESULTS, GROUPS OF 8 AFTER VS SUBTRACTION
7. DL

DM 6000
DELAY and DISABLE DATA
EXCHANGE DATA AND MUX ADDRESSES
(54 delay words; 2 test delay words; left and right exchange data in the order $C M, C L, S M, S L$; input and output mux addresses)
8. DN

DO 6100
(64 words)
9. DP 6200

GO/NO GO DATA
(Delay Line Self Test Results 54 words $=216$ delay lines)
10. $\mathrm{D} Q \mathrm{XXXX}$

RAM DATA SET
( 8 sequential words starting at Ram octal address XXXX, bits 0 thru 21 displayed in octal)
11. DR

PARITY ERROR ADDRESSES
DS 6300
(64 words, contains computer word number for parity error and the BT in which it occurred BOSS computer to SC )
12. DT

DU 6400
ADDRESSES OF MULTIPLIERS REQUESTED
(Maximum of 351 words, each representing one multiplier set requested by VLAC)

INSTRUCTIONS FOR CRT TERMINAL DATA ENTRY

NOTES:
A. All numbers indicated by $X$ are in octal.
B. At the end of each entry instruction, the ENTER key must be depressed to transfer the instruction from the CRT to the SC. This function will appear on the CRT screen as a backwards letter L (e.g. EE XXJ).
C. Spaces within an instruction have no effect and may be used as desired for clarity (e.g. EXX or EE XX).
D. The following table gives the delay word number for each of the eight prototype delay words and the corresponding multiplexer address that tests the associated delay lines:

| DELAY WORD NUMBER |  | DELAY |  | MULTIPLEXER ADDRESS |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Decimal | Octal | Ant. No. | 50 MHz System | Decimal | Octal |
| 37 | 45 | 1 R | A | 19 | 23 |
| 39 | 47 | 1R | B | 20 | 24 |
| 41 | 51 | 2R | A | 21 | 25 |
| 43 | 53 | 2R | B | 22 | 26 |
| 45 | 55 | 1L | A | 23 | 27 |
| 47 | 57 | 1L | B | 24 | 30 |
| 49 | 61 | 2L | A | 25 | 31 |
| 51 | 63 | 2L | B | 26 | 32 |

E. The following table gives the GO/NO GO logic tests for mux addresses 0 and 28-31.

| MUX ADR | INPUT MUX <br> DATA | OUTPUT MUX <br> DATA | GO/NO GO |
| :---: | :---: | :---: | :---: |
| RESULTS |  |  |  |$|$|  | 0 | 0 | GO |
| :---: | :---: | :---: | :---: |
| 28 | 1 | 1 | GO |
| 29 | 0 | 1 | NO GO |
| 30 | 1 | 0 | NO GO |
| 31 | Random Data | Random Data | NO GO |

## TABLE 6 (continued)

1. EA XXXX

## CONTROL WORD

$\uparrow \uparrow$ - Observation/Test Status: Bits CBA (see Table 2)
Parity Error Status = Bits FED (see Table 2)
l thru $6=50 \mathrm{~ms}$ thru 300 ms Dump Period $=$ Bits $\mathrm{P}_{2} \mathbf{P}_{1} \mathbf{P}_{0}$ (see Table 2)
1 = Disable Neg Sampler 2 = Disable Pos Sampler $3=$ Both: Bits $\mathrm{S}_{7} \mathrm{~S}_{5} \mathrm{~S}_{4}$ (see Table 2)
2. EB X XXXXX XX

DELAY DATA, SAME TO ALL DELAY CONTROLS


Sampler delay in 625 picoseconds steps
Delay Line Delay in 10 nanosecond steps
$0=$ Normal $1=$ Delay Line Disable $2=$ Sampler Invert $3=$ Both
3. EC X XXXXX XX. ....X XXXXX XX

54 delay words
each as in EB
4. ED XX .X XXXXX XX


DELAY DATA TO ONE DELAY CONTROL
Same as in EB
(In decimal $1=1 \mathrm{~L} \cdot . .53=27 \mathrm{~L}$
$2=1 R \cdots 54=27 R$
See Note D for prototype)
5. EE XX HOLD MUX ADDRESSES

L -Octal max address to hold
(In decimal $1=$ Ant $127=$ Ant 27
0 and 28-31 $=$ Tests of GO/NO GO Logic) See Note E.
Ga. EF XXXX
EXCHANGE DELAY LINE (S) AT ONE MUX ADP
Octal max. adr. of delay line to be exchanged
Exchange data $1=S L \quad 2=S M \quad 3=$ Both
Exchange data $1=C L \quad 2=C M \quad 3=$ Both
6b. EF XX XXXX
EXCHANGE DELAY LINE (S) AT ONE MUX ADP HOLD INPUT MUX AT AN ALTERNATIVE ADP


Octal mux address of delay line to be exchanged
Exchange data $1=S L \quad 2=S M \quad 3=$ Both
Exchange data $1=C L \quad 2=C M \quad 3=$ Both
Octal address for alternative input max address
7. EG 3317

MULTIPLIER TEST-RANDOM NOISE GENERATOR (All multiplier terminated inputs receive the same data pattern and all bridging inputs receive the same data pattern but different

11. EK XX

DELAY LINE TEST-ROTATE MUX ADR LONG PATTERN
† Octal mux address at which test starts
12. EL

RESET FROM COMPUTER
(Left GO/NO GO
and Exchange
Data)
13. EM

RESET FROM COMPUTER
(Right GO/NO GO
and Exchange Data)
14. EQ

RESET TEST INSTRUCTIONS 5 THRU 11 (Resets storage flip flops F13 thru F17 on L 31 but does not reset the TEST indicator)
15. ER

RESET ALL TESTS
(Same as EQ
but also
resets the
TEST indicator)

TABLE 7
CRT DISPLAY FORMATS

NOTES:

1. The following table is intended to aid the user of the System Controller CRT to interpret the displayed information. This table is intended to be used along with Tables 1-6 to provide a complete users description of the display functions available.
2. For each type display instruction an example display or partial display is shown, and where appropriate, the associated 24 bit computer word is shown to indicate which bits of the word are represented by each character displayed on the CRT screen.
3. If certain conditions are present in the displayed information, the associated character is displayed on the CRT screen as a reverse flashing character. In the display examples these characters are shown with an underline. For certain test conditions that are not errors, the associated display character appears on the screen as a reverse character but without flashing.

EXAMPLES: $\underline{2}$ indicates error condition
2* indicates test condition

## DISPLAY EXAMPLES

1. CONTROL and TIME WORDS

Octal
DB 0000.7137
1 $\underline{2} \underline{2} \underline{2} \underline{2} \underline{2}$ * $6 \underline{2} 57777$ (tens of seconds)
Decimal
DC 0000.7137
$1 \underline{2} \underline{2} \underline{2} \underline{2} \underline{2 *} 6 \underline{2} 5110$ SEC
2. MULTIPLIER RESULTS

## Octal

```
DD XXXX (seq. before }\mp@subsup{\textrm{V}}{\mathbf{S}}{}\mathrm{ )
DH XXXX (seq. after }\mp@subsup{V}{S}{\prime}\mathrm{ )
DF xxxx.10000 (non-seq. before V ( )
DI Xxxx.10000 (non seq. after V (S)
    7 1777777 <8 per line 
```

Decimal
DE XXXX (seq. before $\mathrm{V}_{\mathbf{s}}$ )
DG XXXX. 10000 (non-seq. before $V_{S}$ )
6 $524287+8$ per line $\rightarrow$ 6 524287

## Control Word Only



Multiplier Result


Multiplier Result

3. DELAY VALUES and EXCHANGE DATA

Octal
DL 6000
LEFT - - - - - . - - - - - - - RIGHT
$1 \underline{1} 33773317+4$ per line $\begin{array}{lllllll}1 & 1 & 377 & 3 & 317\end{array}$
14 Lines Total: Line $1=1$ left 1 right 2 left 2 right Line $14=27$ left 27 right Left Right Test Test Delay Delay

| LEFT | RIGHT |
| :---: | :---: |
| $\underline{1} \underline{1} \underline{1} \underline{17}$ | $\underline{1} \underline{\underline{1}} \underline{1} 37$ |
| 37 | 37 |
| 37 | 37 |
| 37 | 37 |



111638315 +4 per line +111638315
14 lines total in same order as above

| LEFT | RIGHT |
| :---: | :---: |
| 111131 | $\underline{1} 11131$ |
| 31 | 31 |
| 31 | 31 |
| 31 | 31 |

Delay Word

## Exchange Data

CM CL SM SL $\quad$ Sin Input Mux Adr
Cos Input Mux Adr
Sin Output Mux Adr
Cos Output Mux Adr

## Delay Word



Exchange Data
Same as for octal
4. SYSTEM MONITOR MEASUREMENTS (2 ANT PROTOTYPE)

| DN 6100 | (octal) |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DO 6100 ( | (decimal) |  |  |  |  |  |  |  |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | Out of Spec Code: |
| 1. $\left.\frac{0}{(+5} 5 \mathrm{SC}\right)$ | $\frac{0}{(+5 \mathrm{D} / \mathrm{M})}$ | $\underline{0} \mathrm{xxxx}$ | $\stackrel{0}{(-5.2 \mathrm{D} / \mathrm{M})}$ | $\frac{0}{(-5.2600 *}$ | $\begin{aligned} & \underline{0} 1200 \\ & (-12 \mathrm{D} / \mathrm{M}) \end{aligned}$ | $\left.\frac{0}{(-12} 1200\right)$ | $\begin{gathered} 02800 \\ (+28 \mathrm{D} / \mathrm{M}) \end{gathered}$ | $\begin{aligned} & 0=\text { In spec } \\ & 3=\text { Emergency Low } \end{aligned}$ |
| $\text { 2. } \frac{0}{(+15 \mathrm{SC})}$ | $\frac{0}{(1500}(-15 \mathrm{SC})$ | $\begin{aligned} & \underline{0} 900 \\ & (-9 \mathrm{SC}) \end{aligned}$ | $\underline{0} \mathrm{XXXX}$ | $\underline{0} \mathrm{XXXX}$ | 0 XXXX | O XXXX | $\underline{0} \mathrm{XXXX}$ | $\begin{aligned} & 5=\mathrm{High} \\ & 7=\text { Low } \end{aligned}$ |
| 3. $\frac{0}{(02 \mathrm{~V}} 1000 *$ | $\underline{0} \mathrm{xxxx}$ | 0 O XXXX | $\underline{0} \mathrm{XXXX}$ | $\underline{0}$ XXXX | 0 XXXX | $\underline{0}$ XXXX | $\underline{0} \mathrm{XXXX}$ | For an Emergency High condition in either the SC or D/M rack, the |
| 4. 0 XXXX | $\underline{0}$ XXXX | $\underline{0}$ XXXX | $\underline{0} \mathrm{XXXX}$ | $\underline{0} \mathrm{XXXX}$ | $\underline{0} \mathrm{XXXX}$ | $\underline{0} \mathrm{xxxx}$ | $\underline{0} \mathrm{XXXX}$ | D/M rack will be automatically powered down |
| $\text { 5. } \underset{\substack{\text { (Mult } \\ \text { Clk) } \\ 750 *}}{\text { ( }}$ | $\begin{gathered} \frac{0}{750 *} \\ \text { (Dly } \\ \text { Clk) } \end{gathered}$ | $\begin{aligned} & \underline{0} 750 * \\ & \text { (Cont A } \\ & \text { Clk) } \end{aligned}$ | $\underline{0} \operatorname{xxx}$ | $\underline{0} \mathrm{XxXX}$ | $\underline{0} \mathrm{XXXX}$ | $\underline{0} \mathrm{XXXX}$ | $\underline{0} \mathrm{XXXX}$ | and all error codes will contain either an 8 or 9 or a punctuation character. |
| 6. 0 XXXX | $\underline{0} \mathrm{XXXX}$ | $\underline{0} \mathrm{XXXX}$ | $\underline{0} \mathrm{XXXX}$ | $\underline{0} \mathrm{Xxxx}$ | 0 O Xxxx | $\underline{0} \mathrm{XXXX}$ | $\underline{0} \mathrm{xxxx}$ |  |
| 7. $\underset{(\mathrm{SC} \text { Temp) }}{1100 *}$ | $\begin{gathered} 0 \\ (\mathrm{SC} \text { Temp) } \end{gathered}$ | $\frac{0}{(\mathrm{D} / \mathrm{M} \text { Tem }}$ | $\underline{0} \mathrm{xxXx}$ | $\underline{0} \mathrm{XXXX}$ | $\underline{0} \mathrm{xxxx}$ | $\underline{0} \mathrm{XXXX}$ | O XXXX |  |
| 8. 0 XXXX | $\underline{0} \mathrm{XXXX}$ | O XXXX | $\underline{0} \mathrm{XXXX}$ | $\underline{0} \mathrm{XXXX}$ | $\underline{0} \mathrm{XXXX}$ | $\underline{0} \mathrm{XXXX}$ | $\underline{0} \mathrm{XXXX}$ |  |

NOTES :

1. The nominal measurement is shown above in decimal. For octal display, only the measurement is in octal.
2. Measurements marked * must be doubled to obtain the value.
3. The user must enter the decimal point mentally.
4. Clock measurements are of the peak value of the sinewave 100 MHz clock.
5. $S C=$ System Controller Rack $\quad D / M=$ Delay-Multiplier Rack.
6. XXXX = Inputs not used in 2 Ant Prototype and spare inputs. These are not all zero on the display.
7. Full range temperature $=81.90^{\circ} \mathrm{C}$.
8. GO/NO GO RESULTS

DP 6200 (octal only)
LEFT - . . . . . . . . . . . . . . . RIGHT

6. RAM DATA SET

DQ $x x x x$ (octal only)

17777777
$\downarrow$ Total of 8 words 17777777
7. PARITY ERROR ADDRESSES

DR 6300 (octal)
DS 6300 (decimal)
6 $677 \leftarrow 8$ per line +6677

Computer Word Bit:

8. ADDRESSES OF MULTIPLIERS REQUESTED

```
DT 6400 (octal)
DU 6400 (decimal)
```

Multiplier set number requested by BOSS Computer (decimal set numbers are 32 thru 382)
$677+16$ per line max $\rightarrow 677$
22 lines total maximum
351 total addresses maximum


FIGURE I
COMMUNICATIONS SYSTEM BETWEEN SYSTEM CONTROLLER AND VLA SYNCHRONOUS COMPUTERS


NOTE: ABOVE COVERS DATA FROM SC TO CORE COMPUTIR-SEE TABLES I\&3. COLUMN 1 IndiCATES WHEN THE SC's Storage receives the mata-FRom hither core computer, delay mulititith or shia imicemal control. COLUMN 2 Indicates whin this data wails used or generated.
BITS A\&B IN TAGLES 2\&4, COMPUTCR WORD O, WILL FOLLOW A PATTERN AS SHOWN WLLOW:


## TABLE I

MULITPLIER INTERCONNECTION ARRAY

See Page 3-4

## DIGITAL DELAY AND MULTIPLIER SYSTEM DRANING LIST

## Block and Timing Drawings

Multiplier Section Block Diagram
Timing for Multiplier Section (D1350017
System Controller Block Diagram
General Timing of Events
D13500B2

Ting Biming of Events
D13500B3
Timing Between Main Control
Delay Words Transfer Timing
D13500B5
E13500B6

## Mechanical Drawings

| Wire Wrap Card - 22 Rows, 100 Contact Conn. | D13520M1 |
| :---: | :---: |
| Wire Wrap Card - 10 Rows, 100 Contact Conn. | D13520M2 |
| Extender Board Connector and Connector Mtg. Block | B13520M3 |
| Extender Board Puller Attachment | A13520M5 |
| Card Guide Bar | D13500M12 |
| Side Plate | C13500M13 |
| Mother Board Buss and Support Bars | D13500M14 |
| Dip Ground Pin Extender | B13500M16 |
| Clip, Scope Ground | B13500M17 |
| Test Chassis Front Panel | C13500M18 |
| Multiplier Mother Board Buss Strip | B13500M19 |
| Bar, Support For 6.2" Wide Card | B13500M20 |
| Bar, Support For 8.5" Wide Card | B13500M21 |
| Puller Arm Assembly For 6.2' ${ }^{\text {' }}$ (side Card | B13500M22 |
| Puller Arm Assemlby For 8.5" Wide Card | B13500M23 |
| Block, Bar Support For Both 6.2" and 8.5" Wide Card | B13500M24 |
| Foot, Bar Support For Both 6.2' and 8.5" Wide Card | B13500M25 |
| Control Logic Chassis Rear Mounting ingle | C13500M33 |
| Control Logic Chassis Side Mounting ingle | C13500M34 |
| Control Logic Chassis Card Guide Support | C13500M35 |
| Control Logic CHassis Side Plate | C13500M36 |
| Brace, Integrator Chassis | B13500M37 |
| Front Panel | C13500M38 |
| System Controller Front Panel | D13500M39 |
| Buss Bar | D13500M41 |
| Buss Bar | D13500M42 |
| Pwr. Control Chassis AC Portection Cover for Cinch Term. Bds | B13500M43 |
| Pwr. Control Chassis Bottom Plate | D13500M44 |
| Pwr. Control Chassis AC Plug Cover Plate | C13500M45 |
| Pwr. Control Chassis Front/Side Angle | B13500M46 |
| Pwr. Control Chassis Rear Panel Top Support | C13500M47 |
| Pwr. Control CHassis Bottom/Side Angle | C13500M48 |
| CRT and System Pwr. Control Chassis Rear Panel | C13500M49 |
| Pwr. Control Chassis Middle/Bottom Rear Panel Supports | C13500M50 |
| CRT and System Pwr. Control Chassis Side Plate | C13500M51 |
| System Controller Cable Roller Assembly | C13500M52 |
| Front Panel Spacer | B13500M53 |
| Air Filter Guide | B13500M54 |
| Waber AC Protection Cover | B13500M55 |


| Firmware |  |
| :---: | :---: |
| Ram Address Memory | Al3500F1 |
| Control For System Controller | Al3500F2 |
| Crt Entry Control | Al3500F3 |
| Crt Display Control | Al3500F4 |
| $V_{s}$ Limits | Al3500F5 |
| Zero Control Rom | Al3500F6 |
| Delay Line Card | Al3500F7 |
| Delay Control Card | Al3500F8 |
| Multiplier Board | Al3500F9 |
| Delay Motherboard | Al3500F10 |
| System Monitor Limits | Al3500F11 |
| Bill of Materials |  |
| Delay Card Assembly | A13500Z5 |
| Delay Control Card | A13500Z3 |
| Multiplier | A1350024 |
| Low Speed Integrator | A1350026 |
| High Speed Integrator | A1350027 |
| $\mathrm{V}_{S}$ Counter and Reset | A1350078 |
| Control A | A13500Z9 |
| Control B | Al3500Z10 |
| Temporary Storage | A13500211 |
| S x C Integrator Storage | A13500212 |
| Delay Word Program Buffer | A13500213 |
| Assembly Drawings |  |
| Multiplier Board Layout | B13500P1 |
| Delay Board Layout | B13500P2 |
| Control Board Layout | B13500P3 |
| Mother Board Connector Layout | D13500P4 |
| Multiplier Mother Board Profile | D13500P5 |
| Multiplier P.C. Board (6 sheets) | D13500P6 |
| Multiplier P.C. Mother Board Layout (2 sieets) | D13500P7 |
| Delay Multiplier Chassis Assembly | D13500P8 |
| Marking, Mult. Test Fixture | B13500P9 |
| Component Platform Negative Pattern | B13500P12 |
| Delay Mother Board Assembly Info. | B13500P13 |
| Delay Line Assembly Info. | B13500P14 |
| Delay Control Assembly Info. | B13500P15 |
| Multiplier Board Assembly Info. | B13500P16 |
| Coaxial Cable Assembly - Variable | C13500P17 <br> Dl3500P18 |
| Rack Layout \& Mult. Rack Card Layout | D13500P18 |
| SC Chassis Layout | C13500P19 |

## Schematic Diagrams

Clock Power Divider ..... B13500S1
Delay Mult. Rack Power Relay Control ..... C13500S3
Clock Buffer Platform ..... B13500S4
System Controller Front Panel Interface ..... D13500S5
-2/15A RegulatorBl3540S1
Printed Circuit Board

|  | Artwork | Silkscreen | Mechanical |
| :---: | :---: | :---: | :---: |
| Printed Wiring Board Extender Board | E13520A1 |  | B13520M4 |
| Logic Symbols | E13520A2 |  |  |
| 100 MHz Test Board (2 sheets) | E1352CAB3 |  |  |
| A.C. Coupled Mult. and Sig. Dist. Test Board | E135 20AD4 |  |  |
| Clock Ampl 100 MHz 20 Watts | E135 20AD5 |  |  |
| 5 Digit Display | A13500AB6 |  |  |
| Wire Wrap Board 8.5' x 11" | F13500AD7 | D13500AB8 | C13500M6 |
| $V_{0}$ Counter BT and Reset Card | E13500AD9 |  | C13500M26 |
| Clock Power Divider | D13500AD10 |  | D13500M40 |
| Over Voltage Relay | B13500AB11 |  |  |
| Component Platform | B13500AD14 |  | B13500M28 |
| Delay Test Fixture Interface Card | B13500AB15 |  |  |
| -2V/500ma. Regulator P.C. Board Plat. | B13500AD16 |  |  |
| Power Relay Control (2 sheets | B13500AB17 |  |  |
| Clock Buffer Platform | B13500AD18 |  |  |
| System Controller Front Panel Interface | Cl3500AB20 |  |  |
| Multiplier Mother Board |  |  | C13500M11 |
| Collins Radio 982-079-0006 (neg) | C13500A21 |  | D13500M10 |
| Delay Mother Board Colling Radio 982-079-0004 (neg) | C13500A22 |  | D13500M8 |
| Delay Test Mother Board Collins Radio 982-079-0005 (neg) | C13500A23 |  | D13500M9 |
| Dealy Line (Negs Only) (Collins) | B13500A24 |  |  |
| Delay Control (negs only) (Collins) | B13500A25 |  |  |
| Multiplier (negs only) (Collins) | B13500A26 |  |  |
| Boss-Test Status Indicator Mask | A13500AD28 |  |  |
| Monty-S.C. Status Indicator Mask | A13500AD29 |  |  |
| -2V/15A Regulator | B13540ABI |  | B13540 ${ }^{\text {M }}$ |

## Logic Diagrams

High Speed Integratcis D13500LI
Delay Line (2 sheets) ..... D13500L2
Control Card (2 sheets) ..... D13500L3
Low Speed Integrators ..... D13500L4
Multipliers ..... D13500L5
Sample Counter BT and Reset Card ..... C13500L6
Multiplier Control A ..... D13500L7
Multiplier Control B ..... D13500L8
Temporary Storage ..... D13500L9
$V_{S}$ and $S \times C$ Integrator ..... D13500L10
Self Test Output MuX ..... D13500L11
Test Fixture - High and Low Speed ..... D13500L12
Test Fixture - Multiplier ..... D13500L13
Delay Test Fixture ..... D13500L14
Delay Program Word Buffer ..... D13500L15
Test Chassis Test Control Logic Card ..... D13500L16
Test Chassis Front Pane1, OSC and -2V Reg. ..... D13500L17
Clock ..... D13500L18
Boss $\rightarrow$ SC Requested Mult. Address and Control Reg. ..... D13500LI9
Delay Word Storage, Delay Test Generator, Delay/Sampler output SR ..... D13500L20
Data Control VLAC $\rightarrow$ SC $S C \rightarrow$ Delay ..... D13500L21
Exchange Data Generator Go/No Go Storage ..... D13500L22
Boss $\rightarrow$ SC Parity Sotrage and Delay Mux. Registers ..... Dl3500L23
System Control ROM 2 ..... D13500L24
RAM Address Memory ROM 1 ..... D13500L25
RAM Bits 20 to 27 Address Reg. ..... D13500L26
RAM Bits $2^{8}$ to 215 ..... D13500L27
RAM Bits $2^{16}$ to 223 ..... D13500L28
$V_{s}$ Subtractor ROM 5 and ROM 6 ..... D13500L29
$C R T \leftrightarrow S C$ CRT - Output and Input and Update Control ..... D13500L30
$C R T \rightarrow S C$ Control and Storage ROM 3 ..... D13500L31
SC $\rightarrow$ CRT Control Rom 4 ..... D13500L 32
SC $\rightarrow$ CRT Storage and Binary to BCD Converter ..... D13500L33
Alarm and Reset Control ..... D13500L34
SC $\rightarrow$ CRT ROM 4 Loop Counters and Display Control ..... D13500L35
System Monitor Analog Muxes ..... Al3500L36
System Monitor Alam and Storage ..... D13500L37
2 ANT Test Set ..... D13500L38
Self Test Input MUX ..... D13500L39

## ROM 2 BIT DESCRIPTION

| LOGIC DWG. D13500L24 |  |
| :---: | :---: |
| ROM OUTPUT |  |
| REGISTER BIT | FUNCTION |
| F3-0 | Ram address register (26F4) clock enable |
| F3-1 | Ram address register ( $26 F 4$ ) clock/load control |
| F3-2 | Ram address register (26F4) input mux. selection control. |
| F3-3 | Rom 1 address register ( 25 Fl ) reset control |
| F3-4 | Rom 1 address register (25F1) clock enable |
| F3-5 |  |
| F3-6 |  |
| F3-7 | Rom 6 address |
| F3-8 |  |
| F3-9 |  |
| F3-10 | Vs Check enable |
| F3-11 | Clock for DT register (19F6) and reset for Observation Initiation Reset register (21F23) |
| F3-12 | Rom 2 address register (24F1) clock enable and reset control for Rom 2 output register (24F3), bits $2^{0}$ thru $2^{11}$ |
| F3-13 | Rom 2 address register (24Fl) clock enable |
| F3-14 | Rom 2 Loop Counter load and advance control |
| F3-15 | Enable for the ram read/write signal |
| F3-16 | O=read/write pulse for Load Ram Cycle |
|  | l=read/write pulse for vs Subtraction Cycle |
| F3-17 | Shift Out Generator and Select Control |
| F3-18 | and 3-St. Select Control par the following table: |
| F3-19 | \} |
| F3-20 F3-21 |  |
|  | 00000 Not used |
|  | $0 \quad 0 \quad 0 \quad 0 \quad 1 \quad$ Not used |
|  | 0 0 0 1 0 Not used |
|  | $\begin{array}{lllll}0 & 0 & 0 & 1 & 1\end{array}$ |


|  | FUNCTION |
| :---: | :---: |
| $\begin{array}{lllll}0 & 0 & 1 & 0 & 0\end{array}$ | System Monitor |
| $\begin{array}{lllll}0 & 0 & 1 & 0 & 1\end{array}$ | GO/NO GO |
| $\begin{array}{lllll}0 & 0 & 1 & 1 & 0\end{array}$ | Boss $\rightarrow$ SC Parity |
| $\begin{array}{lllll}0 & 0 & 1 & 1 & 1\end{array}$ | Request Multiplier Addresses |
| $\left.\begin{array}{lllll}0 & 1 & 0 & 0 & 0\end{array}\right)$ |  |
| $\begin{array}{lllll}0 & 1 & 0 & 0 & 1\end{array}$ |  |
| $\begin{array}{lllll}0 & 1 & 0 & 1 & 0\end{array}$ |  |
| $\left.\begin{array}{lllll}0 & 1 & 0 & 1 & 1\end{array}\right\}$ | Temporary Storage |
| $\begin{array}{lllll}0 & 1 & 1 & 0 & 0\end{array}$ | 3-St. Select Control |
| $\begin{array}{lllll}0 & 1 & 1 & 0 & 1\end{array}$ | via L8 |
| 0 1 1 1 1 0 | Not used |
| $\begin{array}{lllll}0 & 1 & 1 & 1 & 1\end{array}$ | Not used |
| $1 \begin{array}{lllll}1 & 0 & 0 & 0 & 0\end{array}$ | Time Word |
| $\begin{array}{lllll}1 & 0 & 0 & 0 & 1\end{array}$ | SxC Address (Ram Word 8) |
| $1 \begin{array}{lllll}1 & 0 & 0 & 1 & 0\end{array}$ | Control Word |
| $\begin{array}{lllll}1 & 0 & 0 & 1 & 1\end{array}$ | Vs Theoretical Value |
| $1 \begin{array}{lllll}1 & 0 & 1 & 0 & 0\end{array}$ | Vs Subtraction Result |
| $\begin{array}{llllll}1 & 0 & 1 & 0 & 1\end{array}$ | Not used |
| $1 \begin{array}{lllll}1 & 0 & 1 & 1 & 0\end{array}$ | Rom 2 Control Comparator selection |
| $\begin{array}{lllll}1 & 0 & 1 & 1 & 1\end{array}$ | Not used |
| $\begin{array}{llllll}1 & 1 & 0 & 0 & 0\end{array}$ | NO DECODER FOR THIS SELECTION |
| $\begin{array}{lllll}1 & 1 & 0 & 0 & 1\end{array}$ | NO DECODER FOR THIS SELECTION |
| $\begin{array}{llllll}1 & 1 & 0 & 1 & 0\end{array}$ | NO DECODER FOR THIS SELECTION |
| $\begin{array}{llllll}1 & 1 & 0 & 1 & 1\end{array}$ | NO DECODER FOR THIS SELECTION |
| 111100 | NO DECODER FOR THIS SELECTION |
| $\begin{array}{lllll}1 & 1 & 1 & 0 & 1\end{array}$ | NO DECODER FOR THIS SELECTION |
| $\begin{array}{lllll}1 & 1 & 1 & 1 & 0\end{array}$ | NO DECODER FOR THIS SEIECTION |
| $\begin{array}{lllll}1 & 1 & 1 & 1 & 1\end{array}$ | NO DECODER FOR THIS SELECTION |
| SC $\rightarrow$ Computer Transmit Control enable |  |
| ANDed with 19G1-9 <br> Address. The ANDe <br> address register <br> control on Rom 2 a | which indicates the last Requested Mult. Ded output is a clock enable for Rom 2 (24F1) and also controls the clock/load address register (24Fl). |

## ROM 3 BIT DESCRIPTIONS

LOGIC DWG.
D13500L30

ROM OUTPUT
REGISTER BIT

## FUNCTION

```
Fl-0 Load Control Word Storage Register (19F4)
Fl-1 Clock registers 19F2 and 20F1
Fl-2 20Fl recirculate control via 3lG5
Fl-3 Shift 20Fl by 10 via 2lF4
F1-4 Load Delay Input/Output Mux. Address Registers 23F11, 23F12,
    23F13 with address from CRT
Fl-5 Load X-DATA Registers 22F1 and 22F2 GO/NO GO from CRT
F1-6 Load all ones into X-DATA of all delay words, thus
    enabling the random noise generator to feed the inputs
    of the multipliers. Also strobes the mulitplier static
    data pattern-if entered - into 3lF8.
F1-7 Feeds a decoder, see table below
F1-8 Enables delay line test
Fl-9 Selects delay line test pattern 0=short pattern, l=carry
Fl-10 Feeds a decoder, see table below
F1-11 Feeds a decoder, see table below
Fl-12 Enables the shift out clock to CRC }->\mathrm{ SC Storage FlFO (3IFll)
Fl-13 Advance Rom 3
Fl-14 Load and advance loop counter and reset gom 3 output register,
    bits 20}\mathrm{ to 2 }\mp@subsup{2}{}{7
F1-15 Load Rom 3 address register and reset Rom 3 output register,
    bits 20}\mathrm{ to 2 }\mp@subsup{}{}{7
```

| $\begin{aligned} & -1 \\ & -1 \\ & 1 \\ & -1 \end{aligned}$ | $\xrightarrow{-1}$ |  | FUNCTION |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | Do nothing state |
| 0 | 0 | 1 | Reset test storage flip flops 3¢Fl3-36F18 |
| 0 | 1 | 0 | Advance Rom address register via $41 F 8$ after 3DT |
| 0 | 1 | 1 | Reset left GO/NO GO indicators and logic |
| 1 | 0 | 0 | Reset right GO/NO GO indicators and logic |
| 1 | 0 | 1 | Complete reset of Rom 3 logic |
| 1 | 1 | 0 | Hold certain error indicators and alarm from activating |
| 1 | 1 | 1 | Light "TEST" indicator via $\overline{31 G 11}$ |

## LOGIC DRAWING

 Dl3500L32ROM OUTPUT
REGISTER BIT

## FUNCTION

Controls a decoder on $L 35$ which in turn performs one of the following functions

| F2-0 |  |
| :---: | :---: |
|  | $\left\lvert\, \begin{array}{lllll} 0 & 0 & 0 & \text { Do notining } \\ 0 & 0 & 1 & \text { Serially shift } 33 F 21 \text { time and clock } 33 F 41 \text { time } \\ 0 & 1 & 0 & \text { Serially shift } 33 F 22 \text { times and clock } 33 F 42 \text { times } \\ 0 & 1 & 1 & \text { Serially shift } 33 F 23 \text { times and clock } 33 F 43 \text { times } \\ 1 & 0 & 0 & \text { Serially shift } 33 F 24 \text { times and clock } 33 F 44 \text { times } \\ 1 & 0 & 1 & \text { Parallel load } 33 F 2 & \\ 1 & 1 & 0 & \text { Not used } \\ 1 & 1 & 1 & \text { Not usea } \end{array}\right.$ |

Controls a decoder on $L 35$ which in turn performs one of the following functions


| F2-6 | Reset Display Storage Fifo on L33 |
| :--- | :--- |
| F2-7 | Enable shift out clock to CRT $\rightarrow$ SC Storage Fifo (31F11) |
| F2-8 | Reset 33 F4 (Binary to BCD converter) |
| F2-9 | Spare |


| F2-10 | Enable to load Display Storage Fifo with ram data |
| :---: | :---: |
| F2-11 | Enable to load Display Storage Fifo with multiplier results that are not in sequential order in the ram. Used with F2-10 |
| F2-12 | Load Rom 4 address register and reset rom output register bits $2^{0}-2^{9}$ |
| F2-13 | Advance Rom 4 address register |
| F2-14 | Load and advance Loop Counter A and reset rom output register bits $2^{0}-2^{9}$ |
| F2-15 | Load and advance Loop Counter B and reset rom output register bits $2^{0}-2^{9}$ |
| F2-16 | Load and advance Loop Counter $C$ and reset rom output register bits $2^{0}-2^{9}$ |
| F2-17 | Addresses multiplexer on L 35 which selects one of the following to test for a Rom 4 address skip |
| F2-18 F2-19 |  |
|  | ```O``` |
|  | 0 1 1 Test 30G6-0, l=decimal display, $0=0 c t a l$ display <br> 1 0 0 Test last word in display storage fifo - used <br>    for displaying Requested Multiplier Adaresses |
|  | $\begin{array}{\|llll} 1 & 0 & 1 & \text { Test for last non-sequential multiplier to be } \\ & & & \text { entered into the Display Storage Fifo } \\ 1 & 1 & 0 & \text { Test for update } \\ 1 & 1 & 1 & \text { Spare } \end{array}$ |

F2-20
F2-21
Controls what is to be transmitted per the following table


F2-23

Clock enable For $33 F 1$ buffer register
l=load register $x i t i n$ multiplier results before subtraction $0=1$ oad register with multiplier results after subtraction Allow LCA to je advanced by one each time a word is transmitted to CRT

## ABBREVIATIONS

| 1 | $3-S T$ | 3-STATE or TRI-STATE LOGIC |
| :--- | :--- | :--- |
| 2 | $\rightarrow$ | Goes to |
| 3 | ADR | Address |
| 4 | ADV | Advance |
| 6 | AR | Address Register |
| 5 | ANT | Antenna |

$1 \mathrm{~B} \rightarrow \mathrm{BCD}$ CONV Binary to Decimal Conversion
2 B $\rightarrow$ OCT CONV Binary to Octal Conversion
3 BD Board
5 BT Blanking Time
6 BUF Buffer

4 BOSS Boss Computer

| 4 | COMP | Comparator |
| :--- | :--- | :--- |
| 1 | CK | Check |
| 2 | CKT | Circuit |
| 3 | CLK | Clock |
| 5 | CONV | Conversion |
| 8 | CRT | Beehive Terminal |
| 9 | CTRL | Control |
| 6 | COPE A | Core A Computer |
| 7 | CORE B | Core B Computer |
|  | DEC | Decimal |
|  | DT | Dump Time |
|  | EA | Each |
|  | FIFO | First-in-First-out Memorm |

Table 6 (cont.)

|  | GEN | Generator |
| :---: | :---: | :---: |
|  | GR | Ground Return |
|  | I/O | Input/Output |
|  | INT | Integrators |
| 3 | LED | Light Emitting Diode |
| 5 | LSB | Least Significant Bit |
| 1 | L | Left |
| 2 | LC | Left Polarization Cosine |
| 4 | LS | Left Polarization Sine |
| 2 | MSB | Most Significant Bit |
| 3 | MULT (S) | Multiplier (s) |
| 4 | MUX | Multiplexer |
| 1 | M | Memory |
|  | NC | Normally Closed |
|  | NO | Normally Open |
| 1 | OBS | Observation |
| 2 | OCT | Octal |
| 4 | OSC | Oscillator |
| 3 | OR | Output Register |
|  | PROG | Program |
|  | PWR | Power |
| 2 | RC | Right Polarization Cosine |
| 9 | RS | Right Polarization Sine |
| 3 | RDY | Ready |
| 4 | REC | Receive or Receiving |
| 5 | REG | Register |

```
TABLE 6 (cont.)
```

| 1 | R | Right |
| :---: | :---: | :---: |
| 7 | RHVs | Reference High Limit of Vs |
| 8 | RLVs | Reference Low Limit of Vs |
| 6 | REQ | Requested |
| 1 | SAMP | Sampler |
| 2 | SC | System Controller |
| 4 | SEQ | Sequential |
| 5 | SM | System Monitor |
| 6 | SR | Shift Register |
| 7 | STOR | Storage |
| 3 | SxC | Sine x Cosine |
| 8 | SU | Start-Up Reset Pulse at Power On |
| 10 | SYNC | Synchronize |
| 9 | SW | Switch |
| 1 | TP | Test Point |
| 3 | TVs | Theoretical Value of Vs |
| 2 | TS | Temporary Storage |
|  | UAR/T | Universal Asychronous Receiver/Transmitter |
|  | WD (s) | Work (s) |
|  | X-DATA | Exchange Data |
|  | XMIT | Transmit |








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\.)
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```



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Enter the four sxc Multipiiers - Rammadreoses 12 to 1s.
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\mathrm{ 9. Enter the control word - Ram Nadreas}
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2. Enter theoretical vas value -
3. Set Rean nadress nogit teer to 0 .
4. Read fean worda $0-11$ tor display.
Do tho (ssc) - -va subtraction.







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 Fifo ols stopaes clock: 33F7-1

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