

VLA TECHNICAL REPORT #26

MODULE L12

L12 OFFSET MASTER

HARRY BEAZELL

September 1976

TABLE OF CONTENTS

| | <u>PAGE</u> |
|--|-------------|
| 1.0 Related Documents | |
| 1.1 NRAO Drawing Lists - None included | |
| 2.0 Functional Description | 1 |
| 3.0 Detailed Circuit Description | 1 |
| 4.0 Test and Adjustments | 2 |
| 5.0 Schematics and Block Diagrams included: | |
| 5.0.1 Block Diagram | 5-1 |
| 5.0.2 Module Schematic | 5-2 |
| 6.0 Data Sheets, etc. | |
| 6.1 CMP01 | 6-1 |
| 6.2 CD4001 | 6-3 |
| 6.3 Isotemp OCXO30-10 P.O. | 6-4 |

2.0 FUNCTIONAL DESCRIPTION

The L12 Module provides control circuits to phase lock an additional L₁, L₂ module at 600 MHz +19.2 Hz and a phase locked 5 MHz +19.2 Hz oscillator for distribution to all central station L14 and L9 modules.

3.0 DETAILED CIRCUIT DESCRIPTION

3.0.1 600 MHz +19.2 Hz

The short term stability requirements for the 600 MHz +19.2 Hz dictate a VCXO with characteristics equal to those of the reference 600 MHz. To this end, an additional L₁, L₂ module is used. The HP 10545A H37 5 MHz oscillator in the L1 module is mechanically offset to 5 MHz + $\frac{19.2}{120}$ Hz, which is well within its trim range. A +7 dBm level at J₄ is mixed with a 0 dBm level of the 600 MHz master at J₃, by a MIJ mixer. The resulting 19.2 Hz beat is low pass filtered by R₆ and C₃. A CMP01 is used as a zero crossing detector. Its output is differentiated by R₈ and C₄ and clipped and inverted by Q₂. The CRT/H signal (P₁₇) is differentiated and clipped by Q₁. These two outputs provide the Set/Reset inputs to a CD4001 latch, U₄.

The Q & \bar{Q} outputs of the latch are divided by R₁₀, R₁₁ and R₁₃, R₁₂ to limit the maximum excursion to +10V to the inputs of the ADP501 balanced integrator, U₈. The sensitivity of the latch as a phase comparator is 20V/360°. The gain of the HP 10543A H37 is between .02 and .04 Hz/V. This gives a loop gain, Kv = 48 to 96 Hz. The values used for R₁₄, R₁₇ and C₁₂, give a loop of about 5 rad. bandwidth and a damping factor of about 5. Resistor R₁₈ and the Zener diodes CR₁ and CR₂ prevent oscillation of the ADP501 due to cable capacity and limit the excursion of the VCXO. Pull in for errors within the loop bandwidth of 5 radians is less than a second. For errors of several Hz, pull in time may be quite long.

3.0.2 5 MHz +19.2 Hz

The 5 MHz offset is accomplished with only a slight difference in circuitry. The 5 MHz VCXO is board mounted in the L12 module. A DM8830N, U₃₁ dual differential line driver is used as an output buffer and as a differential driver to a SRA-1 mixer. This mixer is used in a differential mode to drive the CMP01 zero crossing detector. The remainder of the circuit is similar to the 600 MHz.

4.0 TEST AND ADJUSTMENT

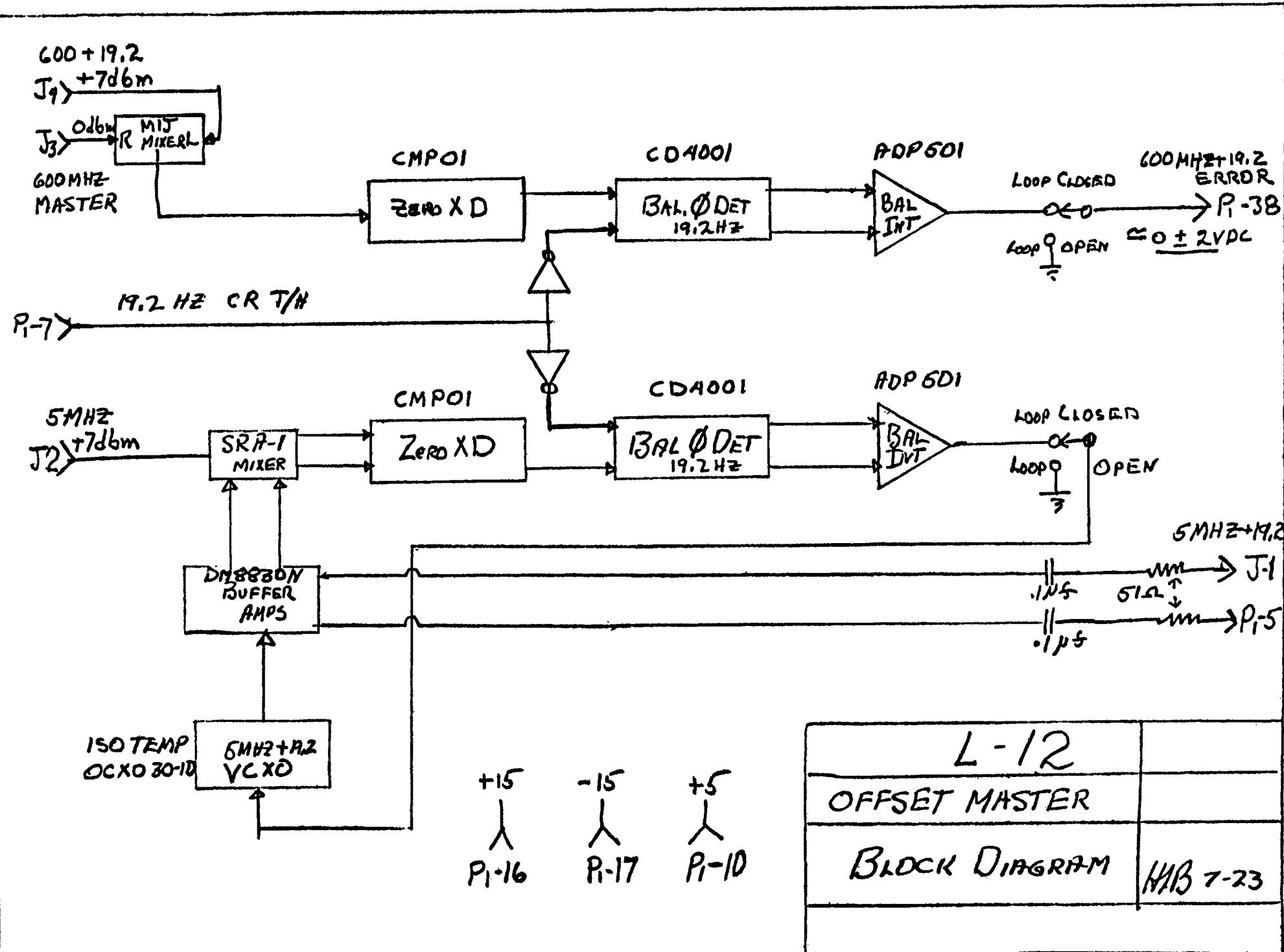
4.0.1 Initial Adjustment

4.0.1.1 600 +19.2

Plug in the L₁ and L₂ modules, if cold, allow 24 hours to stabilize. Place Ll2 on an extender. Set output switch to ground (Pos. 2). Set input monitor switch to view 600 MHz Ø error. Adjust Ll mechanical frequency to give a 19.2 Hz frequency. Sync scope to T/H or compare with T/H etc. Change switch to Pos. 1 (loop closed). Change monitor switch to 600 frequency error. The DC level should be set by adjusting L₁ to within +.5VDC. A 19.2 Hz sawtooth of about .1V peak-to-peak will be evident.

4.0.1.2 5 MHz +19.2

The 5 MHz oscillator requires about one hour to stabilize (a day is better). The adjustment is made in the same way as the 600 MHz. The 5 frequency error output sawtooth is about 1V peak-to-peak.



5.0.2 Module Schematic

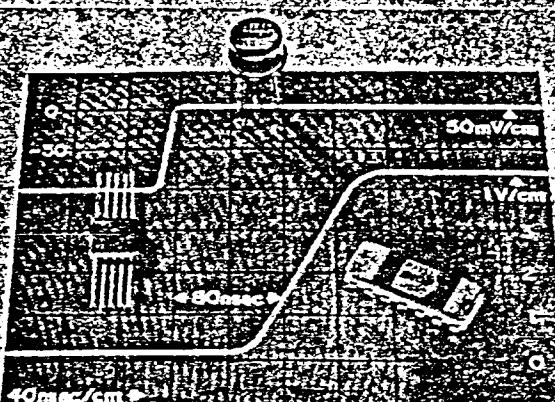
**Copy of schematic is in the envelope in the back of
this report.**

MONO CMP-01

FAST PRECISION COMPARATOR SERIES

FEATURES

- Fast Response Time
 - High Input Slew Rate
 - Low Offset Voltage
 - Low Offset Current
 - Low Offset Drift
 - High Output Current
 - Standard Power Supplies
 - Guaranteed Operation from Single +5V Supply
 - No Pull-up Resistor Required for TTL Drive
 - Wide GND Capacity
 - Fits 111-106-710 Sockets
 - Easy Offset Nulling
 - Easy to Use
- 90 ns typ - 150 ns max.
110 V/μs
- 0.3 mV typ, 0.8 mV max.
1 nA typ, 25 nA max.
1.0 μV/°C, 30 pA/°C
50 mA min.
- +5V to +18V



RESPONSE TIME WITH 5mV OVERDRIVE

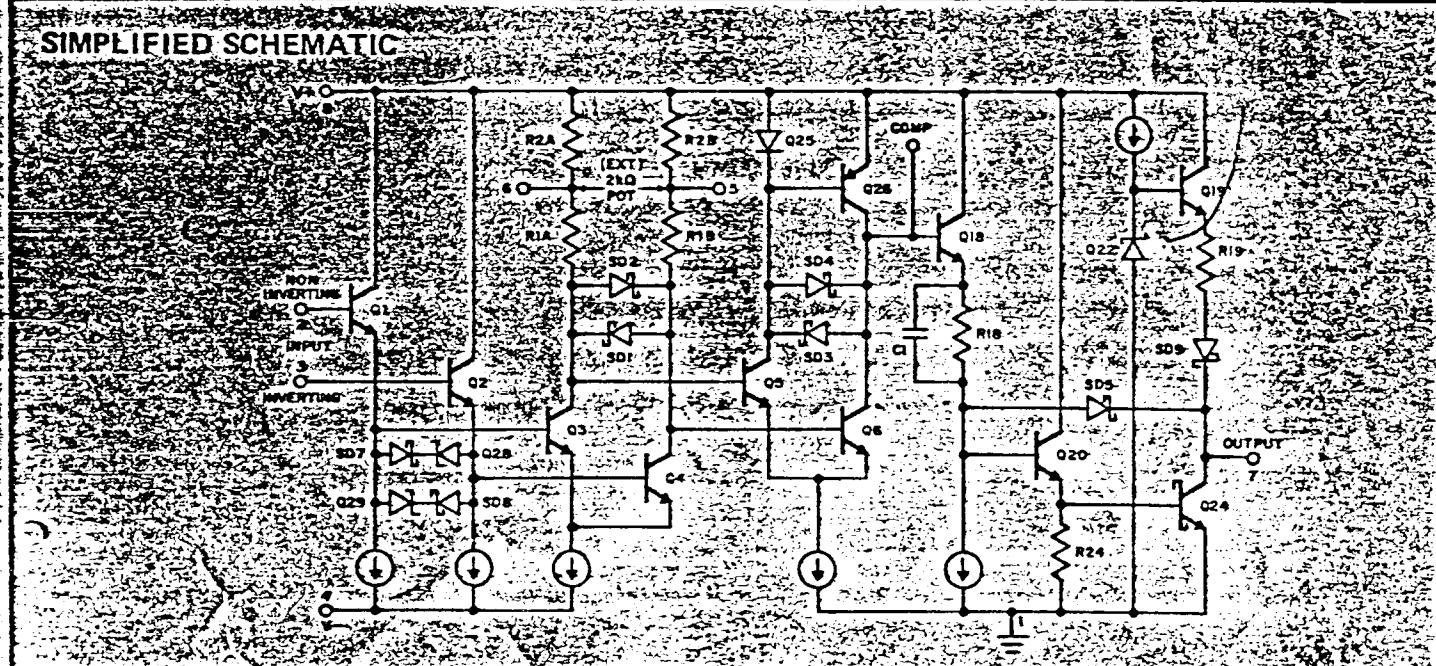
Single 2kΩ Pot
Free from Oscillations

GENERAL DESCRIPTION

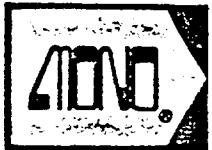
The monoCMP-01 is a monolithic Fast Precision Voltage Comparator using an advanced compatible NPN-Schottky Barrier Diode process. It features fast response time to both large and small input signals, while maintaining excellent input characteristics. The monoCMP-01 is capable of operating over a wide range of supply voltages, including single 5 volt supply

operation. The large output current sinking and high output voltage capability assure good application flexibility, while the combination of fast response, high accuracy, and freedom from oscillation assure performance in precision level detectors and 12 and 13 bit A/D converters. The monoCMP-01 is pin compatible to earlier 111, 106, and 710 types. For applications requiring lower input offset and bias currents, refer to monoCMP-02 data sheet.

SIMPLIFIED SCHEMATIC



All PRECISION MONOLITHICS products are guaranteed to meet or exceed published specifications.



**PRECISION
MONOLITHICS**
INCORPORATED

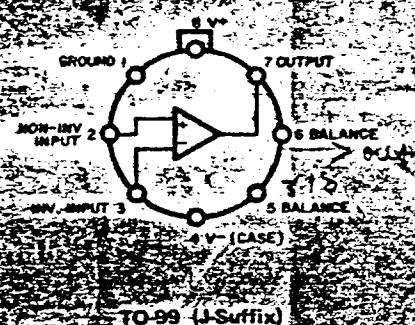
ABSOLUTE MAXIMUM RATINGS

| | | | |
|--|-------------|--|---------------|
| Total Supply Voltage, V+ to V- | 35V | Output Sink Current (Continuous Operation) | 75 mA |
| Output to Ground | -5V to +32V | Operating Temperature Range | -55 to +125°C |
| Output to Negative Supply Voltage | 50V | monoCMP-01 | 0 to 70°C |
| Ground to Negative Supply Voltage | 30V | monoCMP-01E, -01C | -65 to 150°C |
| Positive Supply Voltage to Ground | 30V | Storage Temperature Range | 300°C |
| Positive Supply Voltage to Offset Null | 0 to 2V | Lead Temperature (Soldering, 60 Sec) | Indefinite |
| Power Dissipation (See Note) | 500 mW | Output Short Circuit Duration — to ground | to V+ |
| Differential Input Voltage | ±11V | | 1 min. |
| Input Voltage (V _s = ±15V) | ±15V | | |

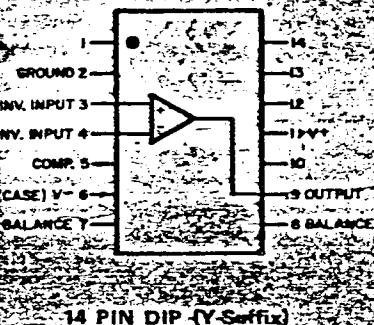
Note: Maximum package power dissipation vs. ambient temperature

| Package Type | Maximum Ambient Temperature for Rating | Derate Above Maximum Ambient Temperature |
|------------------|--|--|
| TO-99 (J) | 80°C | 7.1 mW/°C |
| Dual-in-Line (Y) | 100°C | 10.0 mW/°C |
| Flat (L) | 62°C | 5.7 mW/°C |

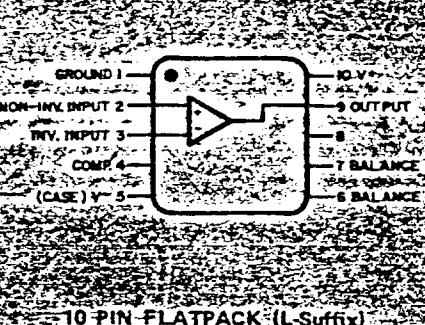
PIN CONNECTIONS (Top View)



TO-99 (J-Suffix)

ORDER: monoCMP-01J
monoCMP-01EJ
monoCMP-01CJ

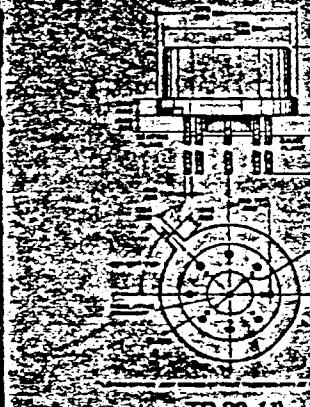
14 PIN DIP (Y-Suffix)

ORDER: monoCMP-01Y
monoCMP-01EY
monoCMP-01CY

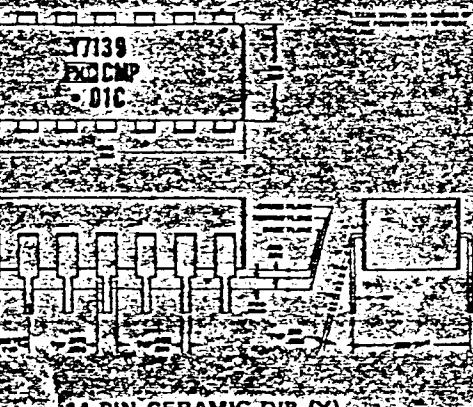
10 PIN FLATPACK (L-Suffix)

SPECIAL ORDER ONLY

PACKAGE DIMENSIONS



TO-99 (J)



14 PIN CERAMIC DIP (Y)



10 PIN METAL-CERAMIC FLATPACK

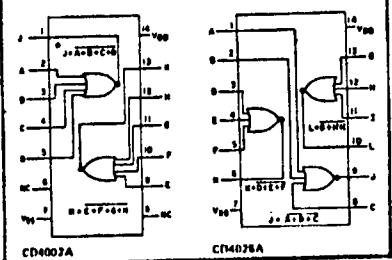
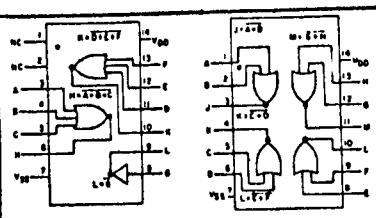
Digital Integrated Circuits

Monolithic Silicon

**CD4000A, CD4001A
CD4002A, CD4025A**
Types

COS/MOS NOR Gates (Positive Logic)

- Dual 3 Input plus Inverter CD4000AD, CD4000AE, CD4000AK
- Quad 2 Input CD4001AD, CD4001AE, CD4001AK
- Dual 4 Input CD4002AD, CD4002AE, CD4002AK
- Triple 3 Input CD4025AD, CD4025AE, CD4025AK



Special Features

- Medium speed operation. $t_{PLH} = t_{PHL} = 26 \text{ ns}$ (typ.)
at $C_L = 15 \text{ pF}$
- Low "high"- and "low"-level output impedance. 500Ω
and 200Ω (typ), respectively at $V_{DD} - V_{SS} = 10 \text{ V}$

The combination of these devices and the RCA NAND positive logic gate types CD4011A, CD4012A, and CD4023A can account for appreciable package-count savings in various logic function configurations.

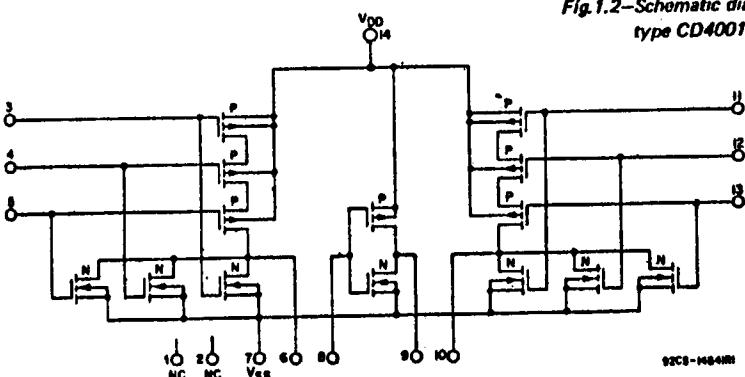


Fig. 1.1—Schematic diagram for type CD4000A.

For maximum ratings, see page 20.

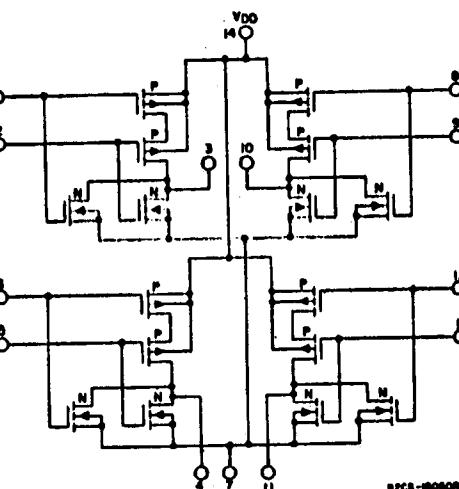


Fig. 1.2—Schematic diagram for type CD4001A.

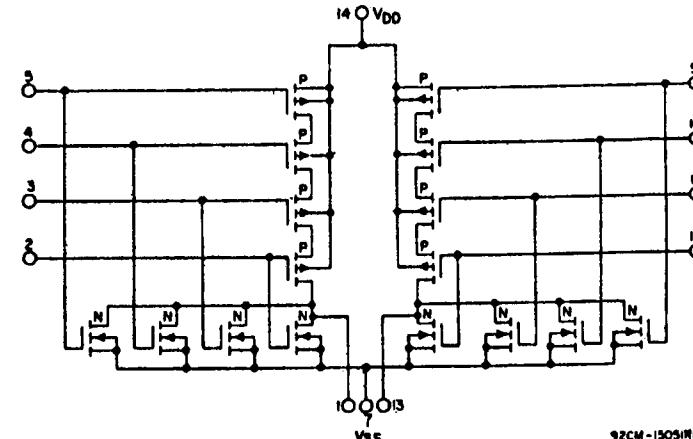


Fig. 1.3—Schematic diagram for type CD4002A.

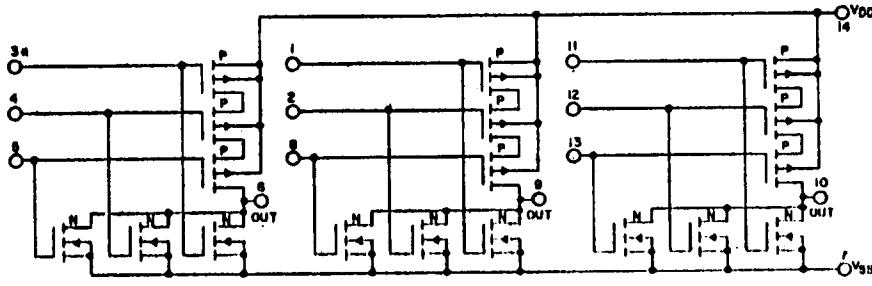


Fig. 1.4—Schematic diagram for type CD4025A.

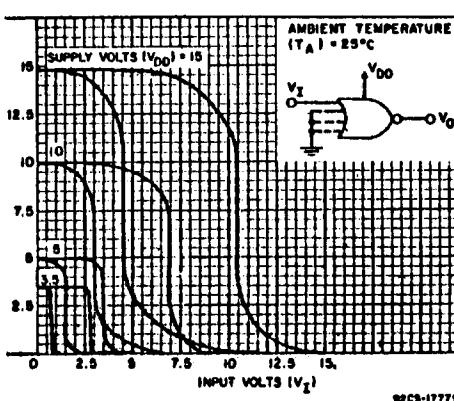


Fig. 1.5—Min. & max. voltage transfer characteristics.

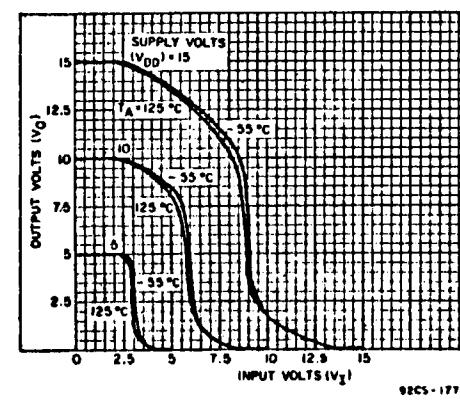


Fig. 1.6—Typ. voltage transfer characteristics as a function of temp.

PURCHASE
ORDER
NO. S 02010

SHEET 1 OF 1

DATE

July 22, 1976

PURCHASE ORDER

V
E
N
D
O
R

Isotemp Research, Incorporated
711 Henry Avenue
Charlottesville, VA. 22901

xx

S
H
I
P
T
O

XX

NATIONAL RADIO ASTRONOMY OBSERVATORY
RECEIVING DEPARTMENT
1000 BULLOCK BLVD.
SOCORRO, NEW MEXICO 87801

TELE 505-835-2924
TELEX 910-988-1710

NATIONAL RADIO ASTRONOMY OBSERVATORY
RECEIVING DEPARTMENT

2015 Ivy Road, Rm. 210

Charlottesville, VA. 22903

Att: Lloyd Tigner

| VENDOR BEST DELIVERY: | TERMS | TO POINT | TRANSPORTATION CHARGES | | | |
|-----------------------------|-------|----------|------------------------|--|--|--|
| N.R.A.O. REQUESTED DELIVERY | | | | | | |

| ITEM NO. | QUANTITY | SHIP DATE | DESCRIPTION | Vendor | UNPACKAGED | PACKED | QUANTITY RECEIVED | BACK ORDER |
|----------|----------|------------|---|--------|------------|----------|-------------------|------------|
| 1 | 2 | 8/30/76 | 1x 10 mhz oven stabilized crystal oscillator, F = 5,000 to 13.2 Hz. Voltage cont. + 1 Hz, stability 10 ⁻⁹ x 10 ⁻¹⁰ 1 day, Isotemp P/N OCXO-30-10 modified | | \$175.00 | \$350.00 | | |
| | | TOTAL----- | | | | \$350.00 | | |

CONFIRMING TELEPHONE ORDER ON 7/22/76. DO NOT DUPLICATE.

ACCOUNT NO.

492

PROJECT NO. 13210

R. F. Q. NO.

REQUISITION NO.

DELIVER TO

LOCATION

H.L. Beazell
2015 Ivy Rd., Rm. 210

N.R.A.O. TECHNICAL INSPECTION APPROVAL
REQUIRED BEFORE PAYMENT

YES NO

RECEIVING DEPT. MATERIAL RECEIVED
APPEARS TO BE IN GOOD CONDITION

YES NO

8

7

6

5

MONITOR
BNC
FP
SHN. POS. 0

MONITOR SWITCH-58

- 10 - 600 FREQ. ERROR
- 20 - 600 Ø ERROR
- 30 - 5 FREQ ERROR
- 40 - 5 Ø ERROR
- 50 - 600 F.FLIP
- 60 - 5 F.FLIP

7 THRU 9 NOT USED

+7 dbm. (600MHz) J4

0 dbm. (600MHz) J3

TP1

R7 10K

U1 MIU

C2 .1

R5 51

C3 1.0

R6 470

U2 CMPO1

C4 .01

-15V

Q2 2N3904

R8 10K

R9 1K

TP2

U4-CD4001

13 11

9 8

1 2 5 6 7

14 +15V

R10 110K ±1%

R11 220 ±1%

R12 10

C9 .01

U5 CMPO1

11 2

3 4

TP6

R35 10K

+15V

UG-SRA-1

7

R33 51

R34 51

C14 .1

R32 51

L2 1.0M

L3 1.0M

C15 .1

R31 51

C16 .1

R30 51

C17 .1

R29 51

C18 .1

R28 51

C19 .1

R27 51

C20 .1

R26 51

C21 .1

R25 51

C22 .1

R24 51

C23 .1

R23 51

C24 .1

R22 51

C25 .1

R21 51

C26 .1

R20 51

C27 .1

R19 51

C28 .1

R18 51

C29 .1

R17 51

C30 .1

R16 51

C31 .1

R15 51

C32 .1

R14 51

C33 .1

R13 51

C34 .1

R12 51

C35 .1

R11 51

C36 .1

R10 51

C37 .1

R9 51

C38 .1

R8 51

C39 .1

R7 51

C40 .1

R6 51

C41 .1

R5 51

C42 .1

R4 51

C43 .1

R3 51

C44 .1

R2 51

C45 .1

R1 51

C46 .1

R0 51

C47 .1

R1 51

C48 .1

R0 51

C49 .1

R1 51

C50 .1

R0 51

C51 .1

R1 51

C52 .1

R0 51

C53 .1

R1 51

C54 .1

R0 51

C55 .1

R1 51

C56 .1

R0 51

C57 .1

R1 51

C58 .1

R0 51

C59 .1

R1 51

C60 .1

R0 51

C61 .1

R1 51

C62 .1

R0 51

C63 .1

R1 51

C64 .1

R0 51

C65 .1

R1 51

C66 .1

R0 51

C67 .1

R1 51

C68 .1

R0 51

C69 .1

R1 51

C70 .1

R0 51

C71 .1

R1 51

C72 .1

R0 51

C73 .1

R1 51

C74 .1

R0 51

C75 .1

R1 51

C76 .1

R0 51

C77 .1

R1 51

C78 .1

R0 51

C79 .1

R1 51

C80 .1

R0 51

C81 .1

R1 51

C82 .1

R0 51

C83 .1

R1 51

C84 .1

R0 51

C85 .1

R1 51

C86 .1

R0 51

C87 .1

R1 51

C88 .1

R0 51

C89 .1

R1 51

C90 .1

R0 51

C91 .1

R1 51

C92 .1

R0 51

C93 .1

R1 51

C94 .1

R0 51

C95 .1

R1 51

C96 .1

R0 51

C97 .1

R1 51

C98 .1

IR SWITCH - S8

600 FREQ. ERROR

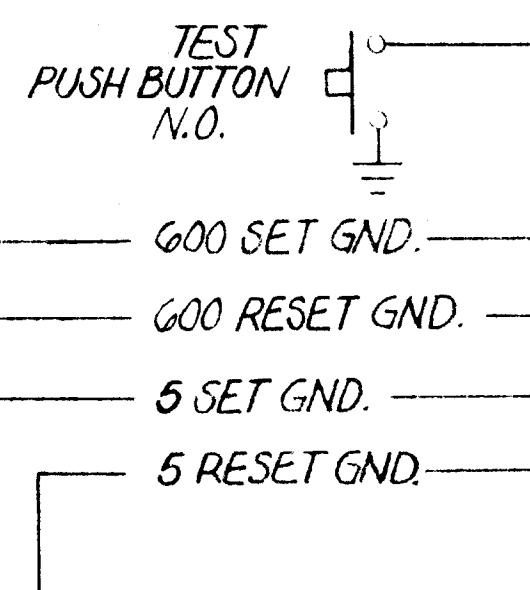
600 Ø ERROR

5 FREQ ERROR

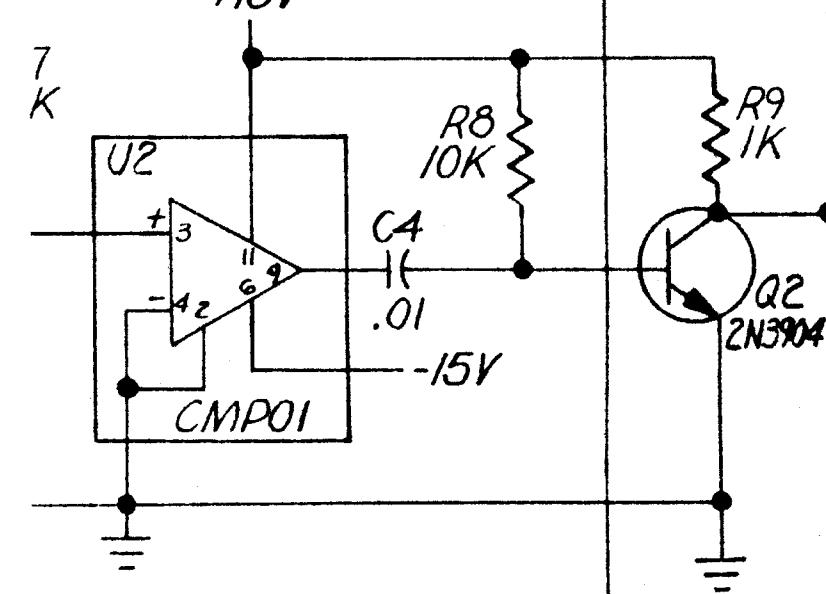
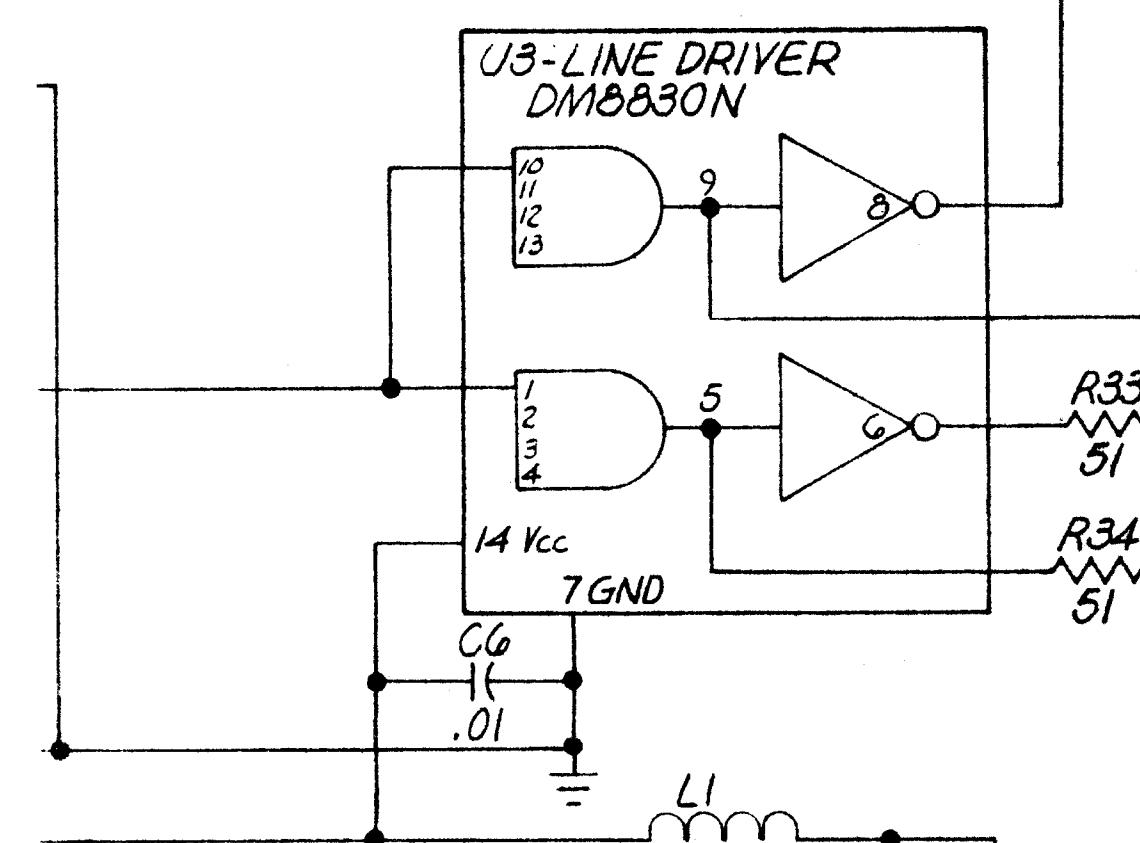
5 Ø ERROR

600 F.FLIP

5 F.FLIP



7 K

U3-LINE DRIVER
DM18830N

| C | U | Q | CR | L | S | TP |
|----|----|---|----|---|---|----|
| 26 | 10 | 4 | 4 | 5 | 3 | 7 |

COMPONENT DESIGN. USED

C U Q CR L S TP

26 10 4 4 5 3 7

UNLESS DIMEN

TOLERANCE

3 PLACE

2 PLACE

1 PLACE

MATERIA

FINISH:

NEXT ASSY

USED ON

J2 (+7dbm)
5MHz REF

3

6

5

4

3

2

1

0

-1

-2

-3

-4

-5

-6

-7

-8

-9

-10

-11

-12

-13

-14

-15

-16

-17

-18

-19

-20

-21

-22

-23

-24

-25

-26

-27

-28

-29

-30

-31

-32

-33

-34

-35

-36

-37

-38

-39

-40

-41

-42

-43

-44

-45

-46

-47

-48

-49

-50

-51

-52

-53

-54

-55

-56

-57

-58

-59

-60

-61

-62

-63

-64

-65

-66

-67

-68

-69

-70

-71

-72

-73

-74

-75

-76

-77

-78

-79

-80

-81

-82

-83

-84

-85

-86

-87

-88

-89

-90

-91

-92

-93

-94

-95

-96

-97

-98

-99

-100

-101

-102

-103

-104

-105

-106

-107

-108

-109

-110

-111

-112

-113

-114

-115

-116

-117

-118

-119

-120

-121

-122

-123

-124

-125

-126

-127

-128

-129

-130

-131

-132

-133

-134

-135

-136

-137

-138

-139

-140

-141

-142

-143

-144

-145

-146

-147

-148

-149

-150

-151

-152

-153

-154

-155

-156

-157

-158

-159

-160

-161

-162

-163

-164

-165

-166

-167

-168

-169

-170

-171

-172

-173

-174

-175

-176

-177

-178

-179

-180

