VLA TECHNICAL REPORT \#28
MODULE T1
MODEM
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### 1.0 GENERAL DESCRIPTION

The "Modem" T1 with its support module, the "IF Combiner" T2 provide a two-way communications system between the control building and each antenna.

The Modem along with the waveguide comprise a closed single sideband millimeter wave system which operates on various channels from 27.4 to 52.4 GHz .

The Modem is basically a millimeter wave/l-2 GHz up/down mixer with a phase locked local oscillator.

The signals to be transmitted are combined from other modules in the accompanying "IF Combiner" T2 module. This unit also distributes the l GHz to 2 GHz received Modem IF passband to various other modules, besides interfacing itself and the Modem to the local Digital Comunications System system.

The Modem system transmits "LO signals", used for electrical measurement of the waveguide length, and digital commands to each antenna. In turn, it receives "Lo signals", digital and analog monitor data, and the front end IF signals from each antenna. All are contained in a Modem IF passband from 1 to 2 GHz . Typical Modem IF passbands are shown in Figure 3-2, 3, 4.

Since there is one common waveguide run between all antennas on a given arm and the control building, the signals are frequency division as well as time division multiplexed. Each antenna position in a given array has a specific channel allocated to it. The channels are given in Figure 1-1. Each antenna modem transmits for 49 msec and receives for 1 msec . Each control building modem transmits for 1 msec and receives for 49 msec .

Because of the broad frequency range covered in the waveguide system, modems are built for specific channels only. Thus only modems of a specific channel are compatible. The modems used at the vertex rooms of the antennas are identical to those used at the control building and may be substituted upon proper adjustment of the receive level on the $T 2$ Module.

Since the T2 Module only operates with the l-2 GHz Modem IF passband, which is not influenced by a specific channel, all IF Combiner T2 Modules are interchangeable upon proper adjustment of the receive level.

| CHANNEL | LOCAL OSCILLATOR <br> FREQUENCY <br> $\mathrm{f}_{\mathrm{O}}, \mathrm{GHz}$ | SIGNAL BAND |  |
| :---: | :---: | :---: | :---: |
|  |  | LOW | HIGH |
| 1 | 26.41 | 27.41 | 28.41 |
| 2 | 28.79 | 29.79 | 30.79 |
| 3 | 31.21 | 32.21 | 33.21 |
| 4 | 33.59 | 34.59 | 35.59 |
| 5 | 36.01 | 37.01 | 38.01 |
| 6 | 38.39 | 39.39 | 40.39 |
| 7 | 40.81 | 41.81 | 42.81 |
| 8 | 43.19 | 44.19 | 45.19 |
| 10 | 45.61 | 46.61 | 47.61 |
| 11 | 47.99 | 48.99 | 49.99 |
|  | 50.41 | 51.41 | 52.41 |

### 2.0 THEORY OF OPERATION

Refer to the modem block diagram of Figure 2-1.
A. R. F. SUBASSEMBLY

The Modem Mixer is used in both transmit and receive, without any switching of diode bias voltages to improve performance in either of the two modes. Thus while performance may not be optimum, reliability is increased because of more mechanically stable diode mounts and because of the elimination of noise pickup on the bias line. Also since the diodes in the "Spacekom" mixers are in a standard sealed pill package, they are more rugged, easier to change, multi-sourced and may be easily replaced later by better devices as the state of the art improves. Two diodes are used in each mixer to provide a better 1 dB compression point in the transmit mode.

The mixers are purchased for individual waveguide channels with the upper sideband RF passband filter attached, since the electrical distance from the mixer to the filter is critical for image enhancement, and thus optimum performance.

Because of the requirements for a low VSWR to be presented to the waveguide system in both transmit and receive, a latching three port circulator with port 3 terminated is used as a two port isolator, and is placed between the mixer/filter combination and the waveguide system to isolate the mixer from the waveguide. This unidirectional device switches direction of propagation on the edges of the transmit/ receive pulse. Because it switches on the edges of the $T / R$ pulse, the $T / R$ pulse must be free of "bounce" or "transients" for reliable operation. A "synchronous debounce circuit" removes any transient noise or bounce from Sl, the front panel transmit/receive/auto switch and prevents the switch from interrupting the circulator $T / R$ pulse train until a complete cycle of transmit or receive has been obtained. This insures a long enough duration of $T / R$ pulse to enable the circulator to fully switch states, when $S l$ is thrown into either manual transmit or manual receive. However, this requires the $T / R$ pulse train to be present for operation of the switch.

The latching circulator changes states by applying a short duration current pulse to an internal hard iron core electro-magnet. Thus when power is removed to the circulator it will remain in whatever


FIGURE 2-1
state it was switched to prior to power removal. Because of the need to switch this inductive load, transients are induced into the wiring of the modem module. But since the modem system is allowed 100 microseconds to acquire a stable state after the T/R pulse, system operation is not affected.

The output of the circulator is coupled to the waveguide system through a waveguide extension (WR-28, $26.5-40 \mathrm{GHz}$, for Channels 1-6 and $W R-22,33-50 \mathrm{GHz}$, for Channels $7-10$ ). It should be noted that WR-19, $40-60 \mathrm{GHz}$, is used for all internal microwave components on Channels 7-10 except for the output side of the circulator and the waveguide extension. WR-22 was chosen for external waveguide runs because of its lower losses. The decision to use WR-19 for the Modem microwave components was arrived at before the decision on external rectangular waveguide runs.

A bidirectional IF port on the modem mixer is gated with the $T / R$ signal between a high 1 dB compression point transmit amplifier and a low noise receive amplifier. (A pin diode driver board interfaces the high current - high voltage requirements of both pin diode switches with the $T T L T / R$ signal.) This single pole double throw pin diode switch has high isolation, $\leq-60 \mathrm{~dB}$, between ports to minimize feedthrough of the transmit signal into the receive system. The high 1 dB compression point on the transmit amplifier of +17 dBm minimum permits the maximum modem output transmit power with minimal intermodulation to be dependent on the limiting factor of mixer diode capability $(\geq+5 \mathrm{dBm}$ at 1 dB compression) rather than on the transmit amplifier.

A level setting pad on the input to the transmit amplifier is custom selected for each modem to provide $\approx+1$ dBm output at the waveguide port for -6.5 dBm input at the transmit $I F$ input port, J16. Thus the +5 dBm minimum compression point of each modem mixer may be taken advantage of even though the amplifier gain and mixer conversion loss may vary.

A single pole single throw pin diode switch with -40 dB isolation and gated by the $T / R$ pulse is placed before the level setting pad to aid in preventing feedthrough of transmit signals into the receive system during receive. If the pad was placed before the pin diode switch, better passband ripple due to input VSWR and the long line of coaxial cable from $T 2$ to $T 1$ would be obtained. However, the transmit amplifier was found to oscillate when the

SPST switch on the input and the SPDT switch at the output were gated off. This problem, probably caused by higher input-output feedback due to the reactances presented to the amplifier with the switches off, could be prevented by placing the level setting pad between the SPST switch and the transmit amplifier's input, thus insuring a good match at the input under any condition and thus stable operation due to less feedback.

A low noise ( 3 dB maximum noise figure) $1-2 \mathrm{GHz}$ receive amplifier is placed at the other port of the SPDT pin diode switch. A noise figure budget is given in Figure 3-6.

## B. PHASE LOCKED LOCAL OSCILLATOR

A "Gunn" oscillator is used as the local oscillator for the modem mixer. No adjustment is provided for setting the power output ( $+17 \mathrm{dBm} \pm 1 \mathrm{~dB}$ ) of the Gunn oscillator. A voltage regulator for the Gunn oscillator includes current limiting and overvoltage crowbar circuits to protect the oscillator from damage in the event of accidental transients. The crowbar is used in conjunction with a 3 amp fuse mounted on the front panel of the module.

In order to maintain frequency stability the Gunn oscillator is voltage tuned and phase locked to signals derived from the external crystal controlled "LO" System. A 2400 MHz reference signal from the LO system is amplified by a $1-2 \mathrm{GHz}$ Avantek broadband amplifier (Avantek ASD-8199M) operated in saturation. The Avantek 1-2 GHz amplifier was chosen for this application rather than another amplifier built for 2.4 GHz because of several reasons. The amplifier still has good performance at 2400 MHz and as a general purpose $1-2 \mathrm{GHz}$ amplifier it is utilized in many other places in the VLA electronics system. Thus replacement is easier. And since the quantity purchased each year is greater it is also cost effective.

A 2400 MHz filter with a -3 dB bandwidth of 200 MHz is placed after the 2400 MHz filter for rejection of spurious frequencies.

Approximately +15 dBm of 2400 MHz carrier at the output of the filter drives a harmonic mixer diode to provide harmonics of 2400 MHz for mixing with the Gunn oscillator output to provide a 10 MHz difference signal for comparison with a 10 MHz reference signal in the modem phase locked loop circuit. The silicon Schottky
barrier diode (Aertech \#A2S123) is mounted in a combination waveguide coupler and diode mount providing 20 dB isolation from the output of the Gunn oscillator and a waveguide backshort tuning adjustment to provide some matching to the diode at the Gunn oscillator frequency in use. Some matching to the 10 MHz IF output and to the 2400 MHz reference input is provided by the harmonic mixer box attached to the SMA connector on the diode mount. No bias adjustment is used. Diodes may have to be hand selected for particular channels and diodes may have to be inserted in the mount in each of the two possible directions to optimize performance. The 10 MHz IF output, $\geq-50 \mathrm{dBm}$, is amplified by a video amplifier in the phase locked loop and is compared against a 10 MHz reference signal from the LO system by a modulo $4 \pi$ phasefrequency detector. A high gain integrator following the phase detector insures a high gain loop. Thus under all legitimate lock conditions the $I F$ and reference signals will be at $0^{0}$ phase difference. Therefore, a simple lock indication circuit can be utilized which is used to turn off the sweep voltage once phase lock is achieved and to indicate proper operation of the phase locked loop system.

Because the Gunn oscillator tuning range ( $\geq 200 \mathrm{MHz}$ ) and temperature drift are much larger than the $I F$ reference frequency ( 10 MHz ) it is necessary to implement a sweep system in the phase locked loop circuit to insure that the loop can acquire lock under worst case Gunn oscillator frequency drift conditions.

A sweep voltage from the timing capacitor of an internal astable multivibrator is added to the phase locked loop integrator output by use of a summing amplifier. Once the loop acquires lock the sweep voltage is removed from the summing amplifier and the loop remains in lock.

Control logic in the phase locked loop box permits a maximum of 8 two-way sweeps to acquire lock. If for some reason the loop cannot acquire lock the control circuitry will open the loop to the varactor and place a bias voltage on the varactor corresponding to the normal lock point for a time period corresponding to another 8 two-way sweeps ( $\approx 10$ seconds).

This "free run" condition serves as a back-up system to the phase locked loop and will permit momentary operation of the
digital control system through the waveguide as long as both modem's Gunn oscillators are within 25 MHz of each other. If during this period a "free run command" (open loop command) is received in the $T 2$ module's free run - search flip-flop, the modem phase locked loop will remain open and digital communications to the antenna can be utilized to diagnose the problem. Note that since a 53 second timer in the $T 2$ module will reset this free run - search flip-flop to the normal search condition, a continuous chain of free run commands, at least one every 53 seconds must be issued.

If no free run command is received by the $T 2$ module, the "search" condition will cause the module to continuously alternate between sweep cycles and free run periods until lock is obtained. A free run - auto - search switch on the front panel of Tl may be used to manually set the loop into either mode for test purposes. This switch has priority over the incoming command from T2.

Because the free run function permits digital communications only if the two modem's Gunn oscillators are within 25 MHz of each other's frequencies, the Gunn oscillators must be manually set to frequency after the modem has reached operating temperature in the rack. This can be done with a screwdriver adjustment on the Gunn oscillator itself, and should be checked periodically for drift.

### 3.0 MODULE SPECIFICATIONS AND POWER LEVELS

Refer to Figure 3-1 for modem system levels. Note that even though the front end "IF" signals are not transmitted by the control room modem, the total power output in full transmit is the same as that from the vertex room modem, +1 dBm . This is accomplished by an increase in the LO signal levels arriving at the $T 2$ transmit input port. Thus full advantage is taken of the modem mixer's 1 dB compression point. Modem RF passbands at the waveguide, and $1-2 \mathrm{GHz}$ Modem IF passbands at the transmit input port and receiver output port, are given in Figures 3-2, 3, and 4 respectively. Note that in the case of a l-2 GHz spectrum, front end IF powers are given in a 300 KHz bandwidth to be convenient for use with a spectrum analyzer. In the case of a waveguide passband, front end IF powers are given in a 50 MHz total individual IF bandwidth, for ease of use with a power meter.

Worst case passband amplitude variations are given in Figure 3-5, and a noise figure budget is given in Figure 3-6. The noise figure budget does not include effects of intermodulation on the 50 MHz noise passbands. Third order intermod on all four IF signals will produce in band products which will raise the level of the noise floor.



VERTEX ROOM (Total Power $\approx+1 \mathrm{dBm}$ )


CONTROL ROOM (Total Power $\approx+1 \mathrm{dBm}$ )

FIGURE 3-2: Tl RF TRANSMIT PASSBAND AT WAVEGUIDE (Discounting Passband Ripple)


VERTEX ROOM (Total Power $=-6.5 \mathrm{dBm}$ )


CONTROL ROOM (Total Power $\approx-6.5 \mathrm{dBm}$ )


CONTROL ROOM (Total Power $\approx-26.5 \mathrm{dBm}$ )
@ 56 dB WG Loss

| Tl Passband Amplitude Variation in Re |  |
| :--- | :--- |
| Component | Worst Case Variation |
| Latching Circulator | $\pm 0.3 \mathrm{~dB}$ |
| Mixer/Filter | $\pm 0.5$ |
| SPDT Switch | $\pm 0.4$ |
| Receive Amplifier |  |
|  |  |
|  | Total |
|  | $\pm 1.7 \mathrm{~dB} *$ |

Tl Passband Amplitude Variation in Transmit
Component Worst Case Variation Spec
SPST Switch $\pm 0.3 \mathrm{~dB}$

Fixed Attenuator
$\pm 0.4$
Transmit Amplifier $\quad \pm 0.5$
SPDT Switch $\pm 0.4$
Mixer/Filter $\quad \pm 0.5$
Latching Circulator $\pm 0.2$
Total $\pm 2.3 \mathrm{~dB}$ *
*NOTE: Total worst case passband variations do not include
variations due to connections or reflection coefficients
of individual components.

COMPONENT
Waveguide Extension
Latching Circulator
s-. 5 dB Loss
<-. 6 dB Loss
Mixer/Filter $\leq 11.8 \mathrm{~dB}$ N.F. with $\leq 4.0 \mathrm{~dB}$ IF N.F.
SPDT Switch $\leq-.8 \mathrm{~dB}$ Loss
Receive Amplifier $\leq 3 \mathrm{~dB}$ N.F.
$\therefore$ IF noise figure $=3.8 \mathrm{~dB}$ maximum which
is less than 4.0 dB .
$\therefore$ Total noise figure $=$ noise figure of mixer/filter plus losses.
$\therefore$ Total noise figure $\leq 12.1 \mathrm{~dB}$

SIGNAL/NOISE CALCULATIONS
IF Transmit Level/IF $=-6 \mathrm{dBm} / 50 \mathrm{MHz}$
Waveguide Loss $=56 \mathrm{~dB}$ Maximum
$\therefore$ Received signal $=-62 \mathrm{dBm} / 50 \mathrm{MHz}$
Noise power in $50 \mathrm{MHz}=\mathrm{KTB}=-97 \mathrm{dBm} / 50 \mathrm{MHz}$
Noise figure $=12 \mathrm{~dB}$
$\therefore$ Total noise power $=$ NKTB $=-85 \mathrm{dBm} / 50 \mathrm{MHz}$
$\therefore$ Signal/noise ratio $=23 \mathrm{~dB}$ less any intermodulation
Lo Transmit Level/LO Carrier $=-8 \mathrm{dBm}$
Waveguide Loss $=56 \mathrm{~dB}$ Maximum
(Control $\quad \therefore$ Received signal $=-64 \mathrm{dBm} /$ Carrier
Room Noise power in $300 \mathrm{KHz}=\mathrm{KTB}=-119 \mathrm{dBm}$
Receive) Noise figure $=12 \mathrm{~dB}$
$\therefore$ Total noise power $=$ NKTB $=-107 \mathrm{dBm} / 300 \mathrm{KHz}$
$\therefore$ Signal/Noise ratio $=43 \mathrm{~dB} / 300 \mathrm{KHz}$ less any intermodulation
LO Transmit Level/LO Carrier $=-2 \mathrm{dBm}$
(Vertex $\quad \therefore$ signal/noise ratio $=49 \mathrm{~dB} / 300 \mathrm{KHz}$ less any intermodulation
Room
Receive)
A. VOLTAGE REGULATOR

Refer to the voltage regulator schematic of Figure 4-1.
An input voltage of +15 VDC is applied to the regulator through the front panel "Gunn supply" crowbar fuse. To prevent the crowbar circuit from firing when power is first applied, resistor R19 and capacitor $C 4$ slow the input power-on transient with a time constant of $75 \mu \mathrm{~s}$.

The crowbar circuit uses a 723 precision voltage regulator chip, Ul to perform a voltage comparison function between the regulator output voltage, sampled through $R 6$, and the voltage set pot, R10. If the output voltage should happen to rise $17 \%$ above the normal regulated voltage value, then the comparator output at $V_{z}$ will go high and provide gate current to silicon controlled rectifier, CRI. CRI will then conduct, shorting the input of the regulator and blowing the front panel "Gunn supply" fuse, thus preventing damage to the Gunn oscillator.

The $V_{Z}$ output (series zener diode from the output of the 723 comparator) is used to insure that no SCR gate current flows when the comparator output is low. Resistor $R_{1}$ is used to limit the current flowing into the SCR gate when the comparator goes high.

Diode CR2 and R7 in the positive feedback loop of the 723's fast comparator latches the comparator into the switched high state, insuring that the SCR will fire even on very short transients.

Voltage regulation is provided by another 723 regulator chip, U2, in conjunction with a series pass transistor Q1, adequately heat sunk to the module left side plate. Connections to the series pass transistor as well as all other voltage regulator board connections are made through a 14 pin IC socket - platform assembly. One might question the use of such a socket at the high current levels of the pass transistor. However, a test run with a +15 VDC supply, current limited to 1 amp, through a single pin resulted in a contact resistance degradation from 4.2 milliohms to only 5.0 milliohms with 500 power-on insertions.

The reference voltage for the voltage regulator is derived from its own internal zener reference. At approximately 7.15 VDC the voltage set potentiometer provides a range of 4.0 to 7.15 VDC

to the crowbar circuit and a range of +3.4 to +6.1 VDC to the reference input of the voltage regulator comparator.

This $17 \%$ tracking of voltages is performed by providing a voltage divider with $R 2$ and $R 3$ to reduce the voltage regulator reference by $17 \%$ relative to the crowbar reference. This is important to protection of the Gunn oscillator since required unit to unit supply voltages vary over a wide range depending on the Gunn waveguide channel in use.

Caution: Because of this wide range of Gunn supply voltages, leave the Gunn oscillator power supply lead unsoldered until the voltage set pot has been adjusted for the particular Gunn in use. Similarly, disconnect the Gunn supply wire from the Gunn before changing voltage regulator boards, and reapply power to the Gunn oscillator only after this adjustment has been made.

The current limit function is also handled by the voltage regulator chip, U2, in conjunction with resistors R15 through R18, R23 and R24. R15 through R18 form a $0.25 \Omega 1$ watt resistor to provide a voltage $=\frac{1}{4} \times$ output current. This voltage is supplied to the crowbar current sense transistor's base to emitter junction by resistive divider R23 and R24. When this voltage rises to $\mathrm{V}_{\text {BESAT }}$ ( $\approx .7 \mathrm{VDC}$ ) the current will be held to a constant level. With the resistor values shown on the schematic, this will occur at $\approx 2.5$ amperes which is greater than the maximum turn-on current required for the Gunn oscillator.

The voltage across Rl5 through R18 is also used as a DCS monitoring point for Gunn current. Unity gain buffer amplifiers U3A and U3B with isolating resistors R12, R14, R20, and R21 provide a differential output corresponding to .25 volts/amp to the $T 2$ interface logic board. Thence, another buffer amp with a gain of 4 normalizes the Gunn current monitor voltage to 1 volt/amp single ended before transmission to the DCS analog mux system. The $T 2$ buffer amp utilizes resistors $R 20$ and R21 on the $T 1$ voltage regulator board to provide the proper gain ratio.

Buffer amplifier U3A also provides a Gunn voltage monitor point through R22 to the T2 interface board.

The voltage output of the regulator is shunted by a $180 \mu \mathrm{Fd}$ 6VDC tantalum capacitor to prevent the output from overshooting the normal operating voltage when the load is instantaneously removed. This overshoot is due to the slow response time of the voltage regulator.

One output of the regulator is connected directly to the Gunn oscillator supply input. However, another output is applied to the phase locked loop Gunn supply varactor voltage clamp to prevent the varactor voltage (referenced to the Gunn supply voltage in the Gunn oscillator) from biasing the varactor into conduction and possibly destroying it. A fixed voltage in the phase locked loop box can not be used for the clamp voltage because of the wide range of Gunn supply voltages used.

## B. SYNCHRONOUS DEBOUNCE CIRCUIT

Refer to the Synchronous Debounce Schematic of Figure 4-2.
The purpose of the synchronous debounce circuit is to interface the Xmit/Auto/RCV switch to the $T / R$ line for both $T 1$ and $T 2$ in such a manner as to switch states synchronously with the normal $T / R$ clock pulses. Thus the minimum width of the $T / R$ pulses to the latching circulator is maintained in spite of the asynchronous timing of manually throwing the Xmit/Auto/RCV switch. Also any noise or bounce from the switch is removed.

This action is necessary from the standpoint of the latching circulator which is an edge triggered device and could easily end up in a random state in the manual mode if the Xmit/Auto/RCV switch were connected directly to the $T / R$ input.

A dual three position on-on-on toggle switch is used for the front panel Xmit/Auto/RCV function. One half of the switch is wired to indicate whether the switch is in a manual state. When the switch is in either manual Xmit or RCV, the "auto warn" LED lights, indicating an abnormal condition. This auto warn signal from the LED also triggers a set-reset flip flop in the $T 2$ module sending a high TTL "auto warn" signal to the DCS analog multiplex monitor system. Thus any tampering of either of the two modem $T 1$ switches can be indicated to the telescope operator.

The other half of the Xmit/Auto/RCV switch interfaces to the synchronous debounce circuit. An on-on-on toggle switch can be wired as a single pole - three position switch. However, because some of the states overlap as the switch is changed in position, it is difficult to debounce. Therefore, the three states of the toggle switch shown on the top of Figure 4-2 are decoded first into three "break before make" outputs by nor gates $\mathrm{U} 2 \mathrm{a}, \mathrm{U} 2 \mathrm{~b}$ and U 2 d . These

gates are used as "and" gates.
In order to debounce the switch, two flipflop storage elements are required. Ula and $U l b$ are used as a set-reset flip-flop to debounce the $(X M T) \leftrightarrow(R C V)$ information. And U4a is also wired as a set-reset flip-flop to debounce the (XMT or RCV) $\leftrightarrow$ (Auto) information. The "or" function in the latter case is performed by "nor" gate, U2c.

Now that the switch is debounced the interruption of the $T / R$ pulse train can be made synchronous with the pulse train by use of D-type flip-flop U4b and a "and-or" select gate consisting of U3b, U3c and U3d. The and-or select gate is used to select either the $T / R$ input pulse train or the switch $X M T-R C V$ information to the $T / R$ output line. The selection of either input is made synchronous with the $T / R$ pulses by applying the $T / R$ pulse train to the clock input on D-type flip-flop, U4b.

The $T / R$ input (from a line driver in L8) is terminated in $50 \Omega$ on the synchronous debounce card by $R 6$ to prevent glitches caused by pulse reflection at the $T / R$ input.

An inverted $T / R$ output is provided by Ulc for easier interfacing to the rest of the $T 1$ sub-assemblies.

## C. PIN DIODE DRIVER

Refer to the pin diode driver schematic of Figure 4-3.
The purpose of the pin diode driver board is to interface the TTL transmit/receive signal from the synchronous debounce board to both pin diode RF switches in the modem $T l$ module. The pin diode switches require a $\pm 50 \mathrm{~mA}$ at 1 volt constant current source in conduction as well as in cut-off, depending on the polarity of the individual switch. Therefore the pin diode driver actually consists of two independent drivers of opposite polarity relative to the incoming $T / R$ signal.

An AD518 high slew rate operational amplifier is used as a comparator to convert the TTL input signal to a voltage swing to approximately each 15 VDC supply rail. The reference input of the comparator is biased to a voltage (1.4 VDC) near the median voltage of worst case TTL input levels (. 8 VDC maximum low and 2.0 VDC minimum high). R4 and R9 are used to stabilize the comparator.

Because of the high current requirements ( 50 mA ) of the pin diode switches, the outputs of the comparators are buffered by complimentary symmetry amplifiers Q1, Q3 and Q2, Q4. Resistors R5, R6, R10 and Rll

limit the output current to the pin diode switches to 50 mA . The emitter follower complimentary amplifier was chosen for its stability. The output voltage swing of this system is adequate at the RF power levels used in the pin diode switches.
D. PHASE LOCKED LOOP

Refer to the schematic of Figure 4-4 and block diagram of Figure 4-5.

## 1. IF VIDEO AMPLIFIER

The signal from the harmonic mixer at $\geq-50 \mathrm{dBm}$ must be amplified to a level compatible with that of the digital phase detector. A video amplifier is required to prevent erroneous lock points on subharmonics of the 10 MHz reference signal.

The beat note produced by the nth harmonic of 2400 MHz mixing with the Gunn diode output in the harmonic mixer is not a pure sinusoid. Because the harmonic mixer diode is not a perfectly square law device harmonics of the beat note will also appear in the output. If the beat note happens to be at a subharmonic of the 10 MHz reference frequency (say 5 MHz , for example) then a component at 10 MHz will exist at the input of the IF amplifier. If a narrow band filter at the 10 MHz reference frequency were placed at the input of the IF amplifier, then a 10 MHz signal would appear at the output and the phase detector could treat it as a proper 10 MHz signal and the loop could lock onto it, even though the beat note occurred at 5 MHz .

In order to prevent this ambiquity from occurring, one would think that the IF amplifier low frequency cutoff must occur at less than one half the reference frequency. This would permit at least some component of all possible subharmonics ( $f_{\text {ref }} \div 2, \div: 3, \div 4$, etc.) to be passed on to the phase-frequency detector. A low frequency component would then offset the output of the detector and prevent any erroneous lock point.

However, the low frequency cutoff given above assumes that the harmonics of the beat note gradually decrease in amplitude with frequency. This is usually not true, and certainly would be difficult to control. Since many low order harmonics of the beat note may be lacking in amplitude, a video amplifier with a very low frequency cutoff is required.


FIGURE 4-4


FIGURE 4-5: PHASE LOCK UNIT BLOCK DIAGRAM

In the actual video amplifier used, a coupling capacitance of $.1 \mu \mathrm{Fd}$ and a load resistance of $51 \Omega$ leads to a low frequency -3 dB point of $\approx 30 \mathrm{KHz}$. This is given by,

$$
f_{-3 A B}=\frac{1}{2 \pi R C}
$$

Therefore, the probability of false locking on a subharmonic is negligible.

Another requirement placed on the IF amplifier is that the output waveform be of constant amplitude over the input signal dynamic range to interface properly to the phase detector. Either a limiting amplifier or an AGC controlled amplifier is required.

A limiting amplifier was chosen in this application because of the dependence on waveform duty cycle of the lock indicator, which is not an edge-triggered device like the phase detector. A differential amplifier chip such as the CA3012 (Ul) can provide symmetrical limiting because the transistors never swing into saturation. And with symmetrical limiting the output duty cycle will remain at $50 \%$ over a wide dynamic range on the input.

Because the limiting action will provide harmonics of the harmonic mixer beat note, the output of the limiting amplifier must also have a video passband response as explained earlier.

The video amplifier ideally should have a high frequency -3 dB point of twice the reference frequency. If the noise power is assymetric with the reference frequency, the edge-triggered phase-frequency detector will interpret the noise power as a frequency error and lock will be more difficult to acquire under weak signal conditions.

The CA3012 has a high frequency -3 dB point of about 8 MHz with a $1000 \Omega$ load resistance, much too low for optimum performance. However, the signal to noise ratio at the input to the IF amplifier is high enough to permit satisfactory operation. A single CA3012 also does not have enough gain to limit on its own input noise power, a requirement for an optimum phase locked loop threshold. But again, the signal level presented to the input of the IF amplifier is adequate for this application.

An extra unity voltage gain 2N5l79 power amplifier stage, Q1, was added to the output of the CA3012 to permit driving a
$75 \Omega$ load composed of the IF monitor isolation resistors, R17 and R18, and the IF comparator bias resistors, R23 and R24. The voltage gain of unity is obtained by the ratio of the collector load resistance to the emitter resistance. A common emitter amplifier with emitter degeneration was chosen instead of an emitter follower to maintain an output waveform duty cycle of 50\%. The 2N5179 collector voltage is obtained from the +5 volt supply to minimize power dissipation. However, this places a restriction on peak to peak output voltage swing of about 1 VPP for maintenance of the duty cycle.
2. COMPARATOR/LEVEL SHIFTERS

Two identical comparator circuits consisting of $84, Q 5$ and Q2, Q3, interface the $I F$ video amp and 10 MHz reference input $A C$ signals of 1 VPP to the TTL inputs of the lock indicator "nand" gate. The comparators are high gain wide bandwidth differential amplifier pairs which produce $\approx 0$ to 2.5 VDC output swing TTI signals. These output signals are interfaced to the ECL inputs (1 VPP @ 3.75 VDC ) of the phase/frequency detector by level shifting networks consisting of R49, R22, C13 and R21, R19, C14.

An offset voltage of approximately .1 VDC is introduced on the inputs of each comparator by bias resistors R28 and R47. This bias voltage insures that the comparator outputs are low in absence of input signals. Thus the lock indicator gate is forced to indicate an out of lock condition in case of absence of signal in the IF amplifier or at the 10 MHz reference source. The duty cycle of the input signals will be modified slightly by this offset.
3. PHASE DETECTOR

The Motorola MCl2040 modulo $4 \pi$ ECL phase/frequency detector was chosen because of its ability in a swept phase locked loop to permit lock at only one IF sideband, as well as being immune to locking to IF frequencies that are harmonics or subharmonics of the reference frequency. This eliminates the additional circuitry needed to require a unique lock point for the Gunn oscillator when a quadrature phase detector is used. The effect of the phase-frequency detector on the Gunn frequency in the harmonic mixing scheme actually used in the modem phase locked loop is diagrammed in Figure 4-6.



```
    f
                                    to Phase Detector
    Nf
        Oscillator Frequency at
        Harmonic Mixer
Gunn Frequency }=>\mathrm{ Output Frequency of Gunn
                    Oscillator at Harmonic Mixer
    Region }\quad=>\mathrm{ One of }8\mathrm{ Unique Initial Conditions
        That the Gunn Oscillator Frequency
        Can Occupy Relative to the nth
        Harmonic of the 2400 MHz Local
        Oscillator Frequency
    Lock Point= Frequency at Which the Gunn
        Oscillator Will Phase Lock to
        the nth Harmonic of the 2400 MHz
        LO Frequency Plus or Minus the
        10 MHz Reference Frequency,
        Depending on the Position of the
        Sideband Select Switch. In This
        Example, an Upper Sideband, (Odd
        Channel), Has Been Selected
    Instability
    Point }\quad=>\mathrm{ Frequency at Which the Gunn
                                    Frequency Will Remain in an
                                    Unstable Condition, If The
                                    Gunn Frequency Previously
                                    Occupied Either Region 1 or 2
```

        FIGURE 4-6: Page 2
    The horizontal arrows show the directions in which the Gunn oscillator's frequency is forced, for given initial conditions. This action may be readily derived from the IF passband response (what is actually presented to the detector) for the mixing scheme used. The passband response is critical to this analysis, since an out of band signal (no signal present) will appear to the phase detector as an IF signal that is lower in frequency than the reference signal. Therefore the phase detector will force the Gunn oscillator higher in frequency, resulting in the response of the top diagram.

Note that an instability point occurs at the edge of the lower sideband passband response in the top diagram. Because of this instability and the directions of Gunn oscillator frequency pull for the various initial conditions, a sweep system in which the Gunn oscillator is forced to be pulled into regions 3,4 or 5 (the only initial conditions in which a stable lock point can occur) is required. Since the bandwidth of operation of the IF amplifier and phase detector is less than the worst case frequency drift of the Gunn oscillator, the sweep system described later operates over the full tuning range of the Gunn oscillator.

The gain of the MCl2040 phase detector is approximately . 16 volts/radian.
4. INTEGRATOR

For a discussion of phase locked loops, refer to Phase Lock Techniques by F.M. Gardner (John Wiley and Sons, Inc., New York, 1966).

A second order high gain integrator was chosen for the loop filter to insure a $0^{0}$ phase difference between the 10 MHz IF and reference frequencies at lock. Thus a simple lock indicator can be designed using this principle to control the sweep logic.

Because a forced sweep is required for this system the loop parameters were chosen for best lock acquisition rather than low noise.
$Y$
Measurements on a number of Gunn oscillators indicated an average varactor gain of $27.3 \mathrm{MHz} /$ volt at the operating frequency.

$$
\begin{aligned}
\therefore K_{\mathrm{O}}= & \left(27.3 \mathrm{MHz} / \text { vol } t \cdot(2 \pi \text { radians } / \mathrm{Hz})=172 \times 10^{6}\right. \text { radians/volt } \\
& \text { where } \mathrm{K}_{\mathrm{O}}=\text { the } \mathrm{VCO} \text { gain constant for the } \mathrm{MCl} 2040 . \\
\mathrm{K}_{\mathrm{d}}= & .16 \text { volt/radian where } \mathrm{K}_{\mathrm{d}}=\text { the phase detector gain } \\
& \text { constant. }
\end{aligned}
$$

For best lock acquisition it is desirable to have as large a loop natural frequency $\left(\omega_{n}\right)$ as possible. However, practical considerations of loop stability permit a nominal loop bandwidth of 40 KHz .
$\therefore \omega_{\mathrm{n}}=(40 \mathrm{KHz}) \cdot(2 \pi$ radians $/ \mathrm{sec} \cdot \mathrm{Hz})$
$\omega_{\mathrm{n}}=2.51 \times 10^{3}$ radians $/ \mathrm{sec}$
Also for best lock acquisition a damping factor ( $\zeta$ ) of 2 was chosen. (Gardner, p. 48)

A differential integrator of the form shown below is required for compatibility with the phase detector.


Where $\tau_{1}=R_{1} C$ and $\tau_{2}=R_{2} C$ from eqn (2-10) (Gardner, p. 9),
$\left.\omega_{\mathrm{n}}=\frac{\mathrm{K}_{0} \mathrm{~K}_{\mathrm{d}}}{\left(\tau_{1}\right.}\right)^{\frac{1}{2}}$
$\zeta=\frac{\tau_{2}}{2}\left(\frac{K_{0} K_{d}}{\tau_{1}}\right)^{\frac{1}{2}}$
or,
$\tau_{1}=\frac{K_{0} K_{d}}{\omega_{n}^{2}}=4.35 \times 10^{-4} \mathrm{sec}$
$\tau_{2}=\frac{25}{\omega_{n}}=1.59 \times 10^{-5} \mathrm{sec}$

$$
\begin{gathered}
\text { Let } C=.033 \times 10^{-6} \mu \mathrm{Fd} \\
\therefore \mathrm{R}_{1}=13.2 \mathrm{~K} \Omega \\
\mathrm{R}_{2}=482 \Omega
\end{gathered}
$$

Because the very narrow correction pulses of the MCl2040 phase detector may not be integrated by the amplifier, an RC filter is imbedded in the integrator input resistor network as shown below.


The time constant of this network as recommended by the Motorola MC4044 (similar to the MCl2040) data sheet (p.9) should be given as below.
$\omega_{c} \approx 5 \omega_{\text {nmax }}$

Where $\omega_{\text {nmax }}=$ the maximum loop natural frequency encountered over the varactor control voltage range.

Measurements on a number of Gunn oscillators indicated a maximum varactor gain of $\omega_{n \max }=4.8 \times 10^{5}$ radians/sec. Therefore $\omega_{c}=24 \times 10^{5}$ radians/sec. From the Motorola MC4044 data sheet (p. 9),

$$
\begin{aligned}
\omega_{c} & =\frac{4}{R_{1} C_{c}} \\
c_{c} & =\frac{4}{R_{1} \omega c} \\
\therefore c_{c} & =126 \mathrm{pF}
\end{aligned}
$$

Therefore, in choosing practical component values,

$$
\begin{aligned}
& \frac{\mathrm{R}_{1}}{2} \approx 6.8 \mathrm{k} \Omega \\
& \mathrm{R}_{2} \approx 470 \Omega \\
& \mathrm{C} \approx .033 \mu \mathrm{Fd} \\
& \mathrm{C}_{\mathrm{c}} \approx 120 \mathrm{pF}
\end{aligned}
$$

These values are shown on the schematic of Figure 4-4.
5. SWEEP CIRCUIT

A sweep oscillator consisting of an op amp comparator circuit (U5b), and timing capacitor (C42 in conjunction with C43) is used to provide both a ramp voltage for addition to the integrator output voltage, and a clock for the logic circuit timing.

The comparator functions as an astable oscillator by charging the timing capacitor to the comparator's switching point determined by resistors R 50 and R52. When the capacitor's voltage reaches this point the comparator switches state and begins charging the capacitor in the opposite direction. Thus a ramp voltage is produced on the timing capacitor, and a clock signal can be derived from the comparator's output by utilizing a voltage clamp circuit (R57, D3, and D4) to interface to the TTL input of counter U9.

The ramp voltage from the timing capacitor is applied directly to the summing amplifier U6 through resistor R 32 . The ratio of this resistor value to the input resistor from the integrator output, R41, insures that the sweep will be able to swing the varactor voltage over its entire range independent of the integrator output voltage.

The ramp voltage can not be removed instantaneously from the summing amplifier input, when the loop achieves lock, since the magnitude of this change, depending on lock point, could produce enough of a frequency change to throw the loop out of lock.

However, it is also desirable to have the sweep input decay to zero after lock to take advantage of the entire varactor tuning voltage range. Therefore, the sweep is removed by opening the timing capacitor charging resistor, R51, with FET switch UlO. The timing capacitor then discharges slowly through R32 to zero since pin 2 of $U 6$ is at virtual ground. Since this time constant, is 10 times longer than the normal sweep time constant, the loop
can follow the discharge.
One disadvantage to this sweep system is the additional noise voltage introduced into the loop by R32.

For any resistor,

$$
\begin{aligned}
& P_{n}= \operatorname{KTB} \\
& \text { Where } P_{n}=\text { Noise Power } \\
& K=\text { Boltzmann's constant } \\
& T=\text { Temperature } \\
& B=\text { Bandwidth } \\
& V_{n}=\sqrt{P_{n} R} \\
& \text { Where } V_{n}=\text { Noise voltage } \\
& R=\text { Resistance }
\end{aligned}
$$

Therefore, the resistor values on the summing amplifier should be minimized to the point where the input noise power of the amplifier dominates.

Unfortunately the sweep system requires a larger resistance to maintain the sweep time constant, since the summing amplifier input resistance is always placed across the timing capacitor, and limits its voltage swing. Therefore, the schematic component values represent a compromise between these two requirements.

Since individual Gunn oscillators vary considerably in varactor gain constants, the gain of the summing amplifier can be varied by selecting the value of the feedback resistor R48 for stable operation. The overcompensation network of R62 and C44 insure op amp stability over a wide range of gain values.
6. VARACTOR CLAMP AND FREE RUN BIAS SET

The Gunn oscillators are built with the varactor diode referenced to the positive Gunn supply voltage. In order to take advantage of the full tuning range available, the varactor voltage must be permitted to swing from the positive Gunn supply voltage to the negative 15 volt supply rail of the integrator.

Since the Gunn supply voltage varies over a 3 to 6 VDC range and the varactor must not be forced into hard conduction, a diode voltage clamp consisting of D7 and R7 prohibit the varactor voltage from exceeding the Gunn supply voltage.

A bias voltage near 0 VDC must be applied to the varactor
input when the loop is opened by FET switch Ul0 in the free run backup mode. This is accomplished by adding $R 8$ to the varactor clamp circuit. In the free run mode,


$$
\begin{aligned}
& I=\frac{V_{G u n n}+15-.7}{10 K+27 \mathrm{~K}} \\
& V_{V A R}=-15+I \cdot 27 \mathrm{~K} \\
& \therefore V_{V A R}=.73 V_{G u n n}-4.6
\end{aligned}
$$

Where,

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{VAR}}=\text { Varactor Voltage in Free Run } \\
& \mathrm{V}_{\text {Gunn }}=\text { Gunn Power Supply Voltage }
\end{aligned}
$$

7. LOCK INDICATION CIRCUIT

A simple lock indication circuit can be formed using a nand gate and comparator, when the phase difference between the IF and reference signals is zero.



In the actual circuit, however, the IF and reference comparators introduce an assymmetry in the input waveforms due to the comparator input offset voltage that is provided to pull each TTL nand gate input low in the absence of signal. (If either input is low, then the nand gate output is high, insuring
an out of lock indication.) This assymmetry along with the limited output swing of the TIL nand gate change the actual circuit in-lock voltage to about 2.8 VDC and the out of lock voltage to about 3.7 VDC.

A schottky TTL nand gate, U7a, is used as the lock indicator. A $220 \Omega$ pull up resistor ( R 36 ) is necessary on the output to minimize temperature drift of the output voltage swing, to maximize the output voltage swing, and to provide a low resistance to the RC low pass filter to produce equal decay and rise times.

The RC low pass filter of R37 and C46 accomplishes two functions. One is to average the output pulse waveform of the THL gate to obtain a DC level which can be used as a lock indication. For this function the time constant would have to be long enough to filter out 10 MHz but short enough to indicate a locked condition before the sweep voltage pulled the loop out of lock.

However, the time constant must also be long enough to prevent the lock indicator from indicating a locked condition, when a low frequency beat note is produced between the signal and a harmonic or subharmonic of the reference frequency. This beat note will produce a w a veform on the output of the nand gate, indicating a false lock with each low going pulse. Therefore, the -3 dB rolloff should be less than the free running short term drift of the Gunn oscillator. The components selected are a compromise between these three factors.

A comparator (U5a) is used to convert the lock indication voltage swing into a TTL level by comparison with a reference voltage provided by R53. This reference voltage should be set midway between the in-band out-of-lock voltage and the in-lock voltage, 2.25 VDC.

A voltage clamp circuit consisting of R38, D1, and D2 provide a TTI compatible output signal to the control logic system.
8. LOGIC

Refer to the PLL control circuit timing diagram of Figure 4-7.
When the loop drops out of lock for any reason, the logic circuit applies a charging current through $R 51$ to the timing capacitor, thus starting the sweep oscillator. The sweep voltage from the timing capacitor is simultaneously applied to the summing amplifier input and the loop remains closed.

The sweep oscillator also applies a clock pulse to $\mathbf{a} \div 16$


FIGURE 4-7: PLL CONTROL CIRCUIT TIMING DIAGRAM
binary counter, U9. If the loop can not achieve lock in 8 counts of the sweep oscillator, the "search" period, then the loop is opened for another 8 counts, the "free-run" period. During the free-run period a bias voltage is applied to the Gunn oscillator varactor input which is equal to the normal operating voltage when the loop is closed. If each modem's Gunn oscillator is within 25 MHz of its normal operating frequency, then it is possible to exchange digital information with the remote antenna. If a free fun command is received once every 53 seconds at the $T 2$ module, the loop will remain open, and further diagnostic checks may be made. If no command is received, the logic will continue to cycle between search and free-run states until lock is obtained.

A phase locked loop truth table on Figure 4-4 explains more completely this operation of the control logic. Note that the logic will immediately go into the search mode upon a change of the free run input to the search state (low). Thus if the T2 module is plugged into the rack, or if the free run/auto/search switch is brought to the search position, or if a search command is received, the logic will immediately go into the search mode. This convenience function is performed by resistor R56 and capacitor C24 which form an edge-triggered pulse generator at the input to $\mathrm{U7b}$.
9. MONITOR BUFFERS

Both the integrator output and the varactor control line are buffered from the monitoring system by $U 4 a$ and $U 4 b$ to prevent external noise from appearing on these two noise sensitive monitoring points. Note that $a \div 2$ resistive divider is required on each op amp input to prevent latch-up when the monitor voltage approaches either supply rail.

## E. MODEM WIRE HARNESS

The wire harness of Figure 4-8 shows the interconnections of the various subassemblies described previously. Note that all four incoming power supply lines are filtered and that the internal +5 VDC buss is generated by a voltage regulator on the +15 VDC incoming power supply line. This was necessary because of the wide voltage variations and noise on the rack +5 VDC buss.

5.0 FRONT PANEL INDICATORS AND CONTROLS

Refer to Figure 5-1.

## Auto Warn IED

Lights when either front panel switch is removed from the automatic position.

## Free Run LED

Lights when either the phase locked loop cycles to the free run condition during a free run/search period, or when the free/auto search front panel switch is placed in the free-run position, or when a free-run command is received. Lock Warn LED

Lights when the Gunn oscillator phase locked loop has lost lock. Numeral

Indicates the waveguide channel number (1-11) of the particular modem. Only modems with the same channel number may be substituted. Varactor Meter

Indicates the voltage applied to the varactor input of the Gunn oscillator with a full scale reading of $+15 / 0 /-15$ VDC. Under normal operation, or when the loop is in free-run, the meter should read approximately 0 VDC. If the loop is in search, and cannot find lock, the meter should sweep with a period of approximately $l^{\frac{1}{2}}$ seconds between the Gunn supply voltage ( +3 to +6 VDC) and approximately -15 VDC. RCV/Auto/XMT Switch

Permits the modem to be placed in full receive or transmit. Since this switch has priority over the transmit/receive timing from L8, it must be placed in the auto position for normal operation. Free/Auto/Search Switch

Permits the modem phase locked loop to be placed in free-run (loop open) or to be placed in search (loop closed) irrespective of the free-run command input from T2. If the modem has been in free-run and the switch is thrown to search, the phase locked loop should immediately start search/free-run cycles. Under normal conditions the loop should lock within one search period, $\leq 1.5$ seconds. Since this switch has priority over the free-run command input from T2, it must be placed in the auto position for normal operation.

Gunn Supply Fuse
A 3 amp fuse supplying +15 VDC to the Gunn voltage regulator
board. This fuse will blow with the regulator over-voltage crowbar.
If the modem does not appear to transmit, nor receive, nor lock, check this fuse.

INT OUT BNC Connection
Monitors the output of the phase locked loop integrator, before the summing amplifier and Gunn supply clamp, through a buffer amplifier with a voltage gain of $\frac{1}{2}$. If the loop is locked it should read $* 0$ VDC. If the loop is unlocked it should read $\approx \pm 7$ VDC. 10 MHz REF BNC Connector

Monitors the external 10 MHz reference input to the phase locked loop board, and should be checked with a spectrum analyzer for power level ( $\geq-8 \mathrm{dBm}$ ) if the loop can not achieve lock.

## 10 MHz IF BNC Connector

Monitors the IF passband at the output of the phase locked loop IF amplifier, and should be checked with a spectrum analyzer set for a high sweep rate of $5 \mathrm{MHz} / \mathrm{div}$., if the loop can not achieve lock. This permits one to see the IF being swept in the search mode. In lock, this signal should read -8 dBm at 10 MHz .


1. Check power supply distribution wiring with ohmmeter. (Refer to drawing. no. Dl3440P11.)
2. With Gunn supply voltage wire and varactor coaxial cable disconnected from Gunn Oscillator, connect the test set to the module.
3. Apply proper power supply voltages to the test set.
4. Set sideband select switch on the phase locked loop board to proper setting for modem channel in use. (Refer to drawing no. Cl3440S3.)
5. Set lock indicator reference voltage pot to 3.25 VDC at pin 2 of U5 on phase locked loop board. (Refer to drawing no. Cl3440P2.)
6. Set the voltage set potentiometer (R10) on the voltage regulator board for the output voltage specified on the Gunn Oscillator case, using a digital voltmeter.
7. Disconnect module from test set and solder Gunn supply voltage wire onto the oscillator.

Caution: Never connect this wire until the voltage has been set on the voltage regulator board for the particular Gunn Oscillator in use. Permanent damage can result if this voltage is too high.
8. Reconnect test set to the module, and throw free/auto/ search switch to search.
a. Module should begin search/free-run cycles as indicated by the varactor meter sweeping for about 13 seconds and then resting near zero for approximately 13 seconds. The varactor meter should sweep from the Gunn supply voltage to about - 14 VDC.
b. Confirm that the voltage on the varactor output port, J5, of the phase locked loop box does not swing above the Gunn supply voltage.
c. The auto warn and lock warn LEDs should remain on.
d. The free-run LED should light when the varactor meter rests near zero.
9. Only if the voltage on the varactor port has been confirmed to not swing above the Gunn supply voltage, connect the varactor coaxial cable to the varactor port, J5, on the
phase locked loop box.
Caution: Never connect this cable until this has been checked out. Permanent damage can result to the oscillator if the varactor voltage rises above the Gunn supply voltage.
10. Apply reference signals to the $T 1$ modules.
a. 2400 MHz at -5 dBm to J4.
b. 10 MHz at +10 dBm to J14.
11. Throw free/auto/search switch momentarily to free then back to search.
a. Lock warn LED should extinguish within one complete sweep of the varactor meter.
12. Attach Spectrum Analyzer to 10 MHz IF port, and observe the wide band noise floor relative to the 10 MHz carrier with the video filter on.
a. The signal to noise ratio should be a minimum of 50 dB in a 300 KHz analyzer bandwidth.
b. Optimize the signal to noise ratio by varying the harmonic mixer backshort and by placing the harmonic mixer diode in each of the two possible directions in the harmonic mixer diode mount.
c. In the case of a channel 7-10 modem also vary capacitor Cl in the harmonic mixer mount for best signal to noise ratio.
d. Note that all of these adjustments interact.
13. Observe the close-in noise floor ( $\leq 1 \mathrm{MHz}$ from carrier) with an analyzer resolution of less than 10 KHz per division. a. If the noise floor peaks on each side of the carrier, change the varactor gain adjust resistor, $R 48$, on the phase locked loop board until a flat frequency response is obtained.
A. Connection of T1 and T2 to TEST SET

1. Proper power supply voltages must be connected to the TEST SET.
2. Reference signals, 2400 MHz and 10 MHz , must be connected to the Tl.
a) 2400 MHz at -5 dBm to J4.
b) 10 MHz at +10 dBm to J 14 .
3. Place TEST SET switches in the following positions.
a) ADDRESS SELECT switches up.
b) Sl in LOCAL.
c) S 2 in CONTROL ROOM.
d) S 3 in AUTO.
4. Place both Tl switches in AUTO.
a) All LED's on Tl should be out.
5. Momentarily close S9, RESET.
a) All LED's on TEST SET should be out.
B. Control Function Checkout
6. Select "l" with ADDRESS SELECT switches (S4 down, free run command).
7. Momentarily close S8, STROBE.
a) FREE RUN and LOCK WARN LED's on TEST SET and Tl should light.
8. Select "O" with ADDRESS SELECT switches (all switches up, search command).
9. Momentarily close S8, STROBE.
a) All LED's on Tl should go out.
10. Momentarily close S9, RESET.
a) All LED's on the TEST SET should go out.
11. Select "l" with ADDRESS SELECT switches (S4 down, free run command).
12. Momentarily close S8, STROBE.
a) FREE RUN and LOCK WARN LED's on TEST SET and Tl should light.
13. After approximately 53 seconds, FREE RUN and LOCK WARN LED's on Tl should go out.
14. Momentarily close S9, RESET.
a) FREE RUN and LOCK WARN LED's on TEST SET should go out.
15. Place XMIT/RCV switch (S1) on Tl to either XMIT or RCV.
a) AUTO WARN LED's on TEST SET and Tl should come on.
16. Place XMIT/RCV switch on $T 1$ to AUTO.
a) AUTO WARN LED on Tl should go out.
17. Momentarily close S9, RESET.
a) AUTO WARN LED on TEST SET should go out.
C. Monitor Function Checkout
18. Starting with test set SUB MUX ADDRESS SELECT switches at " 0 " (all switches up), select each address, "O" through "15", and compare TEST SET Meter, MI, reading with the following table.

SUB MUX ADDRESS SELECT TEST SET METER READING ( $100=10$ VDC)
"0"
1

2
3
4
5
6
7

8

9
10
11
12
13
14
15

0
$\approx+100$
$\approx+100$
0
0
0
0
$\approx 0$ (should $=1.5 \times$ Tl varactor meter reading)
$\approx 0$
+30 to +60 (should $=T 1$ Gunn Volt)
$\approx+10$ (should $=T 1$ Gunn Current)
0
0
+40 (TTL High)
+40 (TIL High)
+40 (TML High)
2. Select "7" with ADDRESS SELECT switches (S7 down). Remove

10 MHz reference signal from Jl4, Tl.
a) TEST SET Meter, M1, should alternate from $\approx+25$ to $\approx-75$.
b) LOCK WARN LED's on TEST SET and Tl should light.
c) After $\approx 15$ seconds, FREE RUN LED should light.
3. Reconnect 10 MHz reference signal to Jl4, Tl.
a) Momentarily throw FREE RUN/SEARCH switch to FREE RUN, then back to SEARCH.
b) LOCK WARN LED on TI should go out within one complete sweep of the meter voltage.
c) TEST SET Meter, M1, should read $\approx 0$.
4. T1 FREE RUN/SEARCH switch to AUTO, momentarily close S9, RESET.
a) All LED's on TEST SET should go out.
5. Select "2" with ADDRESS SELECT switches (S5 down, monitor reset command).
6. Momentarily close S9, STROBE.
7. Select addresses "13", "14" and "15" in turn. TEST SET Meter, M1, should indicate $\approx 0$ (TTL Low) for these three steps.
D. RF Calibration Procedure (Tl)

NOTE: This procedure can be accomplished in conjunction with the above or as a separate check using a Tl only.

1. TEST SET switches are set according to step A3.
a) If $T 2$ is not connected, $S 3$ must be set to LOCKED.
2. Set up Test Oscillator for -6.5 dBm at 1.5 GHz and connect to Jl6 on rear panel.
3. Connect Waveguide Power Meter to waveguide.
a) Power Meter should be set for +5 dBm full scale.
4. Set front panel switch, Sl, to XMIT.
a) Power Meter should read +1 dBm . (This level can be adjusted as required by changing attenuator pad in transmit input line.)
5. Connect Spectrum Analyzer to Jl5 on rear panel.
6. Connect Noise Tube to waveguide.
7. Set front panel switch, Sl, to RCV.
8. Two traces should be stored on the Spectrum Analyzer. One with Noise Tube off and one with Noise Tube on. The difference should be $\approx 8 \mathrm{~dB}$ and should not vary over displayed spectrum.
NOTE: The Spectrum Analyzer should be set up as follows:

| Center Freq | $=$ | 1.5 GHz |
| :--- | :--- | :--- |
| Bandwidth | $=$ | 300 KHz |


| Scan Width | $=$ |
| :--- | :--- |
| Input Atten | $=100 \mathrm{MHz} / \mathrm{Div}$. |
| Scan Time | $=0 \mathrm{~dB}(.1 \mathrm{mw})$ |
| Log Ref Level | $=$ |
| Lin Sensitivity | $=-30 \mathrm{sec}$. |
| Video Filter | $=0 \mathrm{~dB}$ |
| Scan Mode | $=100 \mathrm{~Hz}$ |
| Switch | $=$ |
| Scan Trigger | $=10 \mathrm{~dB}$ Log |
| Storage | $=$ |

Scan is produced by depressing Single Scan Mode Switch.

### 8.0 MODEM MEASUREMENTS

An example of the output signal at the 10 MHz IF port is given in Figure 8.1. Note the close-in noise floor ( $\leq 1 \mathrm{MHz}$ from carrier) created by the summing amplifier in the phase-locked loop. Several small noise spikes from the transmit-receive pulses appear in this passband.

Transmit and receive switching times for T2-Tl combinations appear in Figures 8-2 and 8-3. Note that the transitions occur well within the maximum $100 \mu \mathrm{sec}$ switching time specification, and yet do not bounce.

Complete RF amplitude and phase passband measurements for a system of IF combiners and modems are given in Figures 8-4 through 8-11.


- 0 dBm @ top line with $10 \mathrm{~dB} /$ Division
- 10 MHz center frequency with $1 \mathrm{MHz} /$ Division
- 300 KHz bandwidth with 300 Hz video filter
- Module TlDlo in lock


```
TOP TRACE - \overline{T/R Input Pulse}
        (Vertical 2 Volts/Div)
        (Horizontal 0.5 \muS/Div)
BOTTOM TRACE - Detected Transmit Output
        Level at Waveguide
        (Vertical 2mV/Div)
        (Horizontal 0.5 \muS/Div)
MODULES USED - T2B5 and TlDl2 (phase locked)
```



TOP TRACE - T/R Pulse
(Vertical l Volt/Div)
(Horizontal $0.5 \mu \mathrm{~S} / \mathrm{Div})$
BOTTOM TRACE - Detected Receive Output
At T2-J8
(Vertical 50mV/Div)
(Horizontal $0.5 \mu \mathrm{~S} / \mathrm{Div}$ )
MODULES USED - TlDl4 (phase locked) and T2B5



$T 1011 \xrightarrow{560 B} T 1 D 14$


FIGURE 8-8: PASSBAND RESPONSE



FIGURE 8-10: PASSBAND RESPONSE


9.0 DIGITAL COMMUNICATIONS SYSTEM ADDRESS ASSIGNMENTS

Address assignments for the modem T1 - IF Combiner T2 system are given in Figures 9-1 and 9-2. Note that the monitor addresses are different for the vertex room and control room, and that the interface to the DCS system for both modules occurs in the $\mathbf{T} 2$ module.

| MODEM T1 - IF COMBINER T2 MONITOR POINTS VERTEX ROOM DATA SET NO. 2 |  |  |
| :---: | :---: | :---: |
| Octal Address | Monitor Point | Voltage |
| 40 | Ground | 0 VDC |
| 41 | Temperature Monitor No. 1 | 0.1 VDC $/{ }^{\circ} \mathrm{C}, 0 \mathrm{VDC} \rightarrow 0^{\circ} \mathrm{C} *$ |
| 42 | Temperature Monitor No. 2 | $0.1 \mathrm{VDC} /{ }^{\circ} \mathrm{C}, 0 \mathrm{VDC} \rightarrow 0^{\circ} \mathrm{C}$ * |
| 43 | Ground | 0 VDC |
| 44 | Ground | 0 VDC |
| 45 | Transmit IF Power | 5 VDC Nominal |
| 46 | Received IF Power | 5 VDC |
| 47 | Varactor | ~0 VDC, 1 VDC $\Rightarrow 2$ VDC |
| 50 | Integrator Output | $\sim 0 \mathrm{VDC}, 1 \mathrm{VDC} \Rightarrow 2 \mathrm{VDC}$ |
| 51 | Gunn Oscillator Voltage | 3 to 6 VDC |
| 52 | Gunn Oscillator Current | $\sim 1 \mathrm{VDC}, 1 \mathrm{VDC} \Rightarrow 1 \mathrm{Amp}$ |
| 53 | Ground | 0 VDC |
| 54 | Mixer Voltage | 0 VDC |
| 55 | Auto Warn | *O VDC THTL High $\Rightarrow$ ON |
| 56 | Free Run Warn | zO VDC TTL High $\Rightarrow$ ON |
| 57 | Lock Warn | $\approx \mathrm{O}$ VDC TWTL High $\Rightarrow$ ON |

*when connected.

```
MODEM T1 - IF COMBINER T2 COMMANDS
    VERTEX ROOM DATA SET NO. 2
```

Octal Address
360
361
362

Command
Search
Free Run
Monitor Reset

MODEM T1 - IF COMBINER T2 MONITOR POINTS
CONTROL BUILDING DATA SET NO. 5

| Octal Address | Monitor Point | Voltage |
| :---: | :---: | :---: |
| 120 | Ground | 0 VDC |
| 121 | Temperature Monitor No. 1 | $0.1 \mathrm{VDC} /{ }^{\circ} \mathrm{C}, 0 \mathrm{VDC} \rightarrow 0^{\circ} \mathrm{C} *$ |
| 122 | Temperature Monitor No. 2 | $-.1 \mathrm{VDC} /{ }^{\circ} \mathrm{C}, 0$ VDC $\rightarrow 0^{\circ} \mathrm{C} *$ |
| 123 | Ground | 0 VDC |
| 124 | Ground | 0 VDC |
| 125 | Transmit IF Power | 5 VDC Nominal |
| 126 | Received IF Power | 5 VDC |
| 127 | Varactor | $\sim 0 \mathrm{VDC}, 1 \mathrm{VDC} \Rightarrow 2 \mathrm{VDC}$ |
| 130 | Integrator Oukput | $\sim 0 \mathrm{VDC}, 1 \mathrm{VDC} \Rightarrow 2 \mathrm{VDC}$ |
| 131 | Gunn Oscillator Voltage | 3 to 6 VDC |
| 132 | Gunn Oscillator Current | $\sim 1$ VDC, 1 VDC $\Rightarrow 1$ Amp |
| 133 | Ground | 0 VDC |
| 134 | Mixer Voltage | 0 VDC |
| 135 | Auto Warn | z. 1 VDC, THL High $\Rightarrow$ ON |
| 136 | Free Run Warn | z.1 VDC, TTL High $\Rightarrow$ ON |
| 137 | Lock Warn | z.1 VDC, TTL High $\Rightarrow$ ON |

*when connected.

MODEM T1 - IF COMBINER T2 COMMANDS CONTROL BUILDING DATA SET NO. 5

| Octal Address | Command |
| :---: | :--- |
| 360 | Search |
| 361 | Free Run |
| 362 | Monitor Reset |

Title Number
Schematic \& Logic Diagrams
Phase Lock Loop Unit Schematic Cl3440S3
Voltage Regulator Schematic C13440S4
Synchronous Debounce Schematic Cl3440S6
Harmonic Mixer Schematic Bl3440S7
Pin Diode Driver Schematic Bl3440S8
Bill of Materials
Modem (Top B.O.M.), Ch 1-6 Al3440Z1
Phase Lock Unit Subassembly Al3440z2
Voltage Regulator Subassembly Al3440z3
Harmonic Mixer Subassembly, Ch l-6 Al3440Z4
Synchronous Debounce Subassembly Al3440z5
Pin Diode Driver Subassembly A13440Z10
Modem (Top B.O.M.), Ch 7-10 Al3440Z12
Harmonic Mixer Subassembly, Ch 7-10 A13440213
Assembly Drawings
Modem Top Assembly Drawing Dl3440P13
Phase Lock Loop Assembly Drawing Cl3440P2
Voltage Regulator Assembly Drawing Bl3440P4
Harmonic Mixer Assembly Drawing Cl3440P7
Synchronous Debounce Assembly Drawing C13440P8
Pin Diode Driver Subassembly B13440P10
Modem Wire Harness Dl3440P11
Latching Circulator Cl3440P16
Single Pole Double Throw Pin Switch C13440P17
Single Pole Single Throw Pin Switch Cl3440P18
Transmit Amplifier Cl3440P19
Receive Amplifier Cl3440P20
Gunn Diode Oscillator Cl3440P21
26.5-50 GHz Mixers, Ch l-6 C13440P22-01

Ch 7-10 Cl3440P22-02
Harmonic Mixer Mount
Cl3440P23
Wire Lists
Rear Module Connector Wire List Al3440w2
Block Diagrams
Modem Block Diagram
Cl3440Bl

| Phase Lock Loop Unit | B13440AB2 |
| :---: | :---: |
| Voltage Regulator Board | Bl3440AB3 |
| Harmonic Mixer PC Board | B13440AD5 |
| Synchronous Debounce | Bl3440AB6 |
| Pin Diode Driver Board | B13440AB7 |
| Printed Circuit Board Silk Screen |  |
| Phase Lock Loop Unit | None |
| Voltage Regulator Board | None |
| Harmonic Mixer PC Board | None |
| Synchronous Debounce | None |
| Pin Diode Driver Board | None |
| Printed Circuit Board Drill Drawings |  |
| Phase Lock Loop Unit | Cl3440M21 |
| Voltage Regulator Board | B13440M28 |
| Harmonic Mixer PC Board | B13440M13 |
| Synchronous Debounce | B13440M12 |
| Pin Diode Driver Board | B13440M29 |
| Mechanical Drawings |  |
| Phase Lock Unit Enclosure Plate (Front and Rear) | Cl3440M36 |
| Phase Lock Unit Enclosure Plate (Left and Right Side) | B13440M37 |
| Mounting Plate for Power Transistor | Cl3440M6 |
| Front Panel | Cl3440M2 |
| Rear Panel | Cl3440M4 |
| Left Side Plate, Ch 1-6 | B13440M5-01 |
| Ch 7-10 | B13440M5-02 |
| Enclosure Cover, Top and Bottom | B13440M10 |
| Panel, 50 Pin PWR and Waveguide | B13440M25 |
| Waveguide, Bracket, Top | Bl3440M15 |
| Waveguide, Bracket, Bottom, Ch 1-6 | B13440M16-01 |
| Ch 7-10 | Bl3440Ml6-02 |
| Harmonic Mixer Enclosure Lid | Bl3440M17 |
| Harmonic Mixer Enclosure | Cl3440M18 |
| Guide | Bl3050M4 |
| Right Side Plate | Bl3050M18 |
| Bar Support, Top and Bottom | Bl3050M23 |


| Panel, (10) OMQ Connector Modem | B13440M30 |
| :---: | :---: |
| Cover, Perforated | Cl3050M22-1 |
| Filter Mounting Block | B13440M31 |
| Waveguide Extension, Ch 1-6 | Cl3440M32-01 |
| Ch 7-10 | Cl3440M32-02 |
| RF Component Spacers | Cl3440M35 |
| Specifications |  |
| Switched Circulator | Al3440N3 |
| Single Pole Double Throw Pin Switch | Al3440N4 |
| Single Pole Single Throw Pin Switch | Al3440N5 |
| Transmit Amplifier | Al3440N6 |
| Receive Amplifier | Al3440N7 |
| Gunn Diode Oscillator | Al3440N8 |
| 26.5-52 GHz Mixers | Al3440N9 |
| Tl Assembly/Wiring Operations \& |  |
| Specifications, Channels 1-6 | Al3440N11 |
| Tl Assembly/Wiring Operations \& |  |
| Specifications, Channels 7-10 | Al3440N12 |
| Harmonic Mixer Mount | Al3440N13 |
| Solid State Amplifier | A13450N1 |

### 11.0 SPECIFICATIONS

SPECIFICATION NO: Al3440N3, Revision A
NAME: Switched Circulator
DATE: October 7, 1976
PREPARED BY: $\qquad$ APPROVED BY: $\qquad$

## 1. General Description

A three-port switchable latching circulator with a removable termination supplied on one port is required. This device will be used as an isolator with switchable forward and reverse directions.
2. Frequency Range

All specifications must be met in an 800 MHz bandwidth centered at a frequency, $f_{0}$, related to channel number by the following table; channel number will be specified on purchase order:

| Channel | $f_{0}$ |
| :---: | :---: |
| 1 | 27.91 |
| 2 | 30.29 |
| 3 | 32.71 |
| 4 | 35.09 |
| 5 | 37.51 |
| 6 | 39.89 |
| 7 | 42.31 |
| 8 | 44.69 |
| 9 | 47.11 |
| 10 | 49.49 |
| 11 | 51.91 |

## 3. Marking

Channel number must be marked with a numeral $\geq 0.5^{\prime \prime} \mathrm{high}$ on top and bottom of the unit. Ports must be labeled 1, 2, and 3 with a removable termination supplied on port 3. In addition port 1 must be marked by the word "MODEM" on top and bottom. Forward direction is defined as low loss from port 1 to 2.

## 4. Control Signal

The unit must switch from reverse to forward by application of a single-ended TTL-compatible logical "l" (4 $\pm 1$ volts); a logical "O" must force the reverse state. The control signal will have $\leq 1 \mu s$ rise and fall times. 5. Power

The unit must operate from DC voltages of +15 and +5 volts with $\leq 0.1$ amp of current at a 20 Hz switch rate.

## 6. Isolation

The isolation from ports 2 to 1 in the forward state or ports 1 to 2 in the reverse state shall be $\geq 26 \mathrm{~dB}$.

## 7. Return Loss

The return loss at ports 1 to 2 shall be $\geq 26$ dB with other ports terminated and the switch in either forward or reverse state.
8. Insertion Loss

The insertion loss shall be $\leq 0.4 \mathrm{~dB}$ for $\mathrm{f}_{0} \leq 40 \mathrm{GHz}$ and $\leq 0.6 \mathrm{~dB}$ for $\mathrm{f}_{\mathrm{O}} \leq 50 \mathrm{GHz}$.
9. Switching Time and Rate

All specifications must be met 20 us after application of a control signal transition. The maximum switch rate will be 20 Hz .
10. Environment

The unit will be operated at power levels $\leq 100 \mathrm{~mW}$ and at ambient temperatures of $20^{\circ} \mathrm{C}$ to $40^{\circ} \mathrm{C}$.

## 11. Connectors

Control and power connections shall be thru a Cinch DE-9P connector. Waveguide ports shall mate with UG-599/U for channels 1 thru 6 and as shown on outline drawing No. Cl3440P16 for channels 7-10.
12. Configuration

The unit must conform to the electrical and mechanical specifications of the latching circulator outline drawing, No. Cl3440Pl6.

## 13. Documentation

Measurements of isolation, return loss, and insertion loss for forward and reverse states at $f_{0}-300 \mathrm{MHz}$ and $f_{0}+300 \mathrm{MHz}$ shall be supplied with frequencies accurate to $\pm 50 \mathrm{MHz}$. A schematic of the driver circuit shall be supplied.

# NATIONAL RADIO ASTRONOMY OBSERVATORY 

Post Office Box " 0 "
Socorro, New Mexico 87801

```
SPECIFICATION NO: Al3440N4, Revision A
NAME: Single Pole Double Throw Pin Switch
DATE: October 7, 1976
PREPARED BY:
```

$\qquad$

```
APPROVED BY:
```


## 1. GENERAL DESCRIPTION

```
A single pole double throw pin diode RF switch for use as a transmit/ receive switch is required.
2. FREQUENCY RANGE
All specifications must be met in a passband between 1 and 2 GHz .
3. MARKING
All ports must be labeled as shown on NRAO drawing No. Cl3440P17 on both faces of the unit.
4. BIAS LINES
Bias lines shall require \(\pm 50 \mathrm{MA}\) at 1 volt (current source), with polarities as shown on NRAO drawing No. Cl3440p17.
5. ISOLATION
```

The isolation between the two switched ports shall be $\geq 60 \mathrm{~dB}$.
6. MAXIMUM VSWR

The maximum VSWR of any port in the "ON" state shall be $1.5 / 1$ at $50 \Omega$.
7. INSERTION LOSS

The insertion loss shall be $\leq .8 \mathrm{~dB}$.
8. SWITCHING TIME AND RATE
'The switch must switch from one state to another in $\leq 10 \mu s$. The switch rate shall be 20 Hz .
9. CONNECTORS

RF connections shall be through SMA connectors, as shown on NRAO drawing No. Cl3440P17.
10. CONFIGURATION

The unit must conform to the electrical and mechanical specifications of the single pole double throw pin switch outline drawing No. Cl3440pl7.
11. ENVIRONMENT

The unit will be operated with RF power levels $\leq 100 \mathrm{~mW}$ and at ambient temperatures of $+20^{\circ} \mathrm{C}$ to $+40^{\circ} \mathrm{C}$.
12. MECHANICAL SHOCK

The unit must be able to withstand a shock test without permanent damage. The shock test shall consist of dropping the unit from a height of 6 inches onto a wooden surface.
13. DOCUMENTATION

Passband measurements of return loss and insertion loss shall be supplied with frequencies accurate to $\pm 20 \mathrm{MHz}$. A schematic with proper bias levels noted shall be supplied with proposals.

```
SPECIFICATION NO: Al3440N5, Revision A
NAME: Single Pole Single Throw Pin Switch
DATE: October 7, 1976
PREPARED BY:
APPROVED BY:
```


## 1. GENERAL DESCRIPTION

A single pole single throw pin diode RF switch for use as additional isolation in a transmit/receive system is required. The switch need not be matched in the isolation state.
2. FREQUENCY RANGE

All specifications must be met in a passband between 1 and 2 GHz .

## 3. MARKING

All ports must be labeled as shown on NRAO drawing No. Cl3440P18 on both faces of the unit.

## 4. BIAS LINE

The bias line shall require $\pm 50 \mathrm{MA}$ at 1 volt (current source), with the polarity as shown on NRAO drawing NO. Cl3440P18.

## 5. ISOLATION

The isolation beween the two switched ports shall be $\geq 40 \mathrm{~dB}$.
6. MAXIMUM VSWR

The maximum VSWR of any port in the "ON" state shall be $1.5 / 1$ at $50 \Omega$.
7. INSERTION LOSS

The insertion loss shall be $\leq .6 \mathrm{~dB}$.
8. SWITCHING TIME AND RATE

The switch must switch from one state to another in $\leq 10 \mu s$. The switch rate shall be 20 Hz .

## 9. CONNECTORS

RF connections shall be through SMA connectors, as shown on NRAO drawing No. Cl3440P18.
10. CONFIGURATION

The unit must conform to the electrical and mechanical specifications of the single pole single throw pin switch outline drawing No. Cl3440pl8.
11. ENVIRONMENT

The unit will be operated with RF power levels $\leq 10 \mathrm{~mW}$ and at ambient temperatures of $+20^{\circ} \mathrm{C}$ to $+40^{\circ} \mathrm{C}$.
12. MECHANICAL SHOCK

The unit must be able to withstand a shock test without permanent damage. The shock test shall consist of dropping the unit from a height of 6 inches onto a wooden surface.
13. DOCUMENTATION

Passband measurements of return loss and insertion loss shall be supplied with frequencies accurate to $\pm 20 \mathrm{MHz}$. A schematic with proper bias levels noted shall be supplied with proposals.

```
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            Post Office Box "O"
    Socorro, New Mexico 87801
```


## SPECIFICATION NO: Al3440N6, Revision A

NAME: Transmit Amplifier
DATE: October 7, 1976

PREPARED BY:
APPROVED BY:

## 1. GENERAL DESCRIPTION

A broadband linear power amplifier for use as a transmit amplifier is required.

## 2. FREQUENCY RANGE

All specifications must be met in a passband between 1 and 2 GHz .
3. MARKING

All ports must be labeled as shown on NRAO drawing No. C13440P19.
4. INPUT PONER

The unit must operate from a DC voltage of +28 VDC with less than 250 mA of current.
5. GAIN
$28 \pm 1 \mathrm{~dB}$. The gain at any frequency shall not exceed in-band gain.
6. GAIN FLATNESS
$\pm .5 \mathrm{~dB}$.
7. POWER OUTPUT
+17 dBm minimum at 1 dB gain compression.

## 8. MAXIMUM VSWR

The maximum VSWR of either the input or output port shall be $1.5 / 1$ at $50 \Omega$.
9. NOISE FIGURE

8 dB maximum.

```
Specification Al3440N6, Revision A
```

10. CONNECTORS

SMA female.
11. CONFIGURATION

The unit must conform to the mechanical specifications of the transmit amplifier outline drawing No. Cl3440P19.
12. ENVIRONMENT

The unit will be operated at case temperatures of $+20^{\circ} \mathrm{C}$ to $+40^{\circ} \mathrm{C}$.
13. MECHANICAL SHOCK

The unit must be able to withstand a shock test without permanent damage. The shock test shall consist of dropping the unit from a height of 6 inches onto a wooden surface.
14. DOCUMENTATION

Passband measurements of return loss, gain and compression point shall be supplied with frequencies accurate to $\pm 20 \mathrm{MHz}$.

SPECIFICATION NO: Al3440N7, Revision A
NAME: Receive Amplifier
DATE: October 7, 1976
PREPARED BY: $\qquad$ APPROVED BY: $\qquad$

1. GENERAL DESCRIPTION

A broadband low noise amplifier for use as a receive amplifier is required.
2. FREQUENCY RANGE

All specifications must be met in a passband between 1 and 2 GHz .
3. MARKING

All ports must be labeled as shown on NRAO drawing No. Cl3440P20.
4. INPUT POWER

The unit must operate from a DC voltage of +15 V DC with less than 100 mA of current.
5. GAIN
$35 \pm 1$ dB. The gain at any frequency shall not exceed in-band gain.
6. GAIN FLATNESS
$\pm .5 \mathrm{~dB}$.
7. POWER OUTPUT

0 dBm minimum at 1 dB gain compression.
8. MAXIMUM VSWR

The maximum VSWR of either the input or output port shall be $1.5 / 1$ at $50 \Omega$.
9. NOISE FIGURE
$3 d B$ maximum.
10. CONNECTORS

SMA female.

## 11. CONFIGURATION

The unit must conform to the mechanical specifications of the receive amplifier outline drawing No. Cl3440P2O.
12. ENVIRONMENT

The unit will be operated at case temperatures of $+20^{\circ} \mathrm{C}$ to $+40^{\circ} \mathrm{C}$.
13. MECHANICAL SHOCK

The unit must be able to withstand a shock test without permanent damage. The shock test shall consist of dropping the unit from a height of 6 inches onto a wooden surface.
14. DOCUMENTATION

Passband measurements of return loss, gain, and noise figure shall be supplied with frequencies accurate to $\mathbf{+ 2 0} \mathbf{~ M H z}$.

# NATIONAL RADIO ASTRONOMY OBSERVATORY <br> Post Office Box "O" <br> Socorro, New Mexico 87801 

## SPECIFICATION NO. Al3440NB, Revision A

NAME Gunn Diode Oscillator
DATE October 7, 1976

PREPARED BY $\qquad$ APPROVED BY $\qquad$

## 1. APPLICATION

The Gunn diode oscillator will be phase-locked and used as a local oscillator for an upconverter.
2. OUTPUT LOAD

The oscillator shall be supplied with a 20 dB isolator to start and phase-lock with a load of arbitrary magnitude and phase (i.e., a narrow band filter) at heat sink temperature of $20^{\circ} \mathrm{C}$ to $40^{\circ} \mathrm{C}$.

## 3. FREQUENCY

Each oscillator will be ordered by channel number which is related to local oscillator frequency by the following table.

| CHANNEL | LOCAL OSCILLATOR FREQUENCY $\mathrm{f}_{\mathrm{O}}, \mathrm{GHz}$ | SIGNAL BAND |  |
| :---: | :---: | :---: | :---: |
|  |  | LOW | HIGH |
| 1 | 26.41 | 27.41 | 28.41 |
| 2 | 28.79 | 29.79 | 30.79 |
| 3 | 31.21 | 32.21 | 33.21 |
| 4 | 33.59 | 34.59 | 35.59 |
| 5 | 36.01 | 37.01 | 38.01 |
| 6 | 38.39 | 39.39 | 40.39 |
| 7 | 40.81 | 41.81 | 42.81 |
| 8 | 43.19 | 44.19 | 45.19 |
| 9 | 45.61 | 46.61 | 47.61 |
| 10 | 47.99 | 48.99 | 49.99 |
| 11 | 50.41 | 51.41 | 52.41 |

4. MARKING

The channel number shall be marked on the unit as per NRAO drawing No. Cl3440p21.
5. POWER OUTPUT
$A$ power of $+17 \mathrm{dBm} \pm 1 \mathrm{~dB}$ is required at frequency $\mathrm{f}_{0}$ for heat sink temperatures of up to $40^{\circ} \mathrm{C}$.

## 6. MECHANICAL FREQUENCY TUNING

A mechanical tuning range of $\pm 100 \mathrm{MHz}$ minimum with a varactor bias voltage given by the following formula at a case temperature of $40^{\circ} \mathrm{C}$ is required.

$$
\begin{aligned}
V_{\text {Bias }} & =.73 V_{G u n n}-4.6 \\
\text { where } V_{\text {Bias }} & =\text { varactor bias voltage in volts referenced to ground } \\
V_{G u n n} & =\text { positive Gunn supply voltage in volts }
\end{aligned}
$$

## 7. ELECTRONIC FREQUENCY TUNING

Electronic frequency tuning is required to compensate for a heat sink temperature range of $30^{\circ} \mathrm{C}$ to $40^{\circ} \mathrm{C}$ and long term drift.

The varactor diode shall be referenced to the positive Gunn supply voltage. The varactor tuning port shall have an input voltage swing from the Gunn supply voltage to -14 VDC referenced to ground. Over this voltage range the varactor shall have a worst case minimum gain of $10 \mathrm{MHz} / \mathrm{volt}$ and a worst case maximum gain of $100 \mathrm{MHz} / \mathrm{volt}$. Also, for an individual Gunn oscillator, the maximum ratio of minimum to maximum gain over this tuning range shall be 5 to 1. Maximum gain shall occur at the Gunn supply voltage. Using a 50 ohm source impedance, a minimum modulation bandwidth of 20 MHz is required at the electronic tuning port. The tuning port must have at least 50 dB of isolation at the oscillator frequency $f_{0}$.
8. MECHANICAL CONFIGURATION

Oscillator and isolator should be conductively heat sunk on a surface at right angles to the output waveguide. The oscillator tuning port should be a female SMA connector. The RF port shall mate to WR-28 waveguide (UG599/U Flange) for $f_{0}$ less than 40 GHz and mate to WR-19 waveguide (UG383 (M)/U Flange) for $f_{0}$ greater than 40 GHz . The oscillator must conform to the mechanical specifications of the NRAO Gunn diode oscillator outline drawing No. Cl3440P21.

## 9. DOCUMENTATION

A chart of frequency vs varactor voltage and power vs varactor voltage in 1 volt increments from the Gunn supply voltage to -14 VDC referenced to ground shall be provided with each unit.

## NATIONAL RADIO ASTRONOMY OBSERVATORY

Post Office Box "O"
Socorro, New Mexico 87801

## SPECIFICATION NO: Al3440N9, Revision B

NAME: 26-52 GHz Mixers
DATE: October 7, 1976
PREPARED BY: $\qquad$ APPROVED BY: $\qquad$

## 1. GENERAL

These specifications describe a mixer which will be used for both lownoise reception and, as an up-converter, for transmission of signals at specified frequencies in the $26-52 \mathrm{GHz}$ range. The mixer contains a diplexer for injection of local oscillator power and a filter to pass only the uppersideband.

## 2. FREQUENCY

Each mixer will be ordered by channel number which is related to local oscillator and RF frequency by the following table:

| CHANNEL | $\begin{gathered} \text { LOCAL OSCILLATOR } \\ \text { FREQUENCY } \\ \mathbf{f}_{0}, G H z \\ \hline \end{gathered}$ | SIGNAL BAND |  |
| :---: | :---: | :---: | :---: |
|  |  | LOW | HIGH |
| 1 | 26.41 | 27.41 | 28.41 |
| 2 | 28.79 | 29.79 | 30.79 |
| 3 | 31.21 | 32.21 | 33.21 |
| 4 | 33.59 | 34.59 | 35.59 |
| 5 | 36.01 | 37.01 | 38.01 |
| 6 | 38.39 | 39.39 | 40.39 |
| 7 | 40.81 | 41.81 | 42.81 |
| 8 | 43.19 | 44.19 | 45.19 |
| 9 | 45.61 | 46.61 | 47.61 |
| 10 | 47.99 | 48.99 | 49.99 |
| 11 | 50.41 | 51.41 | 52.41 |

2. (cont.)

Unless otherwise stated all specifications must be met in the RF signal band stated above and for IF frequencies between 1 and 2 GHz .
3. LO REQUIREMENT

Lo power available to the mixer is $17 \pm 1 \mathrm{dBm}$.

## 4. LO LEAKAGE

The 10 power out of the $R F$ port shall be less than -30 dBm (including upper-sideband filter rejection).
5. UP-CONVERTER POWER OUTPUT
a) The RF power output at the 1 dB gain compression point shall be $>+5 \mathrm{dBm}$ measured with an IF input frequency of 1500 MHz .
b) The peak-to-peak variation in power output vs frequency shall be less than 1.0 dB measured at an average +2 dBm output level.
6. CONVERSION LOSS VARIATION

The frequency variation of receive mode conversion loss shall be less than 1 dB peak-to-peak.
7. UPPER SIDEBAND FILTER

An $R F$ signal in the $f_{0}-1 \mathrm{GHz}$ to $f_{o}-2 \mathrm{GHz}$ range shall produce an IF output 40 dB or more below the output level produced by a signal at $f_{0}+1.5 \mathrm{GHz}$. An RF signal at $f_{0}+600 \mathrm{MHz}$ or $\mathrm{f}_{0}+2400 \mathrm{MHz}$ shall produce an output $\geq 10 \mathrm{~dB}$ below the $f_{0}+1.5 \mathrm{GHz}$ level.
8. NOISE FIGURE

The receive mode RF noise figure shall be less than 11 dB averaged over the IF frequency range and measured with an IF amplifier having $\leq 4.0$ dB noise figure.
9. RF RETURN LOSS

The $R F$ return loss shall be $\geq 13 d B$ with a receive $R F$ incident power of 0 dBm .
10. IF RETURN LOSS

The IF return loss shall be $\geq 16 \mathrm{~dB}$ with an $I F$ signal level sufficient to provide +2 dBm RF power.

## 11. CONNECTORS

a) IF Port - Type SMA female
b) RF and LO Ports - UG-599 for channels 1 through 6 and UG-383M (WRI9) for channels 7 through 11.
12. CONFIGURATION

The unit must conform to the mechanical specifications of the $26.5-50 \mathrm{GHz}$ mixer outline drawing No. Cl3440P22.

## 13. ENVIRONMENT

The unit will be used in a laboratory environment at an ambient temperature of $20^{\circ}$ to $40^{\circ} \mathrm{C}$.

## 14. MARKING

Channel number, IF, LO, and RF ports shall be marked as shown on NRAO drawing No. Cl3440P22.

## 15. MIXER DIODE

a) The mixer diode shall be field-replaceable. Selection and adjustment shall not be required upon replacement. One spare diode (or diode-pair, if used) shall be supplied with each mixer.
b) The mixer diode shall withstand $L 0$ power of 3 dB above normal.
c) The mixer shall survive a drop-test of 3 inches to a wooden surface.
16. TEST EQUIPMENT

The manufacturer shall have available the following equipment:
a) Signal source covering frequency of specified channel.
b) Waveguide power meter for specified channel.
c) $1-2 \mathrm{GHz}$ leveled sweep generator.
d) 1-2 GHz reflectometer coupler.
e) 1-2 GHz power meter.
f) RF source to use as local oscillator of specified channel.
g) Waveguide noise source for specified channel.
h) Waveguide 10 dB coupler
i) 1-2 GHz calibrated attenuator. NRAO will supply l-2 GHz amplifier for noise figure measurement.

## 17. TEST DATA

The manufacturere shall perform the following measurements and supply recorded test data for both the original and spare diode. NRAO shall be notified 5 days prior to final measurements and may elect to send an engineer to witness measurements. NRAO may also elect to supply the local oscillators for these tests and will definitely supply a low-noise l-2 GHz amplifier:
a) Receive mode $R F$ return loss and IF conversion loss as shown in Figure 1.
b) Transmit mode output power compression curve, RF output power, and IF return loss as shown in Figure 2.
c) Noise figure as shown in Figure 3.
d) Upper-sideband filter response curve or mixer measurements to prove compliance with Specification 7.


TABLE T - REEEIVE MOOE
R兰TURN ANT EmvERSian loEs

| RR <br> Frea. <br> fre-fo | Revtuan Polvira osm |  |
| :---: | :---: | :---: |
| 1000 1200 1350 1500 1650 180n 2000 Opr |  |  |

[^0]FIGURE 1 - Receive mode test configuration and data table.


TABLE II - TRANSTMIT
Cemprossion DATA

| INEIDENT IF powe R DEM | OUTPU RF <br> POWER <br> Dem | MixER |
| :---: | :---: | :---: |
| 0 |  |  |
| $+3$ |  |  |
| $+6$ |  |  |
| $+7$ |  |  |
| $+8$ |  |  |
| $+9$ |  |  |
| $+10$ |  |  |
| + 11 |  |  |
| $+12$ |  |  |
| $+13$ |  |  |
| $+14$ |  |  |
| $+15$ |  |  |
| - FFF |  |  |

TAOLE III - TRNASMT
JF ROTORAN ANO RTE ONTPUT


IF JNPUT POWER AF LEVEL TO GIVE ANERAGE RF GOTPUT Power of +2 OEm.

[^1]FIGURE 2 - Transmit mode test configuration and data tables.


FIGURE 3 - Noise figure measurement set-up.

SPECIFICATION: Al3440N11 Rev. A DATE: September 29, 1976
UNIT: Modem, Module TYpe Tl, Channels l-6
TITLE: Assembly/Wiring Operations and Specifications
TOP ASSEMBLY DRAWING: D13440P13-01
TOP BILL OF MATERIAL: Al344021
PREPARED BY:
APPROVED BY: $\qquad$
1.0 GENERAL DESCRIPTION AND SCOPE

This specification defines the work required to assemble and wire prefabricated components into a completed assembly, ready for test.

The scope of this specification covers the operations to be performed, the items supplied by NRAO, assembly and wiring requirements and the associated documentation.

The assembly operations identify the operations to be performed in an orderly assembly sequence. The appropriate drawings and documentation are keyed to the sequence.

If problems of fit or drawing interpretation arise, NRAO should be contacted for resolution of the problem.

### 2.0 NRAO-SUPPLIED ITEMS

1. NRAO will supply ALL printed circuit boards; drilled, etched and profiled, ready for assembly.
2. NRAO will supply ALL metal and plastic components; plated, painted and engraved. Metal components will be bagged and will have the part number printed on the bag for identification.

September 9, 1976
3. NRAO will supply ALJ hardware items such as screws, nuts, connector pins, connector blocks, insulator spacers, mylar sheets, coax cable, coax connectors, brackets, housings, etc.
4. NRAO will supply ALL electrical components such as integrated circuits, transistors diodes, resistors, capacitors, LED's, IC sockets, potentiometers, RF components, coaxial cable, PC Board connectors, etc.
5. NRAO will not supply wire, ty-wraps or lacing cord.
6. NRAO will not supply any tools, except for OSM and OMQ coax connector assembly kits.
7. All component parts will be bagged and marked but will not be broken out into kits or tagged with assembly drawing part numbers.

### 3.0 T1 ASSEMBLY INSTRUCTIONS, CHANNELS 1 THROUGH 6

A. Assemble the following Sub-Assemblies. Refer to the indicated drawings for component placement. Be certain that polarities on components are observed and variable resistors are oriented as shown. All integrated circuits are mounted with sockets. The completed boards shall be cleaned of all rosin residue.

Sub-Assembly Al3440Z2, Phase Lock Unit, is mounted in an enclosure. Be certain that the connectors are correctly oriented and that connector pins are wired to the appropriate points on the printed circuit card.

Harmonic Mixer, Al344024, assembly instructions.

1. Trim back Teflon sleeves on SMA connectors, two (17-2) and one (16), such that Teflon extends .150-.025" from flange.
2. Cut connector center conductors to extend .250" from flange.
3. Attach connectors to box (5) using twelve No. 2-56 x . 250 S.S. pan head slotted screws (10-12).
4. Insuring that the PC card (7) is fitted tightly against the floor of the box, solder the connector pins to the PC card.
5. Trim lead on Ll to .250".
6. Insert this lead into hole on box and fasten using one No. 4-40 $x .125$ flat point headless socket set screw (12), applying only enough pressure to secure the lead.
7. Trim other lead of Ll to $.125^{\prime \prime}$ and solder to PC board.
8. Attach lid of box (6) with six No. 0-80 x . 187 S.S. pan head slotted screws (11-6).

SUB-ASSEMBLY
Al344022 Phase Lock Unit
Al344023 Voltage Regulator
Al344024 Harmonic Mixer

ASSEMBLY DRAWING SCHEMATIC DRAWING NUMBER

Bl3440P2
B13440P4
Cl3440P7
B13440P8
B13440P10

NUMBER

Cl3440S3
C13440S4
B13440S7
C13440S6
B13440S8

Note: The module shall be assembled and handled carefully so as to avoid damage such as nicks and scratches on the panels and metal parts. If there are fit or alignment problems, consult NRAO for corrective action. In no case shall mating parts be "forced" to fit.
B. Install the following components on the left side plate (8). 1. Two support bars (10-2) using six No. 6-32 $\times .25$ flat head screws (26-6).
2. Eleven $1.75^{n} \times .25$ threaded spacers (120-11) using No. 4-40 x . 25 binder head screws (101-11) and external tooth lockwashers (131-11). Place lockwashers between spacers and left side plate.
3. One l-2 GHz amplifier (67) using four No. 4-40 $\times .3125$ binder head screws (124-4), hex nuts (42-4), and internal tooth lockwashers (37-4).
4. One bandpass filter (75) using two filter clips (25-2), No. 4-40 x . 25 binder head screws (101-2), external tooth lockwashers (131-2), and hex nuts (37-2).
C. Mount four Spectrum Control filters (50-4) on the filter mounting block (38) using supplied hardware. Mount this assembly on the left side plate using two No. 4-40 x . 3125
binder head screws (124-2), internal tooth lockwasher (42), solder lug (125), and hex nuts (37-2). The voltage regulator, VRl, (44) is mounted under one nut. Use heat sink compound between regulator and mounting block. Surface of filter mounting block and voltage regulator must be clean before applying heat sink compound.
D. Mount the 2 N 3790 transistor (66) on the transistor mounting block (15) using a transistor insulator (121), two shoulder bushings (122-2), two No. 4-40 x . 5 pan head screws (132-2), one internal tooth lockwasher (42), one No. 4 solder lug (125), and two hex nuts (37-2). Mount this assembly on the left side plate using six No. 4-40 x . 25 flat head screws (39-6).
E. Connect the following components together.

1. Coupler (80) to Gunn oscillator (78) using four No. 4-40 $x$ .25 hex socket head screws (115-4) and No. 4 split lockwashers (117-4). Diode (95) is installed in coupler. 2. Space-Kom mixer (82) to coupler using four No. 4-40 x . 25 hex socket screws (115-4) and No. 4 split lockwashers (117-4).
2. Circulator (84) to Space-Kom mixer using four No. 4-40 x . 3125 hex socket head screws (111-4) and No. 4 split lockwashers (117-4).

Mount this assembly on the left side plate.

1. Gunn oscillator is mounted on spacer (76) using two No. 4-40 x . 5 binder head screws (103-2).
A. Use heat sink compound between Gunn, spacer and plate. Be sure all mating surfaces are clean before applying compound.
2. Circulator is mounted directly on plate using two No. 2-56 x . 250 binder head screws (104-2). Two screws must be removed from circulator. Make sure all components are oriented as per top assembly drawing. Do not tighten mounting screws.
F. Connect the following components together. All connectors will be cleaned and inspected. A torque wrench supplied by NRAO will be used to tighten all OSM connectors.
3. SPST pin diode switch JI (88) to l2DB attenuator (47).
4. OSM 219 adaptor (63) to attenuator.
5. XMIT amplifier (91) input to OSM219 adaptor.
6. J3 of SPDT pin diode switch (89) to XMIT amplifier output.
7. Receive AMP (93) input to J2 of DPST pin diode switch. Be certain all mounting surfaces are clean. Mount this assembly to left side plate by connecting Jl of DPST pin diode switch to Space-Kom mixer IF part. Output end of RCV amplifier is mounted on spacer (92) using two No. 2-56 x . 5652 binder head screw (106-2) and No. 2 flat washer (134-2). The XMIT amplifier is mounted on spacer (90) using four No. 4-40 x 1.75 binder head screws (102-4), internal tooth lockwashers (42-4), and hex nuts (37-4). The SPT pin diode switch is mounted on spacer (87) using a No. 2-56 x 1.00 binder head screw (105) and No. 2 flat washer (134).

Retighten all OSM connectors using torque wrench. Check orientation of all components and tighten all mounting screws.
G. Attach waveguide (69) to circulator using four No. 4-40 x . 3125 hex socket head screws (11l-4) and No. 4 split lockwashers (117-4).
H. Mount 50 pin connector block (16) and connector block hood (17) on rear panel (13) using connector guide pin (18), connector guide sockets (19-2), connector ground guide pin (20), and a No. 4 solder lug (125). See top assembly drawing for proper placement.

Attach rear panel to left side plate assembly using two No. 6-32 x . 25 hex socket head screws (29-2).
I. Mount the following components on the front panel (12) using supplied hardware.

1. LED indicators (5l-3). (Long lead indicates +5 V connection.)
2. Meter (52) and half frame bezel (43).
3. DPDT toggle switches (53-2). (See top assembly drawing for detai.
4. Fuse holder (54) and Fuse (55). (Discard rubber grommet.)
5. BNC Jack (56) and ground lug (35).
6. BNC feedthrough connectors (57-2).

Attach front panel to left side plate assembly using two No. 6-32 x . 375 flat head crossed recessed screws (31-2).
J. Install Harmonic Mixer Sub-assembly (4) on coupler.
K. Fabricate and install . 141 coax (64) and connectors. A tool kit for the OSM and OMQ connectors will be provided by NRAO with the appropriate instructions. Each connector must pass a quality control test using NRAO-provided dial indicators. All . 141 coax must be handfitted to the appropriate RF components using the bending tool provided in the tool kit. No coax shall be bent to a radius less than that possible using the bending tool. The finished coax shall be free of any kinks or scratches and shall be cleaned of rosin.

1. Rear panel J4 to $1-2 \mathrm{GHz}$ amplifier input using one OMQ 3043-75 (58) and one OSM 201-1A (60) .(5-3/4").
2. 1-2 GHz amplifier output to bandpass filter using two OSM 201-1A (60-2) (8놀́).
3. Bandpass filter to Harmonic Mixer Sub-assembly Jl using our OSM 201A (60) and one OSM 221-1 (73) (71/n).
4. Rear panel Jl6 to SPST pin diode switch J2 using one OMQ 3043-75 (58), and one OSM 201-1A (60) (22 5/8n).
5. Rear panel Jl5 to RCV amplifier output using one OMQ 3043-75 (58) and one OSM 201-1A (60) (71 ${ }^{n}$ ).
L. Fabricate and install wire harness to all components, subassemblies, front panel, and rear panel using wire harness drawing Dl3440Pll. All wire is color coded No. 22 AWG stranded (113), RG-174 (62), and RG-188 coax (112). Use manufacturers instructions for coax connectors. Heat shrink tubing will be used on all wire terminations except the PC board connectors and rear panel connector wire pins. Wires that terminate on a solder pin will be soldered. In some cases two or three wires may terminate at one point (if specified by the wire list). Solder terminations of stranded wire shall be neat and free of excess solder and wire whiskers. Solder flux residue shall be cleaned.

Hand wiring shall be neatly dressed into bundles. Sufficient service loops shall be used to permit the front panel and the PC cards to be "folded" open for access. Wire bundles shall be confined with lacing cord or plastic ty-wraps.

The following items are used on the wire harness.

1. Connector pins, yellow/red (40-18).
2. OMQ 3043-53 connector (59).
3. OSM 5ll-3 plug, RG-188 (61-6).
4. OSM 531-1 plug, right angle, RG-188 (68-4).
5. 14 pin platform (109-3).
6. Platform cover (110-3).
7. DAl5P connector (45).
8. Connector hood (46).
A. Hood is attached to connector using two No. 4-40 x . 25 pan head screws (36-2), two internal tooth lockwashers (42-2), and hex nuts (37-2).
9. DE95 connector (108).
10. Connector hood (126).
A. Hood is attached to connector using two No. 4-40 $\times .25$ pan head screws (36-2), internal tooth lockwashers (42-2), and hex nuts (37-2).
11. BNC crimp type plugs, 31-315 (65-2).
M. Install the following sub-assemblies.
12. Phase lock unit sub-assembly (2) using two No. 8-32 x . 375 binder head screws (34-2).
13. Voltage regulator sub-assembly (3) using four No. 4-40 x . 250 binder head screws (101-4).
14. Synchronous debounce sub-assembly (5) using three No. 4-40 x . 250 binder head screws (101-3).
15. Pin diode driver sub-assembly (7) using No. 4-40 $x$ .250 binder head screws (101-4).

Connect wire harness to sub-assemblies.
N. Complete the mechanical assembly by installing the following components.

1. Two perforated covers (11-2).
2. Two support bars (10-2) using two No. 6-32 x . 375 flat head crossed recessed screws (31-2) in front panel and two No. 6-32 x . 25 flat head screws (26-2) in rear panel.
3. Four guides (14-4) on rear panel using four No. 6-32 x $.625(28-4)$ and four No. 6-32 x . 875 (27-4) pan head slotted screws.
4. Threaded spacer (33) to rear panel using one No. 6-32 x . 375 pan head screw (32) and internal tooth lockwashers (97).
5. Right side plate (9) using six No. 6-32 x . 25 flat head screws (26-6).
6. Four captive screws (21-4) in front panel using NRAOsupplied installation tool.
P. The waveguide brackets $(22,23)$ will be installed by NRAO. The waveguide installed in step "G" must be removed prior to shipment. Each module shall be individually wrapped with a protective covering and packed carefully in durable shipping containers to prevent damage.


FIGURE 1: "FRONT PANEL - FRONT VIEW"


FIGURE 2: "front panel - rear view"


FIGURE 3: "RIGHT-HAND SIDE VIEW, COMPLETE"


FIGURE 4: "RIGHT-HAND SIDE VIEW, LESS PRINTED CIRCUIT BOARDS"


FIGURE 5: "PHASE LOCK UNIT"


FIGURE 6: "REAR PANEL"

# NATIONAL RADIO ASTRONOMY OBSERVATORY <br> SOCORRO, NEW MEXICO <br> VERY LARGE ARRAY PROJECT 

SPECIFICATION: Al3440N12 Rev. A DATE: September 29,1976
UNIT: Modem, Module Type Tl, Channels 7-10
TITLE: Assembly/Wiring Operations and Specifications
TOP ASSEMBLY DRAWING: Dl3440P13-02
TOP BILL OF MATERIAL: Al3440212
PREPARED BY: $\qquad$ APPROVED BY: $\qquad$

### 1.0 GENERAL DESCRIPTION AND SCOPE

This specification defines the work required to assemble and wire prefabricated components into a completed assembly, ready for test.

The scope of this specification covers the operations to be performed, the items supplied by NRAO, assembly and wiring requirements and the associated documentation.

The assembly operations identify the operations to be performed in an orderly assembly sequence. The appropriate drawings and documentation are keyed to the sequence.

If problems of fit or drawing interpretation arise, NRAO should be contacted for resolution of the problem.

### 2.0 NRAO-SUPPLIED ITEMS

1. NRAO will supply ALL printed circuit boards; drilled, etched and profiled, ready for assembly.
2. NRAO will supply ALL metal and plastic components; plated, painted and engraved. Metal components will be bagged and will have the part number printed on the bag for identification.
3. NRAO will supply ALL hardware items such as screws, nuts, connector pins, connector blocks, insulator spacers, mylar sheets, coax cable, coax connectors, brackets, housings, etc.
4. NRAO will supply ALL electrical components such as integrated circuits, transistors diodes, resistors, capacitors, LED's, IC sockets, potentiometers, RF components, coaxial cable, PC Board connectors, etc.
5. NRAO will not supply wire, ty-wraps or lacing cord.
6. NRAO will not supply any tools, except for OSM and OMQ coax connector assembly kits.
7. All component parts will be bagged and marked but will not be broken out into kits or tagged with assembly drawing part numbers.
3.0 T1 ASSEMBLY INSTRUCTIONS, CHANNELS 7 THROUGH 10
A. Assemble the following Sub-Assemblies. Refer to the indicated drawings for component placement. Be certain that polarities on components are observed and variable resistors are oriented as shown. All integrated circuits are mounted with sockets. The completed boards shall be cleaned of all rosin residue.

Sub-Assembly Al3440Z2, Phase Lock Unit, is mounted in an enclosure. Be certain that the connectors are correctly oriented and that connector pins are wired to the appropriate points on the printed circuit card.

Harmonic Mixer, Al3440Z4, assembly instructions.

1. Trim back Teflon sleeves on SMA connectors, two (17-2) and one (16), such that Teflon extends .150-.025" from flange.
2. Cut connector center conductors to extend .250" from flange.
3. Attach connectors to box (5) using twelve No. 2-56 $x$ . 250 S.S. pan head slotted screws (10-12).
4. Insuring that the PC card (7) is fitted tightly against the floor of the box, solder the connector pins to the PC card.
5. Trim lead on Ll to . $250^{\prime \prime}$.
6. Insert this lead into hole on box and fasten using one No. 4-40 x .125 flat point headless socket set screw (12), applying only enough pressure to secure the lead.
7. Trim other lead of Ll to $.125^{\prime \prime}$ and solder to PC board.
8. Solder Cl in position shown on assembly drawing, using minimal heat and solder.
9. Attach lid of box (6) with six No. 0-80 x . 187 S.S. pan head slotted screws (11-6).

## SUB-ASSEMBLY

Al3440Z2 Phase Lock Unit

## Al344023 Voltage Regulator

Al3440Z4 Harmonic Mixer
Al344025 Synchronous Debounce Bl3440P8
Al34402l0 Pin Diode Driver

ASSEMBLY DRAWING SCHEMATIC DRAWING NUMBER

B13440P2 Cl3440S3

Cl3440S4
Bl3440S7
C13440S6
Bl344058

Note: The module shall be assembled and handled carefully so as to avoid damage such as nicks and scratches on the panels and metal parts. If there are fit or alignment problems, consult NRAO for corrective action. In no case shall mating parts be "forced" to fit.
B. Install the following components on the left side plate (8). 1. Two support bars (10-2) using six No. 6-32 x . 25 flat head screws (26-6).
2. Eleven 1.75" x. 25 threaded spacers (120-11) using No. 4-40 x. 25 binder head screws (101-11) and external tooth lockwashers (131-1l). Place lockwashers between spacers and left side plate.
3. One l-2 GHz amplifier (67) using four No. 4-40 x . 3125 binder head screws (124-4), hex nuts (42-4), and internal tooth lockwashers (37-4).
4. One bandpass filter (75) using two filter clips (25-2), No. 4-40 x . 25 binder head screws (101-2), external tooth lockwashers (131-2), and hex nuts (37-2).
C. Mount four Spectrum Control filters (50-4) on the filter mounting block (38) using supplied hardware. Mount this assembly on the left side plate using two No. 4-40 x . 3125
binder head screws (124-2), internal tooth lockwasher (42), solder lug (125), and hex nuts (37-2). The voltage regulators, VRl, (44) is mounted under one nut. Use heat sink compound between regulator and mounting block. Surface of filter mounting block and voltage regulator must be clean before applying heat sink compound.
D. Mount the 2N3790 transistor (66) on the transistor mounting block (15) using a transistor insulator (121), two shoulder bushings (122-2), two No. 4-40 x. 5 pan head screws (132-2), one internal tooth lockwasher (42), one No. 4 solder lug (125), and two hex nuts (37-2). Mount this assembly on the left side plate using six No. 4-40 $\times .25$ flat head screws (39-6).
E. The following components have been preassembled by NRAO on the left side plate (8).

1. Coupler (81) to Gunn oscillator (79) using four No. 4-40 ST/ST hex cap screws (116-4) and No. 4 split lockwashers (117-4). All waveguide flange screws shall be tightened using a torque wrench, observing proper mating practice.
2. Space-Kom mixer (83) to coupler using four No. 4-40 ST/ST hex cap screws (116-4) and No. 4 split lockwashers (117-4).
3. Circulator (85) to Space-Kom mixer using four No. 4-40 x . 5 hex socket head screws (107-4) and No. 4 split lockwashers (117-4)
4. Waveguide extension (70) to circulator using four No. 4-40 ST/ST hex cap screws (116-4) and No. 4 split lockwashers (117-4). These components have been mounted on the left side plate by NRAO. 1. Gunn oscillator is mounted on spacer (77) using two No. 4-40 x . 25 binder head screws (101-2).
A. Use heat sink compound between Gunn, spacer and plate. Be sure all mating surfaces are clean before applying compound.
5. Circulator is mounted directly on plate using two No. 2-56 x . 250 binder head screws (104-2). Two screws must be removed from circulator.

Make sure all components are oriented as per top assembly drawing. Do not tighten mounting screws.
F. Connect the following components together. All connectors will be cleaned and inspected. A torque wrench supplied by NRAO will be used to tighten all OSM connectors.

1. SPST pin diode switch JI (88) to 12DB attenuator (47).
2. OSM 219 adaptor (63) to attenuator.
3. XMIT amplifier (91) input to OSM219 adaptor.
4. J3 of SPDT pin diode switch (89) to XMIT amplifier output.
5. Receive AMP (93) input to J2 of DPST pin diode switch. Be certain all mounting surfaces are clean. Mount this assembly to left side plate by connecting Jl of DPST pin diode switch to Space-Kom mixer IF part. Output end of RCV amplifier is mounted on spacer (96) using two No. 2-56 x. 5652 binder head screw (106-2) and No. 2 flat washer (134-2). The XMIT amplifier is mounted on spacer (94) using four No. 4-40 x 1.75 binder head screws (102-4), internal tooth lockwashers (42-4), and hex nuts (37-4). The SPT pin diode switch is mounted on spacer (86) using a No. 2-56 x 1.00 binder head screw (105) and No. 2 flat washer (134).

Retighten all OSM connectors using torque wrench. Check orientation of all components and tighten all mounting screws.
G. Completed at NRAO.
H. Mount 50 pin connector block (16) and connector block hood (17) on rear panel (13) using connector guide pin (18), connector guide sockets (19-2), connector ground guide pin (20), and a No. 4 solder lug (125). See top assembly drawing for proper placement.

Attach rear panel to left side plate assembly using two No. 6-32 x . 25 hex socket head screws (29-2).
I. Mount the following components on the front panel (12) using supplied hardware.

1. LED indicators (51-3). (Long lead indicates +5 V connection.)
2. Meter (52) and half frame bezel (43).
3. DPDT toggle switches (53-2). (See top assembly drawing for detail
4. Fuse holder (54) and Fuse (55). (Discard rubber grommet.)
5. BNC Jack (56) and ground lug (35).
6. BNC feedthrough connectors (57-2).

Attach front panel to left side plate assembly using two No. 6-32 x . 375 flat head crossed recessed screws (31-2).
J. Install Harmonic Mixer Sub-assembly (4) on coupler.
K. Fabricate and install . 141 coax (64) and connectors. A tool kit for the OSM and OMQ connectors will be provided by NRAO with the appropriate instructions. Each connector must pass a quality control test using NRAO-provided dial indicators. All . 141 coax must be handfitted to the appropriate RF components using the bending tool provided in the tool kit. No coax shall be bent to a radius less than that possible using the bending tool. The finished coax shall be free of kinks or scratches and shall be cleaned of rosin.

1. Rear panel $J 4$ to l-2 GHz amplifier input using one OMQ3043-75 (58) and one OSM 201-1A (60). (5 3/4n).
2. 1-2 GHz amplifier output to bandpass filter using two OSM 201-1A (60-2) (81 ${ }^{\prime \prime}$ ).
3. Bandpass filter to Harmonic Mixer Sub-assembly Jl using Our OSM 201A (60) and one OSM 221-1 (73) (714").
4. Rear panel Jl6 to SPST pin diode switch J2 using one OMQ 3043-75 (58), and one OSM 201-1A (60) (22 5/8").
5. Rear panel Jl5 to RCV amplifier output using one OMQ 3043-75 (58) and one OSM 201-1A (60) (71 ${ }^{\text {n }}$ ).
L. Fabricate and install wire harness to all components, subassemblies, front panel, and rear panel using wire harness drawing Dl3440Pll. All wire is color coded No. 22 AWG stranded (113), RG-174 (62) and RG-188 coax (112). Use manufacturers instructions for coax connectors. Heat shrink tubing will be used on all wire terminations except the PC board connectors and rear panel connector wire pins. Wires that terminate on a solder pin will be soldered. In some cases two or three wires may terminate at one point (if specified by the wire list). Solder terminations of stranded wire shall be neat and free of excess solder and wire whiskers. Solder flux residue shall be cleaned.

Hand wiring shall be neatly dressed into bundles. Sufficient service loops shall be used to permit the front panel and the PC cards to be "folded" open for access. Wire bundles shall be confined with lacing cord or plastic ty-wraps.

The following items are used on the wire harness.

1. Connector pins, yellow/red (40-18).
2. OMQ 3043-53 connector (59).
3. $O S M$ 5ll-3 plug, RG-188 (61-6).
4. OSM 531-1 plug, right angle, RG-188 (68-4).
5. 14 pin platform (109-3).
6. Platform cover (110-3).
7. DAl5P connector (45).
8. Connector hood (46).
A. Hood is attached to connector using two No. 4-40 x. 25 pan head screws (36-2), two internal tooth lockwashers (42-2), and hex nuts (37-2).
9. DE95 connector (108).
10. Connector hood (126).
A. Hood is attached to connector using two No. 4-40 x. 25 pan head screws (36-2), internal tooth lockwashers (42-2), and hex nuts (37-2).
11. BNC crimp type plugs, 31-315 (65-2).
M. Install the following sub-assemblies.
12. Phase lock unit sub-assembly (2) using two No. 8-32 x .375 binder head screws (34-2).
13. Voltage regulator sub-assembly (3) using four No. 4-40 x . 250 binder head screws (101-4).
14. Synchronous debounce sub-assembly (5) using three No. 4-40 x . 250 binder head screws (101-3).
15. Pin diode driver sub-assembly (7) using No. 4-40 $\times .250$ binder head screws (101-4).

Connect wire harness to sub-assemblies.
N. Complete the mechanical assembly by installing the following components.

1. Two perforated covers (11-2).
2. Two support bars (10-2) using two No. 6-32 x . 375 flat head crossed recessed screws (31-2) in front panel and two No. 6-32 x . 25 flat head screws (26-2) in rear panel.
3. Four guides (14-4) on rear panel using four No. 6-32 $x$ $.625(28-4)$ and four No. 6-32 x . 875 (27-4) pan head slotted screws.
4. Threaded spacer (33) to rear panel using one No. 6-32 $x$ . 375 pan head screw (32) and internal tooth lockwashers (97).
5. Right side plate (9) using six No. 6-32 x . 25 flat head screws (26-6).
6. Four captive screws (21-4) in front panel using NRAOsupplied installation tool.
P. The waveguide brackets $(22,24)$ will be installed by NRAO. The waveguide installed in step "G" must be removed prior to shipment. Each module shall be individually wrapped with a protective covering and packed carefully in durable shipping containers to prevent damage.


FIGURE 1: "FRONT PANEL - FRONT VIEW"


FIGURE 2: "FRONT PANEL - REAR VIEW"


FIGURE 3: "Right-hand side view, complete"


FIGURE 4: "RIGHT-hand side View, less printed circuit boards"


FIGURE 5: "PHASE LOCK UNit"


FIGURE 6: "rear panel"

NAME Harmonic Mixer Mount

DATE October 5, 1976

PREPARED BY
APPROVED BY

## 1. APPLICATION

A harmonic mixer mount, consisting of crossguide coupler, diode mount and adjustable short for diode tuning is required. The unit shall be used with a 2400 MHz signal source to produce a 10 MHz IF beatnote between a harmonic of the 2400 MHz source and a Gunn oscillator output signal for the purpose of phase locking said oscillator.

## 2. FREQUENCY RANGE

All specifications shall be met in one of two broadband frequency ranges. Each range shall cover frequencies of operation related to channel numbers given by the following table:

| CHANNEL | FREQUENCY <br> GHz |
| :---: | :---: |
| 1 | 26.41 |
| 2 | 28.79 |
| 3 | 31.21 |
| 4 | 33.59 |
| 5 | 36.01 |
| 6 | 38.39 |
| 7 | 40.81 |
| 8 | 43.19 |
| 10 | 45.61 |

One range shall cover channels 1-6 (WR-28) and the other range shall cover channels 7-10 (WR-19).

Harmonic mixer mounts will be ordered by one of these two channel number ranges.

## 3. COUPLING

The cross guide coupler shall provide $20 \pm 3.5 \mathrm{~dB}$ coupling with 13 dB minimum directivity.
4. DIODE MOUNT

A diode mount to fit the Aertech Model No. A2S123 diode is required.
5. TUNING

The diode mount is to be tuned by an adjustable short with enough range to provide at least one tuning peak at each channel in the given range.

## 6. COAX CONNECTOR

One side of the diode shall be DC grounded with the other side connected to a female SMA connector. No bypassing shall be used, and only a low loss dielectric such as Teflon shall be utilized for the connector.

## 7. MARKING

The direction of coupling shall be indicated by a symbol as shown on NRAO drawing No. Cl3440P23.

## 8. MECHANICAL CONFIGURATION

The unit must conform to the mechanical specifications of the harmonic mixer mount outline drawing No. Cl3440P23.

## 9. DOCUMENTATION

A chart of coupling and directivity for each channel frequency in the given range shall be provided.

# NATIONAL RADIO ASTRONOMY OBSERVATORY 

Charlottesville, Virginia
VERY LARGE ARRAY PROJECT

```
SPECIFICATION NO: Al3450N1
NAME: Solid State Amplifier
DATE: February 5, 1974
PREPARED BY:
APPPROVED BY:
1. FREQUENCY RANGE: 1.0-2.0 GHz
2. GAIN: 23,5-30 dB (gain of individual units of given type to be equal within
    +1 dB).
3. GAIN FLATNESS: +1 dB
4. POWER OUTPUT: +7 dBm minimum at I dB compression
5. NOISE FIGURE: 6 dB max.
6. VSWR: 2.0 max. (input and output)
7. GATING SPEED: The amplifier must switch on or off in less than 10 microseconds
when the power supply voltage is gated on and off. Switching
time is defined as rise or fall time from 10% to 90% of final
RF power. Insertion loss should be greater than 13 dB from
l to 2 GHz when gated off.
8. INPUT POWER: +15V
9. CONNECTORS: SMA Female
```

10. Manufacturer is to state whether unit is discrete component construction and whether it is reparable in the event of a transistor failure.
12.0 DATA SHEETS

## Series <br> A2S100 <br> A2S700



$$
\begin{aligned}
& C_{P} \supseteq .1 \mathrm{DF} \\
& L_{P} \supseteq \mathrm{nH}_{V}
\end{aligned}
$$

CASF STYLE "P"


## FEATURES

$\square \mathrm{NF}_{0} 6.0 \mathrm{~dB}$ - X-BAND MIXER
$\square \mathrm{NF}_{\mathrm{o}} 6.5 \mathrm{~dB}$ - Ku-BAND MIXER
$\square$ HIGH BURN OUT

## ENVIRONMENTAL RATINGS

| Rating | Mil-Std <br> 750 <br> Method | Conditions |
| :--- | :---: | :---: |
|  |  |  |
| Temperature, Storage | 1031 | $-60^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Temperature, Operating | - | $-60^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Temperature, Cycling | 1051 | $-60^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Shock | 2016 | $1500 \mathrm{G}, 0.5 \mathrm{mSec}$. |
| Vibration | 2056 | $20 \mathrm{G}, 100-2000 \mathrm{~Hz}$ |
| Constant Acceleration | 2006 | $20,000 \mathrm{G}$ |
| Soldering Temperature | - | $230^{\circ} \mathrm{C}, 5 \mathrm{Secs}$. |
| Power Dissipation | - | $200 \mathrm{~mW} @ 25^{\circ} \mathrm{C}$ |
|  |  | Derate to OmW |
|  | $@ 150^{\circ} \mathrm{C}$ |  |

## DESCRIPTION

Aertech Schottky Barrier Diodes use metallurgical bonds throughout. Semiconductor processing, surface cleaning, passivation and metalization processes have been specially developed to provide reliable and reproducible performance. Special features have been incorporated to enhance pulsed power handling capabilities. Custom devices to individual or Hi-Rel specifications are available on special request.

The A2S100 Series employs a relatively high barrier metal/ silicon schottky junction. This process creates diodes with very low noise figure, which are capable of operation in extreme Hi -Rel applications.

The A2S700 Series employs a medium barrier height metal/ silicon schottky junction. This allows for operation at low local oscillator power levels.

## MIXER DIODES <br> SPECIFICATIONS @ + $\mathbf{2 5}{ }^{\circ} \mathrm{C}$

## A2S100 SERIES - HIGH TURN ON

| Aortech Type <br> Number | Test Frequency ${ }^{6}$ (GHz) | $\begin{gathered} \text { Case } \\ \text { Style 1,6 } \end{gathered}$ | Noise Figure ${ }^{2}$ |  | $\begin{gathered} \text { Max } \\ \text { VSWR }^{2} \end{gathered}$ | $z_{1 F^{2}}$ <br> (Ohms) | Typical Parameters ${ }^{3}$ |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typ (dB) | Max (dB) |  |  | $\begin{gathered} C_{j o} \\ (p \mathrm{~F}) \end{gathered}$ |  | $\begin{gathered} R_{g} \text { (Ohms) } \\ 50 \mathrm{~mA} \end{gathered}$ |
| A2S101 | 9.375 | P | 5.6 | 6.0 | 1.5 | 200-400 | 0.12 | 3.0 | 2 |
| A2S102 | 9.375 | P | 6.0 | 6.5 | 1.5 | 200-400 | 0.12 | 3.0 | 3 |
| A2S103 | 9.375 | P | 6.5 | 7.0 | 2.0 | 200-400 | 0.12 | 3.0 | 3.5 |
| A2S106 | 9.375 | $L$ | 5.6 | 6.0 | 1.5 | 200-400 | 0.12 | 3.0 | 2 |
| A2S107 | 9.375 | L | 6.0 | 6.5 | 1.5 | 200-400 | 0.12 | 3.0 | 3 |
| A2S108 | 9.375 | L | 6.5 | 7.0 | 2.0 | 200-400 | 0.12 | 3.0 | 3.5 |
| A2S121 | 16.0 | P | 6.0 | 6.5 | 1.5 | 175-350 | 0.10 | 2.0 | 2.5 |
| A2S124 | 16.0 | P | 6.5 | 7.0 | 2.0 | 175-350 | 0.10 | 2.0 | 3.5 |
| A2S122 | 16.0 | L | 6.0 | 6.5 | 1.5 | 175-350 | 0.10 | 2.0 | 2.5 |
| A2S123 | 16.0 | L | 6.5 | 7.0 | 2.0 | 175-350 | 0.10 | 2.0 | 3.5 |

Note: Above available in case style H .

A2S700 SERIES - MEDIUM TURN ON

| $\begin{aligned} & \text { A25762 } \\ & \text { A25763 } \end{aligned}$ | $\begin{array}{r} 9.375 \\ 9.375 \end{array}$ | $\begin{aligned} & \mathbf{H} \\ & \mathbf{H} \end{aligned}$ | $\begin{array}{r} 6.0 \\ 6.5 \\ \hline \end{array}$ | $\begin{aligned} & 6.5 \\ & 7.5 \end{aligned}$ | $\begin{aligned} & 1.6 \\ & 1.6 \\ & \hline \end{aligned}$ | $\begin{aligned} & 200-500 \\ & 200-500 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.12 \\ & 0.15 \\ & \hline \end{aligned}$ | $\begin{array}{r} 2.0 \\ 2.0 \\ \hline \end{array}$ | $\begin{gathered} 8 \\ 10 \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A2S701 | 9.375 | P | 5.8 | 6.0 | 1.5 | 200-400 | 0.15 | 2.0 | 9 |
| A2S702 | 9.375 | P | 6.3 | 6.5 | 2.0 | 200-400 | 0.15 | 2.0 | 9 |
| A2S703 | 9.375 | P | 6.8 | 7.0 | 2.0 | 200-400 | 0.15 | 2.0 | 9 |
| A2S711 | 9.375 | L | 5.8 | 6.0 | 1.5 | 200-400 | 0.15 | 2.0 | 9 |
| A2S713 | 9.375 | L | 6.3 | 6.5 | 2.0 | 200-400 | 0.15 | 2.0 | 9 |
| A2S714 | 9.375 | L | 6.8 | 7.0 | 2.0 | 200-400 | 0.15 | 2.0 | 9 |
| A2S720 | 16 | $P$ | 6.3 | 6.5 | 1.5 | 200-400 | 0.12 | 2.0 | 9 |
| A25722 | 16 | P | 6.8 | 7.0 | 2.0 | 200-400 | 0.12 | 2.0 | 9 |
| A2S723 | 16 | L | 6.3 | 6.5 | 1.5 | 200-400 | 0.12 | 2.0 | 9 |
| A2S721 | 16 | L | 6.8 | 7.0 | 2.0 | 200-400 | 0.12 | 2.0 | 9 |

NOTES:

1. Heat sink is the cathode.
2. Single sideband overall noise figure, resistive image termination:

$$
\begin{aligned}
& P_{L O}=1 \mathrm{~mW} \\
& N_{I F}=1.5 \mathrm{~dB} \text { @ } 30 \mathrm{MHz} \\
& R_{L} \leqslant 10 \text { ohms }
\end{aligned}
$$

3. Single diodes are available as matched pairs or quads. Suffix " $M$ " denotes a pair; " $\mathbf{Q}^{\prime \prime}$ denotes a quad.

$$
\begin{aligned}
& \Delta N F_{0} \leqslant 0.3 \mathrm{~dB} \\
& \Delta Z_{I F} \leqslant 25 \mathrm{ohms}
\end{aligned}
$$

4. $\mathrm{C}_{\mathrm{io}}$-Junction capacitance $\mathrm{V}_{\mathrm{R}}=0$ volt.
$V_{B R}$ - Measured at $I_{R}=10 \mu A$.
$\mathrm{R}_{\mathrm{s}}$ - Series resistance in ohms.
5. Available tested at 2 or 3 GHz .
6. Available in case style $\mathbf{H}$.

## FEATURES

| "ON" Resistance | $55 \Omega$ |
| :--- | ---: |
| Break-Before-Make Switching <br> Power Dissipation: |  |
| DTL/TTL/CMOS Compatible 3 mW <br> Switch Current  |  |
| Replaces DG-200 | 50 mA |

## GENERAL DESCRIPTION

The AD7513 is composed of two independent single-pole-single-throw switches on a CMOS chip. State-of-the-art design provides TTL/DTL/CMOS compatibility and a low power dissipation of 3 mW .
The AD7513 is an excellent replacement for reed relays and FET switches due to its low power dissipation, direct logic interface capability and low price. Its high surge current capability makes it ideal for use in integrator or sample/ hold circuits.

ABSOLUTE MAXIMUM RATINGS
( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ unless otherwise noted)

V ${ }_{\text {SS }}$ to GND . . . . . . . . . . . . . . . . . . . . . . -17 V
V Between any Switch Terminals . . . . . . . . . . . . +25 V
Switch Current (IDS, continuous) ........... 50 mA
Switch Current (IDS, Surge) --
1 ms duration, $10 \%$ duty cycle . . . . . . . . . . 150 mA
Digital Input Voltage Range . . . . . . . . . . . GND to V $_{\text {DD }}$
Power Dissipation
See page 32
Operating Temperature . . . . . . . . . $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
Storage Temperature . . . . . . . . . . . $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

## CAUTION:

1. Do not apply voltages higher than $V_{D D}$ and $V_{S S}$ to any other terminal, especially when $\mathrm{V}_{\mathrm{SS}}=\mathrm{V}_{\mathrm{DD}}=0 \mathrm{~V}$ all other pins should be at OV .
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

FUNCTIONAL DIAGRAM


LOGIC
Switch "ON" For Address "LOW"

## ORDERING INFORMATION

| PLASTIC DIP <br> (Suffix N) | TO-100 <br> (Suffix H) | OPERATING <br> TEMPERATURE RANGE |
| :--- | :--- | :--- |
| AD7513JN | AD7513JH |  |
| AD7513KN | AD7513KH | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ |
|  | AD7513SH <br> AD7513TH | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |

## PIN CONFIGURATION

| PLASTIC DIP | TO-100 |
| :---: | :---: |
| Top View | Top View |




## 3mm/SMA Coaxial Components



## TYPICAL PERFORMANCE-COAXIAL ATTENUATORS

|  | Attenuation db | Maximum Deviation from Attenuation at $1 \mathbf{G H z}, \mathrm{db}$ |  |  |  |  | VSWR, Maximum |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Model | at 1 CHz | $\text { at } 4 \mathrm{CHz}$ | at 8 CHz | $\text { at } 12 \mathrm{GHz}$ | at 18 GHz | $\mathrm{D}-4 \mathrm{GHz}$ | $4-8 \mathrm{GHz}$ | $8-12 \mathrm{GHz}$ | 12-18CHz |
| 4401 | $1.0 \pm 0.2$ | $\pm 0.2$ | +0.5 | +1.2 | $+2.0$ | 1.10 | 1.15 | 1.2 | 1.7 |
| 4403 | $3.0 \pm 0.2$ | $\pm 0.2$ | +0.4 | +0.8 | +1.7 | 1.10 | 1.15 | 1.3 | 1.7 |
| 4406 | $6.0 \pm 0.2$ | $\pm 0.2$ | $\pm 0.3$ | $+0.7$ | $+1.5$ | 1.10 | 1.15 | 1.3 | 1.7 |
| 4410 | $10.0 \pm 0.3$ | $\pm 0.2$ | $\pm 0.2$ | $\pm 0.3$ | $\underline{+0.5}$ | 1.10 | 1.25 | 1.5 | 1.7 |
| 4415 | $15.0 \pm 0.4$ | -0.5 | -1.3 | $-3.0$ | - 5.0 | 1.10 | 1.25 | 1.7 | 2.0 |
| 4420 | $20.0 \pm 0.5$ | -1.5 | -5.0 | -8.0 | -10.0 | 1,10 | 1.25 | 1.7 | 2.0 |

ORDERING INFORMATION: Insert db value for last two digits of model number, e.g., 4404 is a 4 db attenuator

## (妾毒 MICROWAVE, INC.

## SPECIFICATION AND TEST DATA REPoRT

K\& L Part No. 4 B/20-2Yeo/a once Curt. Part No. $\qquad$ Serial No. 5330 - 37,4e Date $3-11-2 C$

K \& L Order No. 4/96
Test Eng.
Q.C. Inspector


## SPECIFICATIONS

1.0 Ctr. Frequency 2 you MHz 2.0 Relative Bandwidth
$2.13 \mathrm{AB} \mathrm{BW} \quad \frac{2300}{2500}$
$2.2 \ldots \mathrm{~dB}$

MHz MHz


Impedance _50 Ohms
Size

TEST RESULTS

| 32 | 30 | 32 | 40 |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V$ | $V$ | $\sim$ | $\sim$ |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| 2240 | 2295 | 2290 | 229 |  |  |  |  |  |
| 2611 | 2508 | 2610 | 2506 |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| 0.6 | 0.6 | 0.6 | 0.6 |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| 2388 | 2341 | 2333 | 2340 |  |  |  |  |  |
| 2061 | 2450 | 2467 | 2468 |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |

Connectors $\operatorname{smA}-2$ Weight


The MC12040 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648). it is useful in a broad range of phase-locked loop applications. Operation of this device is identical to that of Phase Detector \#1 of the MC4044. A discussion of the theory of operation and applications information is given on the MC4344/4044 data sheet.

- Operating Frequency $=80 \mathrm{MHz}$ typical




## MC12040 (continued)

ELECTRICAL CHARACTERISTICS
The MC12040 has been designed to maet the dc apecifications ahown in the tent table after thermal equilibrium has been entablished. Outputs are terminated through a 50 ohm resistor to +3.0 V for +5.0 V tests and through a 50 ohm resistor to -2.0 V for -5.2 V tests.

supply Voltese $=-5.2 \mathrm{~V}$

| uppl |  |  |  |  |  |  |  |  |  | $\pi{ }^{\circ}$ | 0.720 | -1.30 | -1.06 | -1.450 | 52 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Pm |  |  |  |  | $0 \times$ |  |  |  | TEST | tace arm | IED TOPIN | LISTED Et |  |  |
|  |  | Unter |  | c |  | $2{ }^{4} \mathrm{C}$ |  |  | c |  | TET | , | -0 \% |  |  |  |
| Chemeswarie | Yomber | 1 Tm | min | mm | min | Tw | Mem | min | max | Unix | $\mathrm{V}_{\text {w }}$ | $V_{16}$ min | $v_{\text {ma }}{ }^{\text {min }}$ | velamea | VeE | 0 |
| Pomer Supply Ormen Current | ${ }^{\prime} \mathrm{E}$ | 7 | - | - | - 0 | $\rightarrow \infty$ | -120 | - | - | made | - | - | - | - | 1 | 1.14 |
| Input Cucianı | 'inm | 8 | - | - | - | - | 350 380 | - | - | Madk | 0 | - | - | - | 7 | 1.14 |
|  | TMNL | 8 | - | - | 0.5 0.5 | - | - | - | - | Hade | - | 8 | - | - | ; | 1.14 |
| Lose "1" <br> Ouepur volupp | Von(1) | $\begin{aligned} & 3 \\ & 4 \\ & 11 \\ & 12 \end{aligned}$ | $\left.\right\|^{-1.000}$ | ${ }^{-0,080}$ |  | - |  | $1$ | $\begin{array}{\|c\|} \hline-0.720 \\ \hline \end{array}$ | ${ }_{1}^{v *}$ | - | - | - | - | 1 | ${ }^{1.14}$ |
| Lasc <br> Cusput Youme | vot ${ }^{(1)}$ | $\begin{aligned} & 3 \\ & 4 \\ & 11 \\ & 12 \end{aligned}$ |  |  |  | - |  |  | $1$ | $1^{\text {vade }}$ | $\overline{-}$ | - | - | - | 1 | 1 |
| Lonce "1" <br> Tirsmoted valume | Vowa ${ }^{\text {a }}$ | $\begin{aligned} & 3 \\ & 4 \\ & 11 \\ & 12 \end{aligned}$ |  | - |  | = | - |  | - |  | - | $\overline{-}$ |  | - | 1 | $1^{1,14}$ |
| Love "0" <br> Theranad Values | vola (2) | 3 4 11 12 | - |  | - | - | $1$ | - | $\int_{1}^{-1.87}$ |  | - | - | 8 | 6 8 8 | $i$ | ${ }_{1}^{1.14}$ |



[^2]

NOTES:

1. All input and output cables to the ecope are equal lengthe of $50 \Omega$ cosxial cabla.
2. Unused input and outputs are connected to $550 \Omega$ resistor to ground.
3. The device under teet must be precondi. tioned before performing the ec tente. Preconditioning may be eccomplished by epplying pulse generator 1 for a minimum of two pulses prior to pulse generater 2. The device must be preconditioned again when inputs to pime 6 end 9 are interwhen inputs to pims 6 end ach applies.



## APPLICATIONS INFORMATION

The MC12040 is a logic network designed for use a phme comparator for MECL-compotible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of 42 m radians.

Operation of the device may be illustrated by assuming two weveforms, $R$ and $V$ (Figure 11 , of the same frequency but ditfering in phese. If the logic had established by past history that $R$ was lesding $V$, the $U$ output of the detector (pin 4) would produce a positive pulse width equat to the phase diffarence and the $\mathbf{D}$ output (pin 11 ) would simply remain low.

On the other hand, it is also poasible that $V$ wes leading $R$ (Figure 11, giving rise to a positive pules on the D output and a constant low level on the $U$ output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on pest edge crossing and initial conditions at atart-up. A stable phase-locked toop will result from either condition.

Phase error informetion is contained in the output duty cycle that is, the ratio of the ourput pulse width to total period. By integrating or low-pess filtering the cutputs of the detector and shifting the tevel to eccommodete ECL swings, usable anatoy information for the voltege-controlled oscillator can be developed. A circuit useful for this function is shown in Figure 2.

Proper Ievel shifting is acomplished by differentially driving the operational amplifier from the normally high outputs of the phase


FIGURE 2 - TYPICAL FILTER AND SUMMING NETWORK

detector ( 0 and $\overline{\mathrm{D}}$ ). Using this technique the quiescent differential voltege to the operational emplifier is zero fessuming matched " 1 " levels from the phase detector). The 0 and 0 outputs are then used to pass along phase information to the operational amplifier. Phase error summing is accomplished through resistors R1 connected to the inputs of the coperational emplifier. Some R-C filtering inbedded with in the inpul network (Figure 2) mey be very beneficial since the very narrow correctional pultes of the MC12040 woutd not normelly be integrated by the emplifier. General dosign quides for calculating R1. R2, and C are included in the MC4044 data sheet. Phase detactor gain for this configuration is approximately 0.16 volts/redian.

System phase error stems from input offeet voltege in the operational amplifiar, mismatching of nominally equad resistors, and mismatching of phase detector "high" states between the outputs used for threshold setting and phase measuring. All these effects ere refiected in the gein constant. For example, 16 mV offset voltage in the amplifier would cause an error of 0.016/0.16= 0.1 radian or 5.7 degrees of error. Phase arror can be trimmed to zero initially by trimming either input offset or one of the threshold resistors (R' in figure 2t.- Phase error over temperature depends on how much the offending parameters drift. If better performance were desired, the "charge pump" concept of the MC4044 could be implemented and uubequent errors could be reduced considerably since offsets no longer enter the picture.


DIMENSION "L" TO CENTER OF
LEADS WHEN FORMED PARALLEL.


Al JEDEC dimensions and notes apply.
CASE 632
TO. 116

## Operational Amplifiers

## LM318 operational amplifier general description

The LM318 is a precision high speed operational amplifier designed for applications requiring wide bandwidth and high slew rate. It features a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

## features

- 15 MHz small signal bandwidth
- Guaranteed $50 \mathrm{~V} / \mu \mathrm{s}$ slew rate
- Maximum bias current of 500 nA
- Operates from supplies of $\pm 5 \mathrm{~V}$ to $\pm 20 \mathrm{~V}$
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

The LM318 has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary


#### Abstract

for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over $150 \mathrm{~V} / \mu \mathrm{s}$ and almost double the bandwidth. Overcompensetion can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the $0.1 \%$ settling time to under $1 \mu \mathrm{~s}$.

The high speed and fast settling time of these op amps make them useful in A/D comverters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

The LM318 is specified for operation over $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$.


schematic diagram and typical application


Instrumentotion Amplifier
connection diagrams

*Pin connections shown on schematic diagram and typical applications ere for TO.5 packere.

Order Number LM318H See Paekage 11


Order Number LM318N See Package 20

Dual-In-Line Peckuge


Order Number LM318D See Packrige 1

| absolute maximum ratings |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
| Input Offset Voltage Input Offset Current Input Bias Current Input Resistance <br> Supply Current <br> Large Signal Voltage Gain <br> Slew Rate <br> Small Signal Bandwidth <br> Input Offset Voltage <br> Input Offset Current <br> Input Bias Current <br> Large Signal Voltage Gain <br> Output Voltage Swing <br> Input Voltage Range <br> Common Mode Rejection Ratio <br> Supply Voltage Rejection Ratio | $\begin{aligned} & T_{A}=25^{\circ} \mathrm{C} \\ & T_{A}=25^{\circ} \mathrm{C} \\ & T_{A}=25^{\circ} \mathrm{C} \\ & T_{A}=25^{\circ} \mathrm{C} \\ & T_{A}=25^{\circ} \mathrm{C} \\ & T_{A}=25^{\circ} \mathrm{C}, V_{S}= \pm 15 \mathrm{~V} \\ & V_{O U T}= \pm 10 \mathrm{~V}, R_{L} \geq 2 \mathrm{k} \Omega \\ & T_{A}=25^{\circ} \mathrm{C}, V_{S}= \pm 15 \mathrm{~V}, A, A=1 \\ & T_{A}=25^{\circ} \mathrm{C}, V_{S}= \pm 15 \mathrm{~V} \end{aligned}$ $\begin{aligned} & V_{S}= \pm 15 \mathrm{~V}, V_{\text {OUT }}= \pm 10 \mathrm{~V} \\ & R_{L} \geq 2 \mathrm{k} \Omega \\ & V_{S}= \pm 15 \mathrm{~V} . R_{L}=2 \mathrm{k} \Omega \\ & V_{S}= \pm 15 \mathrm{~V} \end{aligned}$ | 0.5 <br> 25 <br> 50 <br> 20 <br> $\pm 12$ <br> $\pm 11.5$ <br> 70 <br> 65 |  | 10 <br> 200 <br> 500 <br> 10 <br> 15 <br> 300 <br> 750 | $m V$ $m A$ $m A$ $m \Omega$ $m A$ $V / m V$ $V / \mu s$ $M H z$ $m V$ $n A$ $n A$ $V / m V$ $V$ $V$ $d B$ |

Note 1: The moximum junction temperature of the LM318 is $85^{\circ} \mathrm{C}$. For opersting at elevated temperatures, devices in the TO-5 peckege must be derated based on a thermal resistance of $150^{\circ} \mathrm{C} / \mathrm{W}$. junction to ambient, or $45^{\circ} \mathrm{C} / \mathrm{W}$, junction to cese. The thermel rasistance of the dual-in-line peckage is $100^{\circ} \mathrm{CM}$, junction to ambient.
Note 2: The inputs are shunted with beck-to-beck diodes for overvoltege protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is epplied between the inputs unless some limiting resistence is used.
Note 3: For supply voltages leas then E 15 V , the sbsolute maximum input voltage is equal to the supply voltege.
Note 4: These specifications apply for $\pm 5 \mathrm{~V} \leq V_{S} \leq \pm 20 \mathrm{~V}$ and $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$, uniess otherwise apecified. For proper operation, the power supplies must be bypassed with $0.1 \mu \mathrm{~F}$ disc capecitors.





[^0]:    RT INCIOENT BOWGR T OOEM

[^1]:    

[^2]:    (1) Ourputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests.
    (2) The device must atso function eccording to the truth table churing these tests

