VLA Technical Report No. 29

AN INTRODUCTION TO THE VLA ELECTRONIC SYSTEM

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Acknowledgement The electronic system of the VLA was conceived in most essential details by Sander Weinreb in 1972-3. Many members of the VLA Electronics Division as well as the author have contributed to the subsequent development of the electronics described here, both in refinement of system details and design of the hardware required.

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I. INTRODUCTION

The basic purpose of the VLA is to map the brightness of electromagnetic radiation from the sky with a resolution comparable to that of a large optical telescope, but at wavelengths longer than those of light by a factor of the order of 10^5. This calls for an array with dimensions of several tens of kilometers, and the VLA takes the form of an equiangular wye with nine antennas on each arm extending to 21 km from the center. The scale of the array can be reduced in four steps to give a range of 35 to 1 in resolution at any wavelength. When observing the antennas track a chosen area of sky, and the received signals are transmitted back to a central location where they are processed to produce a map of the area observed.

This report outlines the basic requirements of the receiving electronics and then goes on to describe in more detail the block diagram of the system that has been developed. We are not concerned here with the principles by which a radio map of the sky is obtained, except to remark that with 27 antennas there are 351 possible antenna pairs. Signals from each of these pairs are combined so that the array can be considered as a large collection of two-element, multiplying interferometers. Principles of operation of the two-element interferometer will be found, for example, in Krauss (1966), and a detailed mathematical analysis is given by Swenson and Mathur (1968).

A simplified schematic diagram to illustrate the basic requirements of the electronic system is given in Figure I-1. At the antennas the received signals are amplified in a front-end system designed to have low input noise temperatures. The signals are then converted to intermediate frequencies and transmitted via a buried waveguide to the control building near the center of the array. Here the signals from each antenna are combined in a multiplier system with the corresponding signals from every other antenna of the array. Signal voltages are multiplied and the time averages of the products yield the complex visibility from which the desired brightness distribution can be obtained by Fourier transformation.

An incoming wavefront from a source is intercepted at different points in its path by different antennas, and the path lengths in the transmission system from the antennas to the central location are also different. Time delays which compensate for these different signal paths must therefore be introduced before the signals reach the multipliers. Since the free-space component of the differing path lengths varies as the earth rotates, the compensating delays must be continuously variable under computer control.

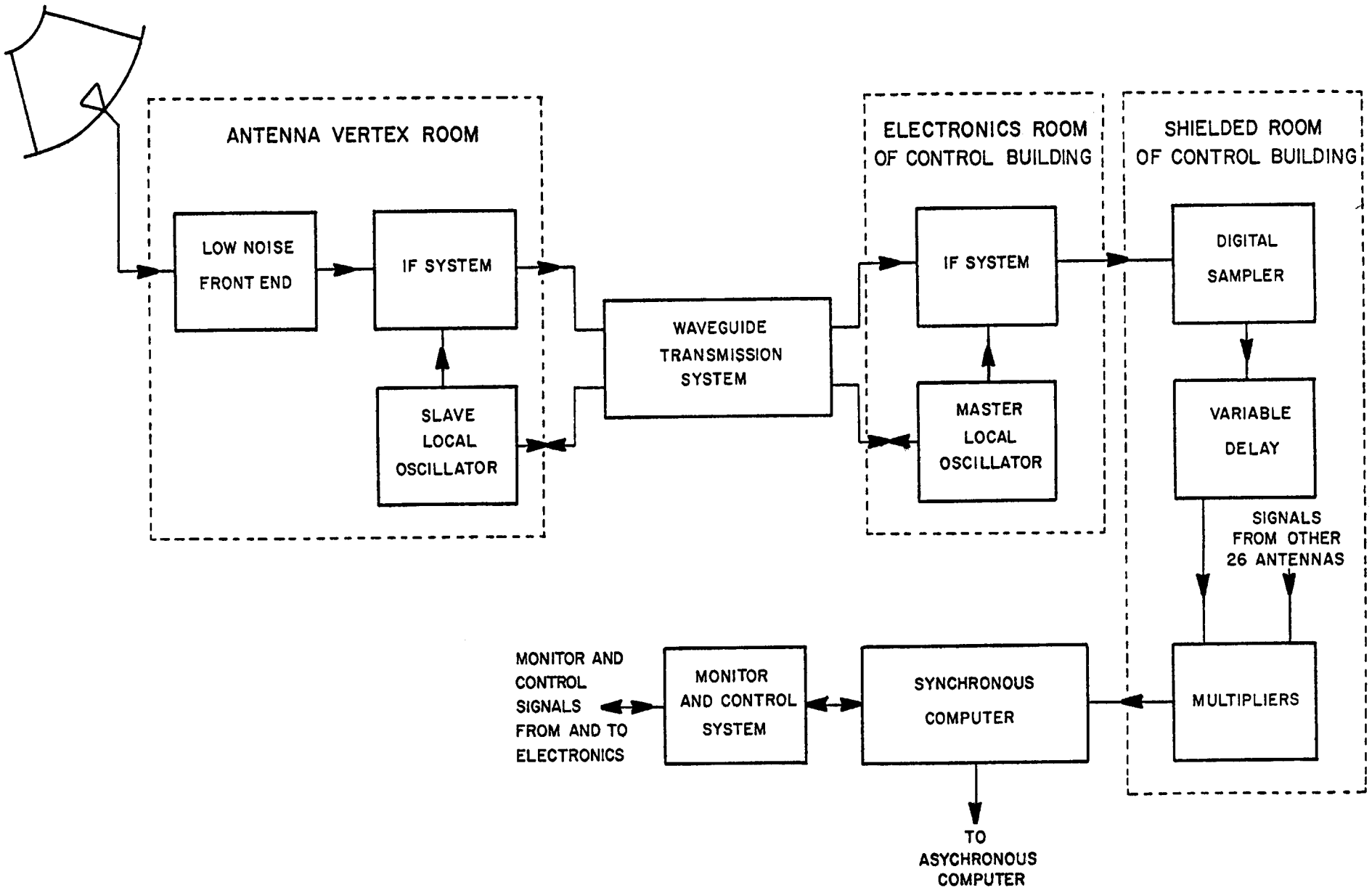


Figure I-1 Basic block diagram of the electronic receiving system. Note that one each per antenna is required for the following blocks: Front End, IF, Slave L.O., Sampler, Delay, Monitor and Control.

The local oscillator signals used in the frequency conversions at each of the antennas must be synchronous in phase to preserve the correlation of the received signals. The oscillators at the antennas are therefore all phase locked to a master oscillator at the control building. Two precisely controlled phase shifts are introduced in the frequency conversion at the antennas. These are a 180^{o} switched phase change which helps to eliminate unwanted offsets in the multiplier outputs and a linearly varying phase shift to compensate for the phase changes in the varying space-transmission paths. The latter is required because the variable time delays are introduced at an intermediate frequency and therefore do not compensate for phase changes of the signals in free space. In interferometer terminology the linear phase shift reduces the frequency of the output fringe patterns to zero.

The computer that controls the antennas and the whole receiving system is referred to as the synchronous computer. It communicates with the electronics through a digital monitor and control system. The synchronous computer also gathers the data from the multipliers and does some initial averaging of it. The main computing tasks in deriving a map are performed by a large computer, the asynchronous computer, that works off-line.

Among the most important considerations in the electronic design are the phase stability, gain stability, frequency responses and signal to noise ratios in the system. The accuracy with which the phases of signals received at the different antennas can be compared is of fundamental importance since it directly affects the accuracy with which the positions of features on the sky can be measured. The relative phases of the local oscillators and the phase changes in the RF and IF signal paths are all involved. Phase characteristics which do not vary with time present no problems since they can be calibrated and removed by observing the signals from any unresolved radio source for which the position is accurately known. It is the time variations in phase which result from changing temperatures, voltages and atmospheric conditions that must be minimized. Similarly the overall gain from each antenna to the multiplier inputs must be constant, but here automatic level control loops simplify the problem.

Low noise input devices are used at the antennas to achieve the best possible sensitivity and care must be taken to ensure that the signal to noise ratio does not become degraded by noise introduced at later stages in the signal paths. Loss in sensitivity can also result from differences

in the phase-frequency responses of the channels from the different antennas, from deviations from flatness of the amplitude-frequency responses, from inaccuracies in the delay system and various other instrumental characteristics. Keeping these unwanted effects within acceptable limits has been a major consideration in the electronic design, and more detailed discussions of the tolerances involved will be found in various VLA Electronics Memoranda.

For convenience the array electronics can be divided into the following subsystems: the Front End, the Oscillator System, the Waveguide Transmission System, the IF System, the Delay and Multiplier System, and the Monitor and Control System. The basic design requirements in each of these areas are outlined in the following section. Innovations which have not previously been used in radio astronomy will be found in the front end design, in the use of TE_{01} mode waveguide for signal transmission, and in the use of a digital delay system. The location and modular layout of the electronics is briefly described in Section III. In Section IV descriptions of the function of each module are given which should enable the reader to follow the full system block diagrams. Section V gives further details of the electronics, and some parameters of other parts of the array such as the antennas, wye and computers are listed in the appendix.

Detailed engineering descriptions of all parts of the electronics will be found in other reports in this series.

II. BASIC DESIGN OF THE RECEIVING SYSTEM

(a) The Front End

The front end is designed to cover four frequency bands of interest to radio astronomers and to achieve high sensitivity at a reasonable cost. A block diagram is shown in Figure II-1, and details of the input frequency bands are given in Table II-1. The four bands span a range of over four octaves from 1·34 to 24 GHz, and each one contains one of the frequency bands assigned to radio astronomy research.

The basic component of the front end is a parametric amplifier with a frequency response of 4·5-5 GHz. When cooled to 18K it has an input noise temperature of about 25 K. The prototype amplifier used three cooled stages, but the third was later replaced by a room-temperature transistor amplifier with a Ga As F.E.T. input stage. The parametric stages have 12 dB gain and for the early antennas were made by Comtech, Inc., but later by the Applied Electronics Division of AIL. The transistor amplifier has a gain of 40 dB and noise figure of 2·5 dB.

A latching coaxial switch allows the input of the parametric amplifier to be connected directly to the 4·5-5 GHz feed, through a parametric upconverter to the 1·34-1·73 GHz feed, or through cooled mixers to the 14·4-15·4 or 22-24 GHz feeds. The upconverter and the mixers are in the same 18K environment as the parametric amplifier. The parametric upconverter was developed for the VLA by the Applied Electronics Division of AIL. It has a gain of approximately 3 dB and is an inherently low noise device. The upconverter uses a fixed frequency pump at 3·2 GHz and covers a 400 MHz band with some tuning adjustment of the varactor bias and pump power. With the parametric amplifier as a second stage the input noise temperature of the upconverter is about 20K. The mixers for the 2 and 1·3 cm bands have input noise temperatures of 200 and 240K respectively. These figures apply to optimum performance at the band center and all of the noise temperature values given above increase by about 20% at the band edges except for the 1·3 cm band where the increase is nearer 40%. Details of the feed performance and system temperatures are given in Table II-2.

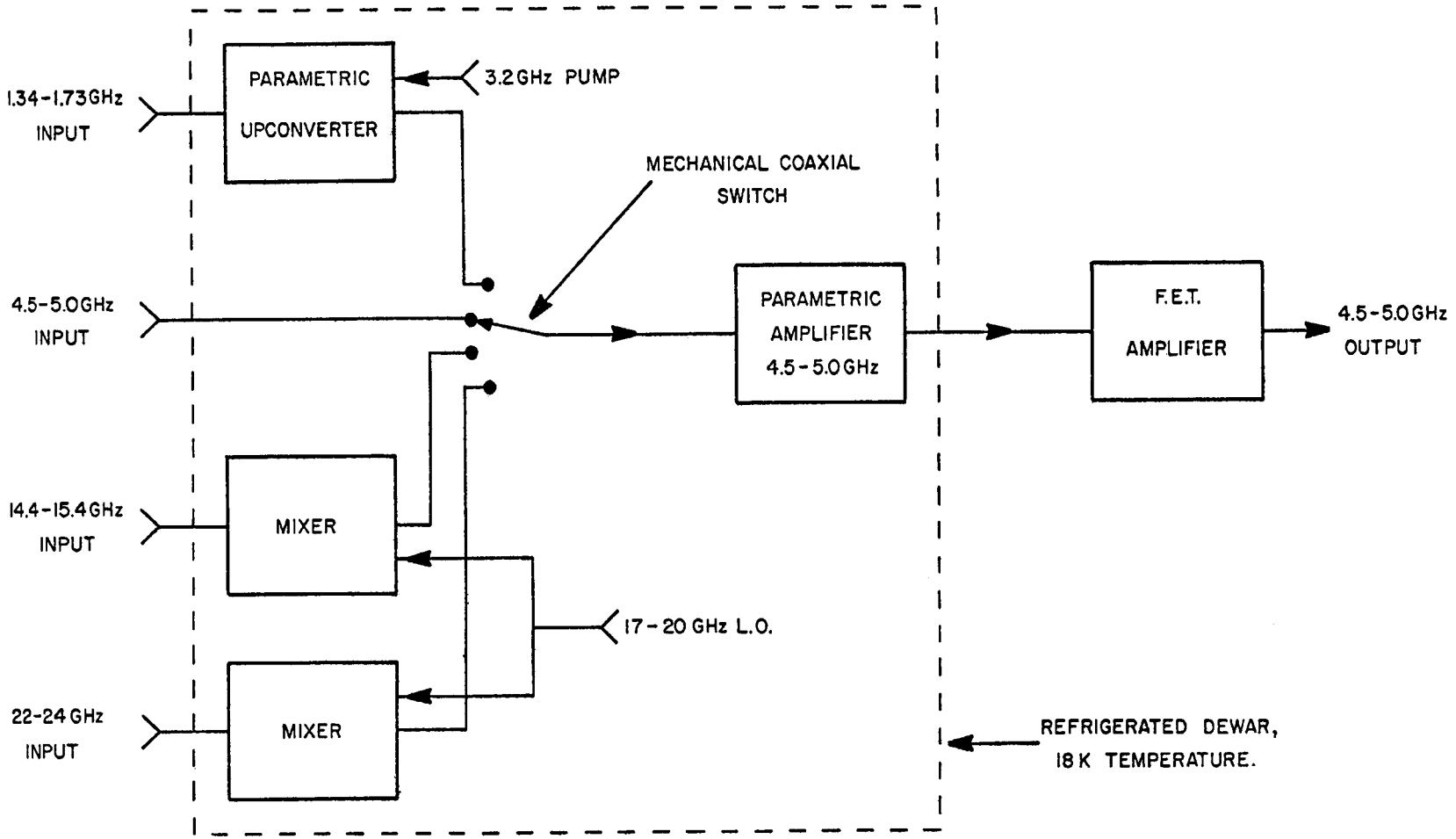


Figure II-1 Block diagram of the Front End. Two systems of the type shown, combined in the same Dewar, are used at each antenna to provide for two oppositely polarized outputs from each feed.

TABLE II-1 VLA OBSERVING BANDS

VLA BAND	WAVELENGTH	MINIMUM DETECTABLE SIGNAL (Approximate)	RADIO ASTRONOMY BAND	ATOMIC AND MOLECULAR LINES
1340-1730 MHz	18-21 cm	10^{-31} $Wm^{-2}Hz^{-1}$	1400-1427 MHz	Neutral Hydrogen 1420·4 MHz $HCONH_2$ (Formamide) 1538-1542 MHz OH 1612, 1665, 1667, 1721 MHz HCOOH (Formic Acid) 1639 MHz
4500-5000 MHz	6 cm	10^{-31} $Wm^{-2}Hz$	4990-5000 MHz	$HCONH_2$ (Formamide) 4617-4620 MHz OH 4660, 4751, 4766 MHz H_2CO (Formaldehyde) 4830 MHz
14·4-15·4 GHz	2 cm	$7x10^{-31}$ $Wm^{-2}Hz^{-1}$	15·35-15·40 GHz	H_2CO (Formaldehyde) 14·489 GHz
22·0-24·0 GHz	1·3 cm	$1·5x10^{-30}Wm^{-2}Hz^{-1}$	23·6-24·0 GHz	H_2O 22·235 GHz NH_3 (Amonia) 22·834-23·870 GHz

TABLE II-2 ANTENNA EFFICIENCIES AND SYSTEM TEMPERATURES

WAVELENGTH	APERTURE EFFICIENCY	SYSTEM TEMPERATURE[1]	TYPE OF FEED
21 cm 18 cm	50% 52%	50K 50K	Dielectric and waveguide lens illuminated by horn
6 cm	65%	50K	Corrugated horn
2 cm	54%	240K	Horn
1·3 cm	46%	290K	Horn

[1]Values given apply to the band center and increase by approximately 20% at the band edges for the three longest wavelength bands and by 40% for 1·3 cm.

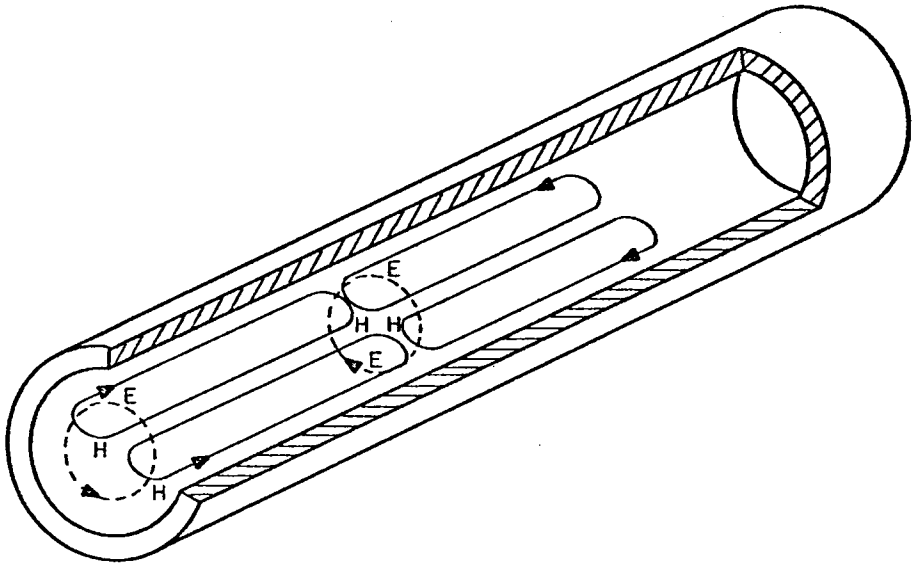


Figure II-2 The E and H field configurations for the TE_{01} mode in circular waveguide.

Two systems of the type described above are used in each front end to accept the two oppositely polarized outputs from each feed. The polarization modes can be opposite circular or crossed linear, and to change between these two possibilities requires manual replacement of the polarization transducer at the output of each feed. A dual frequency mode of operation is also possible in which one front end channel is connected to the 6 cm feed and one to the 2 cm feed. In this case a dichroic reflector in front of the 2 cm horn transmits radiation in this band but reflects 6 cm radiation to the 6 cm feed.

The two sets of front end circuitry are both mounted in a single rectangular Dewar of exterior dimensions 12"x18"x18". They are cooled by a closed cycle helium refrigerator with a cold-station at approximately 18K and an intermediate temperature station at 60K which is used to cool a radiation shield around the cold-station components. A mechanical pump capable of reducing the pressure down to 10^{-4} Torr[1] is mounted with the Dewar. The cryogenic pumping action of the refrigerator becomes effective at about 10^{-2} Torr and takes the pressure down to an operating value near 10^{-7} Torr. The Dewar is mounted in the upper part of the front end rack in the vertex room of the antenna, just below the feed mounting ring. The helium compressor for the refrigerator is located on the alidade platform of the antenna.

A description of the VLA front end has been published by Weinreb, Balister, Maas and Napier (1977). The outputs from the front end at 4·5-5·0 GHz go to the IF system where four bands, each 50 MHz wide, are selected for transmission to the control building. Two IF bands are taken from the output for each polarization.

[1] 1 Torr = 1 mm of mercury

(b) The Waveguide Transmission System

The use of TE_{01} mode waveguide for the transmission between the antennas and the control building is an innovation which has a considerable impact upon the overall electronic design. In other radio astronomy arrays coaxial cables have generally been used to transmit signals to and from the antennas. To achieve sufficient bandwidth with cable for the VLA, frequencies up to one or two gigahertz would have to be used, and even with low-loss cable the attenuation would necessitate the use of repeater amplifiers about every km. These would add considerably to the cost and complexity of the system, especially since signals must be transmitted in both directions. A waveguide system using the TE_{01} mode is therefore a very attractive alternative since a bandwidth of over 50 GHz is available with an attenuation of less than 1·5 dB per km and repeaters should not be necessary. Long transmission lines used in radio astronomy arrays, either cable or waveguide, are generally buried to reduce temperature variations which cause changes in electrical length.

The TE_{01} mode waveguide takes the form of a circular pipe, and that used on the VLA has an internal diameter of 60 mm. The field configuration is shown in Figure II-2. Modes of the circular electric type, TE_{on}, do not require longitudinal conductivity in the walls,and the inner surface of the waveguide is a closely wound helix of copper wire which permits currents to flow in the circumferential direction only. This is backed with a lossy material and surrounded by a steel pipe. Modes other than the circular electric type are not contained by the copper wire helix and are dissipated in the lossy material. The waveguide thus acts as a continuous filter to reject non circular-electric modes. The most troublesome unwanted modes which remain are TE_{02} and TE_{03}. The low loss depends upon the straightness of the waveguide as bends cause power to be converted to unwanted modes and absorbed. The additional loss for a curved section is given approximately by

$$\Delta \alpha = K \left(f/R\right)^2 \text{ dB per km}$$

where f is the frequency in GHz, R is the radius of curvature in meters, and K is a semi empirical constant which depends upon the waveguide structure and has a value of about 10 for the VLA waveguide. The loss in

a perfectly straight section of waveguide decreases as the ratio of the diameter to the wavelength increases, but the additional loss due to bends increases. As a result there is a frequency of minimum attenuation as shown in Figure II-3. The waveguide must be pressurized with dry nitrogen to avoid the attenuation due to oxygen at frequencies above 50 GHz.

TE_{01} mode waveguide is being developed in a number of countries for telephone trunk lines of high capacity. In many cases the helix type of waveguide is interspersed between longer section of dielectric waveguide in which the pipe has an inner conducting surface covered with a thin layer of dielectric. This latter type of waveguide has slightly lower loss but lacks the mode filtering property of the helix. Except for a few special components, all TE_{01} mode waveguide used in the VLA is of the helix type and is manufactured by the Fujikura, Furukawa or Sumitomo Companies of Japan. A general description of TE_{01} mode waveguide is given by Miller (1954) and an example of its application in communications is described by Abele, Alsberg & Hutchinson (1975).

In the VLA one trunk line of 60 mm diameter waveguide runs down each arm of the array. It is given a protective coating and directly buried at a depth of four to ten feet depending upon the level of the ground surface. Two zinc ribbons are buried above it for lightning and cathodic protection. The waveguide passes through a manhole at each antenna station and couplers are inserted at these points. For connection from the coupler to the vertex room of the antenna, waveguide of 20 mm internal diameter is used, since tighter bends can be tolerated in smaller waveguide. Flexible sections which can be bent to one meter radius and rotating joints are used in the 20mm runs.

The signals transmitted along the waveguide lie in the 27-53 GHz range. Local oscillator and IF signals are amplitude modulated onto microwave carriers in modem units which incorporate Gunn diode oscillators and diode mixers working as modulators. The same modems can be used in both transmit and receive modes, and in the latter case the Gunn diode acts as a local oscillator. A different carrier frequency is used for each antenna on any given arm of the wye. Table II-3 lists the frequency assignments of 11 channels of which numbers 1 and 11 are spares. At each antenna the modem connects to the TE_{01} mode waveguide by a rectangular to circular transition. At the control building the three trunk lines

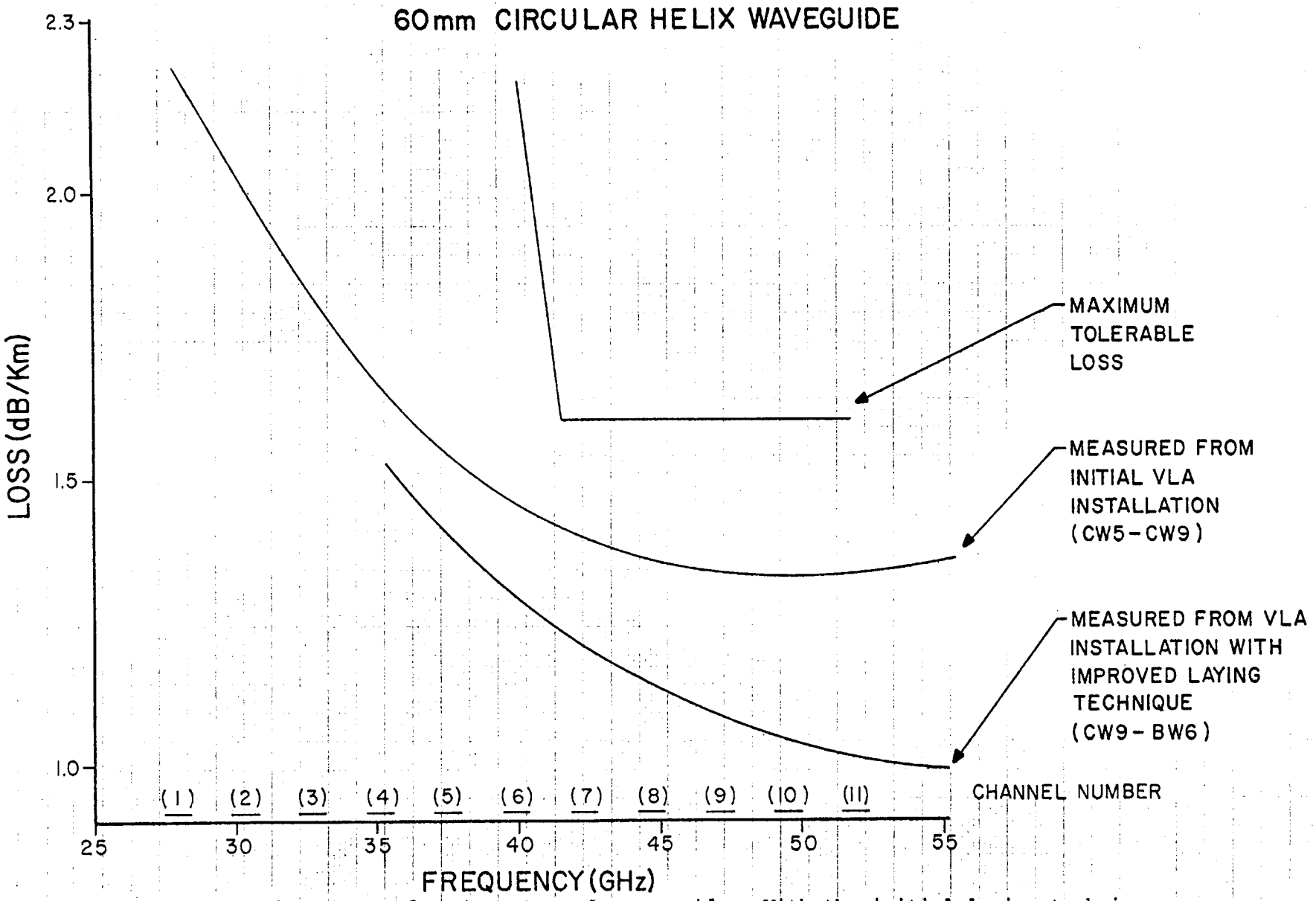


Figure II-3 Attenuation curves for the TE_{01} mode waveguide. With the initial laying technique the attenuation was found to increase during the backfilling of the trench, and a slow attenuation increase continued during subsequent months, attributable to soil settlement. The improved technique involves better compacting of the soil around the waveguide before backfilling, and subsequent attenuation increases are smaller. Both measured curves show data taken about two months after burial.

TABLE II-3 WAVEGUIDE CHANNEL FREQUENCIES

Channel Number	Carrier Frequency	Upper Sideband Frequencies
1	26·410 GHz	27·410 - 28·410 GHz
2	28·790 GHz	29·790 - 30·790 GHz
3	31·210 GHz	32·210 - 33·210 GHz
4	33·590 GHz	34·590 - 35·590 GHz
5	36·010 GHz	37·010 - 38·010 GHz
6	38·390 GHz	39·390 - 40·390 GHz
7	40·810 GHz	41·810 - 42·810 GHz
8	43·910 GHz	44·190 - 45·190 GHz
9	45·610 GHz	46·610 - 47·610 GHz
10	47·990 GHz	48·990 - 49·990 GHz
11	50·410 GHz	51·410 - 52·410 GHz

terminate in signal distributor units which perform a demultiplexing function and provide a separate output in rectangular waveguide for each of the channels in Table II-2. For every antenna there is a modem in the central building connected to one of these outputs. The signal distributor was developed for the VLA by the Hitachi Company of Japan.

Two characteristics of the waveguide impinge rather widely upon the design of the electronic system. The first is the dispersion in phase velocity which follows the usual waveguide formula

$$v = c\ (1-f_c^2/f^2)^{-\frac{1}{2}}$$

where v is the phase velocity at frequency f, c is the free space velocity and f_c is the waveguide cutoff frequency. The cutoff frequency varies with the mode and the waveguide diameter and is 3·83 GHz for TE_{01} in 60 mm diameter waveguide. The frequency band of the signals that must be transmitted in any one channel is sufficiently large that the velocity difference between the upper and lower sidebands would cause distortion in signals received after traversing a few kilometers of waveguide. Because of this, only one sideband is used in the signal transmission. To make the sidebands easily separable by filtering, all modulation signals lie in the range 1-2 GHz, and both the lower sideband and the carrier are removed by a filter in the output of the modem. The IF and local oscillator signals which go to and from the modems must therefore be arranged to lie in the 1-2 GHz band, a requirement which significantly affects the design of the electronics involved.

The second result of the waveguide characteristics is that simultaneous transmission cannot take place in two directions at once within the waveguide, and a time multiplexing sequence is required. Signals being transmitted and received simultaneously at any point in the waveguide could only be separated if they were sufficiently widely spaced in frequency. However, the operation of the system requires that signals go out and back to each antenna at very closely the same frequency in both directions. This is because the phases of the outgoing and incoming local oscillator signals are compared at the control building to monitor, and correct for, changes in the path length to each antenna. Errors in this round-trip phase measurement can be introduced by mismatches if the phase of the standing wave pattern varies significantly between the outgoing and incoming frequencies. Because

of the very low attenuation of the waveguide, small reflections cause effects at long distances which result in rapid variation of the standing wave pattern with frequency.[1] Thus the frequencies of signals to and from any antenna must not differ by more than a few kHz.[2]

To lose as little observing time as possible, received signals are transmitted back from the antennas for 51 ms out of every 52 ms and the local oscillator reference signals are transmitted out to the antennas during the remaining 1 ms. These figures are approximate and the exact frequency of the transmit-receive cycles is 19·2 Hz. This timing sequence has widespread effects on the design of the electronics system. It also necessitates the use of a high stability crystal oscillator for the slave oscillator at each antenna, as described in the following subsection.

The spectrum of the signals which are modulated onto each carrier of the waveguide transmission system is shown in Figure II-4. Signals transmitted out to the antennas are oscillator reference signals at 1200 and 1800 MHz with 5 MHz reference amplitude modulated onto the former and digital control signals modulated onto the latter. The same signals are transmitted back from the antennas with monitor data replacing the control signals and with the addition of four 50 MHz-wide IF bands centered at 1325, 1425, 1575 and 1675 MHz. The 1200 and 1800 MHz signals are used in converting the required IF signals to base band, and the phases of the transmitted signals are therefore independent of the phase stability of the carrier-frequency oscillators in the modems. The power levels transmitted from the modems are -2 or -8 dBm for the 1200 and 1800 MHz signals, depending on the direction, and -6 dBm for each IF band. The total loss between the modem at each antenna and the corresponding one in the control building is adjusted to be close to 56 dB in all cases.

A description of the waveguide system has been published by Weinreb, Predmore, Ogai and Parrish (1976).

[1]For example, a reflection of -26 dB at a distance of 5 km will produce a VSWR of 1·02, which can introduce a phase error of 1·14° between signals spaced 15 kHz in frequency.

[2]Note that there is some advantage in a small frequency offset as certain low-level spurious signals in the local oscillator system which would otherwise fall on top of wanted signals are then displaced by the frequency offset and phase errors that they would otherwise cause are averaged to zero. An offset of about 1 kHz is therefore introduced between the modem oscillators at the antennas and the corresponding ones in the control building.

(c) The Oscillator System

The oscillator system provides a series of frequencies at each antenna that are phase locked to a master oscillator at the control building. From these the various local oscillator signals required for frequency conversion of the received signals are synthesized. The system also contains provision for measuring the phase variation resulting from changes in the electrical path length of the waveguide so that compensation for this can be made in the computer. The system is designed to give an rms phase error of not more than one degree per gigahertz between corresponding signals at any pair of antennas. With this criterion, atmospheric effects should dominate the phase stability of the array.

First consider phase locking an oscillator at the antenna to a reference signal at the same frequency received over the waveguide transmission system. The reference signal appears for intervals of approximately 1 ms at a 19·2 Hz rate, and because of this a conventional phase lock circuit can lock the oscillator not only at the desired reference frequency but also at integral multiples of 19·2 Hz away from it. The unwanted lock frequencies occur because the relative phase of the oscillator and the reference changes by an integral multiple of 2π radians between reference samples, and thus to the phase detector the two signals appear to remain in phase. To avoid such undesirable offsets the oscillator at the antenna is a high stability crystal that cannot depart from its nominal value of 5 MHz by more than a fraction of one Hz. The required local oscillator frequencies are then generated by synthesis techniques, but to prevent phase ambiguities frequency division is generally avoided and most frequencies are multiples of 5 MHz. This permits a fine enough tuning interval at the antennas. The synthesis techniques result in rather more complex circuitry than is required in systems where the reference frequency from the central station is tunable, but are a direct result of the time shared transmission in the waveguide.

The accuracy with which the phase of the 5 MHz oscillator can be controlled depends upon the signal to noise ratio of the reference frequency. An effective improvement of almost 42 dB can be obtained by using a reference of 600 MHz instead of 5 MHz, and comparing this

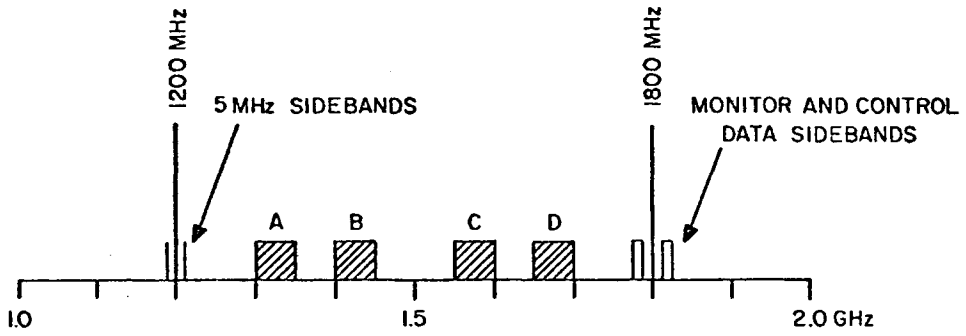


Figure II-4 The spectrum of the modulation in the waveguide transmission system. The IF signals A, B, C and D are present in transmission from the antennas only, but the other signals travel in both directions.

with 600 MHz generated by frequency multiplication from the 5 MHz oscillator. This is the adopted scheme, as shown in the block diagram of the oscillator system in Figure II-5. At the antennas signals are received at both 5 and 600 MHz, the former from the modulation on the 1200 MHz signal and the latter from the frequency difference between the 1200 and 1800 MHz signals. Locking only on the 600 MHz signal would result in phase ambiguities at intervals of 3^{o} in the 5 MHz oscillator. A phase comparison is therefore made at 5 MHz also, and the loop is first closed using the output of the 5 MHz phase detector. When the 5 MHz phase error is less than 1^{o}, control is switched over to the 600 MHz phase detector, and can be returned if the 5 MHz phase error becomes too large. The time constant on the phase lock loop is one second and another locked oscillator is used at 50 MHz to help reduce noise and unwanted sidebands.

To monitor the effects of variations in the electrical length of the waveguide the 5 and 600 MHz signals are transmitted back to the control building in the same way in which they are sent out. At the control building locked oscillators at 1200 and 1800 MHz remove the noise and sidebands on the received signals, and the 600 MHz difference frequency is derived and compared with 600 MHz from the master oscillator in a phase detector. The output of the phase detector goes to the synchronous computer.

To receive signals at any frequency within the front end passbands using 50 MHz-wide IF bands the local oscillator must be tunable in steps of 50 MHz or less. The chosen scheme makes use of a 2-4 GHz YIG-tuned oscillator that is phase locked to harmonics of 50 MHz with a 10·1 MHz IF offset in the loop. This allows tuning steps at alternate intervals of 20·1 and 29·9 MHz. In addition the local oscillator that converts signals in the 2 and 1·3 cm bands to the input frequency of the parametric amplifier is tunable in 100 MHz increments. At the control building, local oscillator signals for the final frequency conversions are tunable in 2 Hz steps. These are derived from frequency synthesizers in the master oscillator system and are distributed through a branching cable network to each of the 27 racks that receive the signals from the antennas.

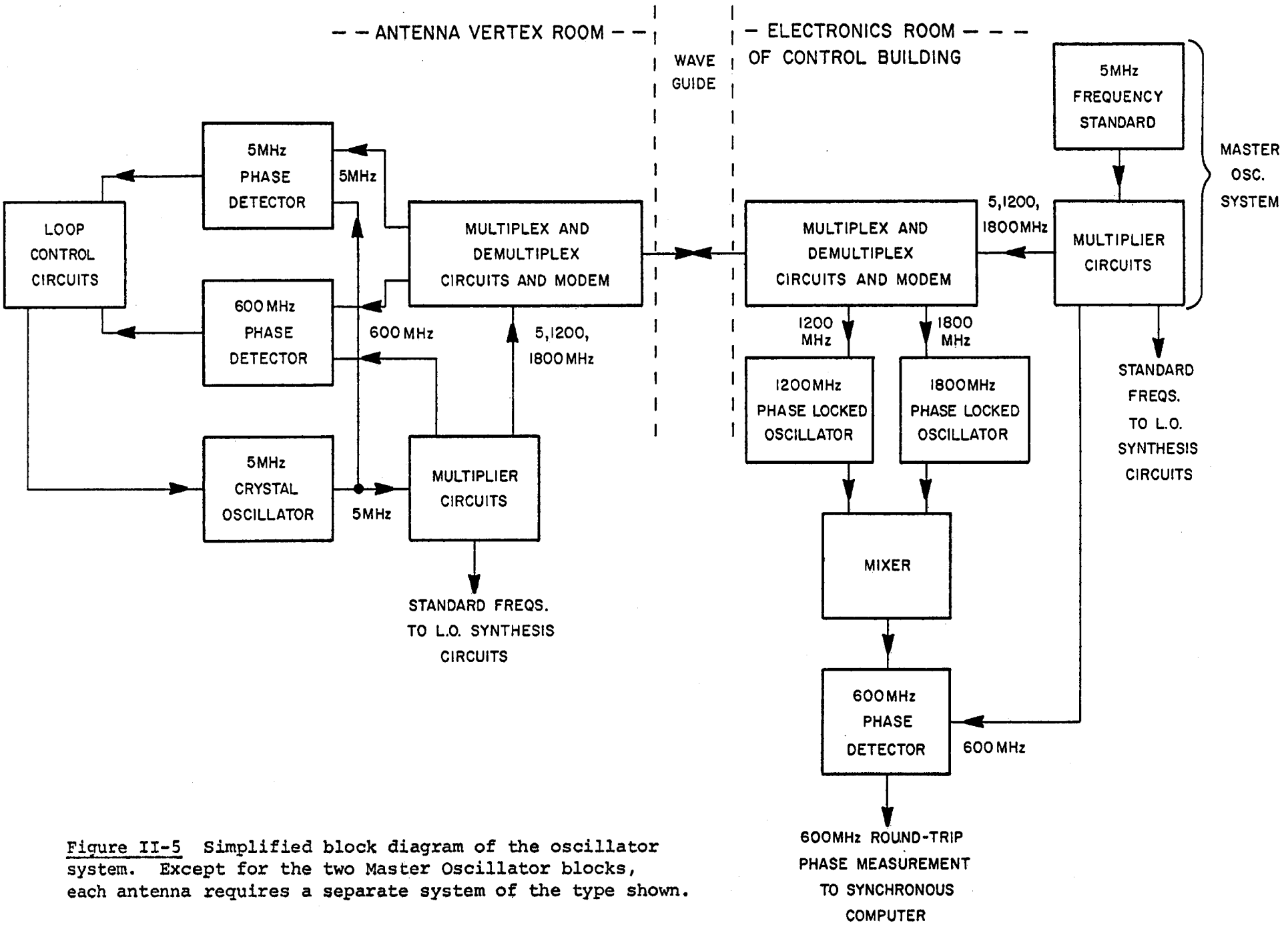


Figure II-5 Simplified block diagram of the oscillator system. Except for the two Master Oscillator blocks, each antenna requires a separate system of the type shown.

Signals that control the transmit-receive sequence in the waveguide and a 100 KHz reference frequency are generated at the antennas from the standard 5 MHz. Frequency division is used, and the required timing to synchronize these signals is derived from the rising edge of the pulses of the 1200 MHz reference signal. The 100 KHz reference is used in a unit (the Fringe Generator) that synthesizes a signal with phase and frequency offsets which are introduced under computer control to reduce the frequency of the output fringe patterns to zero. This signal is used as a reference in the phase lock loop of the 2-4 GHz oscillator mentioned in the last paragraph. The Fringe Generator also introduces 180^{o} phase reversals so that phase switching can be used to eliminate offsets in the outputs of the signal multipliers. The switching sequences take the form of Walsh functions generated by the synchronous computer, and with this scheme orthogonal switching functions are obtained for all antenna pairs without the requirement of very high switching rates. [See Section V (b).]

(d) The IF System

For signals received in the 18-21, 2 and 1·3 cm bands the parametric amplifier acts as the first IF amplifier, but this section is concerned with the IF channels from the output of the front ends to the digital samplers. Four signal bands, each 50 MHz wide, are selected from the front end outputs at each antenna. They are converted several times to different intermediate frequencies before arriving at the digital samplers. Fifty megahertz is the maximum bandwidth of each channel, and additional filters to decrease the bandwidth can be switched in at the antennas and in the final IF amplifiers at the control building. The narrower bandwidths are used to match the system response to the assigned radio astronomy bands, to improve the selectivity when working outside these bands, and for spectral line observations. A block diagram of the IF system is shown in Figure II-6.

The four channels are designated A, B, C and D, and channels A and B come from the parametric amplifier for one polarization and channels C and D from the other. The two polarization outputs can be interchanged between the AB and CD channel pairs by a transfer switch, and this facility is helpful in testing or reducing instrumental effects. The four signals are converted to an IF of 1025 MHz[1] using the local oscillator mentioned in the last section that is tunable in alternate steps of 29·9 and 20·1 MHz. Filters with bandwidths of 55, 25 or 12·5 MHz can be inserted at this stage, and provision is made to add other filters as the necessity arises. Because of the discrete tunability of the local oscillator the center frequencies of the narrower filters must be appropriately chosen if it is desired to encompass a specific frequency at the front end input. The four channels A, B, C and D are then converted to center frequencies of 1325, 1425, 1575 and 1675 MHz respectively. Filters at these frequencies pass the full 50 MHz bandwidth. The signals then go to the modems and travel down the waveguide at frequencies equal to the intermediate frequency (1325 MHz, etc.) plus the carrier frequency for the particular waveguide channel. From the modems at the control building the signals emerge at 1325, 1425, 1575 and 1675 MHz again. They are then converted to a base band of 1-50 MHz by local oscillators tunable in 2 Hz steps. A series of narrow band filters can be inserted under computer control into the 1-50 MHz IF amplifiers. Details of bandwidths and center frequencies are given in Table II-4.

[1]In the prototype electronic system the signals are converted directly from the parametric amplifier passband to 1325, 1425, 1575, and 1675 MHz.

TABLE II-4 BANDWIDTHS AND CENTER FREQUENCIES OF THE FINAL IF STAGES

FINAL SYSTEM

Bandwidth	Center Frequency
50 MHz	25 MHz (low pass)
25 "	12·5 " "
12·5 "	6·25 " "
6·25 "	3·125 " "
3·125 "	1·563 " "
1·563 "	2·349 " (band pass)
0·781 "	1·172 " "
0·391 "	0·586 " "
0·195 "	0·488 " "
0·098 "	0·440 " "

PROTOTYPE SYSTEM

Bandwidth	Center Frequency
50 MHz	25 MHz (low pass)
12 "	40 " (band pass)
1·5 "	40 " "

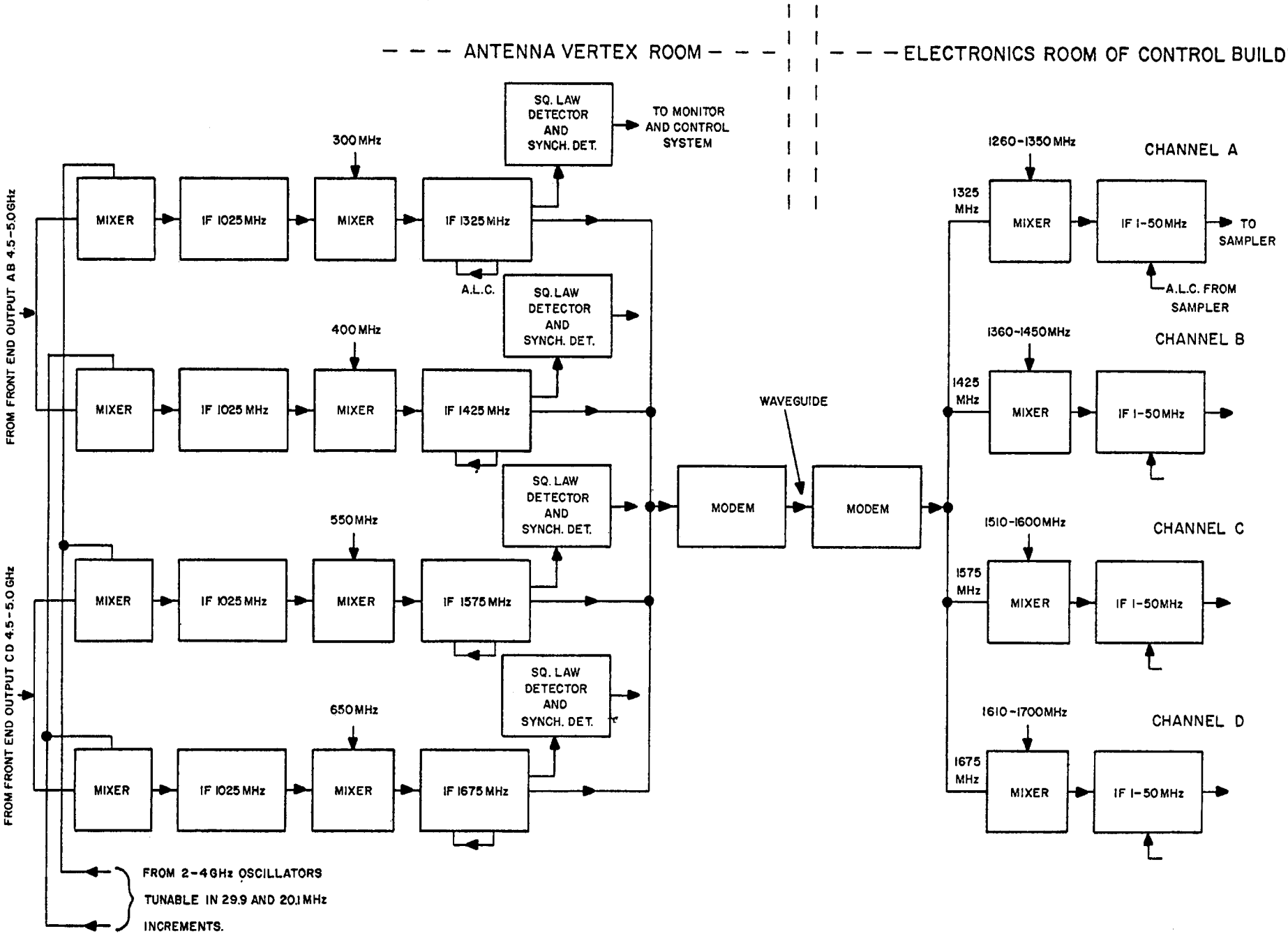


Figure II-6 Basic block diagram of the IF system for each antenna. The 1025 MHz and 1-50 MHz IF amplifiers contain filters of various bandwidths selectable under computer control.

Two automatic level control loops are included in each signal path. One at the antenna controls the level at the modem and one at the control building controls the level in the sampler. At the antenna there is also a square law detector and a synchronous detector for each channel, for use in single-antenna observations and calibration measurements with switched noise sources. [See Section V (c).]

(e) The Digital Samplers and the Delay and Multiplier System

The signals from the IF system are converted to digital form with two bit quantization in the sampler modules, so that they can be processed by a digital delay and multiplier system. The sampling rate appropriate for the 50 MHz bandwidth is 100 MHz which is close to the maximum frequency that can be comfortably handled by e.c.l. (emitter coupled logic) circuitry. This last point was a consideration in choosing the 50 MHz IF bandwidths.

Cooper (1970) has shown that the signal to noise ratio obtainable in multiplication of two bit signals is 81 to 88% of that for a corresponding analog system, compared with 64% for one-bit quantization. The 81% figure applies to the case where only the products of high level signals are counted in the multiplication, and products involving one or two low level signals are ignored. This is the scheme used in the VLA since each multiplied product can then be specified by a two bit number, whereas the weighting required if the other products were included would require 5-bit numbers. The high speed counters that integrate the multiplier outputs are therefore much less complicated if only high level products are counted.

A block diagram of the sampler is shown in Figure II-7(a). A quadrature network which is accurate over the full 1-50 MHz frequency response is used to generate two versions of the signal in which all frequencies are shifted by $\pi/2$ in phase. These are referred to as the cosine and sine components, and they go to separate sampling circuits. In the sampling the signals are compared with d.c. levels of $\pm 0{\cdot}612\sigma$ where σ is the r.m.s. signal level. Two bits are then generated, as indicated in Figure II-7(b). The r.m.s. signal level must be maintained at the required value relative to the reference levels, and an a.l.c. loop is used in which the signal level is measured in the sampler unit and a control voltage is fed back to an attenuator in the 1-50 MHz IF amplifier.

The delay system that follows the samplers operates in 10 ns increments controlled by the 100 MHz clock. To provide for smaller increments in the delay the phase of the clock in each sampler module can be shifted in increments of 625 ps which is 1/16 of a clock period.[1]

[1]The delay increment is 1/32 of the reciprocal of the maximum signal bandwidth. This is more than sufficient to prevent significant loss of correlation, but the minimization of phase errors provides a more stringent criterion.

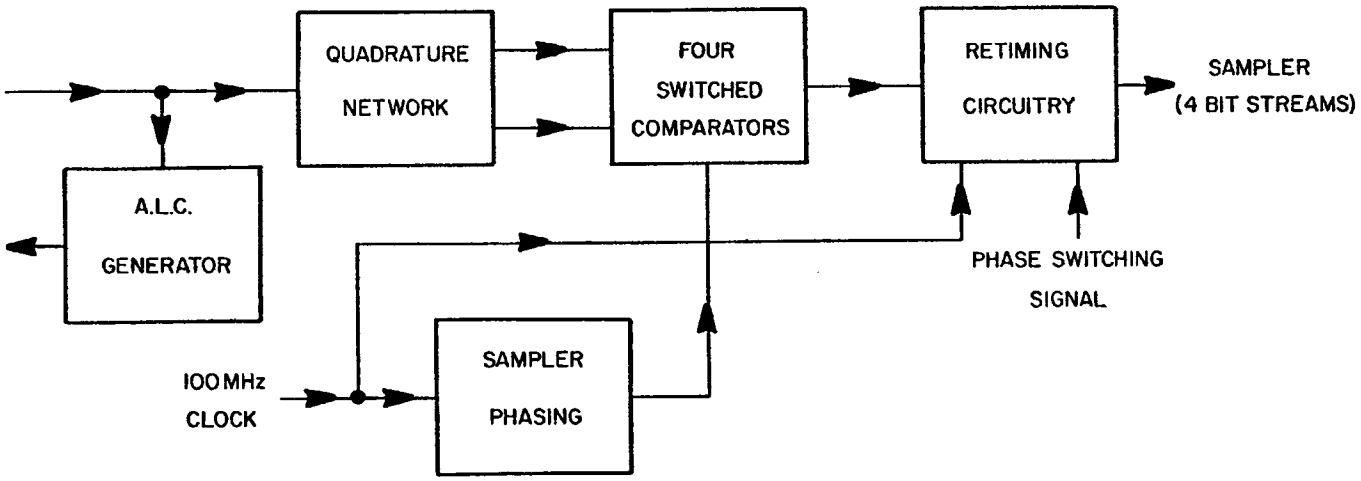


Figure II-7(a) A sampler unit.

SIGNAL LEVEL	BIT 1	BIT 2
$+0.612\sigma$	1	0
0	0	0
0	0	0
-0.612σ	0	1

Figure II-7(b) Bit coding for signal levels in the samplers. σ is the r.m.s. signal level.

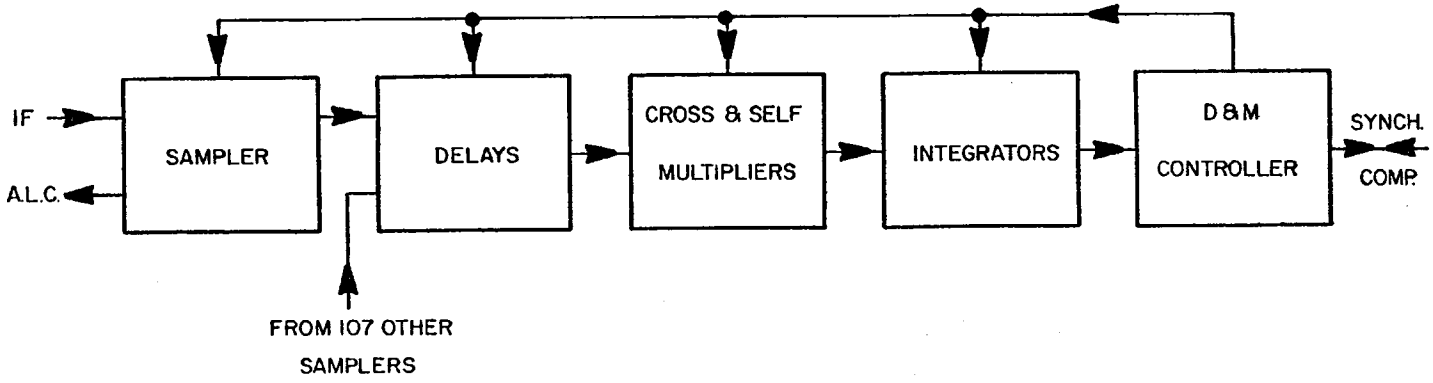


Figure II-7(c) The Delay and Multiplier system. Communication with the synchronous computer is through a special controller as data rates are too high for the general Monitor and Control system.

The output bit streams from the samplers are then resynchronized with the standard 100 MHz clock before going on to the main part of the delay system.

The synchronous detection for the phase switching scheme is also implemented in the sampler modules. The same Walsh functions that control the phase switching at the antennas are also fed to the samplers and used to reverse the sign information in the output bits. Note that in systems with analog multipliers the synchronous detection must be done at the multiplier outputs, but, being digital, the delay and multiplier circuitry used here does not generate spurious offsets.

The output of each sampler module consists of four bit streams with a 100 MHz clock rate. These data go to the delay system where they are initially processed by e.c.l. circuitry and then, for economy, each 100 MHz stream is translated into sixteen 6·25 MHz streams. The bits are stored in m.o.s. shift registers with 256 and 512 bit capacity. The range of variability of the delay is 164μs and the bit streams emerge from the delay system with a clock frequency back at 100 MHz again. The delay values are set by the synchronous computer through an interface unit, the delay and multiplier controller, which also displays monitor data on the delay and multiplier system.

The multipliers operate at the 100 MHz frequency and only produce a non-zero output for combinations of two high-level signal samples. The products have values -1, 0 or +1 but are counted as 0, 1 or 2 respectively. This enables unidirectional counters to be used for integration, and correction is made in the computer by subtracting the number of multiplications involved. The integrated products are transferred to the controller every 52 ms (the cycle period of the waveguide transmission) and can then be further integrated for periods up to 312 ms before being transferred to the computer.

Sixteen multipliers are used for each antenna pair. For any two signals both sine x sine and sine x cosine products are formed, and these represent the real and imaginary parts of the visibility.[1] For polarization measurements four signal products are required: LL, RR, LR and RL, where L and R represent two signals at the same frequency but with opposite polarizations such as left and right circular. Finally, the four IF

[1]Some people prefer to count the two multipliers for sine x sine and sine x cosine as one complex multiplier.

channels allow polarization measurements to be made at two frequencies. For 27 antennas a total 16 x 351 = 5616 multipliers would be required, but the system described here is being implemented for preliminary operation with a maximum of 12 antennas only, and will be replaced by a more complex system with spectral line capability for operation with the full array. {See Section II (f).}

In addition to the multipliers described above, which perform cross multiplication between two signals, the system includes eight multipliers per antenna which are referred to as self multipliers. Each sine or cosine signal component is fed to both inputs of one of these and the output gives a measure of the accuracy with which the signal level is set relative to the reference levels in the corresponding sampler. The output of each cross multiplier is divided in the computer by the mean of the outputs of the corresponding self multipliers. This reduces by a factor of approximately 10 the sensitivity of the visibility data to the signal levels in the samplers, and with the aid of this procedure the a.l.c. loops provide adequate level control.

(f) The Spectral Processor

The spectral processor is a delay and multiplier system that provides measurements of cross correlation, i.e. complex visibility, as a function of frequency. From these the distribution on the sky of spectral line features both in emission or absorption can be determined. The spectral processor will replace the delay and multiplier system described in Section II (e) which was developed for preliminary operations only. The spectral information is obtained by measuring the correlation of the signals from each pair of antennas with a series of time delays which are integral multiples of the sampling interval. These time delays should not be confused with the delays introduced to compensate for the signal propagation times in space and in the electronics. The compensating delays are introduced first, and are under computer control. The delays required for spectral measurements are generated separately and are automatically controlled within the processor.

To obtain the brightness distribution at N intervals across an IF bandwidth B, N values of time delay from zero to (N-1)/2B are used. If the multiplications for each pair of signals are performed for both a positive and negative lag of one signal with respect to the other, it is not necessary to use both sine x sine and sine x cosine products, so only the former are implemented for spectral observations. The number of multipliers in the spectral processor is sufficient to provide 16 channels, i.e. measurements at 16 frequency intervals, across a single 50 MHz bandwidth. This requires 27 x 26 x 16 = 11232 multipliers plus a small number of self multipliers.

A recirculating scheme is used to provide greater numbers of channels as the IF bandwidth is decreased. This is based on the recirculating correlator concept (Ball, 1973) in which the data processing makes the fullest use of the capacity of the multipliers. If the IF bandwidth is halved and becomes B/2 the sampling frequency[1] can also be halved and becomes B. However,

[1]This refers to the sampling frequency at the multipliers. In the VLA processor the samplers always run at their maximum frequency and the frequency of the samples is reduced as required before reaching the multipliers.

if the multipliers are still used at the data rate appropriate for the full bandwidth, i.e. 2B, they are capable of handling twice as many time delays as in the full bandwidth case. To realize this capability the signals must be circulated through the multipliers twice, first for delays from 0 to (N-1)/B and then from N/B to (2N-1)/B. A recirculator is required to store the signal data and emit them with an additional time delay N/B for the second series of multiplications. Further reduction in IF bandwidth allows more recirculation and corresponding increases in the number of channel as indicated in Table II-5. The recirculator is designed for a maximum of 512 channels, but the present capacity of the assynchronous computer imposes an overall limit of 256 channels.

The spectral processor is capable of operating in five principal modes, as outlined below, the channel capacities of which are given in Table II-5.

(a) Single Band Mode

Only one of the four IF bands is processed and the number of channels for the full 50 MHz bandwidth is 16 as outlined above.

(b) Two Band Mode

Two of the four IF bands are processed and half the multipliers are used for each, so the number of channels per band is naturally half of that for the one channel mode. Note that the two IF bands can be any two of the four available, A, B, C and D. The chosen bands can be on different wavelengths if the dichroic mode is used, on different parts of the same wavelength band, or they can cover the same frequencies with opposite polarizations to increase the signal to noise ratio.

(c) Four Band Mode

All four IF bands are processed and the number of channels for a given IF bandwidth is one-fourth of that for the single band mode. Again the channels can be distributed

TABLE II-5 CHANNEL CAPACITIES ETC. FOR THE VARIOUS IF BANDWIDTHS

IF Bandwidth	Sampling Frequency	Sampling Factor[1]	Number of Channels per IF Band				Minimum Integrating Time
			Single Band Mode	Two Band Mode	Four Band Mode	Polarization Mode	
50 MHz	100 MHz	2	16	8	4	4	312·5 msec.
25 MHz	50 MHz	2	32	16	8	8	625 msec.
12·5 MHz	25 MHz	2	64	32	16	16	1·25 sec.
6·25 MHz	12·5 MHz	2	128	64	32	32	2·5 sec.
3·125 MHz	6·25 MHz	2	256	128	64	64	5 sec.
1·5625 MHz	3·125 MHz	2	512	256	128	128	10 sec.
781·25 KHz	1·5625 MHz	2	512	256	128	128	10 sec.
390·625 KHz	1·5625 MHz	4	512	256	128	128	10 sec.
195·3125 KHz	781·25 KHz	4	512	256	128	128	10 sec.
97·65625 KHz	390·625 KHz	4	512	256	128	128	10 sec.

[1]Sampling frequency divided by IF bandwidth.
Values greater than 2 indicate oversampling.

as desired over the various wavelength bands and polarizations, limited only by the simultaneous operating capability of the front end. Note that if one considers the total number of channels in the four bands, this mode provides the greatest number of channels in a given signal bandwidth.

(d) Polarization Mode

A pair of channels with oppositely polarized signals, either A-C or B-D, are processed to obtain full polarization data. In addition to products of signals with the same polarization, an equal number products of oppositely polarized signals are required in this case. The number of channels for a given bandwidth is therefore half of that for the two band mode without cross polarization products.

(e) Continuum Mode

All four IF bands are processed, each as a single channel, and full polarization data are derived. No recirculation or time delays between signals are required. With 11,232 multipliers there are 32 for each of the 351 antenna pairs. Both the sine and cosine outputs of the samples are used, and for two IF channels with opposite polarization the 16 products listed below are derived. Here S and C denote the sine and cosine components, L and R the oppositely polarized channels, and X and Y the antennas.

XRS x YRS	XRC x YRC
XLS x YLS	XLC x YLC
XRS x YLS	XRC x YLC
XLS x YRS	XLC x YRC
XRS x YRC	XRC x YRS
XLS x YLC	XLC x YLS
XRS x YLC	XRC x YLS
XLS x YRC	XLC x YRS

The preceding multiplications are performed for both the A-C and B-D IF pairs. If analog multipliers were used, the results of corresponding products in the two columns above would be identical and half of the data would be redundant. However, the use of two bit quantization and omission of low and intermediate products in the multiplication reduces the signal to noise ratio obtainable from either one of the two sets to 84% of that from analog multipliers. Derivation of the other eight products restores some of the lost information and increases the signal to noise ratio by about 10%.

The basic blocks of the spectral processor are shown in Figure II-8. The interconnection of the blocks is different for the various modes of operation, and not all of the blocks are used in each case. The samplers are identical to those described for the interim continuum system in Section II (e) and run at a rate of 100 MHz. The compensating delay units are functionally identical to those of the interim system. Reduction of the sample rate to that in Table II-5 occurs at the input of the recirculator, where unwanted samples are rejected. For the three narrowest IF bandwidths oversampling by a factor of two is retained to improve the signal to noise ratio. The recirculator is capable of cycling the data into the multipliers up to 32 times with delays up to a maximum of 512 sample intervals. In the continuum mode the signals are transmitted straight through the recirculator to the multiplier. In the spectral line mode a driver unit distributes the signals from the recirculator to the multiplier inputs, inserting delays that are integral multiples of the sample interval. Depending upon the mode of operation, the 16 multiplier inputs may receive one signal with delays from zero to 15 sample intervals, two signals with delays from zero to seven sample intervals, or four signals with delays from zero to three sample intervals. The multipliers operate at a rate of 100 MHz and are functionally

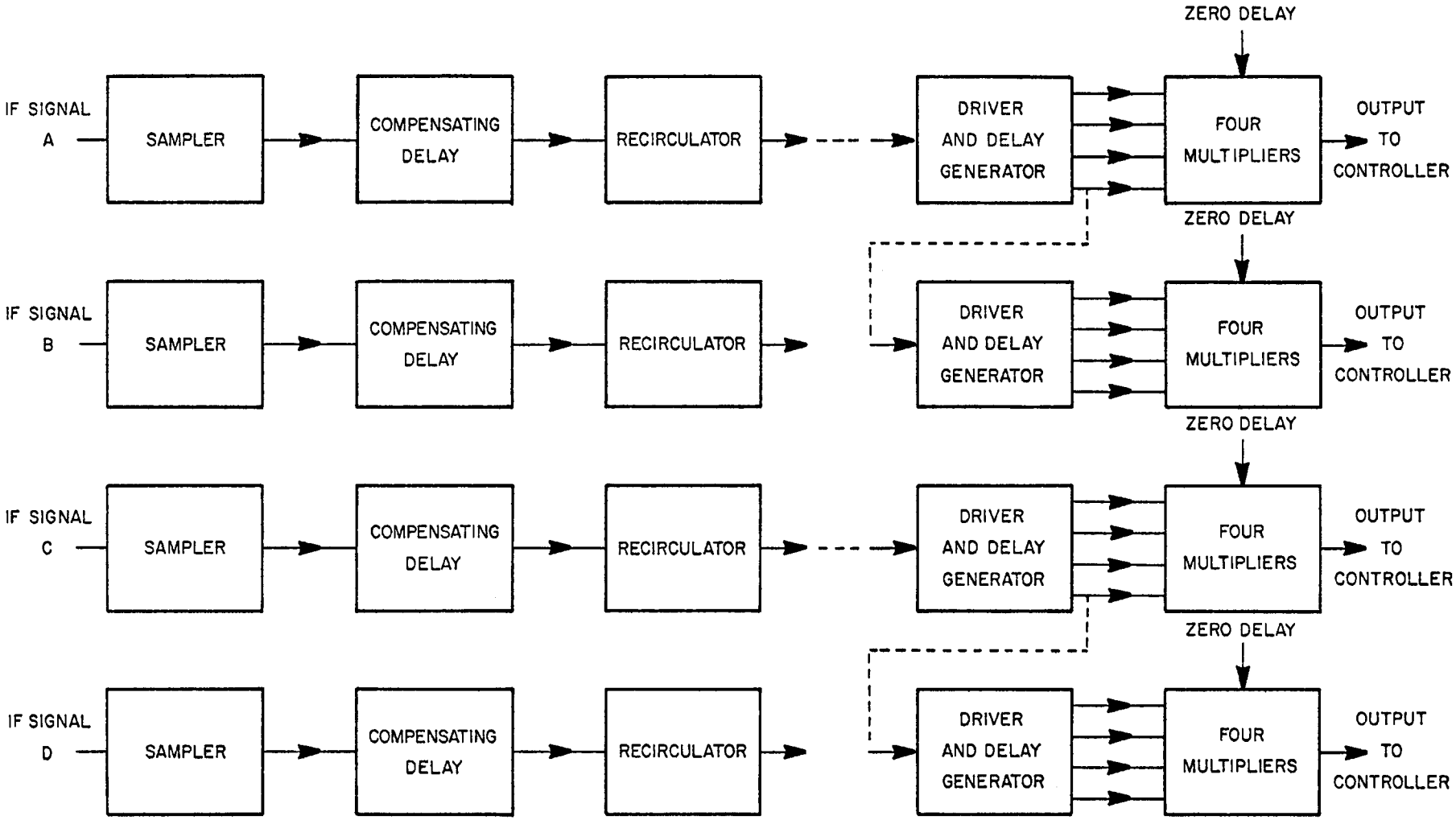


Figure II-8 Schematic block diagram of a subunit of the Spectral Processor. The IF signals from one antenna enter the samplers at the left and the signals from another antenna, with timing corresponding to zero delay in the recirculators, enter the multipliers at the zero delay inputs. The four outputs from each of the drivers to the multipliers have delays increasing from top to bottom in steps of one sample interval. For each antenna, one set of four samplers, compensating delays and recirculators is required. For each antenna pair, two sets of the drivers and multipliers shown are required because it is necessary to obtain products with the recirculator and driver delays applied to each antenna of the pair. Not all blocks are used in all modes of operation and, as an example, the broken lines show the interconnections for the two band mode with IF signals A and C.

identical to those described in Section II (e).

A control section of the spectral processor provides an interface with the synchronous computer. This controller incorporates a Modcomp II/45 computer, the same type of which the synchronous computer is comprised. The controller also contains a fast Fourier transform processor which transforms the multiplier output data from visibility as a function of time delay to visibility as a function of frequency. Before this transformation the data are averaged for periods of 312·5 msec to 10 sec depending on the bandwidth (see Table II-5), and further integration can be applied in the transform processor if required.

Two integrated circuits were custom designed for the VLA spectral processor. One is a dual 3-level[1] multiplier and the other an integrating counter. The custom design greatly reduces the number of interconnections external to the circuit packages as well as the size and power consumption of the multiplier section.

The spectral processor contains a system for detection and faults in which pseudo-random test signals are injected at the delay unit inputs during the intervals of the 19·2 Hz cycle in which no data is received from the antennas. The multiplier outputs are examined for the expected results and a malfunction can be traced to a delay unit, recirculator, driver or multiplier. If the fault is in a delay unit or recirculator, a self-repairing action takes place in which a spare unit is switched in to replace the malfunctioning one.

Further details of the spectral processor can be found in VLA Electronics Memoranda Nos. 133 and 134.

[1]The two bit digitizing scheme in which the low level bits are assigned zero value is often referred to as three-level digitizing.

(g) The Monitor and Control System

The monitor and control system distributes control signals from the synchronous computer to all parts of the array and gathers monitor data which are fed to the computer. Examples of control data are antenna pointing commands, fringe generator parameters, and synthesizer frequency-selection commands. Examples of monitor data are power supply voltages, signal levels, and readback of some commands to check for correct transmission. The monitor and control system is sometimes referred to as the digital communication system (d.c.s.).

A block diagram of the system is shown in Figure II-9. All blocks represent modules except for the computers and the serial line controller. Interfacing with the receiving equipment takes place through the data sets, and the data taps provide visual readout of individual data words. Commands from either of two computers in the synchronous system are accepted by the serial line controller which adds address information. Data are then handled in the form of 45 bit words which contain 24 bits of command or monitor data, 16 bits of address information and 5 parity bits. The data then go to the central buffers, of which there is one per antenna in the central control building. Commands for the control room electronics go to a data set and those for electronics at an antenna go to the corresponding antenna buffer via the waveguide communication system. The antenna buffer has five interfaces for data sets, one of which is not used. Two data sets are located in the vertex room, one in each equipment rack there. In the pedestal room there is a third data set,and the antenna control unit which presents the same type of interface to the antenna buffer. The command simulator provides manual entry of commands for test purposes.

The flow of monitor data is essentially similar to that described above, but in the reverse direction. Data tap modules can display either command or monitor words, and these are selected by manually entering the appropriate address. Words representing analog voltages are reconverted to analog to allow monitoring by oscilloscope or chart recorder. The data taps at the antennas can display only words relating to equipment at the particular antenna, but the data taps in the control building can display all monitor and control data. To achieve this, each central buffer also receives all data within the system.

For transmission down the waveguide, data are converted to a biphase M code and modulated onto the 1800 MHz signal. Transmission in the two directions in the waveguide follows the 19·2 Hz sequence described in Section II (b), with bit lengths of 4μs for transmission out to the antennas and 50μs for transmission back to the control building. During each cycle up to four command words are transmitted to each antenna and up to eight to each local data set. Two monitor words per cycle are received from each data set.

Transfer of digital data between the data sets and the receiving equipment is in a serial manner with the data sets providing clock pulses. Each data set has three serial outputs, each of which can be submultiplexed by a four bit address which is also provided by the data set. A data set can therefore provide up to 48 different command words. It also has four digital and eight analog inputs, and four-bit submultiplex addressing allows up to 64 digital words and 128 analog voltages to be monitored by each data set. An analog to digital converter in the data set converts the analog inputs to 12-bit digital signals, two of which can be contained in one data word. For each antenna the five data sets provide the capacity for up to 240 different 24-bit digital commands, 320 24-bit monitor words and 640 analog monitor voltages, not including the antenna pointing commands. Only about 25% of this capacity is used by the present receiving system.

The addresses to which command words are issued are specified by the computer. The addresses from which monitor data are taken are generated in the data sets. For the first monitor word in each cycle the address is selected by stepping sequentially through 192 preprogrammed addresses in a read-only memory in the data set. For the second word the address is selected by stepping sequentially through the 192 possible addresses in order, so that each one is sampled every ten seconds. Alternately the address of the second word can be commanded to remain fixed and monitor one function at the 19·2 Hz rate.

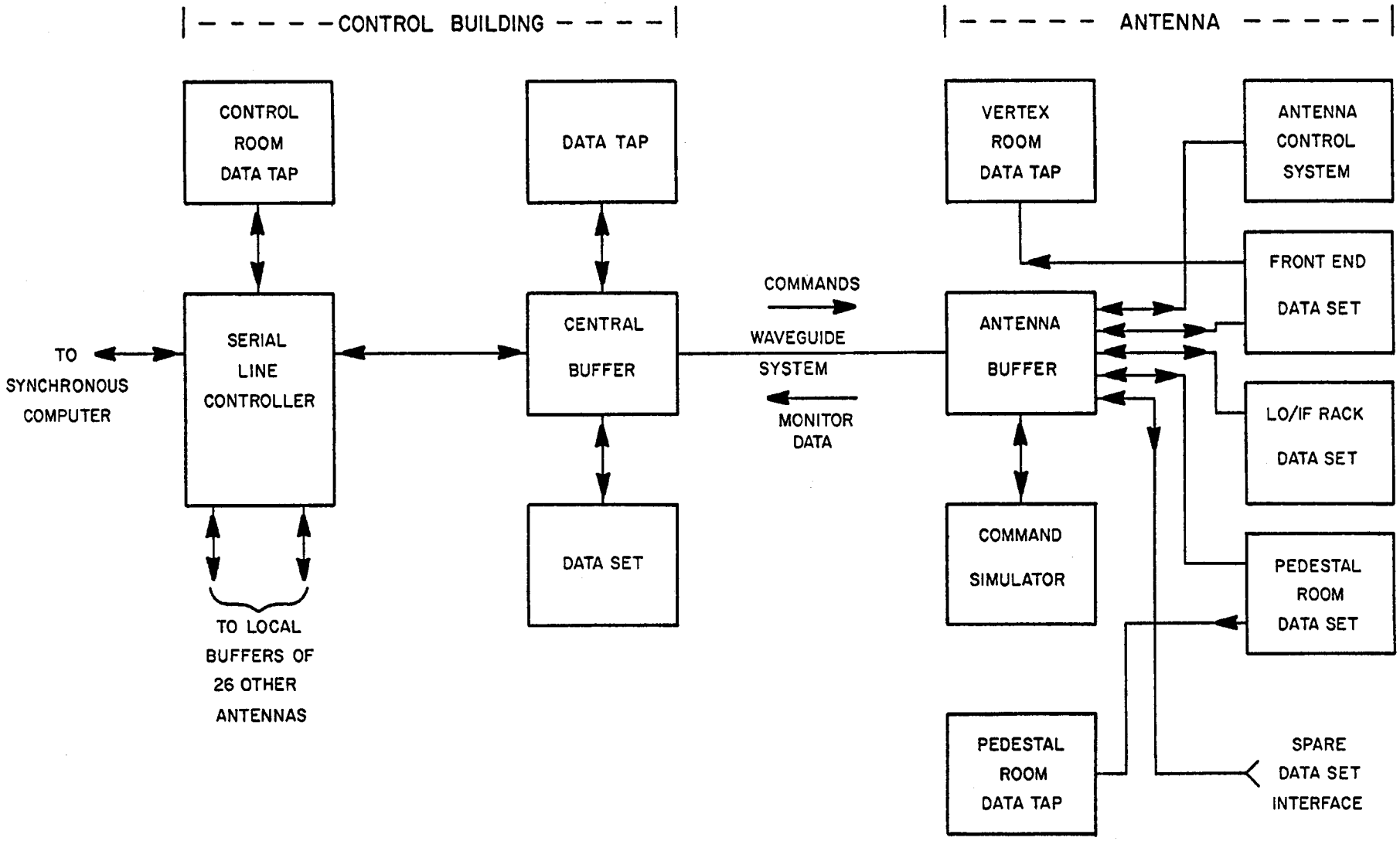


Figure II-9 Block diagram of the Monitor and Control system. One each of the units shown is required per antenna except for the Serial Line Controller and the Control Room Data Tap.

III. Physical Layout of the Racks, Bins and Modules

The location of all of the major parts of the electronic system is shown in the schematic diagram in Figure III-1. There are two equipment racks in the vertex room of each antenna. Rack A contains the front end and the IF stages preceding the modem. Rack B contains most of the local oscillator system at the antenna, and the modem. The vertex room is temperature controlled to $\pm 2^{o}$ F. In the pedestal room rack C contains the equipment that controls the driving of the antenna and the focus and rotation of the subreflector.

In the central electronics room of the control building there are three rows of nine racks each, one row for each arm containing one rack for each antenna. These are the D racks which contain modems, local oscillator equipment and the final IF stages. The rows are designated N, E, or W for the north, east or west arms. The three signal distributor units which terminate the waveguide trunk lines are located under the corresponding rows of racks, and are mounted against the ceiling of the laboratory below. The signal distributors are designed with outputs spaced at intervals equal to the width of a rack. The master local oscillator racks are also located in the electronics room, and signals are distributed to the D racks through branching cable networks which are also located below the floor of the electronics room. An opening in the floor below each rack provides access for cable and rectangular waveguide connections and an air conditioning duct. The air temperature is held constant to $\pm 2^{o}$ F at the input to the racks.

The racks containing the samplers and the delay and multiplier system are located in a shielded room adjacent to the electronics room. This equipment could generate substantial radio interference since the final system, which will include spectral line capability, will dissipate close to 50 kilowatts of power, and much of this in circuits switching at a 100 MHz clock rate. The shielding provides 100-120 dB of isolation at 1 MHz to 10 GHz.

Almost all of the electronics except for the front ends and the delay and multiplier system are built in the form of modules which are inserted into bins. Modules are 19·44 inches long, 7·22 inches deep, and multiples of 1·385 inches wide. These modules were designed specifically for the VLA and somewhat resemble the standard Nuclear Instrumentation Modules, but the VLA modules are longer and of more rugged design. Widths up to six times the unit width are used, and a bin can accommodate up to 12 single-width

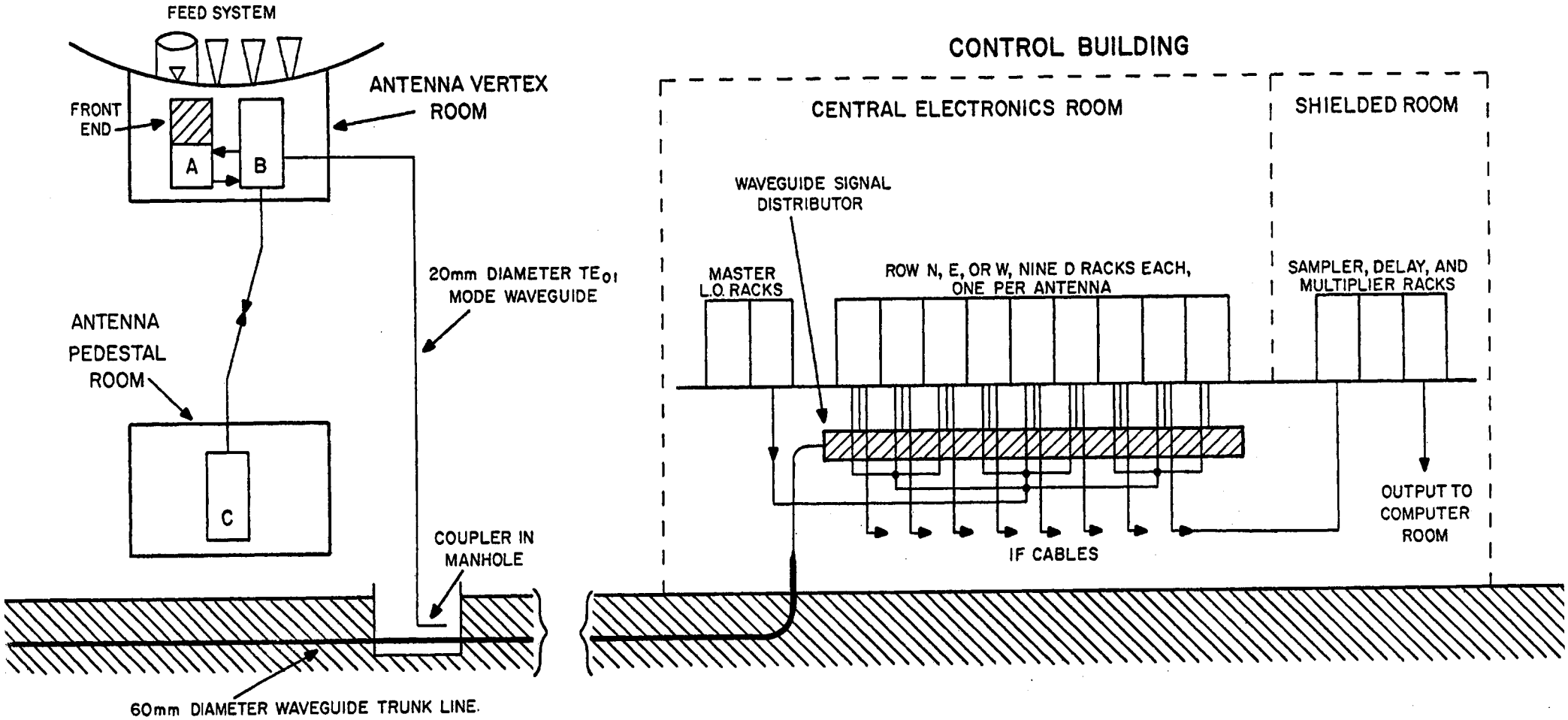


Figure III-1 Schematic diagram showing main locations of electronic equipment.

modules. Power and signal connections are made through Amp series M connectors and Omni-Spectra series OMQ coaxial connectors on the rear panels of the modules which mate with corresponding connectors on the bins when the modules are inserted.

Specifications of the reference numbering system for the racks, bins, modules and connectors are given in Section V (d).

IV. DETAILS OF THE MODULES, AND THE SYSTEM BLOCK DIAGRAMS

D1, SAMPLER

Subsystem, Digital Delay and Multiplier

Project No. 13520

4 per antenna, Sampler rack (shielded room)

Design Engineers, R. Mauzy and R. P. Escoffier

The sampler acts as a two-bit analog-to-digital converter for the IF signals. One D1 module is used for each 50 MHz-wide IF channel. The IF signal drives a level detecting circuit that produces the a.l.c. signal which is fed back to the IF Receiver (T5). The IF signal is then split into two components (the cosine and sine components) by a quadrature network. These two quadrature components are sampled by two-bit samplers and the resulting four bits go to the delay system. The sampling clock rate is 100 MHz and this can be phased in 0·625 ns increments to provide the fine adjustment of the delay. The sampler output pulses are then retimed to be in synchronism with the main 100 MHz clock. The signs of the digitized signals can be reversed by a one-bit control signal to remove the phase reversals put in at the Fringe Generator (L7) for phase switching. Communication with the computer is through the delay and multiplier controller.

F1, BIAS CONTROL

Subsystem, Front End

Project No. 13170

2 per antenna; Rack A, Front End Bin, Slots 13 and 14 (antenna vertex room)

Design Engineer, S. Weinreb

L1 provides adjustable bias voltages for up to three parametric amplifier stages, an upconverter, a 2 cm wavelength mixer and a 1·3 cm wavelength mixer. Two bias modules are used with each front end. The bias voltages for the parametric amplifiers are controlled by front-panel potentiometers, that for the upconverter by an analog signal from the Upconverter Pump (F2), and those for the 2 cm and 1·3 cm mixers by analog voltages from the 17-20 GHz LO Module (F3). The bias voltages and currents can be monitored through an analog multiplexer, the output of which goes to a Data Set (M1).

F2, UPCONVERTER PUMP

Subsystem, Front End

Project No. 13150

1 per antenna; Rack A, Front End Bin, Slots 15-16 (antenna vertex room)

Design Engineer, G. K. Barrell

L2 provides pump power at a fixed frequency of 3·2 GHz to both of the upconverters used in each front end for reception in the 18-21 cm wavelength range. The pump oscillator is a varactor-tuned transistor oscillator and it is phase locked in a loop in which its output is mixed with 3·0 GHz from the L.O. Transmitter (L3) to provide a 200 MHz IF signal. The required input reference frequencies are 200 MHz and 3 GHz. The two outputs to the upconverters have separate attenuators for level control.

F3, 17 to 20 GHz LOCAL OSCILLATOR

Subsystem, Front End

Project No. 13160

1 per antenna; Rack A, Front End Bin, Slots 3-4 (antenna vertex room)

Design Engineer, G. K. Barrell

F3 provides a local oscillator signal to the 2 cm and 1·3 cm wavelength mixers. 2 cm signals are received using the lower sideband response and 1·3 cm signals using the upper sideband. The oscillator is a YIG-tuned Gunn diode oscillator and it is phase locked to the standard frequencies of the system by mixing with a harmonic of 600 MHz to provide an IF signal at 100 or 200 MHz. Input reference frequencies required are therefore 100, 200 and 600 MHz. Lock frequencies are (m x 600 ± n x 100) MHz where n takes values of 1 or 2. This tunability together with the 500 MHz bandwidth of the parametric amplifiers allows all frequencies within the 14·4-15·4 and 22-24 GHz bands to be covered. Lock points are selected by a tuning signal derived from a digital to analog converter which receives an eight-bit tuning command from the Front End Control Module (F5).

F4, FREQUENCY CONVERTER

Subsystem, Front End

Project No. 13180

4 per antenna; Rack A, Front End Bin, Slots 5, 6, 8 and 9 (antenna vertex room)

Design Engineer, S. Weinreb

Four F4 modules are used at each antenna to select the four 50 MHz wide IF bands from the 4·5-5·0 GHz outputs of the parametric and transistor amplifier chains, and to convert them to a center frequency of 1025 MHz. Local oscillator signals for this conversion are provided by the 2-4 GHz Synthesizers (L6). The IF signals then go to the Front End Filter Unit (F7) where they pass through bandwidth limiting filters and are converted to four bands centered at 1325, 1425, 1575 and 1675 MHz. They are then returned to the F4 modules where they are amplified and then passed to the IF Combiner Module (T2). The final stages of the F4 include a power law detector and a synchronous detector for monitoring power levels {see section V(c)}, and an automatic level control loop.

In the prototype system the conversion to 1025 MHz is omitted, the signals are converted to 1325 MHz etc. in the F4 units, and F7 is not used.

F5, FRONT END CONTROL MODULE

Subsystem, Front End

Project No. 13170

1 per antenna; Front End Bin, Slots 10-11 (antenna vertex room)

Design Engineer, G. K. Barrell

F5 acts as an interface between the front end modules and the monitor and control system. It also contains front panel switches which allow alternate manual control of several functions. Units or functions controlled include the dichroic reflector and de-icer on the feed system, the calibration signals, the transfer switch and attenuators in F6, the gain and the alternate input switch in F4, the parametric amplifier pump on/off, the observing bands used, the tuning of the upconverter and the tuning of the 17-20 GHz Local Oscillator (F3). Numerous analog signals are also monitored through this module.

F6, RF SPLITTER

Subsystem, Front End

Project No. 13170

1 per antenna, Rack A, Front End Bin, Slot 7 (antenna vertex room)

Design Engineer, S. Weinreb

F6 takes the two outputs of the 4·5-5·0 GHz parametric and transistor amplifier chains and splits them into four outputs which go to the four Frequency Converters (F4). Monitoring couplers provide RF and logarithmically detected outputs for sweep testing of the front end response. The module also contains attenuators which are controlled through the Front End Control Module (F5) for observations of very strong sources such as the sun. A transfer switch is included to exchange the two 4·5-5·0 GHz signal bands. This facilitates calibrating out the instrumental response of the later parts of the receiving system, which can be useful in polarization measurements and isolating malfunctions.

F7, FRONT END IF FILTERS

Subsystem, Front End

Project No. 13190

1 per antenna, Rack A (antenna vertex room)

Design Engineer, unassigned

F7 contains filters that provide selectivity at the antennas. Four IF signals at 1025 MHz come from the Frequency Converter (F4) Modules to F7. They then pass through filters with bandwidths of 55, 25 or 12·5 MHz, selectable under computer control. The four signals are converted to the 1325, 1425, 1575 and 1675 MHz IF bands before being returned to the F4 modules.

F7 is not used in the prototype system.

L1, 5 to 50 MHz VOLTAGE CONTROLLED CRYSTAL OSCILLATOR

Subsystem, Local Oscillator

Project No. 13230

1 per antenna; Rack B, Bin L, slots 1-2 (antenna vertex room)
2 in Master L.O.; Rack M, Bin T, Slots 1-2, and 9-10 (central electronics room)

Design engineer, H. L. Beazell

L1 contains the 5 MHz crystal oscillator at the antennas that is locked to the master oscillator in the control building. The loop amplifier is in the Local Oscillator Control Module (L5) and error signals which control the loop are generated in the Local Oscillator Receiver (L4). L1 also contains x2 and x5 frequency multipliers and outputs are at 5, 10 and 50 MHz. The warmup time for the crystal oscillator to reach full stability is about 24 hours, and batteries are included in the module to keep power on the oscillator for up to four hours if external supplies are interrupted. Two modules of the same type are used in the master L.O.

L2, 50 MHz HARMONIC GENERATOR

Subsystem, Local Oscillator

Project No. 13230

1 per antenna; Rack B, Bin L, Slots 3-4 (antenna vertex room)
2 in Master L.O.; Rack M, Bin T, Slots 3-4, and 11-12 (central electronics room)

Design engineer, D. S. Bagri

L2 constains a harmonic generator that produces signals at multiples of 50 MHz. A step recovery diode is driven by a 50 MHz VCXO which is phase locked to 50 MHz from L1. The diode is included within the loop so that any changes in its characteristic do not produce phase changes at the harmonic frequencies. The spectrum of harmonics goes to the 2-4 GHz Synthesizers (L6) and filtered outputs at 50, 100, 200, 1200 and 1800 MHz are provided.

A version of L2 used in the prototype system and the master local oscillator contains a multiplier chain from 50 to 600 MHz. It was designed by H. L. Beazell and is called the 50 to 600 MHz Multiplier.

L3, LOCAL OSCILLATOR TRANSMITTER

Subsystem, Local Oscillator

Project No. 13230

1 per antenna; Rack B, Bin L, Slots 5-6 (antenna vertex room)

Design Engineer, D. S. Bagri

L3 produces the L.O. signals that are returned from the antenna to the control building. 1200 and 1800 MHz from L2 are further filtered by phase lock loops. The 1200 MHz is amplitude modulated with 5 MHz from L1 and the 1800 MHz is amplitude modulated with monitor data from the Antenna Buffer (M4). These modulated signals are combined and go to the IF Combiner (T2). The unmodulated 1200 MHz and 1800 MHz are combined to generate 600 MHz and 3000 MHz, and the 1200 MHz is also doubled to produce 2400 MHz. Outputs at 600, 2400 and 3000 MHz are used as references by the Upconverter Pump (F2), 17-20 GHz L.O. (F3), and Modem (T1).

A version of L3 used in the prototype system incorporates a multiplier chain from 600 MHz and was designed by H. L. Beazell.

L4, LOCAL OSCILLATOR RECEIVER

Subsystem, Local Oscillator

Project No. 13230

1 per antenna; Rack B, Bin L, Slots 7-8 (antenna vertex room)

Design Engineer, H. L. Beazell

L4 receives the modulated 1200 and 1800 MHz signals from the Modem (T1) via the IF Combiner (T2) and separates them and recovers the modulated 5 MHz and data signals. It also combines the 1200 and 1800 MHz signals to produce 600 MHz. This 600 MHz signal is combined in a phase detector with 600 MHz from the 50 MHz Harmonic Generator (L2) (which comes through L3) and the resulting phase error signal goes to L5 which contains the phase lock circuitry for the 5 MHz oscillator in L1. The 5 MHz from the 1200 MHz modulation is combined in another phase detector with the 5 MHz from L1, and this phase error signal also goes to L5.

L5, LOCAL OSCILLATOR CONTROL

Subsystem, Local Oscillator

Project No. 13230

1 per antenna; Rack B, Bin L, Slot 9 (antenna vertex room)

Design Engineer, H. L. Beazell

L5 contains the phase lock circuitry for the 5 MHz crystal oscillator in L1. The loop is first closed using the 5 MHz phase error signal from L4. When the phase error is less than ± 1.0° the loop switches to the 600 MHz error signal, and switches back only if the 5 MHz error exceeds ± 1.0° or lock is lost. A front panel LED indicator displays the range of the 5 MHz and 600 MHz phase errors. L5 also receives monitor signals from other parts of the LO system and interfaces them to the monitor and control system. Inputs and outputs are low frequency or TTL signals.

L6, 2-4 GHz SYNTHESIZER

Subsystem, Local Oscillator

Project No. 13250

2 per antenna; Rack B, Bins H and K, Slots 1-3 (antenna vertex room) Slots 7-9, Bins H and K, are wired for 2 further units.

Design Engineer, A. R. Thompson

L6 provides a local oscillator signal in the range 3·5 to 3·95 GHz for frequency conversion of the IF signals from the 4·5-5·0 GHz output of the front end to 1025 MHz. A 2 to 4 GHz YIG-tuned oscillator provides the output signal. It is mixed with a 3·0 GHz reference from L3 and then locked to a harmonic of 50 MHz using a 10·1 MHz IF reference in the loop. Output frequencies are (3000 + N x 50 ± 10·1) MHz where N can take integral values from 6 to 24. Any of these frequencies can be selected through the monitor and control system, thus providing a coarse tuning facility at the antennas. Input reference frequencies are 50 MHz harmonics from L2, 3000 MHz and 10·1 MHz. The output goes to the Frequency Converter Modules (F4).

In the prototype system the first reference frequency is 2·4 GHz and the output range is 2·7 to 3·6 GHz for direct conversion from 4·5-5·0 GHz to 1325 MHz etc. Also in the prototype the 50 MHz harmonics are internally generated.

L7, FRINGE GENERATOR

Subsystem, Local Oscillator

Project No. 13250

2 per antenna; Rack B, Bins H and K, Slot 5 (antenna vertex room)
Slot 11 of Bins H and K is wired for 2 further units.

Design engineer, A. R. Thompson

L7 provides the 10·1 MHz reference frequency to L6, and inserts computer-controlled frequency and phase offsets which cancel out the relative phase changes in the signals at the antennas resulting from earth rotation. The fringe frequencies at the outputs of the signal multipliers are thereby reduced to zero. The module takes a 50 MHz signal and divides it down to 100 kHz. The initial phase is controlled by the initial setting of the divider and the frequency offsets are introduced by adding or subtracting pulses at a controlled rate in the first divider stage. Every 1·25 sec. the frequency and initial phase are reset by the computer, the latter setting being relative to a reference 100 kHz from L8. The phase of the generated 100 kHz can also be reversed by a one-bit signal from L8, and this is used to implement phase switching. Finally, the 100 kHz is added to 10 MHz from L1, using a mixer and crystal filter, to generate the 10·1 MHz output.

L8, TIMING GENERATOR

Subsystem, Local Oscillator

Project No. 13230

1 per antenna; Rack B, Bin L, Slot 9 (antenna vertex room)
1 in Master L.O.; Rack M, Bin T, Slot 9 (central electronics room)

Design engineer, R. P. Escoffier

L8 counts down from the standard 5 MHz signal to produce a number of 19·2 Hz waveforms that are required by various modules to control the sequence of data transfer between the control room and the antennas. It also produces a 9·6 Hz waveform that is used in the front end for switching of calibration signals or receiver inputs (when observing in a single-dish mode), and a 100 kHz reference waveform that is used in the Fringe Generator (L7). The synchronization of the above waveforms at the antennas is performed by using the rising edge of the 1200 MHz signal from the L.O. Receiver (L4). The Timing Generator also contains a shift register that receives from a Data Set (M1) the Walsh-function phase switching waveform sent out by the computer. This waveform is shifted out to the Fringe Generator at a rate of 1 bit every cycle of the 19·2 Hz.

L9, CENTRAL LOCAL OSCILLATOR RECEIVER

Subsystem, Local Oscillator

Project No. 13240

1 per antenna; Rack D, Bin R, Slots 2-3 (central electronics room)

Design engineer, H. L. Beazell

L9 is located in the central electronics room and it obtains from the IF Combiner (T2) the 1-2 GHz signal band received from the antenna via the Modem (T1). The 1200 and 1800 MHz signals are selected out by filters, and 5 MHz and data signals are demodulated from them. The phase of the 5 MHz is compared with that of the offset 5 MHz from L12 and the resulting 19·2 Hz waveform goes to L11. The data waveform goes to the Antenna Buffer (M4). The Central L.O. Receiver is very similar to the L.O. Receiver (L4) at the antennas except that instead of combining the 1200 MHz and 1800 MHz signals to produce a 600 MHz output the two signals go directly to the Central L.O. Filter (L14).

L10, CENTRAL LOCAL OSCILLATOR TRANSMITTER

Subsystem, Local Oscillator

Project No. 13240

1 per antenna; Rack D, Bin R, Slots 6-7 (central electronics room)

Design engineer, H. L. Beazell

L10 produces the modulated 1200 MHz and 1800 MHz signals that are transmitted to the antenna. It receives 1200 MHz and 1800 MHz at a single input from the 600-1800 MHz Multiplier (L13), separates them, modulates them, recombines them and thus provides an input to the IF Combiner (T2). Data modulation is received from the Central Buffer (M3), 5 MHz modulation from the master local oscillator, and gating signals for the modulation from the Timing Generator (L8). The function of this module is similar to that of the L.O. Transmitter (L3) at the antenna.

L11, CENTRAL LOCAL OSCILLATOR CONTROL

Subsystem, Local Oscillator

Project No. 13240

1 per antenna; Rack D, Bin R, Slot 1 (central electronics room)

Design Engineer, H. L. Beazell

L11 acts as an interface between the LO modules in Rack D and a Data Set (M1) and thereby provides monitor and control of that part of the oscillator system. It also contains digital phase detectors which measure the 5 MHz and 600 MHz round-trip phases. The 5 MHz from the antenna is received in L9 where its phase is compared with that of a signal at 5·0000192 MHz from the master local oscillator. Similarly 600 MHz from the antenna is compared in L14 with 600·0000192 MHz from the master local oscillator. The two resulting 19·2 Hz waveforms go to L11 where the phase of either one can be compared with the standard 19·2 Hz, and the measured phase values go to the synchronous computer through the monitor and control system.

L12, MASTER LOCAL OSCILLATOR OFFSET

Subsystem, Local Oscillator

Project No. 13240

1 in Master LO; Rack M, Bin T, Slot 8

Design Engineer, H. L. Beazell

The function of L12 is to provide signals at 5·0000192 and 600·0000192 MHz (i.e. 5 and 600 MHz offset by the 19·2 Hz switching frequency) that are required for the round-trip phase measurement scheme described under L11. It contains phase lock loop circuitry that controls an L1 and an L2 in the master LO rack to provide the offset 600 MHz. It also contains a 5 MHz VCXO which is phase locked at the offset 5 MHz frequency.

L13, 600 to 1800 MHz MULTIPLIER

Subsystem, Local Oscillator

Project No. 13220

1 in Master L.O.; Rack M, Bin T, Slots 5-6 (central electronics room)

Design engineer, H. L. Beazell

L13 receives a 600 MHz signal from the 50 MHz Harmonic Generator (L2) and produces 1200 MHz and 1800 MHz signals which are combined and provided to the Central L.O. Transmitters (L10). The 1200 MHz is also doubled to provide a 2400 MHz signal to the Modems (L1) where it is used to lock the carrier oscillator.

L14, CENTRAL LOCAL OSCILLATOR FILTER

Subsystem, Local Oscillator

Project No. 13240

1 per antenna; Rack D, Bin R, Slots 4-5 (central electronics room)

Design engineer, H. L. Beazell

L14 takes the 1200 MHz and 1800 MHz signals from the antenna, which come from the Central L.O. Receiver (L9), and locks two voltage-controlled cavity-tuned oscillators to them. The loop time constants are long enough that the oscillators act as clean-up filters and remove the modulation sidebands and much of the noise from the received signals. Outputs at 1200 MHz and 1800 MHz are provided to the L.O. Offset modules (T4A and T4B). The 600 MHz difference frequency is generated and its phase is compared with that of the offset 600 MHz from the master local oscillator, and the resulting 19·2 Hz waveform goes to L11.

L17, SYNTHESIZER PHASE-LOCK MODULE

Subsystem, Local Oscillator

Project No. 13220

2 in Master L.O.; Rack M, Bin U, Slots 9-10 and 11-12 (central electronics room)

Design Engineer, W. E. Dumke

Four tunable signals are distributed to the L.O. Offset Modules (T4A and T4B) to provide a fine tuning capability. The tuning ranges of the signals are 125±25 MHz, 225±25 MHz, 225±25 MHz, 125±25 MHz for IF channels A, B, C, and D respectively[1]. The signals are obtained from four Fluke Model 6160B Frequency Synthesizers those for channels B and C being frequency doubled. The variable signals are thus tunable in 1 or 2 Hz steps. For operation in the polarization mode coherence between channels A and C and between channels B and D must be preserved. To achieve this the synthesizers for channels A and C are phase locked so that the sum of the output frequencies is 350 MHz. The synthesizers use an external 5 MHz reference frequency, and for one of them this is derived from the master L.O. and for the other from a voltage controlled crystal oscillator (VCXO). The outputs from the two synthesizers are summed and compared in a phase detector with 350 MHz derived from the master L.O., and the output of the phase detector is used to close a phase lock loop that controls the VCXO. An identical system is used for channels B and D.

L17 contains the circuitry required to control each synthesizer pair; the frequency doubler, 350 MHz phase detector and 5 MHz VCXO. It also contains switching so that all synthesizers can be directly referenced to the master L.O. for observations requiring independent tuning of the four channels.

L18, VARIABLE FREQUENCY DRIVER

L19, MASTER L.O. DRIVER

Subsystem, Local Oscillator

Project No. 13220

1 each in Master L.O.; Bin U, Slots 4-5 (L18) and 6-8 (L19)

Design Engineers, A. R. Thompson and L. R. D'Addario

The above modules contain medium power amplifiers that drive distribution networks for signals that are distributed from the master local oscillator subsystem to each of the D racks in the central electronics room. The amplifiers are all commercially made units. L18 contains four amplifiers for the four fine-tuning signals from the Synthesizer Phase-Lock Modules (L17). L19 contains amplifiers for signals at 5, 10, 600 and 2400 MHz.

[1]Wider ranges are used in the prototype system to accommodate the 40 MHz intermediate frequencies.

L20, MASTER LOCAL OSCILLATOR CONTROL MODULE

Subsystem, Local Oscillator

Project No. 13220

1 in Master L.O.

Design engineer, unassigned

L20 provides direct computer control and monitoring of the master L.O. subsystem. It has not yet been designed (February 1976).

M1, DATA SET

Subsystem, Monitor and Control

Project No. 13720

5 per antenna; Rack A, Front End Bin, Slot 12; Rack B, Bin D, Slot 7 (antenna vertex room)

Pedestal Room Rack and Bin, Slot 2; Control Unit in Pedestal Room Rack; (Antenna pedestal room)

Rack N, E or W, Bin Q, Slot 7 (central electronics room)

Design Engineers, Metrics Systems and D. W. Weber

The Data Set is a data collection and distribution unit that provides the interfaces between the monitor and control system and the electronic receiving system. Digital data are exchanged in the form of 24-bit words with serial input and output, the clock and other control waveforms being provided by the Data Set. Three digital outputs and four digital inputs can each be submultiplexed with a four-bit address provided by the Data Set, thus allowing up to 48 command functions and 64 monitor functions, each involving 24 bits of data. There are also eight analog monitor inputs which can similarly be submultiplexed to allow monitoring of up to 128 analog voltages. Analog inputs are in the ±10V range and are converted to 12-bit digital values, two of which can be included in one monitor word.

A Data Set communicates with the computer through a Central Buffer (M3) or an Antenna Buffer (M4), using 45-bit words which contain the 24 data bits, 16 address bits and five parity bits. Up to eight command words can be issued per 19·2 Hz cycle, but at the antenna this number is further limited by the capacity of the waveguide communication channel. Two monitor words per 19·2 Hz cycle are read back from each Data Set. The address of the first is obtained by stepping once per cycle through 192 addresses stored in a programmable read-only memory. The address of the second word is obtained by incrementing a 192-bit counter, or it can be held at a constant value under command from the computer.

M2 DATA TAP

Subsystem, Monitor and Control

Project No. 13720

2 per antenna; Rack B, Bin D, Slots 3-6; (antenna vertex room)

Pedestal Room Rack and Bin, Slots 3-6; (antenna pedestal room)

10 per array; Rack N, E or W, Bin Q, Slots 3-6 (central electronics room)

Design Engineers, Metric Systems and D. W. Weber

The Data Tap Modules provide display of a data word when the octal address of the word is manually entered on thumbwheel switches. All data words are displayed on a 24-bit binary presentation and can also be displayed in octal form. For words representing two analog voltages, the data are displayed in decimal form and are also reconverted to analog for monitoring on an oscilloscope or chart recorder. In addition, the Data Tap provides the facility for selecting any word with a parity error and displaying both the data and the address.

M3, CENTRAL BUFFER

Subsystem, Monitor and Control

Project No. 13720

1 per Antenna, Rack N, E or W, Bin Q, Slot 2 (central electronics room)

Design Engineers, Metric Systems and D. W. Weber

The Central Buffer is a link between the Serial Line Controller and the other units of the monitor and control system. Commands with the appropriate address are selected and transmitted to the Antenna Buffer (M4) or the Data Set (M1) in Rack D. Up to four words per 19·2 Hz cycle can be transmitted to the Antenna Buffer. Up to ten monitor words per cycle are received from the Antenna Buffer and up to two from the Data Set. The Central Buffer contains modulating and demodulating circuitry which interfaces with the Central L.O. Transmitter (L10) and Central L.O. Receiver (L9) for communication via the waveguide.

M4, ANTENNA BUFFER

Subsystem, Monitor and Control

Project No. 13720

1 per antenna, Rack B, Bin D, Slot 2 (antenna vertex room)

Design Engineers, Metric Systems and D. W. Weber

The Antenna Buffer stores and emits up to four commands per cycle to the Data Sets (M1) at the antennas. It also polls the Data Sets for two monitor words per cycle. The Antenna Buffer contains modulating and demodulating circuitry which interfaces with the L.O. Transmitter (L3) and L.O. Receiver (L4) for communication via the waveguide.

M5 COMMAND SIMULATOR

Subsystem, Monitor and Control

Project No. 13720

1 per antenna, Rack B, Bin D, Slots 8-11 (antenna vertex room)

Design Engineer, D. W. Weber

The Command Simulator provides a means of injecting commands manually at the antenna for testing units of the electronics that require setup commands from the monitor and control system. Address and data bits can be entered on front panel switches, and the command word thus generated goes to the Antenna Buffer (M4) and then to the appropriate Data Set (M1). The Command Simulator also contains provision for displaying monitor words transmitted by the Antenna Buffer to check for correct operation of that unit.

M7, FOCUS/ROTATION CONTROL
M8, FOCUS/ROTATION POWER SUPPLY

Subsystem, Monitor and Control

Project No. 13740

1 each per antenna; Pedestal Room Rack and Bin, Slots 1 (M7) and 7-12 (M8), (antenna pedestal room)

Design Engineer, D. W. Weber

The Focus/Rotation Control module accepts commands from the Data Set (M1) in the antenna pedestal room and generates the pulse trains required to drive the mount of the Cassegrain subreflector. The pulse trains go to translator units that drive stepping motors on the mount. Position readback voltages allow servo loops to be closed within the module, and accelerating and decelerating pulse rates are produced to speed up the motion of the mounts. The module also contains circuitry associated with limit switches and brake controls.

The Focus/Rotation Power Supply provides dc power for the Focus/Rotation Control, a Data Set and a Data Tap in the pedestal room. It also contains front panel switches for manual control of the focus and rotation motions.

P1 TO P5, POWER SUPPLY MODULES

Project No. 13040

P1,+5V and -5·2V
1 per antenna, Rack B, Bin J, Slots 1-6 (antenna vertex room)

P2, ± 15V
1 per antenna, Rack B, Bin J, Slots 7-12 (antenna vertex room)

P3, ± 28V
1 per antenna, Rack B, Bin I, Slots 1-3 (antenna vertex room)

P4, +5V and -28V
1 per antenna, Rack D, Bottom Bin, Slots 1-6 (central electronics room)
1 in Master L.O. Rack M, Bottom Bin, Slots 1-6 (central electronics room)

P5,± 15V and +28V
1 per antenna, Rack D, Bottom Bin, Slots 7-12 (central electronics room)
1 in Master L.O., Rack M, Bottom Bin, Slots 7-12 (central electronics room)

The power supply modules use Lambda units of type LCS or LXS.

T1, MODEM

Subsystem, IF

Project No. 13440

2 per antenna; Rack B, Bin I, Slots 11-12 (antenna vertex room) and Rack D, Bin R, Slots 11-12 (central electronics room)

Design Engineer, W. E. Dumke

In the T1 modules the IF and LO signals in the 1 and 2 GHz range are modulated onto the high frequency carriers for transmission down the waveguide system, and demodulated when received. Each modem contains a Gunn diode oscillator in the 26-52 GHz frequency range which is locked to a harmonic of 2·4 GHz with an IF offset of 10 MHz. The oscillator frequencies are (N+10)x2400 ± 10 MHz where N is the channel number (1 to 11) and the minus sign applies when N is even. A different oscillator frequency is used for each antenna on the same arm of the wye. The signals to be transmitted are modulated onto the oscillator output in a diode mixer, and the carrier and lower sideband are removed by a filter before transmission. In reception the same oscillator and mixer act as a synchronous demodulator. Diode switches and a switched circulator are used to control the transmit and receive functions. Timing waveforms for the transmit and receive sequence are obtained from the Timing Generator (L8). If the Gunn diode oscillator loses lock the the loop goes into an automatic search mode for eight seconds, after which it alternates between periods of search and fixed tuned operation. The latter enables monitor and control data to be transmitted to help locate the fault.

T2, IF COMBINER

Subsystem, IF

Project No. 13440

2 per antenna, Rack B, Bin I, Slots 9 - 10 (antenna vertex room) and Racks D, Bin R, Slots 8 - 9 (central electronics room)

Design Engineer, W. E. Dumke

T2 acts as a combiner for IF and LO signals going to the modem (T1) for transmission down the waveguide, and as a divider for signals received by the modem. At the antenna, inputs are the combined IF outputs of the four Frequency Converters (F4) and the 1200 and 1800 MHz signals with their 5 MHz and data sidebands from the Local Oscillator Transmitter (L3). These are combined and amplified and go to the Modem (M1). Received signals from the Modem go from T2 to the L.O. Receiver (L4). At the central electronics room the signals to be transmitted come from the Central L.O. Transmitter (L10) and the received signals go to the Central L.O. Receiver (L9) and the four IF Receivers (T5). The transmitted and received signals go through separate amplifier chains which are switched on and off in the transmit/receive sequence to improve isolation between the signals. Monitoring terminals for the transmitted and received signals are provided.

T4A and T4B, LOCAL OSCILLATOR OFFSET MODULES

Subsystem, IF

Project No. 13450

2 per antenna, Rack D, Bin S, Slot 1 (T4A) and Slot 2 (T4B) (central electronics room)

Design Engineer, A. R. Thompson

T4A and T4B supply the local oscillator signals to the IF Receivers (T5) required to convert the four IF bands in the 1-2 GHz range down to 0-50 MHz. T4A supplies signals at 1300^{+50}_{-40} MHz and 1400^{+50}_{-40} MHz for conversion of channels A and B respectively. These are obtained by adding signals from a Synthesizer Phase-Lock Module (L17) to 1200 MHz from the Central L.O. Filter (L14). The ranges indicated can be covered in 2 Hz steps and thus provide a fine tuning capability. Similarly T4B provides signals at 1550^{+40}_{-50} MHz and 1650^{+40}_{-50} MHz for conversion of channels C and D by subtracting signals from an L17 from 1800 MHz.

T5, IF RECEIVER

Subsystem, IF

Project No. 13450

4 per antenna, Rack D, Bin S, Slots 4, 6, 8 and 10 (central electronics room)

Design Engineer, A. R. Thompson

In the T5 modules the four IF bands centered at 1325, 1425, 1575 and 1675 MHz are converted down to the 0 - 50 MHz range and amplified to a level of approximately 2 V rms before going to the Sampler (D1). A separate T5 is used for each channel. In each one the signal is converted using an oscillator signal from the appropriate L.O. Offset Module (T4A or T4B) and passes through filters that define the frequency range as 1 to 50 MHz. Additional filters with bandwidths and center frequencies given in Table II-4 can be switched in as desired by Pin diodes. A current controlled attenuator for external control of the output level is included, and this usually operates in an a.l.c. loop under control from the Sampler (D1). A monitoring detector is also included.

T6, IF CONTROL MODULE

Subsystem, IF

Project No. 13450

1 per antenna, Rack D, Bin S, Slot 12 (central electronics room)

Design Engineer, A. R. Thompson

T6 enables the filters in the four IF Receiver (T5) Modules and four Spectral Line IF(T7) Modules to be selected either manually or under computer control, and the gains of the same units to be set manually or controlled by a.l.c. loops. Manual control is effected through front panel switches and potentiometers on the T6 module. An interface with a Data Set (M1) enables the filter select signals to be received from the computer, and the voltages of the a.l.c. signals and the outputs of the IF level monitoring detectors to be fed back to the computer.

BLOCK DIAGRAMS OF THE SYSTEM

Block schematic diagrams of the electronics at an antenna and in the central electronics room, including the master local oscillator, are located in the pocket at the end of this report. The division of the system into modules is shown in these diagrams, and the functioning of the system should be largely explained by the foregoing notes in this section.

Note that the diagrams show the prototype electronic system and some details may be inconsistent with the text of this manual. Revised versions are in preparation.

V. FURTHER ELECTRONIC SYSTEM DETAILS

(a) Determining Observing Frequencies and Bandwidths

Because of the number of frequency changes in the IF transmission path, and the fact that three of the local oscillator signals are tunable in discrete steps, determination of the center frequency of the signal band is rather complicated. The sequence of frequency conversions and bandwidth limiting elements is shown in Figure V-1. The frequency response of the system is limited at two points. The first is the front end filter unit where the signals are confined to the 1000-1050 MHz band. Filters can be introduced to provide selectivity against interfering signals and in some cases the response is matched to one of the radio astronomy bands[1]. The second point is in the final IF stages in the T5 modules in the control building. Generally the final IF response will dominate, but in some cases it may be necessary to consider the combined response.

The center frequency of the signal band, as limited by the front end filter unit, is given by

$$f_{signal} = \pm f_1 \pm [f_2 + f_{filter}] \qquad (1)$$

where f_1 and f_2 are defined below and f_{filter} is the center frequency of the filter.

The center frequency of the signal band, as limited by the final IF stages, is given by

$$f_{signal} = \pm f_1 \pm [f_2 - f_3 + f_4 + f_{IF}] \qquad (2)$$

First ± sign The first ± sign in equations (1) and (2) is - for the 18-21 cm band and + for all other cases.

f_1 f_1 is the frequency of the first local oscillator. For the 18-21 cm band it is the upconverter pump frequency of 3200 MHz. For the 6 cm band it is zero since there is no frequency conversion in front of the parametric amplifier. For the 2 and 1·3 cm bands it is the frequency of the 17-20 GHz local oscillator which is discretely tunable as follows:

$$f_1 = m \times 600 \pm n \times 100 \text{ MHz},$$

m and n being integers. For details see the manual on F3.

[1] In the prototype system these filters are omitted and the full 50 MHz bandwidth is passed at the antennas.

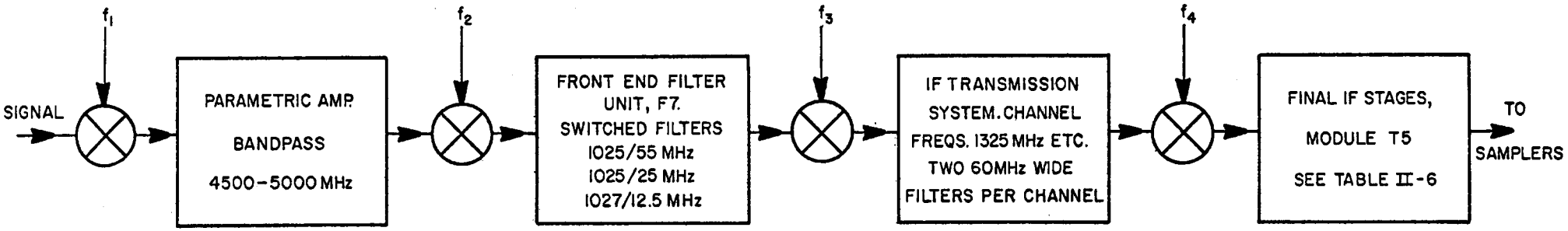


Figure V-1 Schematic diagram of a signal channel showing frequency conversions and bandpass limiting elements.

Second ± sign The second ± sign in equations (1) and (2) is - for the 2 cm band and + for all other cases.

f_2 f_2 is the frequency of the 2-4 GHz Synthesizer module. It is given by

$$f_2 = 3000 + N \times 50 \pm 10{\cdot}1 \text{ MHz}^1,$$

N being an integer. For details see the manual on L6. Two of these units, which are independently tunable, are used at each antenna. One is for channels A and C, and one for B and D.

f_3[1] f_3 is the oscillator which converts the signal frequencies from 1025 MHz to the four bands centered on 1325, 1425, 1575 and 1675 MHz. It has the following fixed values.

300 MHz, channel A
400 MHz, channel B
550 MHz, channel C
650 MHz, channel D

f_4 f_4 represents the frequencies used to convert the bands at 1325 MHz, etc., down to the 0-50 MHz band. Tunability in 2 Hz steps is possible using four frequency synthesizers (Fluke model No. 6160B) in the master local oscillator. Two modes of operation are provided.

Independent Tuning Mode

$$\begin{aligned} f_4 &= 1200 + f_{SA} \text{ MHz, channel A} \\ &= 1200 + 2\, f_{SB} \text{ MHz, channel B} \\ &= 1800 - 2\, f_{SC} \text{ MHz, channel C} \\ &= 1800 - f_{SD} \text{ MHz, channel D} \end{aligned}$$

f_{SA}, f_{SB}, f_{SC}, f_{SD} are the frequencies of the four synthesizers, which are independently tunable in 1 Hz steps.

[1]For the prototype system the 3000 figure in the expression for f_2 is 2400 and f_3 is zero for all channels.

Polarization Mode

For polarization observations correlation must be preserved between channels A and C and between channels B and D. In this case the synthesizers for channels A and C and for channels B and D are phase locked to maintain the following conditions:

$$f_{SA} + 2\, f_{SC} = 350 \text{ MHz}$$

$$2\, f_{SB} + f_{SD} = 350 \text{ MHz}$$

For further details see the description of L17 in Section IV.

f_{IF}

f_{IF} is the center frequency of the IF amplifier at the control building. The center frequency for each bandwidth is given in Table II-6. Bandwidths go in steps of a factor of two and the corresponding center frequencies are chosen to be appropriate for bandpass sampling for spectral line observations.

Local oscillator frequencies must, of course, be chosen so that the signal band falls within all of the pass bands shown in Figure V-1. Selection of oscillator frequencies and bandwidths is usually accomplished through the synchronous computer and the monitor and control system. Command and address codes are given in the manuals describing the modules involved.

(b) The Use of Walsh Functions in Phase Switching

Phase switching is used in the VLA to eliminate unwanted offsets at the multiplier outputs. Such offsets can result from reference level errors in the samplers, spurious correlated signals in the receiving channels, or cross coupling of the IF signals. Signals entering the antennas undergo phase switching twice, once at the antennas and once at the sampler outputs, and the two phase reversals cancel one another. Spurious signals are most likely to be introduced in the waveguide transmission system, and such signals are phase switched only once. If the phase switching signals are orthogonal; i.e., the infinite integral of the product of any pair is zero, the products of signals which are switched only once will also average to zero.

For simplicity, phase switching by 180^{o} is preferred to sinusoidal or other forms of phase modulation. Twenty seven two-state waveforms are required, all possible pairs of which are orthogonal. Simple squarewaves[1] which are related by factors of two in their periods are orthogonal and simple squarewaves of the same frequency but in phase quadrature are also orthogonal. If one antenna is unswitched, two sets of quadrature squarewaves with frequencies running from f_o to $2^{13} f_o$ could be used. The frequency f_o should be of the order of 1 Hz or greater for effective reduction of the unwanted responses. (For a more detailed discussion see VLA Electronics Memoranda Nos. 116 and 122.) The highest frequency, $2^{13} f_o$ is then about 8 kHz, which is rather inconveniently high if accurate phase relationships are to be maintained between waveforms at the antennas and the control building.

The use of Walsh functions for phase switching was suggested by B. G. Clark. These waveforms can be described as squarewaves of varying period, and their rate of change between the two states is given by the sequency, measured in zps {(zero-crossings per second)/2}. For a further description see, for example, Harmuth (1969) or Siemens and Kitai (1969). Two orthogonal series, cal and sal, are available and to obtain 27 orthogonal switching functions a range of sequencies from f_o to only $13 f_o$ is required if both series are used. The minimum switching interval is then $(32 f_o)^{-1}$ which is fairly close to the period of the transmit-receive

[1]The term simple squarewaves is used to denote squarewaves of constant period; i.e., like strongly clipped sine waves.

cycles in the waveguide. Using Walsh functions for the switching waveforms it is therefore possible to perform all switching transitions during the intervals of transmission from the control building when the received signals are not used. This eliminates switching transients, and the accuracy of the transmission timing ensures that the correct phasing is maintained between the cal and sal functions. The Walsh functions are generated by the synchronous computer and transmitted to the antennas by the monitor and control system. One 24-bit word, containing the Walsh function states for 24 cycles, is transmitted to each antenna every 1·25 seconds.

For an array with two antennas the switching functions are given by the matrix

$$\begin{array}{l} \\ \text{Antennas} \downarrow \end{array} \begin{array}{c} \text{Time} \longrightarrow \\ \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix} \end{array} \qquad (1)$$

where the different columns indicate time intervals and the rows indicate different antennas. The matrix for four antennas is given by replacing each element of (1) by the full matrix;

$$\begin{array}{l} \\ \text{Antennas} \downarrow \end{array} \begin{array}{c} \text{Time} \longrightarrow \\ \begin{pmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{pmatrix} \end{array} \begin{array}{l} \text{Wal(0,t)} \\ \text{Sal(2,t)} \\ \text{Sal(1,t)} \\ \text{Cal(1,t)} \end{array}$$

The process can be repeated for greater numbers of antennas. Note that both sal and cal functions of the same sequency are included.

(c) Built-in Calibration

A gain calibration scheme using switched noise sources is incorporated into the electronic system. The noise sources are usually gated on and off during alternate cycles of the 19·2 Hz transmission system; i.e., they are modulated with a squarewave of frequency 9·6 Hz. Noise sources are provided for all four wavelength bands, and separate sources are used for the two opposite polarization inputs. The noise power is injected through directional couplers and levels are generally set to be 10-20% of the system temperature.

A power law detector in the frequency converter module (F4) provides measurements of power levels which are recorded by the synchronous computer through the monitor and control system. Two measurements are provided for each channel. The first uses a synchronous detector to measure the difference in levels between the on and off conditions of the noise source, and is referred to as the synchronous detector output. The second uses a gating circuit to measure the power level when the noise source is off, and is referred to as the gated total power output. The synchronous detector output is proportional to the injected noise level (which can be assumed to be constant) and the channel gain. The gated total power output is proportional to the system noise temperature and the channel gain. The two levels thus provide a means of calibrating changes in system temperature, which varies with antenna elevation, etc., and the corresponding gain changes produced by the a.l.c. circuits. The synchronous detector and gating circuits are also located in the frequency converter and further details on them can be found in the manual on that module.

In addition to the noise sources it is intended to add a system using synchronous trains of narrow pulses injected at the antennas. This will provide correlated signals for calibration of the bandpass characteristics of the channels. Such a system is required mainly for spectral line observations, and it will be developed as the spectral line system is brought into operation.

(d) Numbering System for the Racks, Bins and Modules

NATIONAL RADIO ASTRONOMY OBSERVATORY
Post Office Box "O"
Socorro, New Mexico 87825

SPECIFICATION NO.: A13010N1A

NAME: VLA Electronics Rack, Bin, Module, and Connector Numbering System.

DATE: June 24, 1974 Revised September 21, 1976

PREPARED BY: S. Weinreb
A. R. Thompson
L. R. D'Addario

APPROVED BY:

A. APPLICATION

This numbering system applies to all equipment in the module-bin system; it does not apply to digital equipment utilizing card and motherboard packaging.

B. MODULE TYPE NUMBER

Each module type will be identified by a 2 or 3 character code such as F2 or L12. The first character denotes subsystem:

F ≡ Front-end
L ≡ Local Oscillator
T ≡ Signal Transmission or IF
M ≡ Monitor and Control
P ≡ Power Supply
D ≡ Delay and Multiplier

The second character is a one or two digit number denoting a particular type of module in a subsystem. The module type number will be marked with 3/16" letters on the lower front panel. (The module name will also be marked on the upper front panel.)

C. MODULE SERIAL NUMBER

Each module will have a 2 or 3 character serial number such as A1 or B13. The first character notes a particular version or revision; the second character is a consecutive serial number not affected by the revision letter (i.e., if 2 version A modules, A1 and A2, were built the first revision B module would be labeled B3). The serial number will be marked with 1/8" letters on the lower front panel.

D. RACK TYPE DESIGNATION

Letters are used to designate types of racks in the system as follows:

A ≡ Front-end Rack (antenna vertex room)
B ≡ IF/LO Rack (antenna vertex room)
C ≡ Pedestal Room Rack (antenna pedestal room)
D ≡ IF/LO Rack (control building, central electronics room)
M ≡ Master LO (control building, central electronics room)

One each of types A, B, C and D is required for each antenna.

Racks and antennas will have serial numbers in the range 1 to 28. In general racks located at antennas (types A, B and C) will be chosen so that their serial number is the same as that of the antenna. Racks of type D are not permanently related to a particular antenna, but are related by their location to a particular arm of the wye and waveguide channel number. Individual D racks can be referred to by arm (N, E or W) and channel number (e.g., W5) as well as by serial number.

E. BIN NUMBER

Bins will be lettered as follows:

G	Front-end Rack
H, I, J, K	IF/LO Rack at Antenna (top to bottom)
Q, S, R	IF/LO Rack at Control Room (top to bottom)
T, U	Master LO Rack

F. SLOT NUMBER

Slots within a bin will be numbered 1 through 12 (1 through 20 for bin G which is extra wide) from left to right as viewed from front and right to left as viewed from rear. If a module occupies more than one slot width its location will be designated by the lowest slot number it occupies.

G. CONNECTOR AND PIN NUMBER

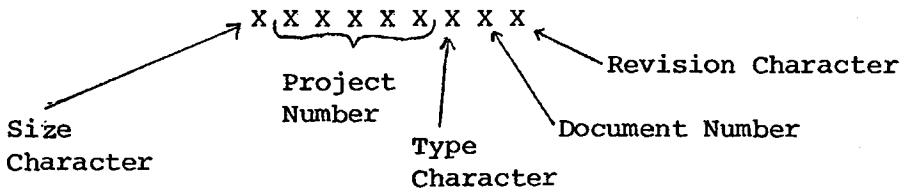
Plugs and jacks will be noted P or J, respectively, followed by a number which increases from top to bottom of the slot. For multi-pin connectors this will be followed by a dash and the pin number; i.e., J1-42.

H. EXAMPLE

In most cases the complete number will not be necessary; i.e., we will refer to "Rack B1", "Bin H" or "Module T2". However, an example of a specific pin number is 27BH12J1-42 which refers to antenna 27, rack B, bin H, slot 12, jack 1, and pin 42.

(e) Documentation

The basic documentation for the VLA electronics consists of a large number of drawings, specifications, parts lists, wire lists, etc., which are on file at the site. Each of these is assigned a reference number of the following form.



Size Character

A	8·5 x 11 inches
B	12 x 18 inches
C	18 x 24 inches
D	24 x 36 inches

Project Number

This number is in the range 13000 to 13999 for all electronics documents. Project numbers for the modules are given in Section IV.

Type Character

N	Specifications
P	Parts List
T	Test Procedure
R	Test Results
F	Fabrication Procedure
D	Manufacturing Test Data
A	Artwork
B	Block Diagrams
L	Logic Diagrams
M	Mechanical Drawings
P	Pattern Drawings
S	Schematic
W	Wiring List

Document Number

This is a consecutive serial number. It is not affected by the size character.

Revision Character

A, B, C, etc.

Example

D13250L3B is a logic diagram for the 2-4 GHz Synthesizer module, size 24 x 36 inches, second revision.

In addition to the above documents a manual should exist for each module or similar electronics unit. The manual describes the function of the unit, assembly, test and maintenance procedures, and lists all relevant documents. The manuals comprise a series of VLA Technical Reports.

VLA Electronics Memoranda are a series of documents that contain data of various types relevant to the electronics. They include design studies, discussions of tolerances on design parameters, reliability estimates, etc.

Copies of the Reports and Memoranda and lists of their titles are available through the VLA project office.

Appendix (a) Antennas

The antennas have 25 meter diameter main reflectors which are shaped to optimize the gain when used in the Cassegrain mode. The mounts are altazimuth and fully steerable. The base of the antenna structure is triangular with sides of length 32 feet, and each corner is supported by a concrete foundation pedestal. The antennas are manufactured by E-Systems, Inc., of Dallas, Texas. Some details of design and performance are listed below.

Reflector diameter, 25 m (82 feet)

Total geometrical aperture, 421m^2

Focal Length of main reflector, 9m

Maximum width of subreflector (asymmetric), 1·83m (6 feet)

Effective magnification, 8·8

Total blockage (subreflector and support legs) gives apperture efficiency reduction factor 0·85.

Surface accuracy,	panels,	< 0·038 cm r.m.s.
	panel setting,	< 0·046 cm r.m.s.
	gravity, wind, thermal,	0·036 cm r.m.s.
	Total	< 0·070 cm r.m.s.

Azimuth and elevation position readouts, Inductosyn, 20 bits for 360^o.

Non-repeatable pointing errors, < 15 arcsec (combined az. and el. for wind < 15 mph and temperature differences of structure < 5^{o}F)

Slew rates, azimuth 40^o per minute
elevation 20^o per minute.

Drive, servo controlled 5 H.P. electronic motors, 2 per axis.

Minimum elevation, 9^o; Stow position, zenith

Total weight of antenna, 419,000 pounds (~ 210 tons)

Resonant frequency, torsional 2·2 Hz
rocking 2·3 Hz

Wind speed specifications,	precision operation	< 15 m.p.h.
	normal operation,	< 40 m.p.h.
	survival at stow,	110 m.p.h. with snow load of 20 lbs.per sq.ft.

Diameter of Feed Circle, 1·95m.

Appendix (b) Transporter and Rail Track

The transporter that carries the antennas between foundations runs on two standard gauge (4 ft. 8½ in.) rail tracks spaced 18 ft. apart. It has four six-wheeled trucks, two on each track. The wheels on the trucks can be raised and lowered hydraulically, and the trucks can be turned horizontally through 90° to enable the vehicle to go from the main track to a spur track and vice versa.

The double rail track runs along the total length of each arm. The antenna foundations are centered 110 ft. from the center line of the rail tracks, and are reached by spur tracks which intersect the main track at right angles. The spur tracks are 2-3/4 inches above the main tracks, and short bridging sections of rail are inserted at the rail crossings when the transporter is on a spur track.

The vertical motion on the transporter wheels is 6 inches which allows the transporter to be raised to lift an antenna off a foundation or lowered to place it down on one. When making a turn between the main track and a spur the transporter is positioned with the trucks centered on the intersecting tracks. Three stabilizing jacks are then lowered to contact the ground. For each truck in turn, the wheels are lifted, the truck is swiveled through 90° and the wheels lowered onto the desired track. The turning operation takes approximately fifteen minutes.

Diesel engines on the transporter provide hydraulic and electric power. A hydraulic motor on one wheel of each truck provides propulsion at speeds up to 5 m.p.h. The transporter weighs 154,000 lbs. (77 tons). Antennas are moved in the stow (zenith) position and when on the transporter are safe in winds up to 60 m.p.h. However, antennas are generally not moved in winds above 25 m.p.h. A cherry picker with a 48 ft. boom is included on the transporter for maintenance work on antennas. The transporter was manufactured by E-Systems, Inc., who also made the antennas.

Appendix (c) Positions of Antenna Stations

Four configurations of antennas are available with the array, and these are referred to as A, B, C and D; A being the most extended. In each configuration the distance of the antenna stations from the center of the wye is proportional to n^{α} where n is the antenna number counting outwards along each arm. Chow (1976) has shown that such a power law arrangement gives good coverage in the (u,v)-plane for a three armed array. With hour angle coverage of eight hours or more, the array performance is broadly optimized over a wide range of declinations if the value of α lies in the vicinity of 1·6. For the VLA, α = 1·716 which is equal to the logarithm to base 2 of the scale factor between adjacent configurations. With this scheme the n^{th} station on any configuration coincides with the $2n^{th}$ station on the next smaller configuration. The total number of stations for all configurations is thereby reduced from 108, which would be required with no coincidences, to 72. This reduction results in significant savings both in construction costs and reconfiguration time.

The relative positions of antennas corresponding to the power law configuration is shown in Figure A-1. The D configuration is slightly modified to avoid congestion near the array center by putting the n = 1 stations of the southeast and southwest arms on a short southern extension of the north arm.

Table A-1 gives the positions of all antenna stations in terms of their distance from the center of the array. Stations are designated by A, B, C or D for the configuration, N, E or W for the arm, and 1 to 9 for the station number along the arm. The position angles of the arms are as follows:

north 354° 59' 42"
southeast 114° 59' 42"
southwest 236° 00' 03"

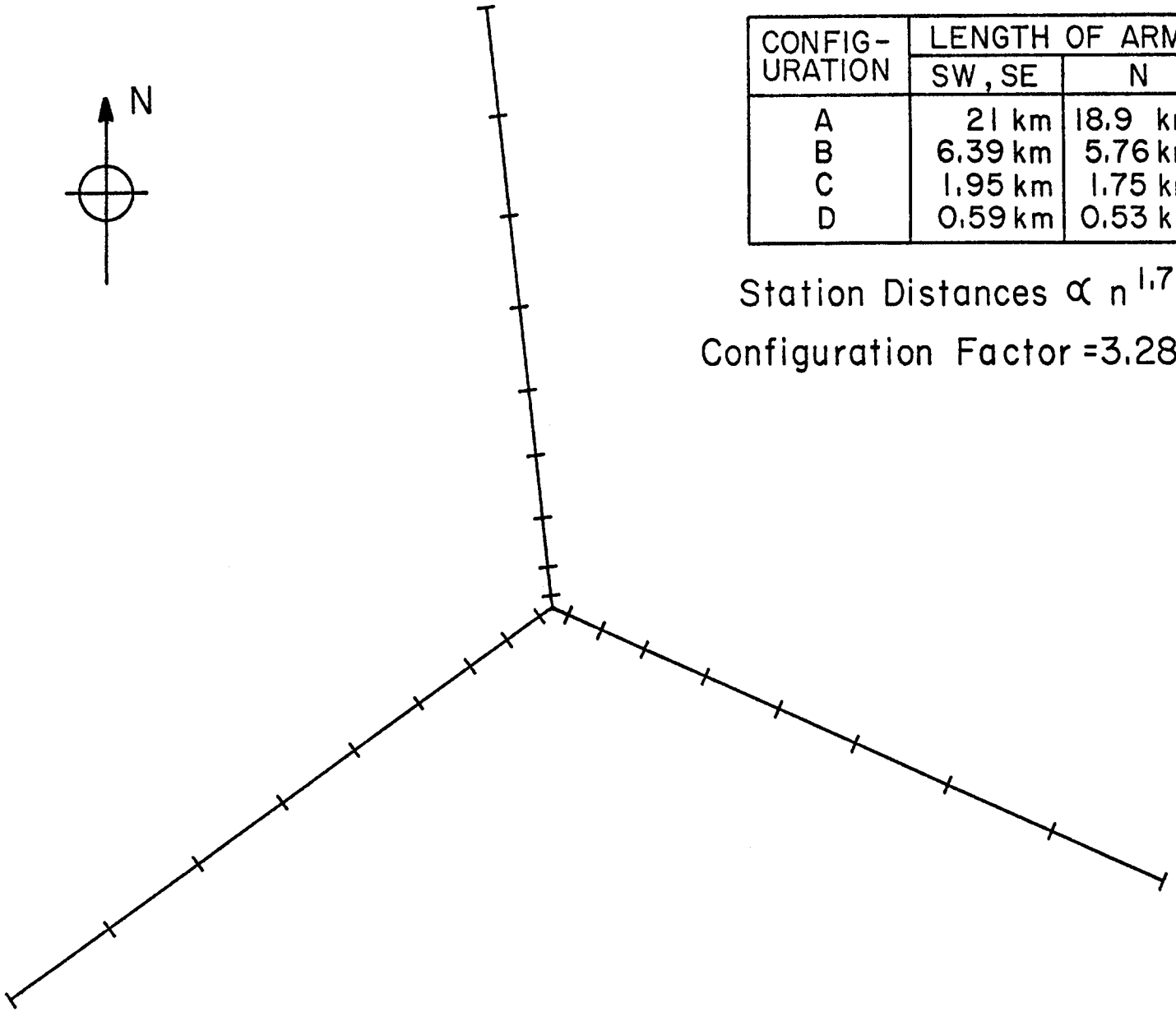
The geodetic coordinates of the center of the array are:

latitude 34° 04' 43·497" north
longitude 107° 37' 03·819" west

The height of the center point is 6,970 ft. above sea level and the height variations along the arms lie within ± 200 ft.

STATION	DISTANCE (M)	STATION	DISTANCE (M)	STATION	DISTANCE (M)
DW1	-40.00	DE1	-80.00	DN1	0.00
DW2-CW1	44.85	DE2-CE1	44.85	DN2-CN1	54.86
DW3	89.93	DE3	89.93	DN3	94.86
DW4-CW2-BW1	147.33	DE4-CE2-BE1	147.33	DN4-CN2-BN1	134.86
DW5	216.07	DE5	216.07	DN5	194.82
DW6-CW3	295.43	DE6-CE3	295.43	DN6-CN3	266.38
DW7	384.89	DE7	384.89	DN7	347.04
DW8-CW4-BW2-AW1	484.00	DE8-CE4-BE2-AE1	484.00	DN8-CN4-BN2-AN1	436.40
DW9	592.40	DE9	592.40	DN9	534.15
CW5	709.79	CE5	709.79	CN5	639.99
CW6-BW3	970.50	CE6-BE3	970.50	CN6-BN3	875.07
CW7	1,264.35	CE7	1,264.35	CN7	1,140.03
CW8-BW4-AW2	1,589.92	CE8-BE4-AE2	1,589.92	CN8-BN4-AN2	1,433.58
CW9	1,946.03	CE9	1,946.03	CN9	1,754.67
BW5	2,331.65	BE5	2,331.65	BN5	2,102.37
BW6-AW3	3,188.09	BE6-AE3	3,188.09	BN6-AN3	2,874.59
BW7	4,153.40	BE7	4,153.40	BN7	3,744.98
BW8-AW4	5,222.90	BE8-AE4	5,222.90	BN8-AN4	4,709.31
BW9	6,392.69	BE9	6,392.69	BN9	5,764.08
AW5	7,659.48	AE5	7,659.48	AN5	6,906.29
AW6	10,472.87	AE6	10,472.87	AN6	9,443.03
AW7	13,643.92	AE7	13,643.92	AN7	12,302.27
AW8	17,157.23	AE8	17,157.23	AN8	15,470.10
AW9	21,000.00	AE9	21,000.00	AN9	18,935.00

Table A-1 Distances in meters of antenna stations from the array center. DW1 and DE1 are on a southern extension of the north arm and the distances of DN2, DN3 and DN4 have been slightly modified from the power law values to allow rail tracks to pass through.



CONFIG-URATION	LENGTH OF ARM	
	SW, SE	N
A	21 km	18.9 km
B	6.39 km	5.76 km
C	1.95 km	1.75 km
D	0.59 km	0.53 km

Station Distances $\propto n^{1.716}$

Configuration Factor $= 3.285 = 2^{1.716}$

Figure A-1 The power law configuration.

Appendix (d) Computers

The synchronous computer system which performs the on-line tasks of generating control commands for the array and collecting output and monitor data consists of four Modcomp units made by Modular Computer Systems of Fort Lauderdale, Florida. All four computers were initially obtained as model II/25 but two have been upgraded to model II/45 by increasing the memory ports to four. The two model II/45 units are the master processor (Boss), and the monitor and control computer (Monty) that interfaces with the serial line controller. The two remaining computers (Cora and Corb) interface with the controller of the delay and multiplier system and handle the output data of the array. A fifth model II/45 is to be obtained as a repair computer to replace any of the four units if a failure occurs.

A word length of 16 bits is used in the Modcomp computers. They have been programmed mainly in assembly language although a version of Fortran IV has also been used for some programs.

The asynchronous computer system which performs the main data analysis tasks consists of a PDP-10, manufactured by Digital Equipment Corporation of Maynard, Massachusetts, and a large collection of peripheral units. The latter includes a fast Fourier transform processor, minicomputers dedicated to specific tasks and output devices including graphics units. The system is likely to remain in a stage of development for several years.

The PDP-10 has a word length of 36 bits and interfaces with the synchronous computer system through a fixed head disk. The main programming language which is being used with it is Sail, a version of Algol developed by the Stanford Artificial Intelligence Laboratory. A special control language, Candid, is being developed for manipulating radio astronomy data.

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FOLD OUT

Box _____ of _____

Item # #1

Between Pages last page & Cover

Bind in rear pocket

ALL FEEDS
2 - LINEAR OR
2 - CIRCULAR
POLARIZATIONS

PARAMP PUMPS (2 REG'D)
GUNN OSCILLATOR
31.83 GHz
PUMP DISTRIBUTOR
-20dB MON
MON
+24dBm WG
WG +24dBm

FEED RING
FEED 18-21 cm
FEED 6 cm
FEED 2 cm
FEED 1.3 cm
-25dB
-28dB
NOISE SOURCE
7.0 MHz
-20dB
-28dB
NOISE SOURCE
9.6 MHz

ANTENNA

DEWAR RACK A (AB SHOWN)
UP CONVERTER 1.55-1.93 GHz
PUMP
CONTROL BITS
31.83 GHz PUMPS
PARAMP 2 STAGES
COAXIAL SWITCH
SYSTEM TEMPERATURES

18-21cm	50 °K
6	50
2	220
1.3	290

15 GHz COOLED MIXER
LO
28 GHz COOLED MIXER
LO
WG SWITCH
WG
4.5-5.0 GHz
AB
40dB
-25dBm/300MHz FOR 300°K INPUT TERMINATION
AB J1
CD J2

F6 RF SPLITTER RACK A
MONITOR
LEVEL
-6dB
VCA
TRANSFER SWITCH
DIVIDER
J6 A
J4 B
J3 C
J5 D

-40dBm/300MHz FOR 300°K INPUT TERMINATION

F4 FREQUENCY CONVERTER 4 PER ANTENNA RACK B
4950/790
ISOLATOR
27dB
SYNC. DET.
J3
J4 ALTERNATE
J5 IF FILTER
J6
J1-N 9.6 MHz
1325/50
1425/50
1675/50
1675/50
4

2-4 GHz LO +6 TO +15dBm

L6
DCS INTERFACE AND CONTROL
PHASE LOCKED LOOP
TUNING COIL
FM COIL
VCO 2-4 GHz YTO OSCILLATOR
J12
10.1 MHz REF
10.1 MHz IF
SECOND MIXER
FIRST MIXER
-10dB
0-1.2GHz AMP
2-4 GHz SYNTHESIZER RACK B
LO
600/LPF
1200/LPF
RANGE SELECT
HARMONIC GENERATOR
50 MHz
J8
-29dBm
J9 2400 MHz -19dBm
J9 ALTERNATE
J13 FIBER IN OUT
(4 PER ANTENNA)
10.1 MHz ± 500Hz GEN. OUT +10dBm

F2 UPCONVERTER PUMP RACK A
LOCK MONITOR
200MHz
90° HYBRID
3.2GHz
VCO TRANSISTOR
LOOP AMP
-20dB
POWER SET
90° HYBRID
CD 3.2GHz PUMP J9
3GHz 0dBm
J1
J2
J4 200MHz 0dBm

AB 3.2GHz PUMP +10 TO +16 dBm

F3 17-20GHz LO RACK A
IF MON
LOCK MON
50-3,000 MHz
÷120
75dB
4 BIT ERER CONTROL
90° HYBRID
-10dB
YIG VCO
LOOP AMP
19.3-19.9GHz
WG
-10dB
J3 J2 -10dBm 200 MHz
100 MHz -10dBm
17.3-19.9 GHz LO +11dBm

L7 FRINGE GENERATOR RACK B
10.1/.03
LOGIC
P1-5 100 KHz
P1-1 PHASE SW
DCS INTERFACE
(4 PER ANTENNA)
50 MHz CLOCK -9dBm
J1
J3
J2

L2 50-600 MHz MULTIPLIER RACK B
50 MHz
VCXO
DIVIDER
X2
X2
X3
PHASE LOCKED LOOP
Φ DET
50/4
100/8
200/16
100/50
DIVIDER
3dB
J10
J4 50 MHz +20dBm
J3 100 MHz +20dBm
J2
J9
J7
DIVIDER
20dB
+20dBm 200 MHz

BIAS SETTINGS IN F2 AND F3
F1 BIAS CONTROL RACK A 2 PER ANTENNA
BIAS LEVELS TO DEWAR

F5 FRONT END CONTROL RACK A
DCS INTERFACE

600 MHz +15 dBm

DIGITAL COMMUNICATIONS SYSTEM
QQ
5MHz
M4 ANTENNA BUFFER RACK B
L3-P1-5 DATA OUT
L4-P1-5 DATA IN
ANTENNA CONTROL UNIT RACK C DSA "0"
M1 DATA SET RACK A DSA "1"
RACK A
M1 DATA SET RACK B DSA "2"
M2 DATA TAP RACK B
RACK B
M1 DATA SET RACK C DSA "3"
M2 DATA TAP RACK C
M7 FOCUS/ROTATION CONTROL RACK C
M8 COMMAND SIMULATOR RACK B
QQ
5MHz

10MHz -9dBm
DIVIDER
T1-J14
10dB
DIVIDER
50MHz 0dBm
20MHz +10dBm J6
10MHz +10dBm J2
J1
J3
J4 5MHz +10dBm
+7dBm 5 MHz
DIVIDER
+14dBm 600 MHz
5MHz +10dBm
5MHz
P1-38
X5
10dB
X2
X2
Φ SHIFTER
5MHz PHASE ADJ
L1 5-50MHz VCXO RACK B
P1-7 SYNC
P1-5 5MHz
L8
T1A

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A				EXTENSIVE CHANGES

T1 MODEM RACK B

T2 IF COMBINER RACK B

L4 L.O. RECEIVER

L3 L.O. TRANSMITTER RACK B

L6 L.O. CONTROL RACK B

L8 DIGITAL DIVIDER RACK B

TIMING GENERATOR

DCS INTERFACE FOR T1 AND T2

SWITCHED T/R TTL

T1 MODEM WAVEGUIDE TRANSMIT SPECTRUM

T1 MODEM WAVEGUIDE RECEIVE SPECTRUM

MODEM WAVEGUIDE CHANNEL ALLOCATIONS

CHANNEL	LOCAL OSCILLATOR FREQUENCY f_o, GHz	SIGNAL BAND LOW	HIGH
1	26.41	27.41	28.41
2	28.79	29.79	30.79
3	31.21	32.21	33.21
4	33.59	34.59	35.59
5	36.01	37.01	38.01
6	38.39	39.39	40.39
7	40.81	41.81	42.81
8	43.19	44.19	45.19
9	45.61	46.61	47.61
10	47.99	48.99	49.99
11	50.41	51.41	52.41

RACK B

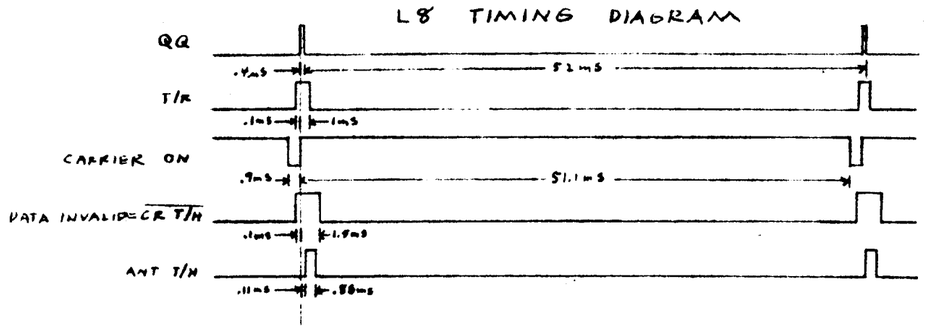
RACK A

NOTES:

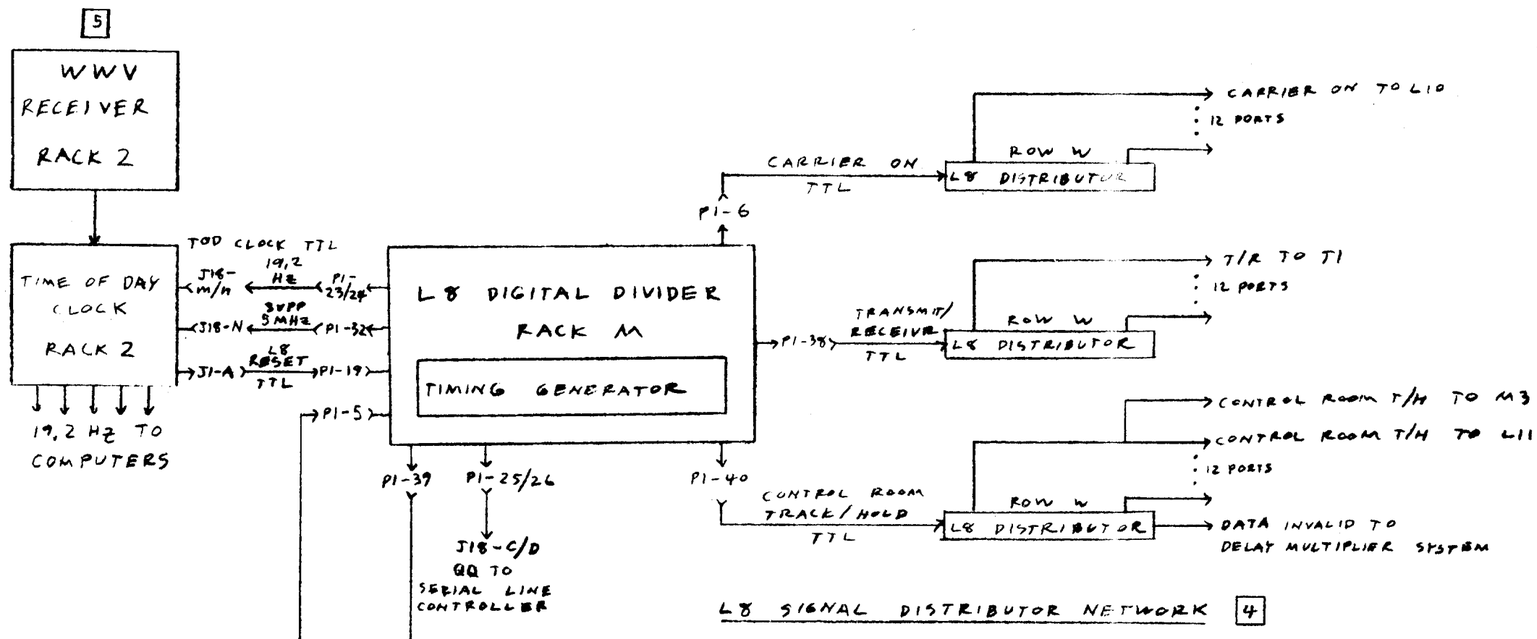
1. THIS DIAGRAM DESCRIBES ELECTRONICS FOR ANTENNAS 1-6 ONLY.
2. L4 LEVELS ONLY HOLD FOR "B" VERSION.
3. POWER SUPPLIES, MONITOR POINTS, SWITCHES AND CONTROL CIRCUITRY NOT SHOWN.
4. F4 IF FILTER BANDWIDTHS ONLY HOLD FOR ANTENNAS 3-6.
5. LEVELS INDICATED ARE APPROXIMATE AND REFLECT TOTAL POWER LEVELS UNLESS OTHERWISE INDICATED
6. T2 XMT IF LEVELS APPLY ONLY FOR ALL 4 IF PASSBANDS IN OPERATION.
7. ONE A AND ONE B RACK REQUIRED PER ANTENNA

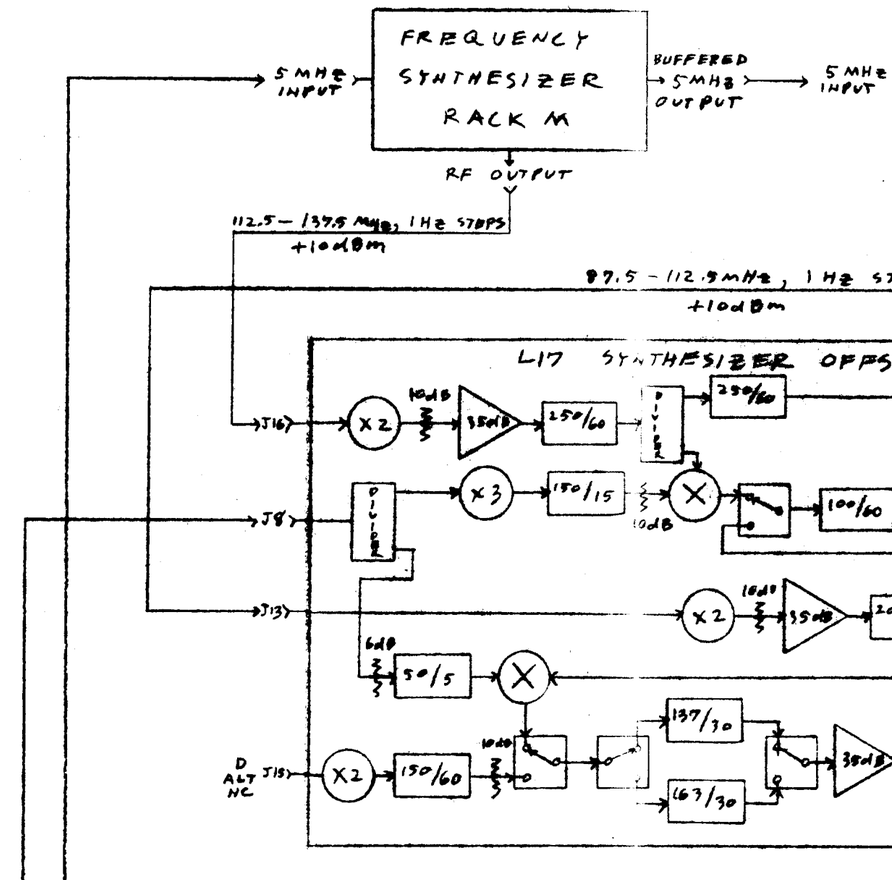
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	PROJECT	NATIONAL RADIO ASTRONOMY OBSERVATORY
TOLERANCES: ANGLES ±	VLA	SOCORRO, NEW MEXICO 87801
3 PLACE DECIMALS (.XXX): ±	TITLE: ANTENNA ELECTRONICS BLOCK DIAGRAM	DRAWN BY — DATE 3/4
2 PLACE DECIMALS (.XX): ±		DESIGNED BY — DATE
1 PLACE DECIMALS (.X): ±		APPROVED BY — DATE 3/9
MATERIAL:		SHEET NUMBER — DRAWING NUMBER D16000 B3 — REV. A — SCALE
FINISH:		
NEXT ASSY / USED ON		

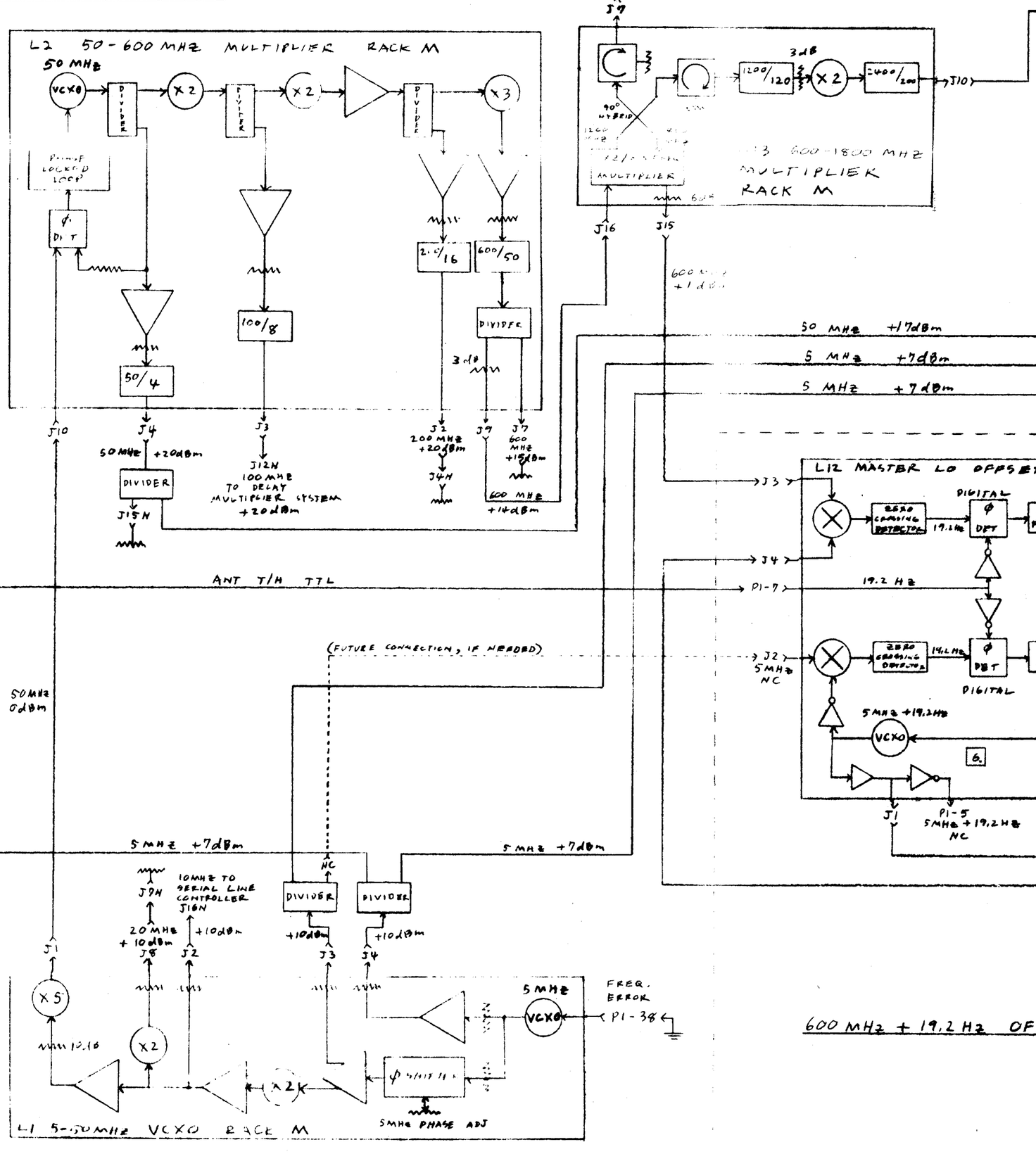
L8 TIMING DIAGRAM

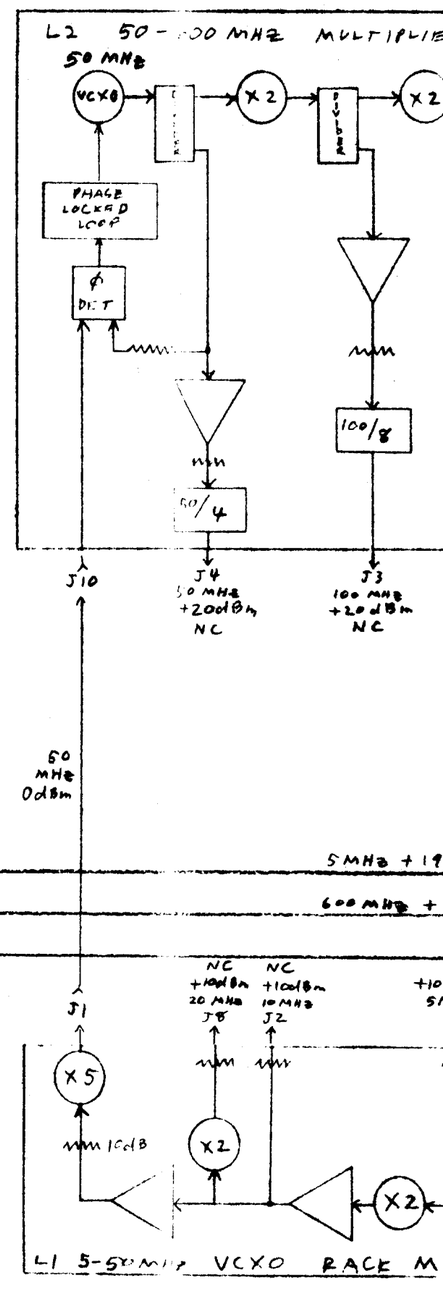


L8 SIGNAL DISTRIBUTOR NETWORK [4]





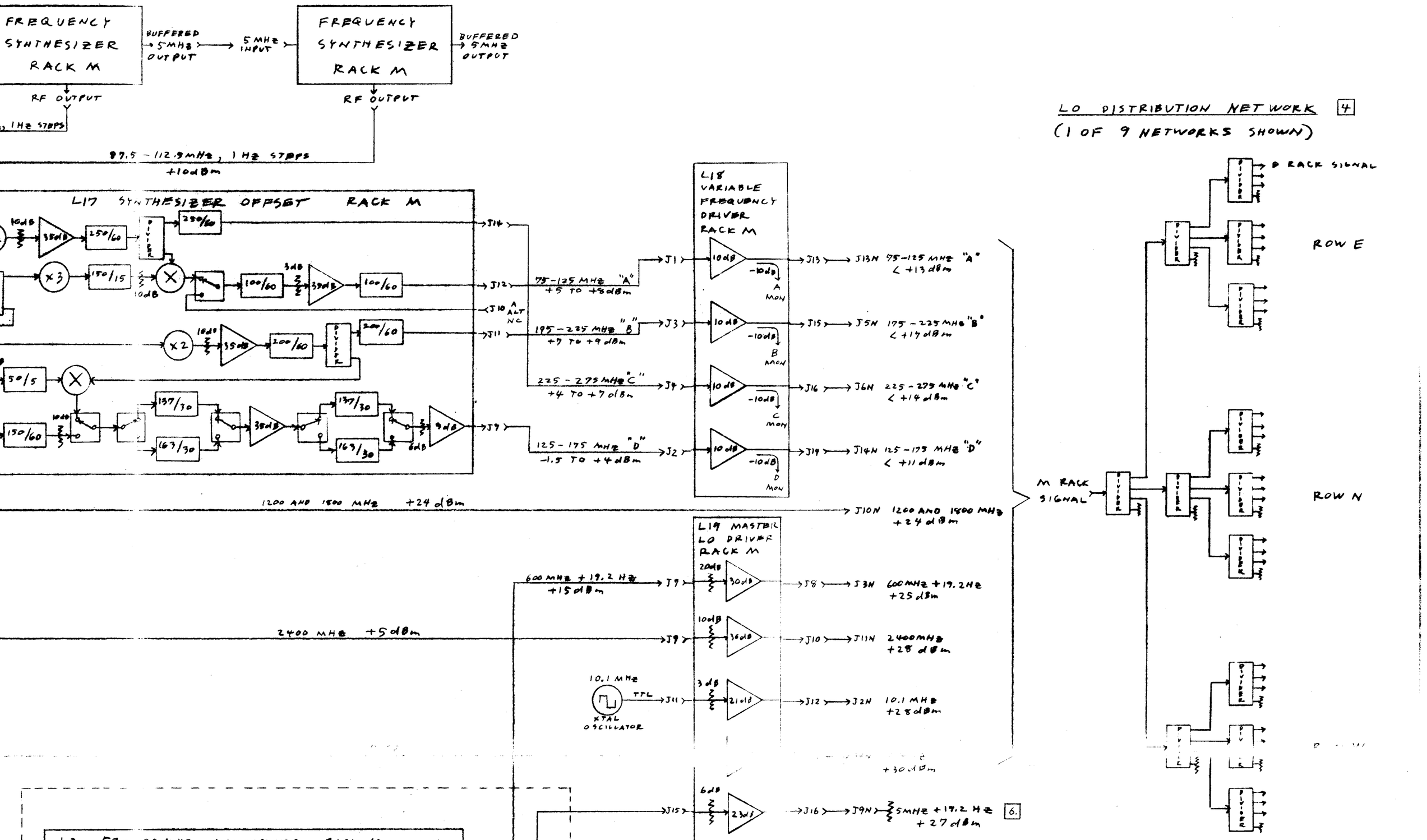




REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

LO DISTRIBUTION NETWORK [4]

(1 OF 9 NETWORKS SHOWN)



NOTES:

1. THIS DIAGRAM DESCRIBES PROTOTYPE ELECTRONICS FOR ANTENNAS 1-6 ONLY.
2. POWER SUPPLIES, MONITOR POINTS, SWITCHES AND CONTROL CIRCUITRY ARE NOT SHOWN
3. LEVELS INDICATED ARE APPROXIMATE AND REFLECT TOTAL POWER LEVELS UNLESS OTHERWISE INDICATED.
4. DISTRIBUTION NETWORKS ARE LOCATED IN THE CABLE TRAYS.
5. THE WWV RECEIVER AND MASTER CLOCK ARE LOCATED IN RACK 2 OF THE COMPUTER ROOM.
6. THE 5MHz OFFSET SYSTEM IS NOT USED AT THIS TIME.
7. ONE M RACK REQUIRED FOR SYSTEM.

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
2 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:

PROJECT: VLA

TITLE: MASTER LO CENTRAL ELECTRONICS ROOM BLOCK DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 3/9/77
DESIGNED BY	DATE
APPROVED BY	DATE 3/9/77

SHEET NUMBER | DRAWING NUMBER D16000B4 | REV. A | SCALE

T2 IF COMBINER RACK D

RCV MONITOR POINT

10dB

DIVIDER

27dB

1500/1000

XMT MONITOR PT

SW T/R

27dB

RCV GAIN

VOLTAGE CONTROLLED ATTENUATOR

10dB

J7

RCV IF

DCS INTERFACE FOR T1 AND T2

10dB

DIVIDER

-10dB

J10

J11

26dB

10dB

COMBINER

SW T/R

27dB

J13

XMT IF

-6.5dBm

J16

P1-M

SW T/R TTL

RCV IF -4dBm

T1 M[illegible] RACK

GUNN OSCILLATOR

J15

35dB

SW T/R

SW T/R

TRANSMIT AMPLIFIER 1-2GHz

RCV LO

-4dBm (-13dBm/CARRIER)

J9

J8

6dB

3dB

J1

1200 AND 1800 MHz

-14 dBm

6dB

J15

L9 CENTRAL LO RECEIVER RACK D

DIVIDER

1200/120

1800/180

27dB

27dB

-6dB

-6dB

LPF 1.5MHz

J6N

5MHz +10dBm

DIVIDER

Ø SHIFTER

J9

ZERO CROSSING DETECTOR

J1-7

J13

J14

P1-5 DATA OUT TO M3

L10 CENTRAL LO TRANSMITTER RACK D

1800/1060

COMBINER

DATA MODULATOR DRIVER

P1-5 DATA FROM M3

1200/120

1800/120

DIVIDER

5MHz MODULATOR DRIVER

600/50

600/50

J11 600MHz NC +7dBm

-6dB

31dB

P1-6

J8

J13

1200 CARRIER ON

TTL

J14-E

1200 AND 1800 MHz -3dBm

J13H

6MHz Ø

5MHz +5dBm

5 MHz +5dBm

1200 MHz 0dBm

1800 MHz 0dBm

J2

J3

L14 CENTRAL LO FILTER RACK D

Ø DET

Ø DET

PHASE LOCK CIRCUIT

PHASE LOCK CIRCUIT

VCO 1800MHz

1200MHz VCO

6dB

6dB

DIVIDER

DIVIDER

1800/180

1200/120

MON

MON

20dB

600/100

25dB

-10dB

MON

ZERO CROSSING DETECTOR

J1

J7

P1-7

J15

1800 MHz +11dBm

5 MHz +5dBm

1200 MHz +11dBm

RACK D

J1

J2

J4

RACK D

J1

J2

J4

MASTER SWITCHES

1. [illegible] Ø ERROR
2. [illegible] FREQ. ERROR
3. 19.2 Ø ERROR
4. 1800 FREQ. ERROR
5. [illegible] MHz RT Ø
6. [illegible] MHz RT Ø

TEST SWITCHES

1. ONE SHOT
2. OPEN 1200
3. OPEN 1800
4. OPEN 1200 AND 1800

L[illegible] CENTRAL LO CONTROL RACK D

5MHz Ø

P1-7

19.2 kHz

PHASE DETECTOR

PERIODS AVERAGED COUNTER

12 BIT COUNTER

12 BIT STORAGE REGISTER

RESET

LATCH

VCO

÷2^12

TIMING LOGIC

DCS INTERFACE FOR LO MODULES

PHASE LOCKED LOOP

J18-J

CR T/H TTL

P1-40

19.2 kHz REF

P1-39

19.2 kHz

PERIODS AVERAGED COUNTER

12 BIT COUNTER

12 BIT STORAGE REGISTER

600 MHz +19.2 Hz +7 dBm

Ø SHIFTER

600 MHz ZXD TTL

J1

J7

P1-7

J15

MASTER LO

19.2 kHz CLOCK INTERRUPT

10MHz

CMOS

CRT

MONTY

DMA

SERIAL LINE CONTROLLER

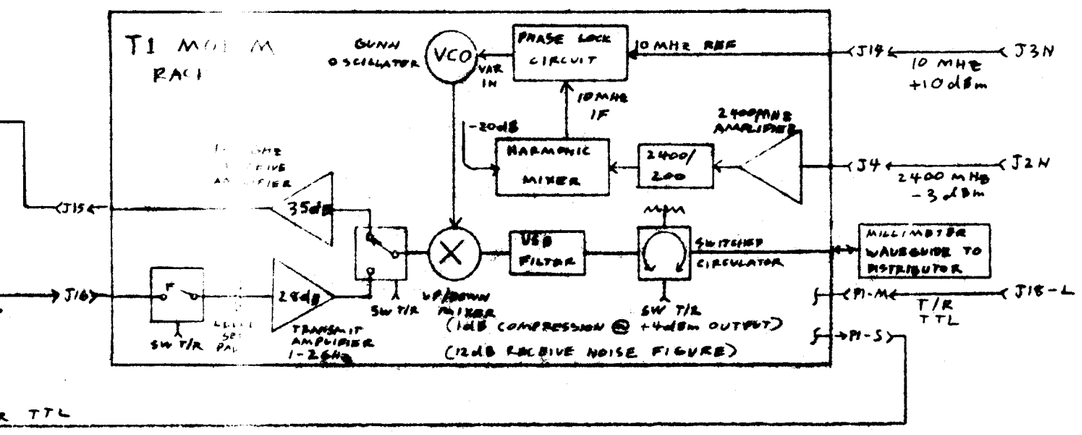
32 PORTS

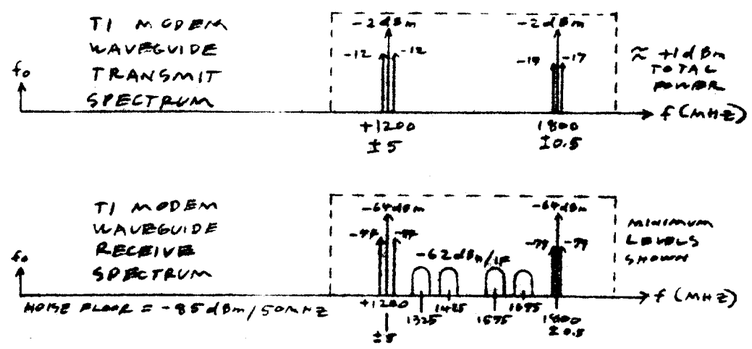
MON DATA

CONTROL ROOM

DIGITAL COMMUNICATIONS SYSTEM

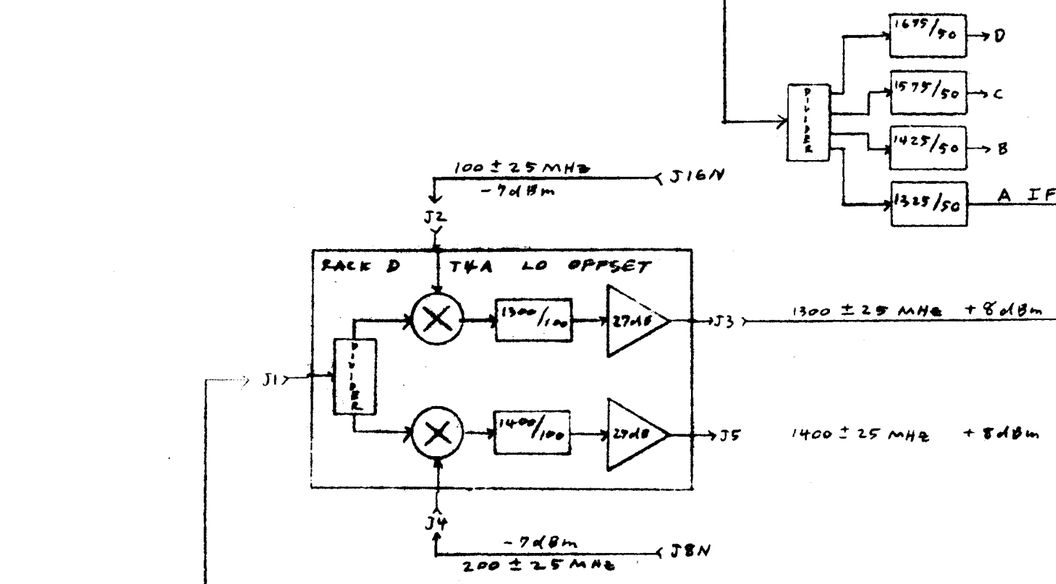
REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

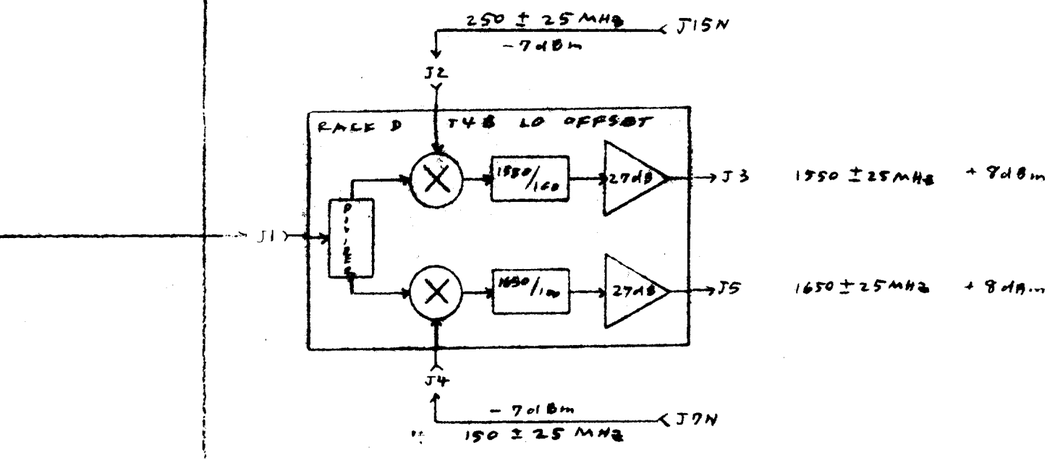


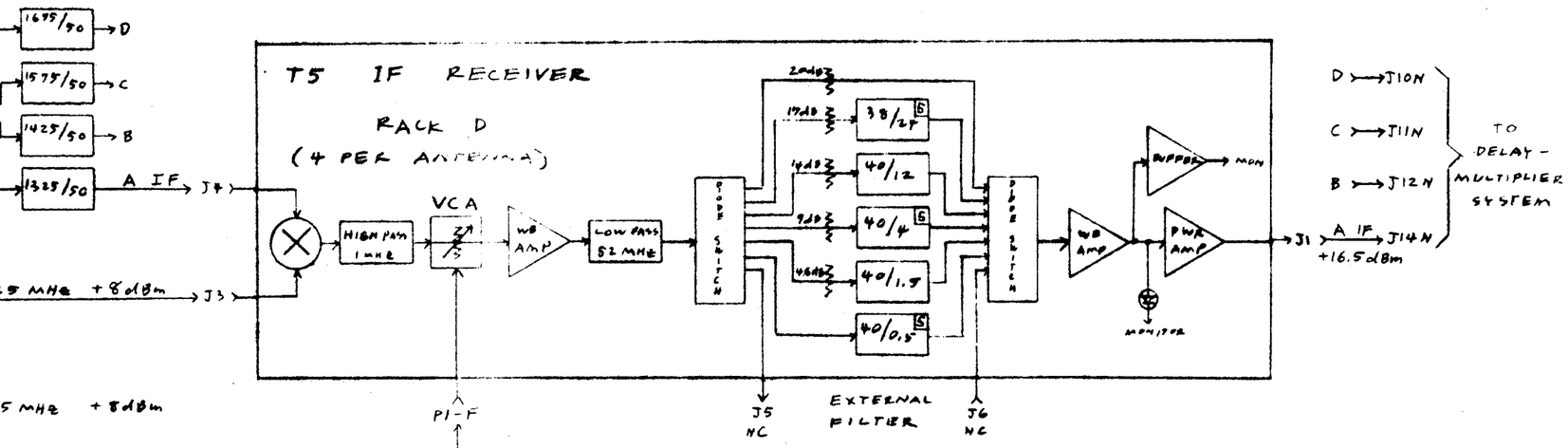


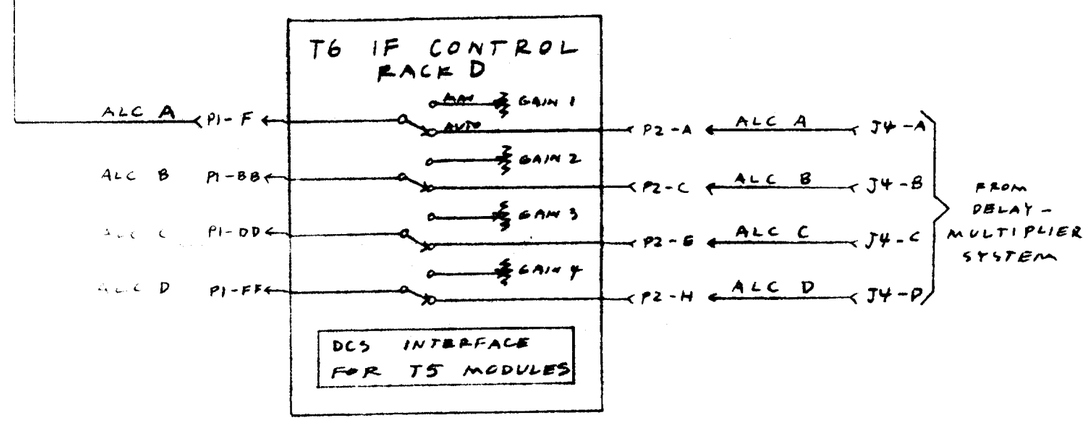
MODEM WAVEGUIDE CHANNEL ALLOCATIONS

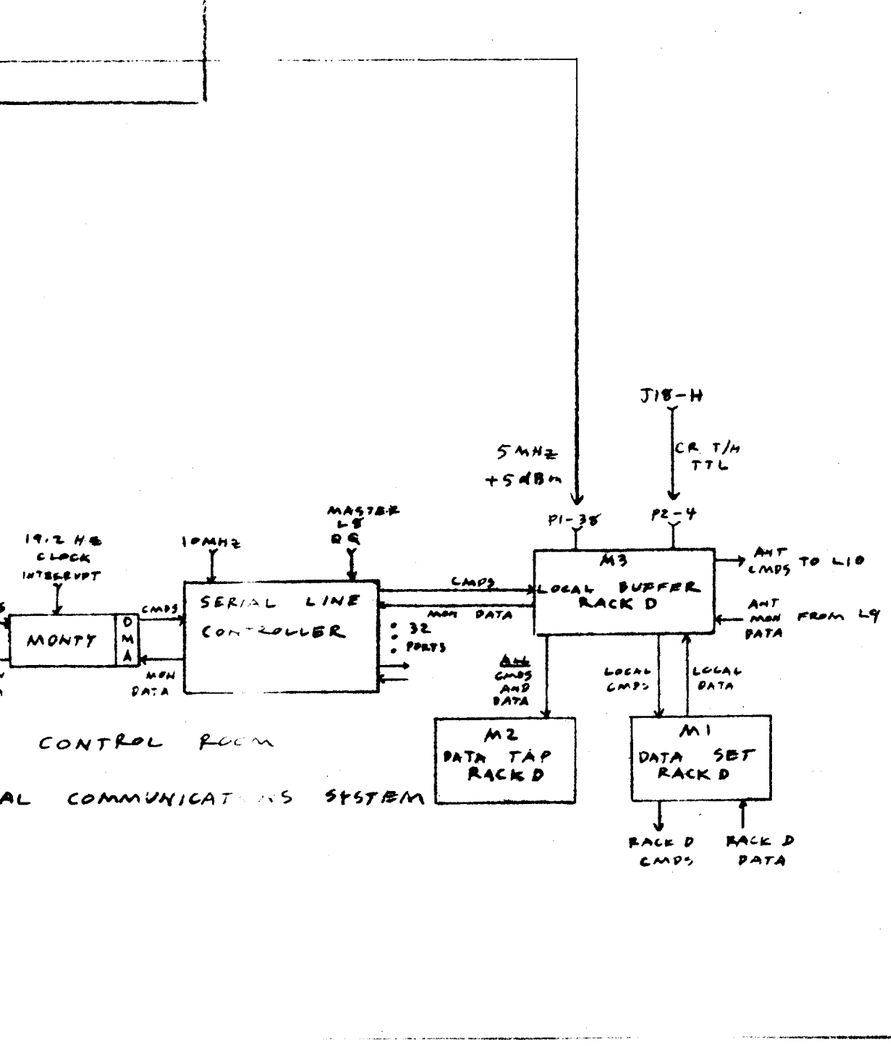
CHANNEL	LOCAL OSCILLATOR FREQUENCY f_o, GHz	SIGNAL BAND LOW	SIGNAL BAND HIGH
1	26.41	27.41	28.41
2	28.79	29.79	30.79
3	31.21	32.21	33.21
4	33.59	34.59	35.59
5	36.01	37.01	38.01
6	38.39	39.39	40.39
7	40.81	41.81	42.81
8	43.19	44.19	45.19
9	45.61	46.61	47.61
10	47.99	48.99	49.99
11	50.41	51.41	52.41

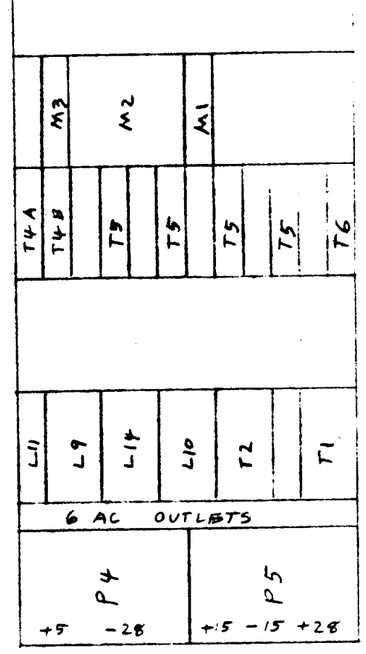












NOTES:

1. THIS DIAGRAM DEPICTS ELECTRONICS FOR RACKS D-1 THROUGH D-6
2. POWER SUPPLIES, MONITOR POINTS, SWITCHES AND CONTROL CIRCUITRY ARE NOT SHOWN.
3. LEVELS INDICATED ARE APPROXIMATE AND REFLECT TOTAL POWER LEVELS UNLESS OTHERWISE INDICATED.
4. ONE D RACK REQ'D PER ANTENNA
5. FOR T5-A1 THROUGH T5-A9, FILTERS ARE 25/25, 25/4, AND 25/0.5 RESPECTIVELY.

NEXT ASSY	USED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
TWO PLACE DECIMALS (.XXX): ±
ONE PLACE DECIMALS (.XX): ±
NO PLACE DECIMALS (.X): ±
MATERIAL
FINISH

PROJECT: VLA

TITLE: RACK D CENTRAL ELECTRONICS ROOM BLOCK DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 3/17/11
DESIGNED BY	DATE
APPROVED BY	DATE 3/17/11

SHEET NUMBER | DRAWING NUMBER D16000B5 | REV | SCALE