VLA Technical Report No. 30

THE HANDYMAN'S GUIDE TO THE DATA SET, MODULE TYPE M1

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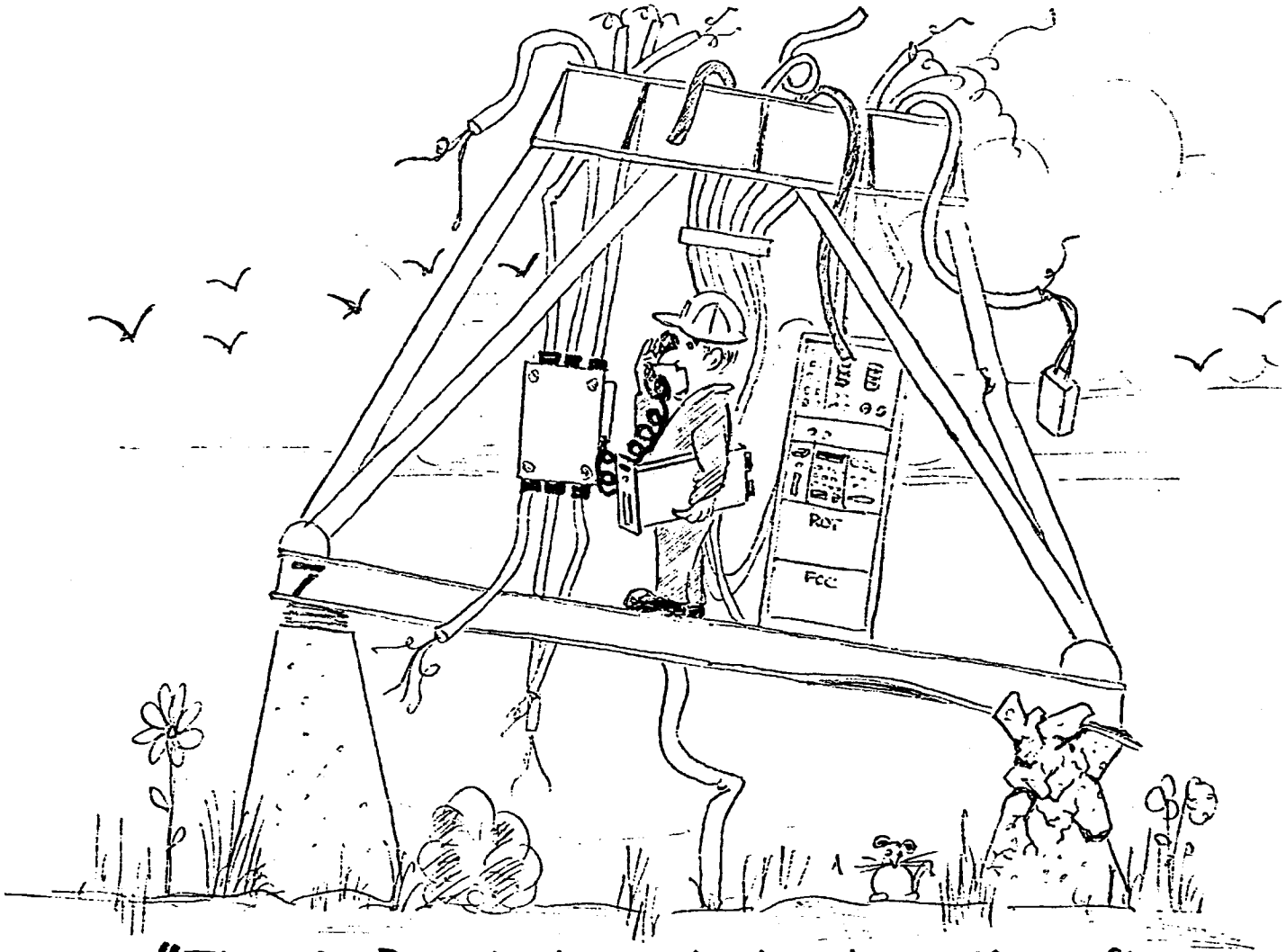
September 1977



"This is Dave Weber out at antenna 7... after a careful investigation, I just don't really think a new DATA SET will fix this problem!"

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1.0 INTRODUCTION

This manual describes the DCS Data Set (module type M1) functions, operation and specifications and is primarily intended to serve as the principle maintenance, repair and alignment guide. In addition, interfacing information and guidelines are included which may be useful for those who design command or data channels which interact with the Data Set.

The functional descriptions contained in this manual are treated in two levels of detail:

1) A brief functional description which provides a general understanding of Data Set functions and operation and is intended to serve as conceptual base for the detailed description which follows. This description also may be useful to the reader who is interested in a general knowledge of the Data Set properties but who has no interest in the circuitry details.
2) A detailed functional description keyed to a block diagram and augmented by logic timing diagrams which graphically illustrate important circuit timing relationships. This detailed description is oriented toward the reader who has a well-developed knowledge of digital machinery and is familiar with the TTL logic families. The reader is referred to commercial logic data books for detailed characteristics of the logic elements used in the Data Set.

The Data Set is the prime focus of interest in this manual but functions of the Antenna and Central Buffers are developed where it is necessary to explain aspects of the Data Set operation. For an understanding of these Buffer units, the reader is referred to the appropriate module or DCS System Manual.

The DCS System Manual describes the usage of the Data Set in the VLA system. The reader is urged to consult this manual for details on the command and data flow timing.

2.0 GENERAL FUNCTIONAL DESCRIPTION

The Data Set physical package is fabricated from a one-unit wide, standard VLA module and contains wire-wrapped logic connector boards for the digital logic chips and a removable (for alignment and test) analog multiplexer and A/D converter PC board assembly.

A front panel numeric LED indicates the Data Set address (discussed later) and flashing green and red LEDs respectively indicate monitor data output activity and malfunctioning signal conditions. Front panel test points permit direct oscilloscope observation of the Data Set operation in place. For a general understanding of the Data Set physique see the Data Set Top Assembly Drawing in the pocket in the back cover of this manual.

The Data Set is a synchronous digital machine which detects, error tests and distributes time-serial digital command messages to commanded devices. The Data Set also gathers, converts, formats and emits time-serial digital monitor data messages. Both time and space division multiplexing is utilized by the Data Set in interacting with commanded devices and data sources.

The command messages originate in the central control computers and are routed to the Data Set via the Serial Line Controller, Central Buffer, L.O. System, WCC and Antenna Buffer, (see the DCS and VLA system manual for details). The monitor data messages are routed to the Buffers for storage and transmission to the control computers via the units cited above.

The Data Set is a passive machine in that it performs a command or data operation only when stimulated by a Buffer. The Buffer emits a time-ordered serial stream of command, monitor data and data request messages and depending upon the character of the messages the Data Set performs the command and monitor data operations.

The reader should refer to Figure 1 which depicts the formats of the command, monitor data and data request messages. Figure 2 illustrates the relationships of the Data Set inputs and outputs to the other VLA units. Table I relates the multiplex address ranges and Data Set command/data functions.

In performing a command operation the Data Set detects, loads and tests the command message for parity errors. If the command message

contents satisfy the error detection logic, the data set address components of the message are compared with the data set address to determine if the command is directed to the Data Set in question. If so, then the command information and multiplex address are stored for execution of the command. In executing the command the multiplex address is decoded to activate output information, clock and strobe lines causing the command to be serially loaded and stored in the multiplex address-designated device. The antenna address component of the command is not tested by the Data Set other than for parity purposes. The Buffers store only the commands which pertain to their associated antenna so that the Data Sets need not test for antenna address relevance.

The Data Set is caused to perform a monitor data operation when it detects a Data Request Message emitted by a Buffer. The Data Set then gathers both digital and analog data which is formatted into a monitor data message along with multiplex address data set address, antenna address and message parity data components. In the case of monitor data messages which contain analog data there are <u>two</u> analog data values and only one multiplex address. The multiplex address for the second analog value is implied and is the message multiplex address +1. The monitor data message is then serially output to the Buffer. The Data Set monitor data control logic has a 200 microsecond delay for analog data settling and A/D conversion delay.

The Data Set monitor data sampling operations are time and multiplex address ordered in the VLA cycle. The Buffer evokes two monitor data messages from each Data Set in one VLA cycle. The multiplex addresses for the first monitor data message are derived from an address program stored in a programmable read-only-memory (PROM) which may be programmed to produce any arbitrary sequence of multiplex addresses within a 192 message sequence. The multiplex addresses for the second monitor message are derived in either of

two ways:

1) Sequential mode in which 128 analog channels are sequentially sampled twice and 64 digital channels are sequentially sampled once over a ten second period.
2) Selected mode in which the multiplex address is set to a fixed channel specified by the Control Computers.

Commands directed to the Data Set designate the selected address and control Select/Sequential mode states. In addition the PROM address may be initialized to a base value so that all Data Sets with identical PROMs sample the same data in any given cycle.

The monitor data messages emitted by the Data Set are rebroadcast by the Antenna Buffer as they are stored in the Buffer data memory. This rebroadcasting enables a data tap (see data tap manual for details) to be connected to any Data Set in the antenna for visual display of command or monitor data messages. The Data Set is inhibited from responding to its own monitor data messages to prevent positive feedback perturbations to the logic.

When the Data Set detects a distorted command or monitor data message, parity error detection logic inhibits the execution of the message (if it is a command) and the multiplex and Data Set address of the distorted message are stored for future monitor data readout as binary monitor data is read out by multiplex address 200_8. An additional feature of the error data readout is a flag bit which is set if the error is detected in the multiplex address component of the message. A binary counter is included in the error data logic and is used to count the parity errors that occurred in the intervals between address 200_8 data readout meassages. The counter is reset to zero as part of the readout process. Because the Data Set is unable to respond to its own monitor data messages, it cannot test or report its own malfunctioning output.

Analog data is multiplexed in the Data Set by an eight channel differential input multiplexer-buffer amplifier. Each of these inputs

is driven by an eight or sixteen channel single-ended or differential multiplexer located in the modules serviced by the Data Set. The lower four bits of the multiplex address drive the remote multiplexer and the next three bits drive the eight input Data Set multiplexer. The multiplex address is incremented after the first analog to digital conversion so that the second analog data channel can be selected and converted.

The output of the Data Set multiplexer-amplifier drives a sample and hold unit which "holds" the analog data level constant for the analog to digital converter. The Data Set conversion control logic provides a 30 microsecond settling delay for the analog data before the data is held by the sample and hold unit. Ten microseconds after the data is held, the A/D converter is triggered to start conversion. The end-of-conversion pulse from the A/D converter causes the data to be loaded into a storage register for subsequent readout when the monitor data message is output.

The dominant properties of the analog multiplexer - A/D converter are:

Analog signal range - +10.235 to -10.240
Multiplexer "on" input impedance - 100 megohms
Analog Settling Delay - 30 microseconds
Multiplexer "on" resistance - 2KΩ/line
A/D Conversion Period - 50 microseconds
Common Mode Rejection - >60 dB with a 1KΩ source unbalance
Conversion Code - 12 bit offset binary code, 5mv/bit
Settling Time - <4μsec to .01% of full scale
Cross Talk - <1mv, P-P @ 10KHz
Input Over Voltage Tolerance - 35 V, max

Each device serviced by a Data Set contains a small logic controller driven by the Data Set which decodes addresses and accepts and stores command information. Under address control from the Data Set, the controller loads binary data and serially

emits it to the Data Set. Analog data is routed to the Data Set A/D converter by either single-ended or differential analog multiplexers in the controller. Many different implementations of controllers are possible to service any combination of command or binary and analog monitor channels. The most general implementation utilizes all three and consists of about 13 chips which can decode and store a 24 bit command, load and output 24 bits of binary data and multiplex 8 channels of differential analog data. Figure 3 shows the logic diagram of a typical controller. The use of these controllers located in the various VLA functional modules permits the rack wiring to be minimized and enables the Data Set to service a great many command and data channels. The full command/data capacity of a Data Set is:

1) 128 analog channels, converted to 12 bit binary values, ±10 volt analog signal range.
2) 64 channels of 24 bit binary data (1536 binary bits).
3) 48 channels of 24 binary command (1172 binary bits).

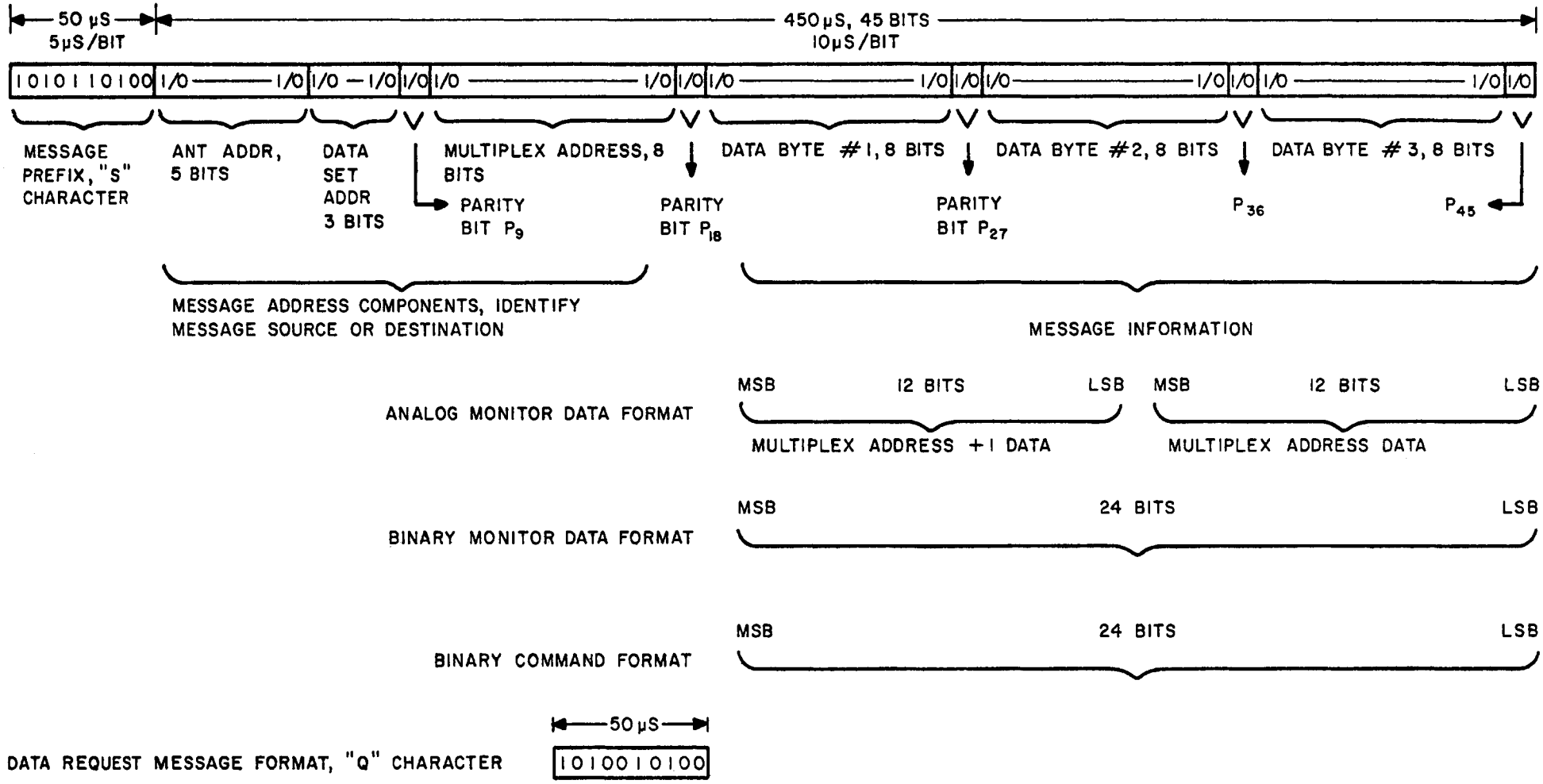


FIGURE 1: DATA SET COMMAND AND MONITOR DATA AND DATA REQUEST MESSAGE FORMATS

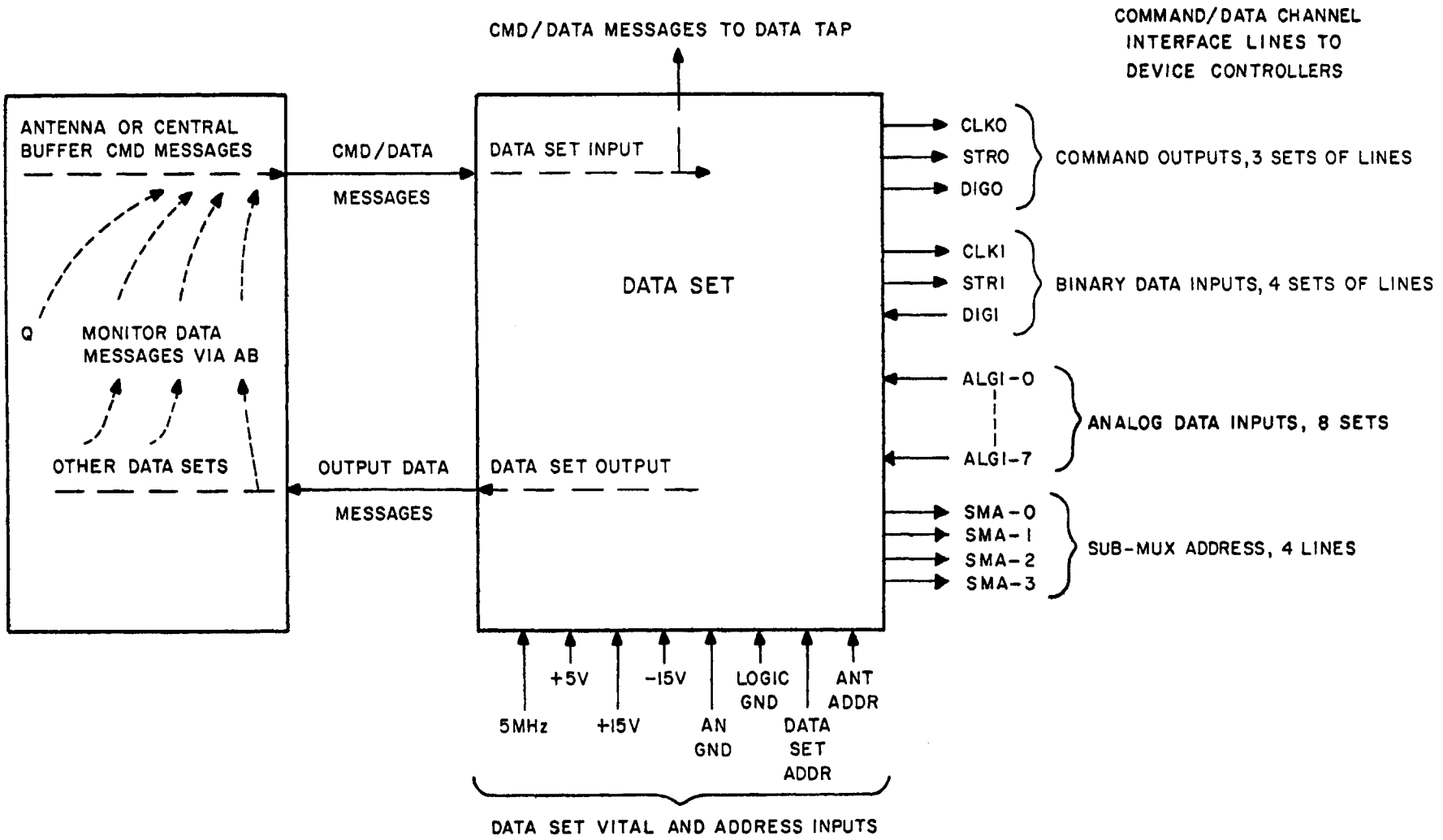


FIGURE 2: DATA SET INPUTS, OUTPUTS, AND VITAL SIGNALS

MULTIPLEX ADDRESS	FUNCTION
0 to 17_8	Analog Data Input, ALGI-0
20 - 37_8	Analog Data Input, ALGI-1
40 - 57_8	Analog Data Input, ALGI-2
60 - 77_8	Analog Data Input, ALGI-3
100 - 177_8	Analog Data Input, ALGI-4
120 - 137_8	Analog Data Input, ALGI-5
140 - 157	Analog Data Input, ALGI-6
160 - 177_8	Analog Data Input, ALGI-7
200_8	Parity Data Readout
201 - 217_8	Binary Monitor Data, DIGI-0
220 - 237_8	Binary Monitor Data, DIGI-1
240 - 257_8	Binary Monitor Data, DIGI-2
260 - 277_8	Binary Monitor Data, DIGI-3
300_8	Set Data Set to Select Mode
301_8	Set Data Set to Sequential Mode
302_8	Reset PROM Address Counter
320 - 337_8	Binary Command, DIGO-0
340 - 357_8	Binary Command, DIGO-1
360 - 377_8	Binary Command, DIGO-2

TABLE I: DATA SET MULTIPLEX ADDRESSES AND ASSOCIATED FUNCTIONS

3.0 DETAILED FUNCTIONAL DESCRIPTION

This section contains a detailed description of the theory of operation of the Data Set and is broken into sections which have a distinct natural structure, closely keyed to the Data Set Block Diagram, (Figure 4). The Data Set logic is straightforward and easily grasped by those with digital backgrounds, therefore the logic descriptions in the sections are brief and emphasize the most important aspects of the logic rather than exhaustive gate-by-gate discussions of the functions of each and every logic element. The logic sections are discussed in the order of increasing functional dependency.

The reader should study the timing diagrams referenced by the description as they graphically illustrate logic operations and are a literal replica of the timing waveforms which may be observed with an oscilloscope. The timing diagrams are keyed to signal source points by the location designator and pin number. Important causative relationships are indicated by arrows from one waveform to others. Clocking relationships are implied by an up or down arrow which indicates the portion of the waveform which causes driven devices to be triggered. Where it is important to the discussion, logic states, time durations, delays or frequencies are marked on the diagrams. A linear time base is employed in all diagrams but delays may be exaggerated for emphasis of race or delay considerations. Waveform sampling is indicated by arrows, tick marks and the letter S to denote sampling.

Finally, logic elements are designated by the location designation and pin number of the driving source. This treatment is one of the conventions of the wire-listing programs which enables close correlation of the wiring documentation with the logic diagrams.

The discussions refer to the "Rev. C" and "D" versions of the Data Set. Earlier revision levels will be upgraded to the "D" level. Revision "C" and "D" are logically identical except for wiring details.

The Revision "D" Data Set logic diagrams are in the pocket in the back cover of this manual.

3.1 5 MHz Clock Detection and Doubling Logic

An externally provided, 5 MHz 1.5 volt peak (nominal) sine wave signal is the clock source for the Data Set. A 72710 differential analog comparator A30B "squares" up the 5 MHz signal to drive the A14 harmonic generator which doubles the 5 MHz clock. The A14 tank circuit rings at 10 MHz and is "kicked" by the positive-going edge of the drive from inverter A1002. A10 is a 74S04 because of its high switching speed which produces sharp edged drive pulses for the harmonic generator. The drive edges are differentiated by the 10 pf/1 KΩ circuit in the MPS 918 base circuit and the positive-going edge provides a narrow current impulse to the transistor base. Inverter A1004 is caused to operate in a quasi-linear region by the 2K resistor in A14. The output of A1006 is the highest frequency clock source in the Data Set and all clock rates are derived from it.

3.2 Input Signal Synchronization Logic

The optically-coupled isolator A30A detects the Data Set input signals and provides ground isolation between the Data Set and Buffers. The data is clocked into shift register A25 by the 10 MHz clock. 1/0 or 0/1 data edges are detected by exclusive or gate A2403 which presets counters A12 and A13 to a count state of 41. This counter is incremented by the 10 MHz clock to a count of 90 which then causes the counter to be reset to the 41 state via the 7402 D3004. Timing Diagram 1 depicts the timing relationships. Output A1313 is a 200 kHz waveform whose positive-going edge is delayed 2 microseconds from the 1/0 or 0/1 input signal edges. This 200 kHz signal is the clock for counters A16 and A11 and also the sample clock for shift register A18. The purpose of the delay is to sample the input signal at the approximate center of the "S" character bits. A 1 MHz clock is tapped off counter A1211. The use of this clock is discussed later.

3.3 Message Detection/Loading Logic

Shift register A18 is serially loaded with the input data stream by the phase adjusted 200 kHz clock from A1313 described above. Two gates A2610 and A2710 serve as matched filters to detect the presence of a data request message (Q) or start of a command or monitor data message (S) in shift register A18. When the last eight bits of the Q message are loaded into A18, gate A2610 goes true for 5 µsec. This Q detection initiates the monitor data gathering sequence described later. Similarly gate A2710 goes true for 5 µsec when the last eight bits of the start (S character) portion of a command or monitor data message are loaded into A18. This S detection activates the message loading sequencing counter consisting of flip-flops B2106 and synchronous counters A16 and A11. This counter generates 45 shift clocks to serially load the message into the loading registers B30, B25, B20, B15 and B10. See Timing Diagram 2 for waveform details. Counter A16 operates with a radix of 9 to program a parity test of the message data on a byte by byte basis. The parallel contents of register B30 are presented to B26, a parallel parity checker/generator, and at the count of 9 the output of B26 will enable the J input of flip-flop B2110. If there is a parity error, B2110 will be clocked true. At the completion of the loading sequence, the counter is shut off by the fall of A1111 which also triggers one-shot C1810. The strobe output of C1810 causes parity error data to be stored in the error data register (discussed later) if an error occurred in the message. If the message passes the parity test, the C1810 strobe is enabled onto comparator B8 which compares the hardwired data set address with the data set address standing in register B10. If the addresses agree, B8 A=B output passes the B2110 strobe to gate B2914 which further tests the message to determine if it

is a command by anding mux address bits 128 and 64 (both true only for commands). If the message is a command addressed to the Data Set in discussion then the 24 information bits of the message are parallel loaded into registers B24, B19 and B14. The Cmd Busy flip-flop B1111 is also set by B2914. The command multiplex address is caused to be stored in the multiplex register A15 and A2 via multiplexers D21, D22, D26 and D27. The multiplexers are pointed to the portions of the message loading registers which contain the command multiplex address by gates D506/10 and D2406/10 and the Cmd Busy flip-flop B1111. The mux address is strobed into registers A15 and A2 by the leading edge of one shot C3009. C3009 is triggered by the trailing edge of one shot C1810 and provides 100 ns of delay to enable the mux address to propagate through the multiplexers and stabilize at the A15 and A2 inputs before being clocked by C3009. If a parity error should occur, one shot C1807 is triggered on to provide a stretched illumination of the front panel red parity error LED.

Note that the parity test logic operates on <u>both</u> command and monitor data messages and causes error data to be stored for both classes of messages. Thus a parity error in a monitor data message is heard by all Data Sets in the antenna and is multiply reported. Also note that the antenna address is not tested or used in the loading process other than in the parity error tests.

3.4 Command Output Logic

In the previous section we saw how the command messages were loaded, error tested and parallel stored. The storage process is completed by about 200 ns after the last load shift clock. The 24 command information bits are immediately unloaded to the command destination which leaves the message loading circuitry free to accept the next message which may immediately follow. The unload

operation is initiated by gate B2914 (mentioned above) which sets control flip-flops B1105 and C1511. B1105 enables counters B17 and B22 to count out 24 100 kHz shift clocks and one clock pulse time later a strobe pulse. The 24 command data bits, checks and strobe are enabled to one of three pairs of digital outputs by address decoder B12 which is driven by the four high order bits of the multiplex address. The four lower order bits of the multiplex address are decoded by the commanded devices and enable the information output on the three sets of outputs to be loaded and stored. Note that both time and space division multiplexing are used in this command distribution logic. For more details on the utilization of these signals see Section 6 of this manual which contains a typical command channel logic diagram.

The trailing edge of the strobe pulse resets the command busy flip-flop B1111. B1111 forces the multiplex address registers A2 and A15 to be cleared via the DS busy gate B0613. Thus the multiplex address storage registers are cleared to address 0 between command operations.

Timing Diagram 3 shows the time relationships of the command output logic.

3.5 Word 1/Word 2 and Mux Load Sequence Logic

When a data request message (Q) is detected (see Section 3.3), it toggles D2305 which controls the word 1/ word 2 steering of the multiplex address multiplexers D21, D22, D26 and D27. D2305 also increments the PROM address counters D17 and D18. The reader will remember that word 1 (i.e., the first monitor data message evoked by the Buffer in a VLA machine cycle) contains data selected by the program residing in the PROM. Word 2 data is associated with either a computer-specified (i.e., selected address) or a sequentially

scanned address. The word 1/word 2 ordering is accomplished by the two one shots D0405 and D0409, which are triggered by the Q pulses from A2610. The Q pulses occur in pairs (1 pair/ VLA machine cycle) and are separated by either 800 microseconds or 4.5 milliseconds depending upon which Buffer drives the Data Set. One shot D0406 is retriggerable with a period of 5 Ms which is greater than the Q pulses separation. This delay causes flip-flop D2305 to be left in the proper state to steer the PROM addresses to the address register when the Buffer requests the first monitor word in the VLA cycle. Shift register D9 is a clock phase generator which generates a time delayed clock to allow the multiplex address enough time to propagate through the address multiplexer to the address register. Other functions of the clock phase generator are initialization of the 200 kHz divider A0705, triggering of the output data sequencing logic, loading of the multiplex address, data set address and antenna addresses in C22 and C27, and the "S" character bits in registers C24 and C26. Timing Diagram 4 shows the clock terms generated by the clock phase generator D9.

The PROM is physically located on the analog multiplexer - A/D board for packaging convenience because of its 24 pin physique.

3.6 Monitor Data Multiplex Address Formulation

Counters D17 and D18 are incremented by the leading edge of the Q detector and have a radix of 192, thus the PROM address recycle rate is 192 VLA machine cycles in 10 seconds. Since counters D17 and D18 are incremented by the leading edge of the Q detector, the address program contents of the PROM have about five microseconds to settle through the multiplexer before they are loaded into the multiplex address registers A2 and A15 by the logic described in the section above. This same settling time also applies to the select address and sequential address data.

The select address data is stored in shift register C21 which is loaded by a command addressed to multiplex address 300_8.

When this command is detected, the lower eight bits of the command are shifted into C21 and the select/sequential flip-flop is set to the select state. This flip-flop then causes the multiplex address multiplexer to route the selected address stored in C21 to the address registers A2 and A15.

The sequential address is formed algorithmically by 2 to 1 multiplexers D19 and D20 and full adder D13 under the control of gates D2903, D2906, D1203, C1213, C0510, C0514 and C0506. The sequential addresses scan all 128 analog addresses twice in ten seconds and the 64 digital addresses once in ten seconds. The digital address scan is broken into two scans of 32 channels each between analog data scans. The base for the sequential address counter is the PROM address counter which sequences from 0 to 191 and is incremented once per cycle.

The sequential address algorithm is very simple and involves using the PROM address counter directly, doubling the counter value and/or adding 64 to the count. Briefly the algorithm is as follows:

PROM Address Counter Range	Sequential Address Counter Range	Algorithm Rule
$0 \leq Np \leq 63$	$0 \leq Ns \leq 126$	$Ns = 2\ Np$
$64 \leq Np \leq 95$	$128 \leq Ns \leq 159$	$Ns = Np + 64$
$96 \leq Np \leq 159$	$0 \leq Ns \leq 126$	$Ns = 2\ Np$
$160 \leq Np \leq 191$	$160 \leq Ns \leq 191$	$Ns = Np$

The control gates enable or inhibit the add 64 and left or no shift logic operations in the adder and multiplexers on the basis of the PROM address register states. The contents of the multiplex address register are used extensively in the Data Set to control the distribution of monitor data and command output clocks, strobes and data. The lower four bits of the

address register are buffered out of the Data Set as low true lines by power Buffer A8. After the completion of a command or monitor data operation, the D5 busy logic A17 and B6 force the multiplex address register to a zero state. This then makes the sub-mux address assume the zero state so that all external devices will sense this state. The external analog multiplexers will all select this channel and will route it to the Data Set. This forced channel selection is not a problem condition as the Data Set is not perturbed by the presence of this signal.

3.7 Analog Data Gathering Sequence

Counter C17 and C1605 are enabled by control flip-flop C1611 which is set by the clock phase generator discussed in Section 3.5. The multiplex address had been loaded 1 microsecond earlier in multiplex address registers A2 and A15. The counter is incremented by 100 kHz clocks from A705 to generate sequential control terms for the sample and hold unit and A/D converter. At 30 microseconds, the sample and hold is set to the hold mode; at 40 microseconds, the A/D start conversion input is triggered by one shot D1006. After a 50 microsecond conversion, the A/D end of conversion line drops and triggers one shot D1010 which resets flip-flop A0710 to reset the sample and hold unit to the sample state. Gate C1913 steers the 500 ns one shot to load the A/D data into shift registers C1 and C2. At 100 microseconds, counter C17 increments the multiplex address registers (if the mux address is in the analog data address range) which then causes the next sequential analog channel to be selected by the external analog multiplexer. With the new analog data the sample and hold unit, start conversion, end of conversion and data storage operations occur at 130, 140 and 190 microseconds respectively. At 200 microseconds, flip-flop C1610 is reset and the output data shift operation is initiated by setting flip-flop C1505.

Gate C1913 generates a binary data strobe which is used to cause binary data sources to load the registers for an impending unload shift.

3.8 Output Data Sequencing Logic

The data output operation essentially consists of serially shifting out the address and A/D data stored in the registers described above. Counters C14 and D16 are incremented by 100 kHz clock pulses from A705 and generate sequencing and control terms which program the output of the monitor data message. Counter C14 operates with a radix of nine to cause parity data to be output at the appropriate points in the output message. Shift register B27 is a Johnson counter with a radix of 10 and is incremented by 1 MHz clock pulses from A1211. The counter is initialized to an all zero state by flip-flop C1505. When C1505 goes high at the start of the output sequencing operation, a wave of five "1"s followed by a wave of five "0"s circulate around the register. The gates driven by B27 generate time-phased clocking terms to clock all the monitor data registers. Timing Diagram 5 shows these waveforms and the basic logic. The logic driven by these terms are: parity counter C8, output register C29 and C26, data set/ ant/multiplex address registers C22 and C27, data registers C1, C2, C6 and C11, parity error registers B5 and C9 and the binary data registers in external binary data channels. These sample clocks are time-phased to avoid race conditions in clocking the long string of concatenated shift registers and also to enable the Data Set to be very tolerant of logic delays in external binary data channels. Timing Diagrams 6 and 7 show the generation and usage of these clock terms. Under multiplex address control multiplexer C7 selects either the A/D converted data or binary data from a binary data channel in some module serviced by the Data Set. And-or-invert gate D0210 selects either the C7 data mentioned above or the parity error data from parity data registers C9 and B5. Every ninth count state of

counter C14, the parity readout control logic (consisting of gates B1310, inverters C2514 and C2502 and flip-flop A1705) causes and-or-invert gate D0206 to steer the parity data from flip-flop C8 into the output data stream.

Gate B0110 causes the clock inhibit flip-flop D1412 to be set at a count of 24 so that the three data registers (i.e., converted analog data, parity error data and external binary data register) see only 24 unload clock pulses which is enough to unload them completely. An additional 16 clock pulses are required to bring these data to the output register C24. This 24 clock pulse count is chosen to permit command channels to operate in a 24 bit circular shift mode so that the contents of command channels may be read out non-destructively as binary data. Module L7 uses this feature. Counter D16 is preset to a count of 3 which provides sufficient time for all data to propagate completely through registers C24 and C26 with an additional 45 microseconds of shift time after the last data has shifted through C24 and C26.

The DS busy flip-flop A1710 is reset at the completion of the output data shift operation.

An output of flip-flop C1506 is used to inhibit the ability of the Data Set to "hear" its own output when used with an antenna Buffer. The inhibit disables the phase adjust term from exclusive or gate A2403 and clears shift register A18 so that the 200 kHz clocks are not phase perturbed by the Data Set's own output (a positive feedback) and it does not detect the S in its output message.

Parity counter C8 is initialized to the "1" state by the multiplex address clock phase generator and is reinitialized after the parity data for each byte is read out.

Buffers A0411 and A0409 drive the data to the Buffer and the data out LED respectively.

3.9 Parity Error Data Readout Logic

In the event that a distorted command or monitor data message is detected by the Data Set, gate B1606 causes the message multiplex and Data Set address components and the error count to be stored in registers B5 and C9. In addition if the error occurred in byte 2 of the message, gate B0106 sets flip-flop D2311 which is also stored with the data above. In the event that the parity rate is high, counter B4 counts the number of errors (up to 16) between the error data readouts on multiplex address 200_8. Gate D0610 goes true when multiplex address 200_8 occurs and enables the parity data in registers C9 and B5 to be routed to the output logic via and-or-invert gate D0210. The data is clocked and sampled in the same manner as analog or digital data.

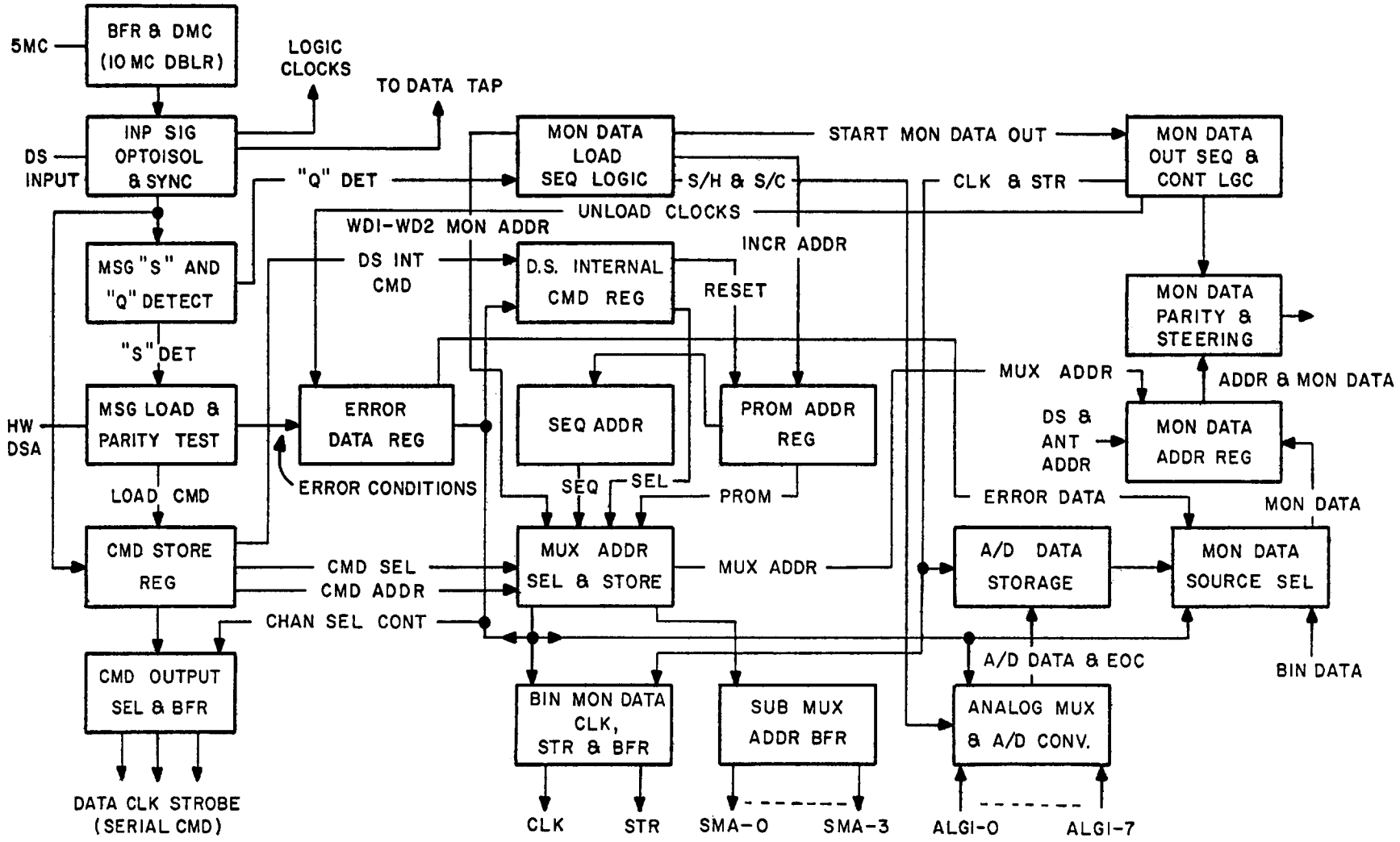
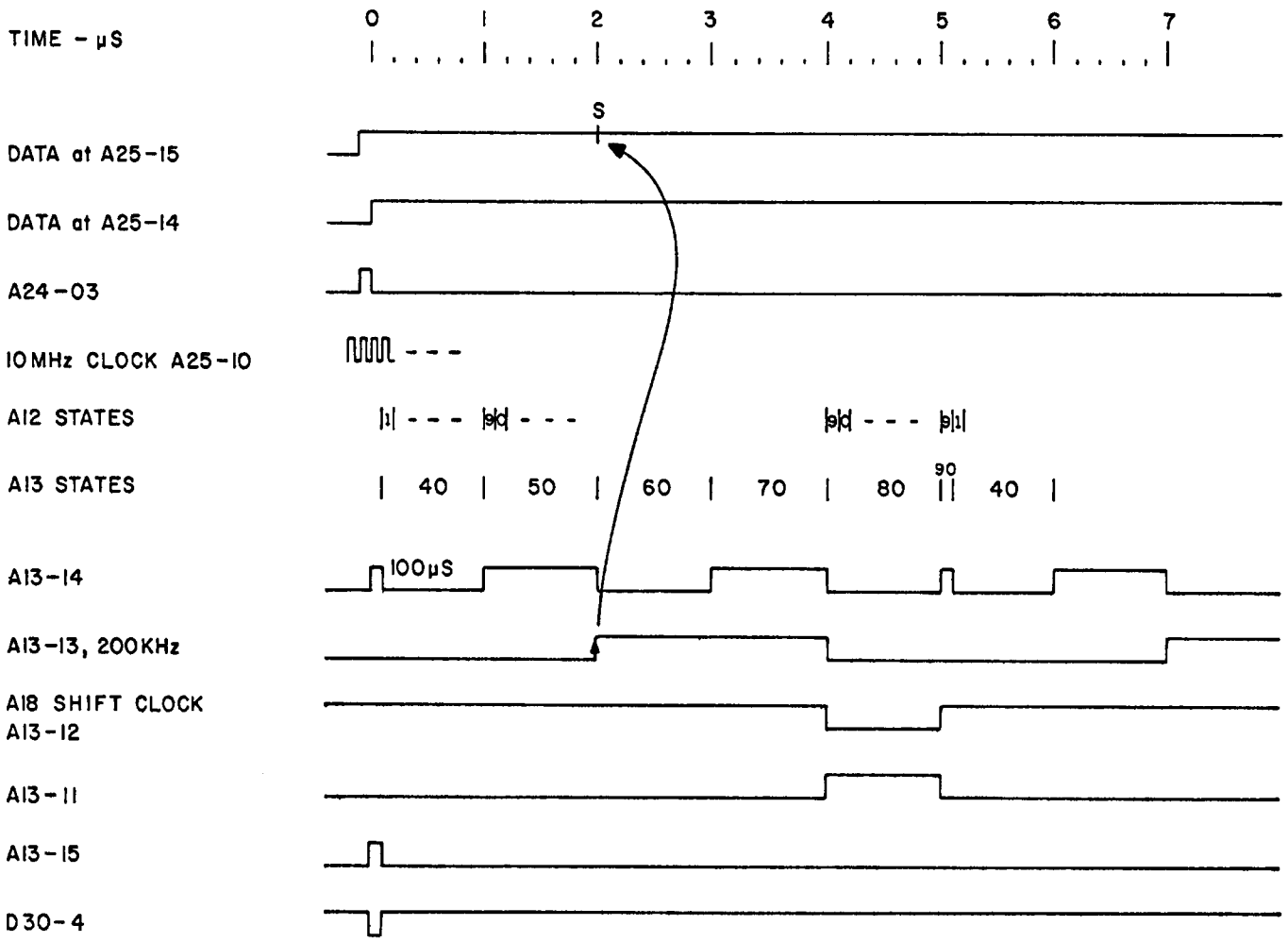
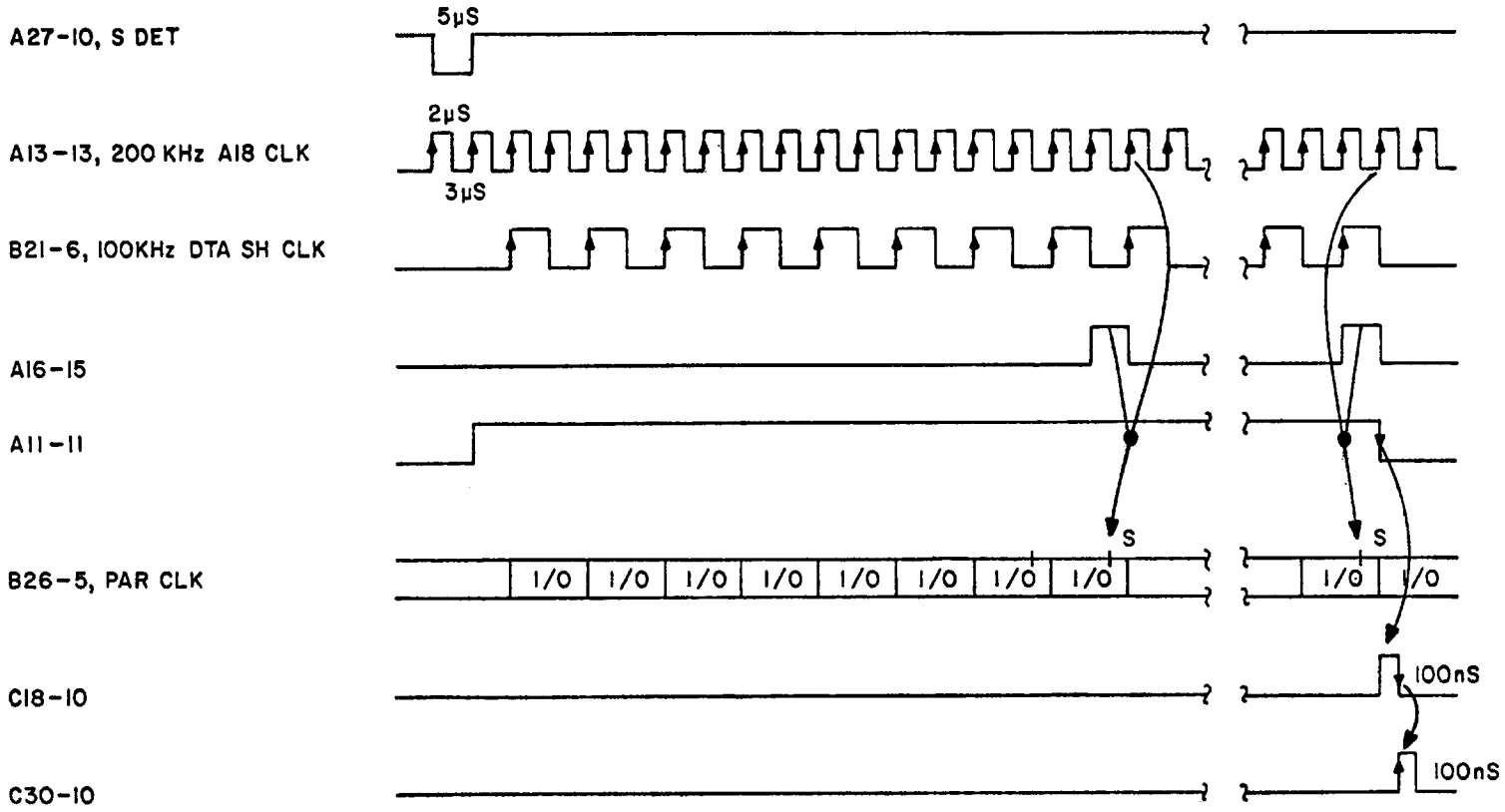


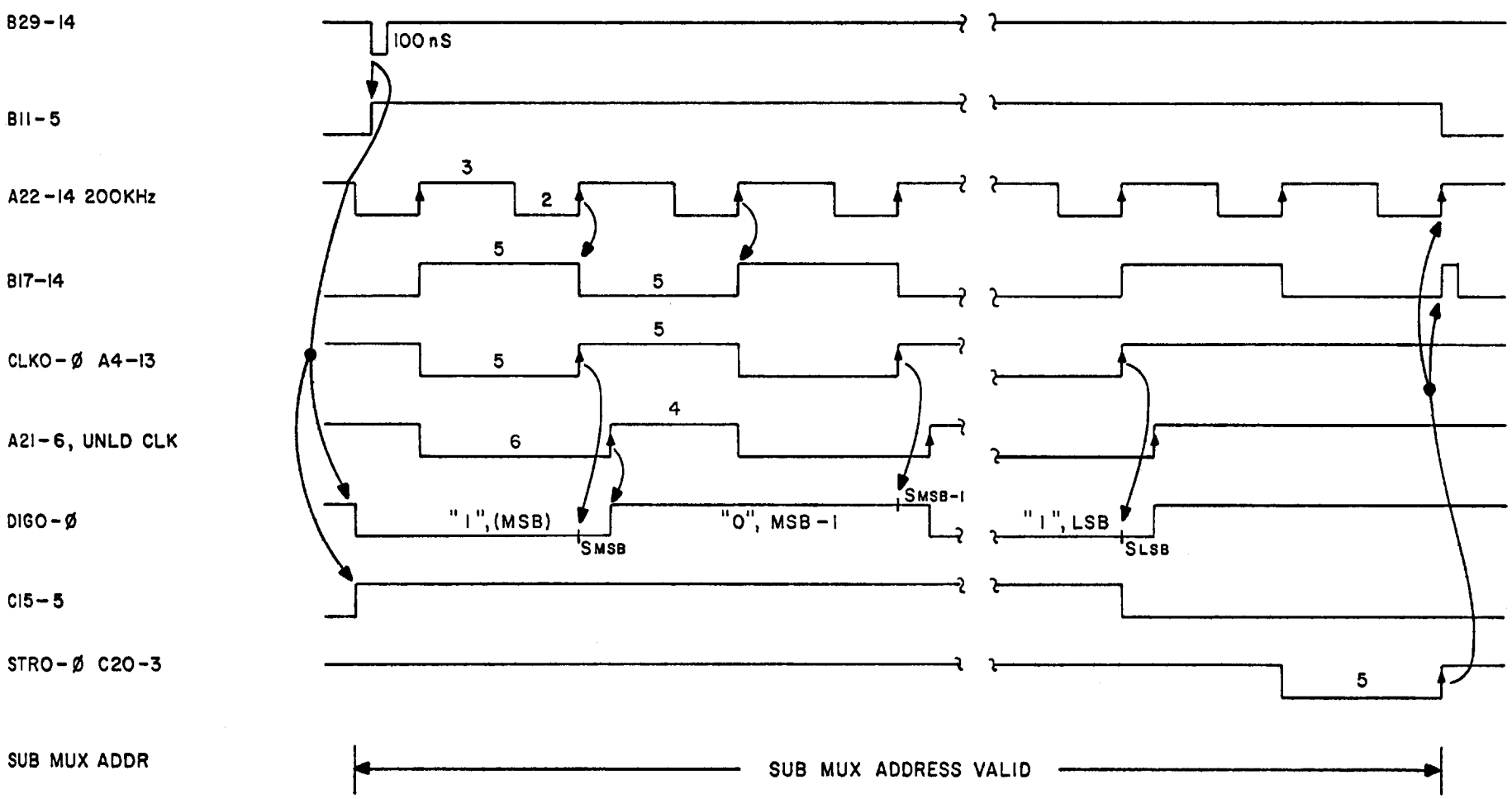
FIGURE 4: DETAILED FUNCTIONAL BLOCK DIAGRAM



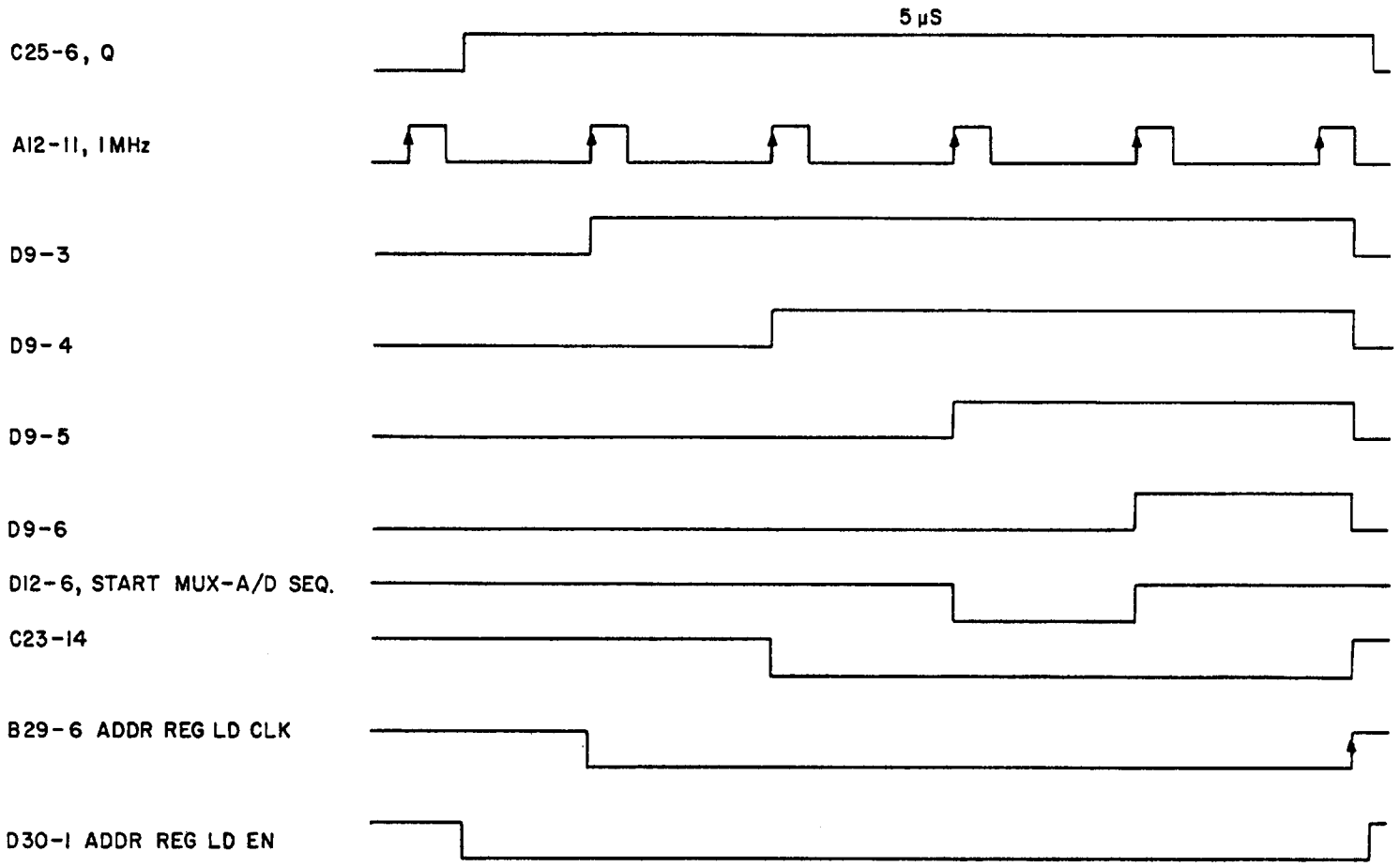
TIMING DIAGRAM 1: INPUT SIGNAL SYNCHRONIZATION TIMING



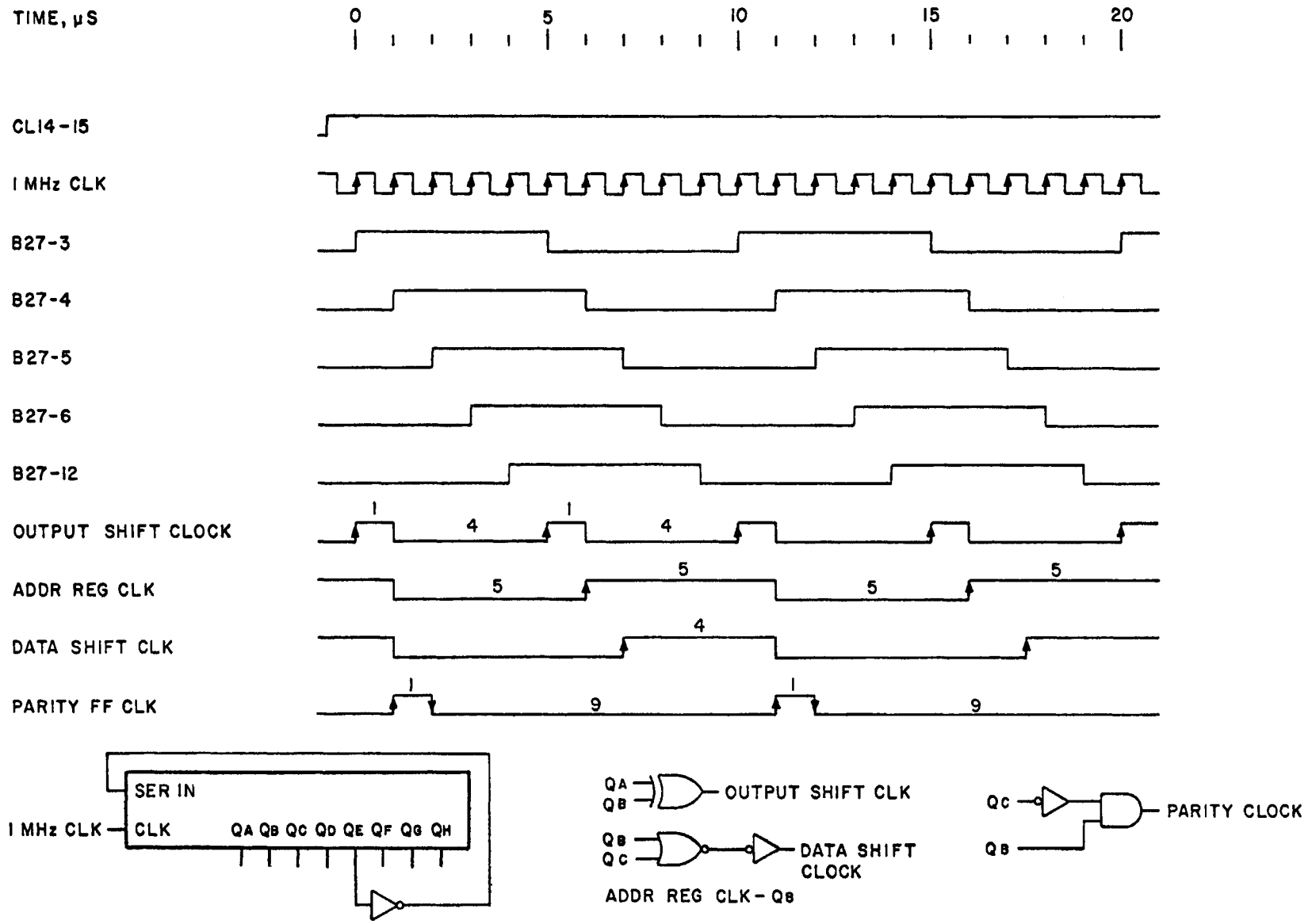
TIMING DIAGRAM 2: MESSAGE DETECTION – LOADING TIMING



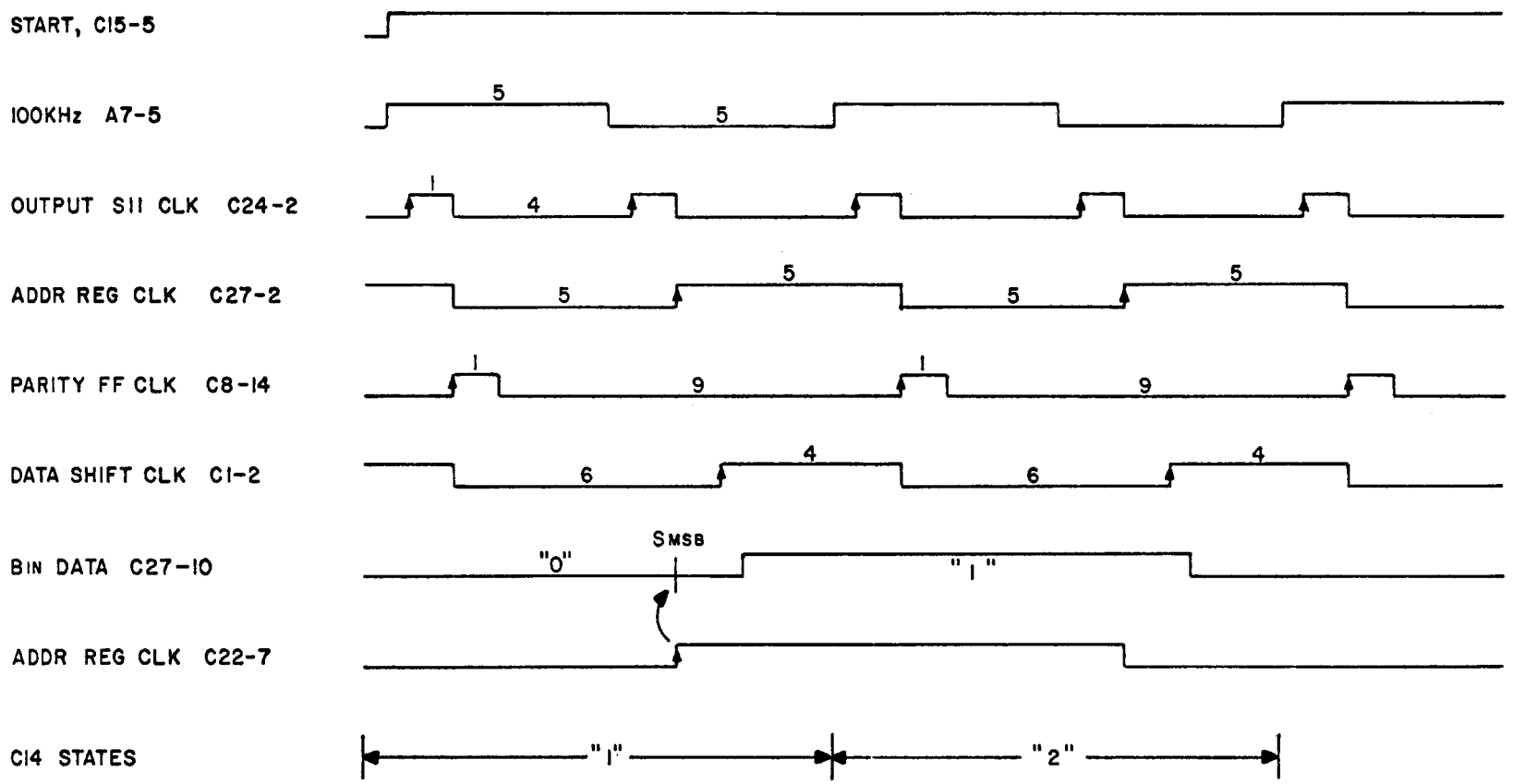
TIMING DIAGRAM 3: COMMAND OUTPUT TIMING



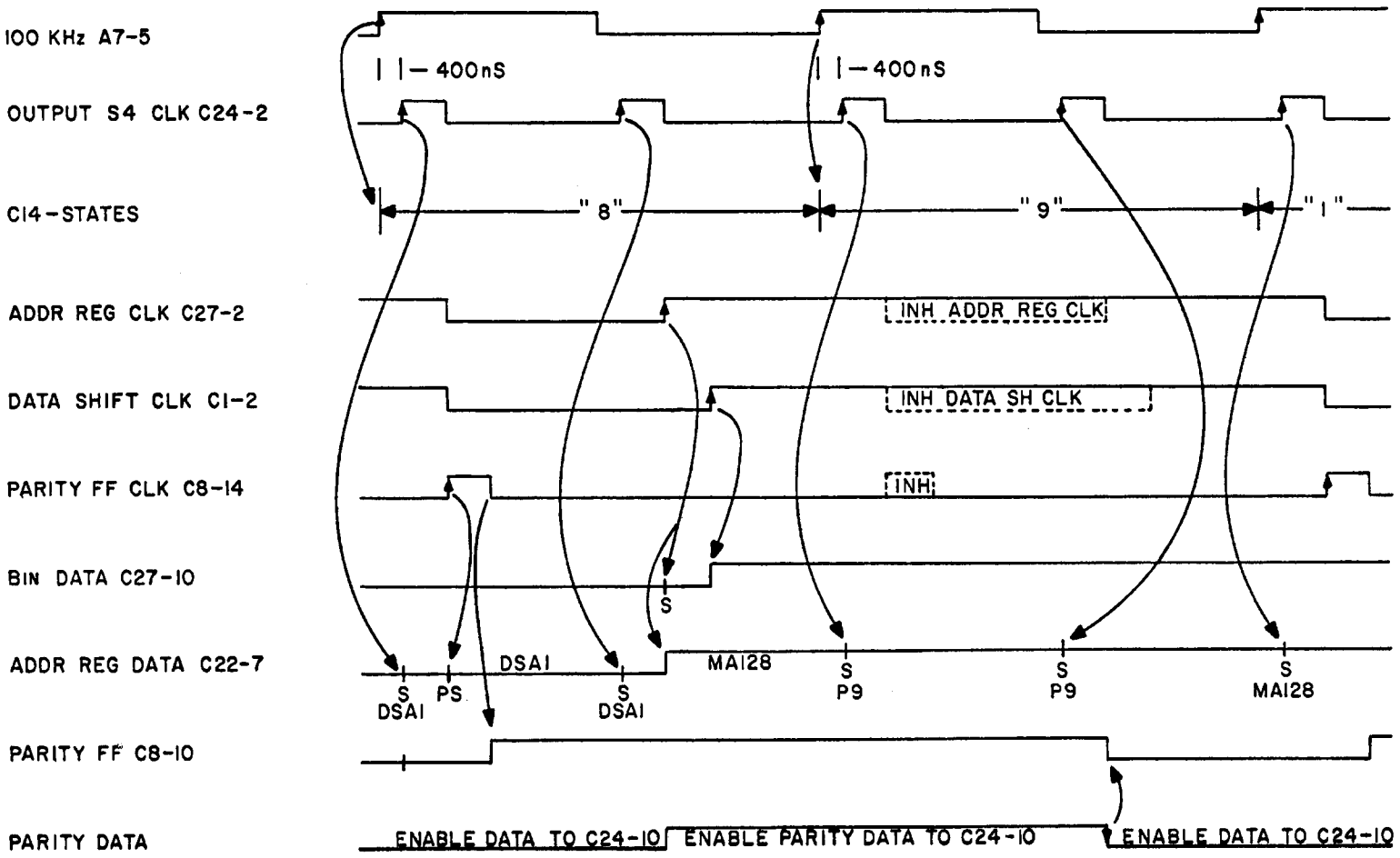
TIMING DIAGRAM 4: MONITOR DATA MULTIPLEX ADDRESS CLOCK PHASE GENERATOR



TIMING DIAGRAM 5: MONITOR DATA OUTPUT CLOCK GENERATOR



TIMING DIAGRAM 6: MONITOR DATA OUTPUT CLOCKING, START OF DATA OUTPUT



TIMING DIAGRAM 7: MONITOR DATA OUTPUT TIMING, PARITY DATA OUTPUT

4.0 ANALOG SUBSYSTEM ALIGNMENT AND TESTS

The analog multiplexer - A/D converter board is removable from the Data Set for alignment and test in a controllable analog and logic environment. This environment is provided by an A/D-mux test fixture, (dwg. D13720L45) a high precision adjustable DC source (Fluke 343A), a digital multimeter and an oscilloscope.

The A/D-mux test fixture has a dual bus switching structure and several analog signal sources. Control and conversion logic sequences the multiplex address, triggers the sample/hold unit and A/D converter and displays the converted digital value and mux channel. The timing of these terms is identical to those in the Data Set. Control switches permit the multiplex address to sequence or be set at any channel. These switches also permit the selection of continuous or manually triggered conversions and the use of various alignment and perturbation sources.

4.1 Alignment Procedure for Revision C A/D Board

1. Set the front panel switches of the mux-A/D test fixture unit as follows:

CMP/LC	- LC
SCAN/SEL	- SEL
MANUAL/OFF	- OFF
BUS A 0-J0	- 0
BUS A DIFF/CM	- DIFF
BUS A +/-	- +
BUS B 0-50	- 0
BUS B DIFF/CM	- DIFF
CHANNEL SELECT	- CH 0
BUS A SOURCE	- GND
BUS B SOURCE	- GND

   Set all channel switches to BUS A.

   Plug a Revision C A/D board (component side up) into the top socket and turn power switch on.

2. Connect a 4 digit Data Precision DVM between the S/H out

and the analog ground test points, and adjust the S/H offset pot for a reading of 0.0000V.

3. Move the DVM to the analog out and analog ground test points and set the zero adjust pot on the MMD-8 multiplexer for 0.000V out.
4. Remove the DVM and adjust the ADC offset pot for a tester display of 0.000V.

4.2 DC Common Mode

1. Set the BUS A DIFF/CM switch to CM. Set the BUS A source to 100 Hz square wave. Switch the desired channel to BUS A and all others to BUS B (GND). With a scope of at least 5 MV/cm sensitivity connected between the analog out and analog gnd terminals, adjust the DC CMR pot on the MMD-8 for the absolute minimum signal.

4.3 AC Common Mode

1. Using the procedure outlined above, set the BUS A source to a 1 kHz sine wave and adjust the AC CMR pot on the MMD-8.
2. Repeat the DC CMR adjustment of step 4.2.1 to insure proper AC and DC CMR alignment.

4.4 A/D Adjustment and Test

1. Set the BUS A DIFF/CM switch to DIFF and the BUS A source to external. Apply a precision DC reference between the BUS A Hi and Low terminals.
2. Set the reference for +10.000V and adjust the ADC gain pot for a panel reading of 10.000V.
3. Set the reference for +0.000V and adjust the ADC offset adj. pot for 0.000V. Return to step 2 and repeat until no further adjustment is necessary.
4. Using the test data sheet, Figure 10, vary the external reference from +10.000V to -10.000V in 1.0V increments and record the displayed converted values. It may be convenient to set in small offsets to the 1V increments to more effectively evaluate any error biases which may exist in the A/D converter.

4.5 CMR Test

1. Install a 1 kΩ resistor between the BUS A Hi and Low terminals. Connect desired channel to BUS B.
2. Set BUS A source to external. Set RSA and RSB switches to 0 resistance. Set A and B +/- switches to +. Set A and B CM/DIFF to CM.
3. Set BUS B source to 1 k, and note converted value.
4. Set BUS B source to 1V and record value.
5. Set BUS B source to 10V and note value.
6. Calculate and record following values:

$$CMR_1(dB) = 20 \log \frac{|(\text{step 3} - \text{step 4})|}{1.000V}$$

$$CMR_2(dB) = 20 \log \frac{|(\text{step 3} - \text{step 5})|}{10.000V}$$

In handling the A/D-mux board, it is very important to avoid touching the PC board contact fingers as human skin oil and salts may contaminate and corrode the edge connector contacts in the Data Set. This will cause unreliable contact in a few months time. If the contact fingers are touched, the edge connector contact area should be thoroughly cleaned before installing the A/D-mux board in the Data Set.

DATA SET MUX - A/D TEST DATA

Board Type REVISION C Serial # _____

Date _____ Test/Set-up By _____

Input Volts	Conv'rtd. Value	Error, MV
+10.000		
+ 9.000		
+ 8.000		
+ 7.000		
+ 6.000		
+ 5.000		
+ 4.000		
+ 3.000		
+ 2.000		
+ 1.000		
± 0.000		
- 1.000		
- 2.000		
- 3.000		
- 4.000		
- 5.000		
- 6.000		
- 7.000		
- 8.000		
- 9.000		
-10.000		
CMR, dB		CMR-2

A/D SN _____

MUX SN _____

Installed in

DS _____

DATE _____

FIGURE 10: MULTIPLEXER - A/D CONVERTER CARD TEST DATA SHEET

5.0 DIAGNOSTIC/TROUBLESHOOTING OBSERVATION POINTS AND DEPENDENCY RELATIONSHIPS

Figure 8 shows the timing waveforms which may be observed on the front panel test connector (J1). These test points are connected to important points in the logic and are a valuable diagnostic aid in evaluating the Data Set logic operations.

Figure 7 shows the Data Set logic flow diagram. This schema illustrates the logic and dependency relationships of the Data Set inputs, stimulus and outputs.

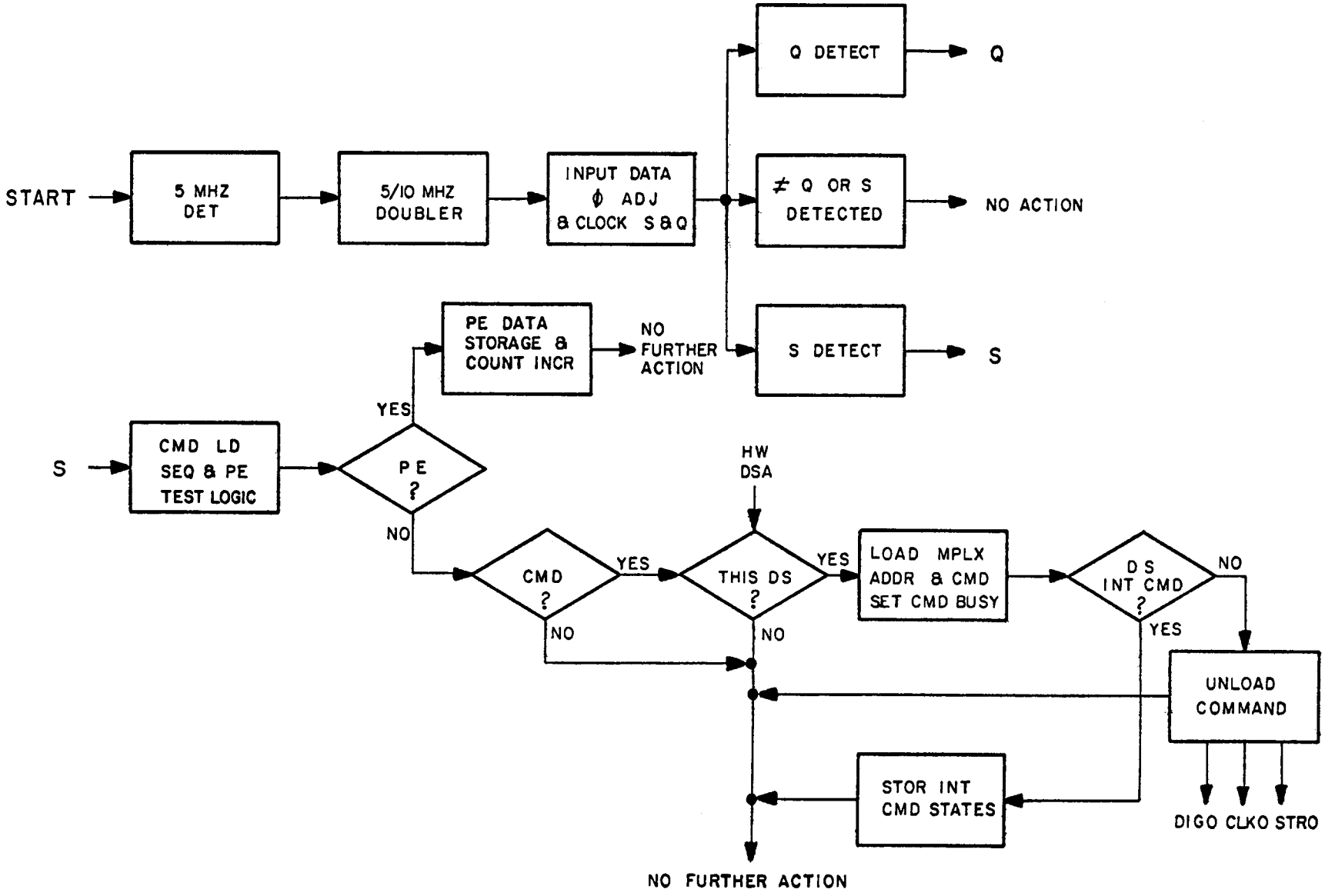


FIG. 7: DATA SET LOGIC FLOW DIAGRAM

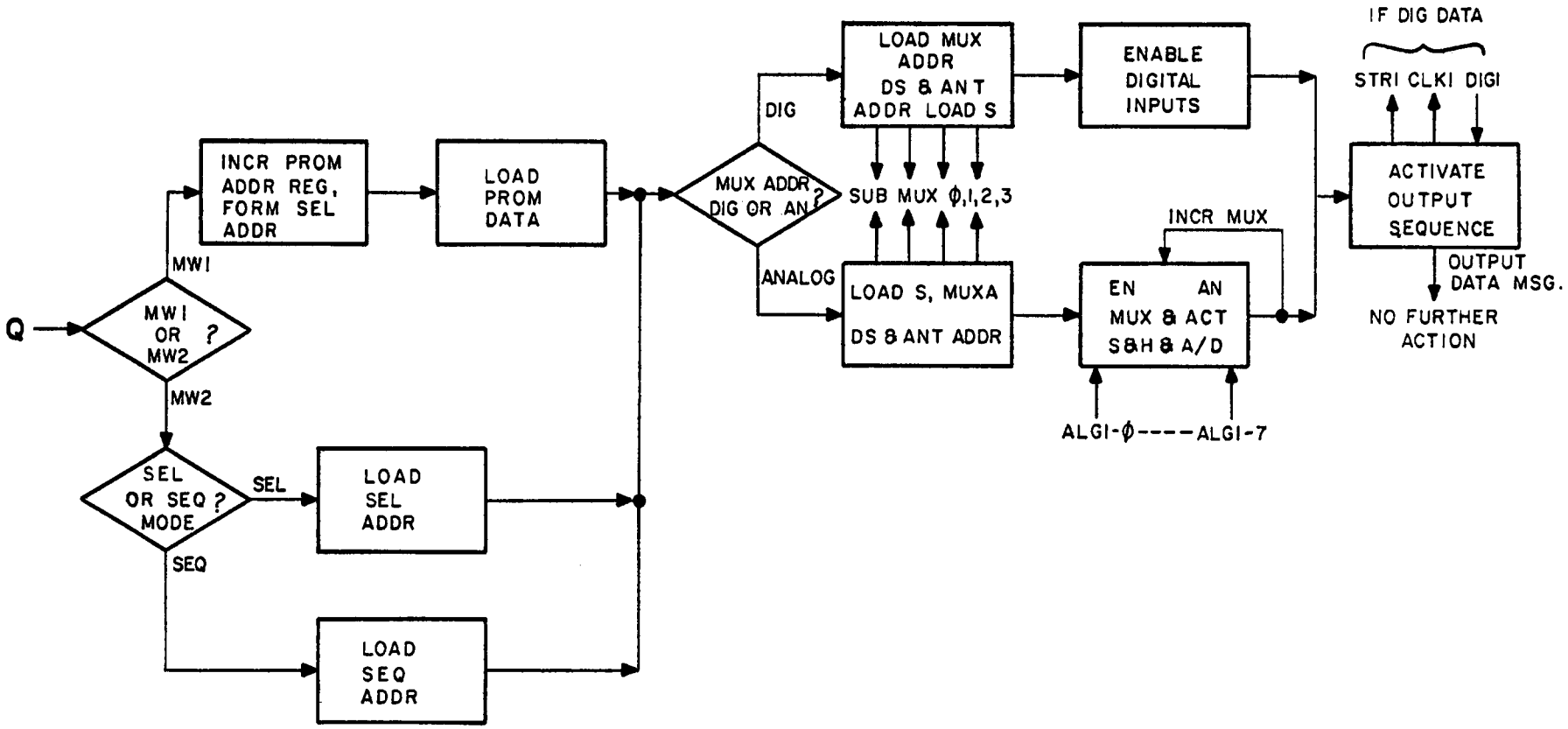
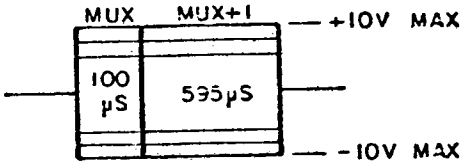
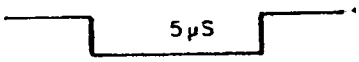
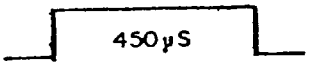
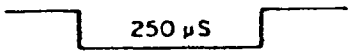
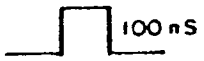
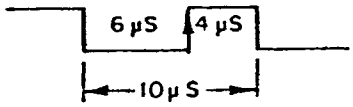
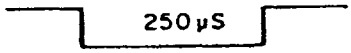
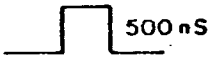
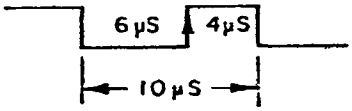
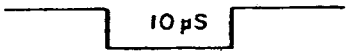
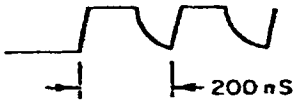
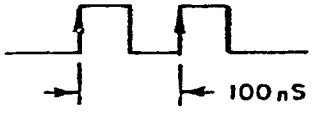
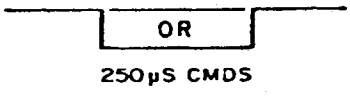
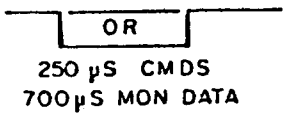
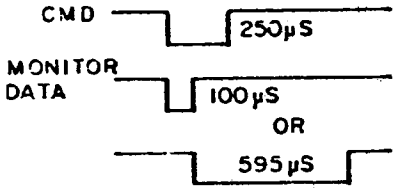
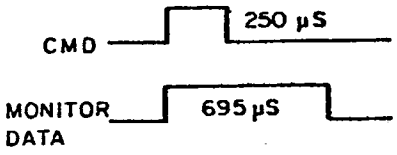
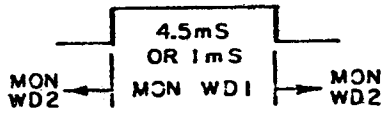


FIG.7 : CONT. DATA SET LOGIC FLOW DIAGRAM

FIGURE 8: DATA SET TESTPOINT (J1) WAVEFORMS

J1 Pin	Signal	Comment	Waveform (+3.5 = HI, Gnd = LO)
1	+5SYNC	+5 VDC	DC, +5
2	GNDSYNC	Logic Conn	DC, Gnd
3	ANMON	Multiplexed Analog Data	
4	PARERR	Parity Error Detected	
5	DTAOUT	Monitor Data to Buffer	Monitor Data Message, Hi-True
6	DSINP	Data Set	Cmd/Monitor Messages, Lo-True
7	CLKDIN	Clocked Input Message	Cmd/Monitor Messages, Hi-True
8	SHFTCLK	Input Message Load Clock	
9	SHFTEN	Input Message Shift Enable	
10	SDET	Cmd/Mon Message Detected	
11	QDET	Data Request Message Detected	
12	SERCMD	Output Cmd Information	10 µs/Bit, Lo-True
13	ADEOC	A/D Conv End of Conversion	

14	192EN	DS Int Cmd En	
15	DSSEL	Message Directed to Data Set	
16	SER/SEL	Sequential/Select Mode Control	Hi = Sequential Mode Control
17	CMDCLK	Command Output Shift Clock, 24 Pulses	
18	RSPPOM	Reset Prom Address Register	
19	A/DSC	A/D Converted Start Conversion	
20	DSCLK	Binary Monitor Data Shift Clock	
21	BINSTR	Binary Monitor Data Load Store	
22	DINDTA	Binary Monitor Data Input to Data Set	Low True Serial Waveform
23	CMDSTR	Cmd Chan Load Strobe	
24	5MHZ	5 MHz detector Output	
25	10MHZ	Doubled 5 MHz	
26	SMA-4	Mux Address - 4, "16", Hi True	

27	SMA-5	Mux Address - 5 "32", Hi True	
28	SMA-6	Mux Address - 6 "64", Hi True	SAME AS ABOVE
29	SMA-7	Mux Address - 7 "128", Hi True	SAME AS ABOVE
30	SMA-0	Sub-Mux Address - 0 "1", Low-True	
31	SMA-1	Sub-Mux Address - 1 "2", Low-True	SAME AS ABOVE
32	SMA-2	Sub-Mux Address - 2 "4", Low-True	SAME AS ABOVE
33	SMA-3	Sub-Mux Address - 3 "8", Low-True	SAME AS ABOVE
34	A/DDATA	Converter Analog Data Storage Reg	24 Bits, Low True
35	DSBUSY	Data Set Busy, Executing CMD or Gathering New Data	
36	WD1/WD2	Monitor Word 1/2 Control Flip-Flop	
37	PEDATA	Parity Error Data Storage Reg Output	PE Message Data, Hi-True

6.0 TYPICAL COMMAND/DATA CHANNEL LOGIC

In this section, we consider the logic circuitry and functions of a generalized controller which may be used for module control and monitoring. The controller can accept and store a 24 bit binary command, read out a 24 bit binary data word and multiplex 16 channels of analog data. Figure 3 depicts the logic diagram of this generalized controller. The logic description in this section is a simplistic treatment. The interested reader may refer to the earlier section for a more detailed discussion of the generation and use of the clocking and strobe signals.

A fundamental requirement for a command or data channel is multiplex address enabling or activation. Each channel serviced by the Data Set has a unique 8 bit multiplex address assignment which when decoded enables a command to be stored or data gathered. The four high order bits of the multiplex address are decoded internally in the Data Set and cause the Data Set internal analog multiplexer, binary data and command lines to be activated to interact with a module controller. Each decode state of these higher order bits is associated with a group of 16 multiplex addresses; therefore, up to 16 channels of analog data, command or binary data may be serviced by the analog, command and binary data lines. Referring to Table I we see that the Data Set analog multiplexer can service eight controllers having up to 16 analog channels for a total of 128 analog channels. Combinations of eight and sixteen channel controllers may also be implemented. Four sets of binary monitor lines can service up to 64 channels of 24 bit binary monitor data or 1536 binary bits. Three sets of command lines can service up to 48 channels of 24 bit binary commands or 1172 bits.

The four lower order bits of the multiplex address are bussed to each module controller in a daisy chain. The controllers then decode these lines to generate enabling terms which permit the controller to load commands and output binary and analog data. These low true multiplex address terms are called sub-mux address

and are labeled SMA-0 ("1"), SMA-1 ("2"), SMA-3 ("4") and SMA-3 ("8") on the wire lists and logic diagrams.

All logic lines to a device controller are low true and should not burden the Data Set with more than one standard TTL load. The binary monitor data output gate should be an open collector gate as the binary monitor data lines (DIGI-X) are a daisy chain with the pull-up resistor in the Data Set.

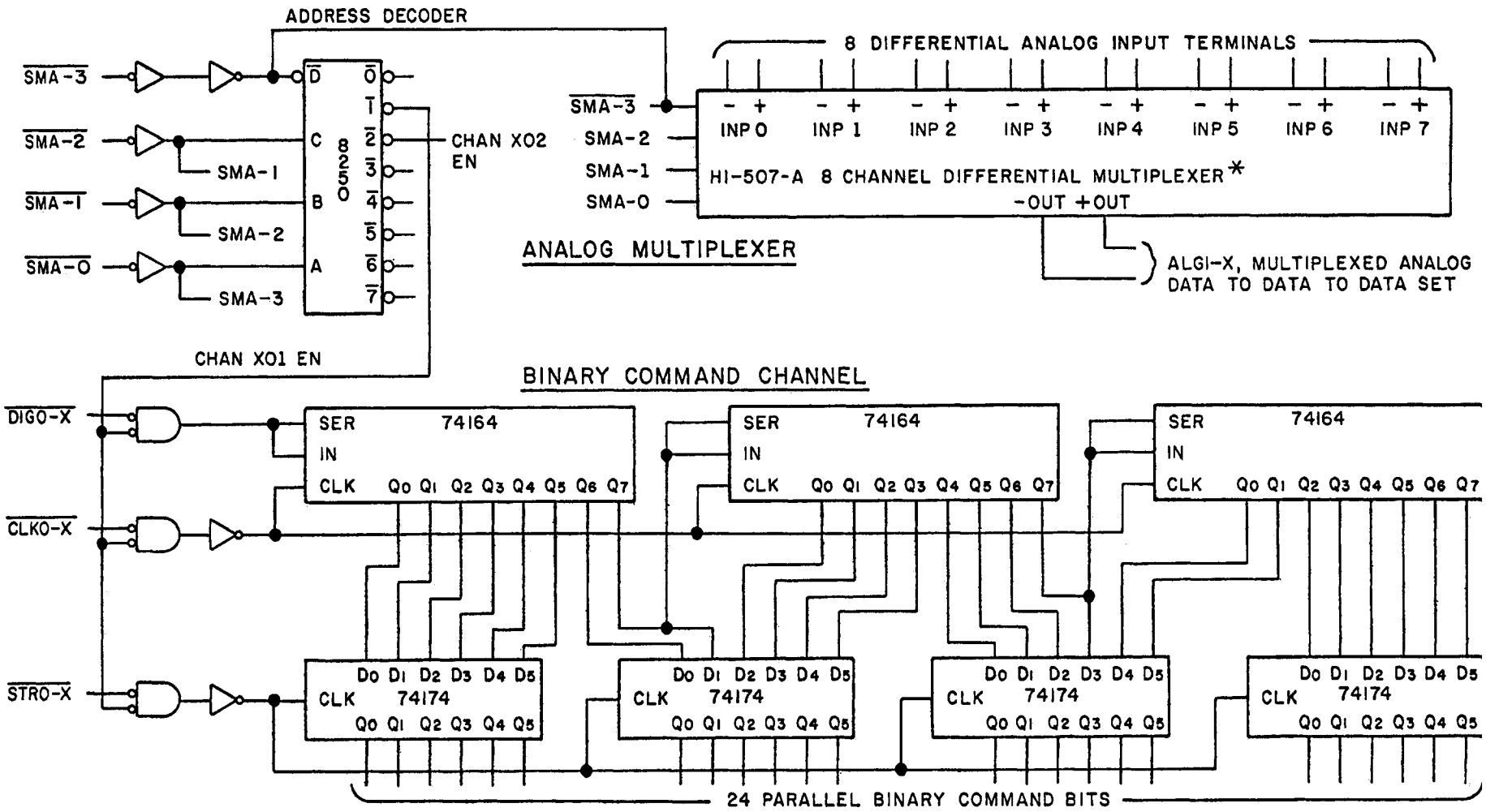
The command portion of the controller consists of a serially loaded shift register, enabled by the decoded multiplex address. At the completion of the serial load, the 24 command information bits are parallel loaded into static storage by the command strobe pulse (STRO-X). Note that the command loading samples (shifts) the command information line (DIGO-X) on the trailing (rising) edge of the clock pulse (CLKO-X). The Data Set shifts out the command information on the leading edge of the clock thus providing a large margin of settling delay.

Binary monitor channels operate in a similar manner but the information flow is reversed. Again the decoded multiplex address enables the logic operations. A strobe (STRI-X) pulse causes the data loading register to parallel load 24 discrete logic level lines. Then a 24 pulse shift clock from the Data Set causes the information to be serially loaded into the Data Set. The data loading, register shifts on the trailing edge of the clock (CLKI-X) pulses while the Data Set samples the data on the leading edges.

The analog multiplexer is driven by the sub-mux lines and may operate in either single-ended or differential mode. The differential mode is preferred in cases where there is more than a few millivolts of common mode signal impressed upon the data. By tying the multiplexer low sides to the common mode sources (there may be more than one), the differential amplifier in the Data Set is able to "buck" out the common mode signal to provide a more accurate conversion of the analog signal.

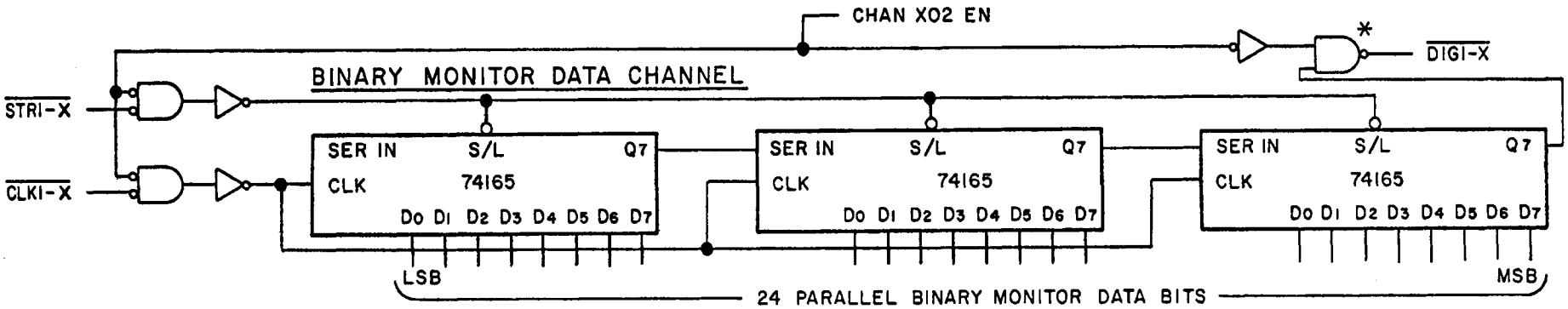
Timing Diagrams 8, 9 and 10 illustrate the time relationships of the sub-mux address, command, binary and analog signals.

The generalized controller logic schematics shown here are obviously not the only implementation possible (many other arrangements are possible) but they illustrate the interfacing techniques to be used with the Data Set.



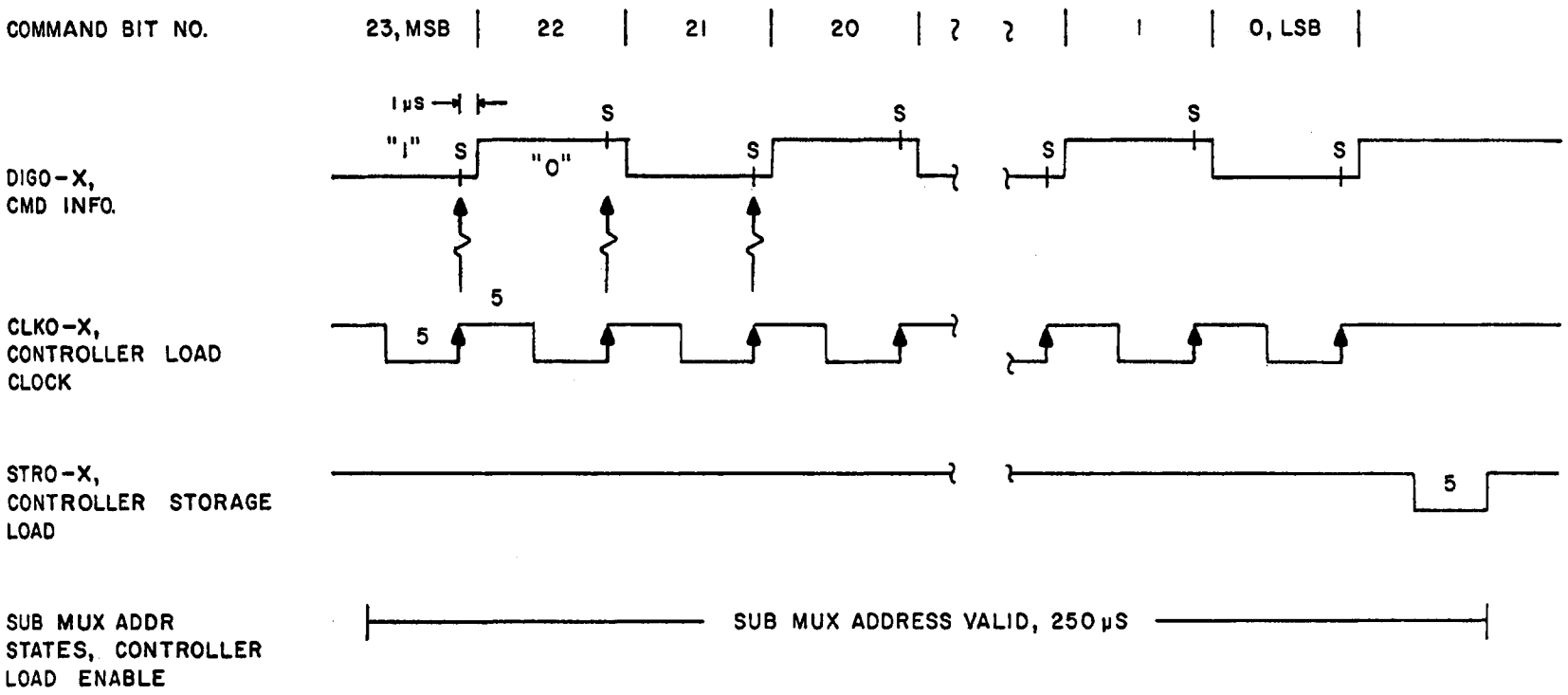
* ANOTHER 8 CHANNEL DIFFERENTIAL MULTIPLEXER MAY BE ADDED OR 16 CHANNEL SINGLED MULTIPLEXERS SUBSTITUTED IF COMMON MODE VOLTAGES ARE LOW.

FIGURE 3: TYPICAL MODULE CONTROLLER LOGIC DIAGRAM



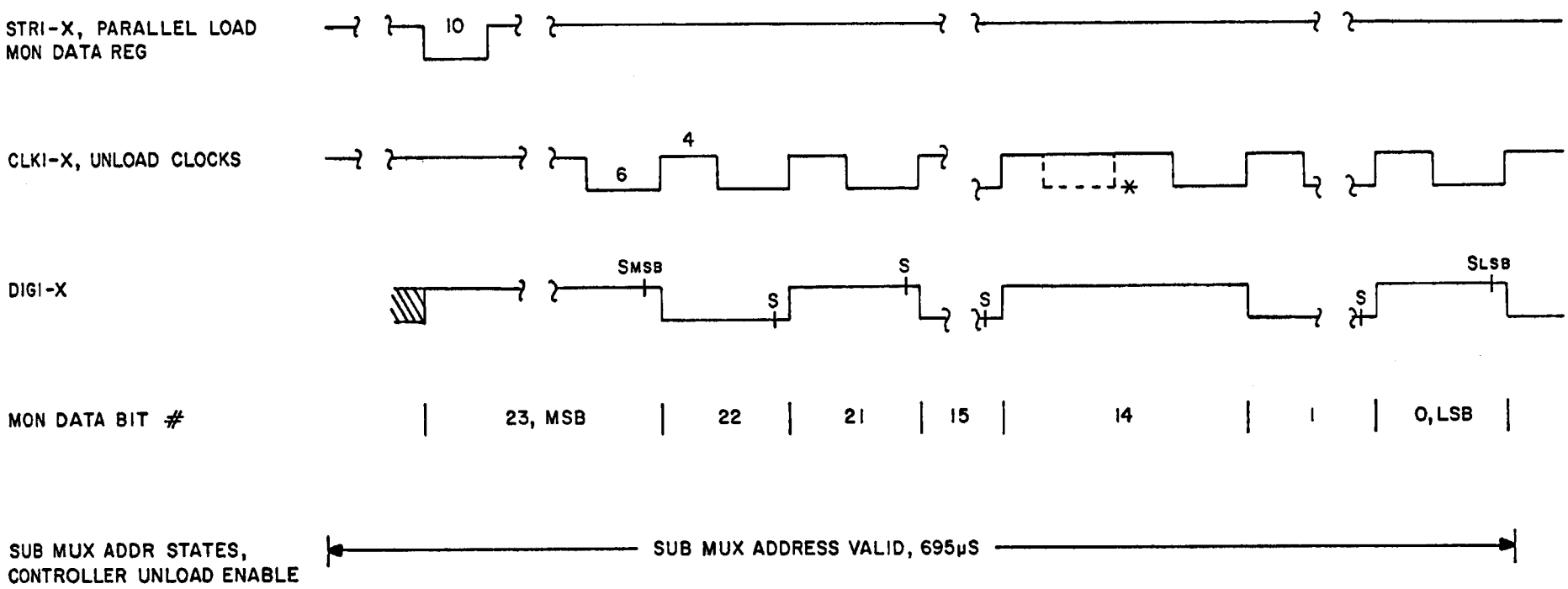
* - THIS GATE MUST HAVE AN OPEN COLLECTOR AS THE DIGI-X LINE IS A PARTY LINE WITH THE PULL-UP RESISTOR IN THE DATA SET.

FIGURE 3: CONT.



S = CONTROLLER SAMPLES (ie. LOADS SHIFT REG.) CMD INFO. AT THIS POINT

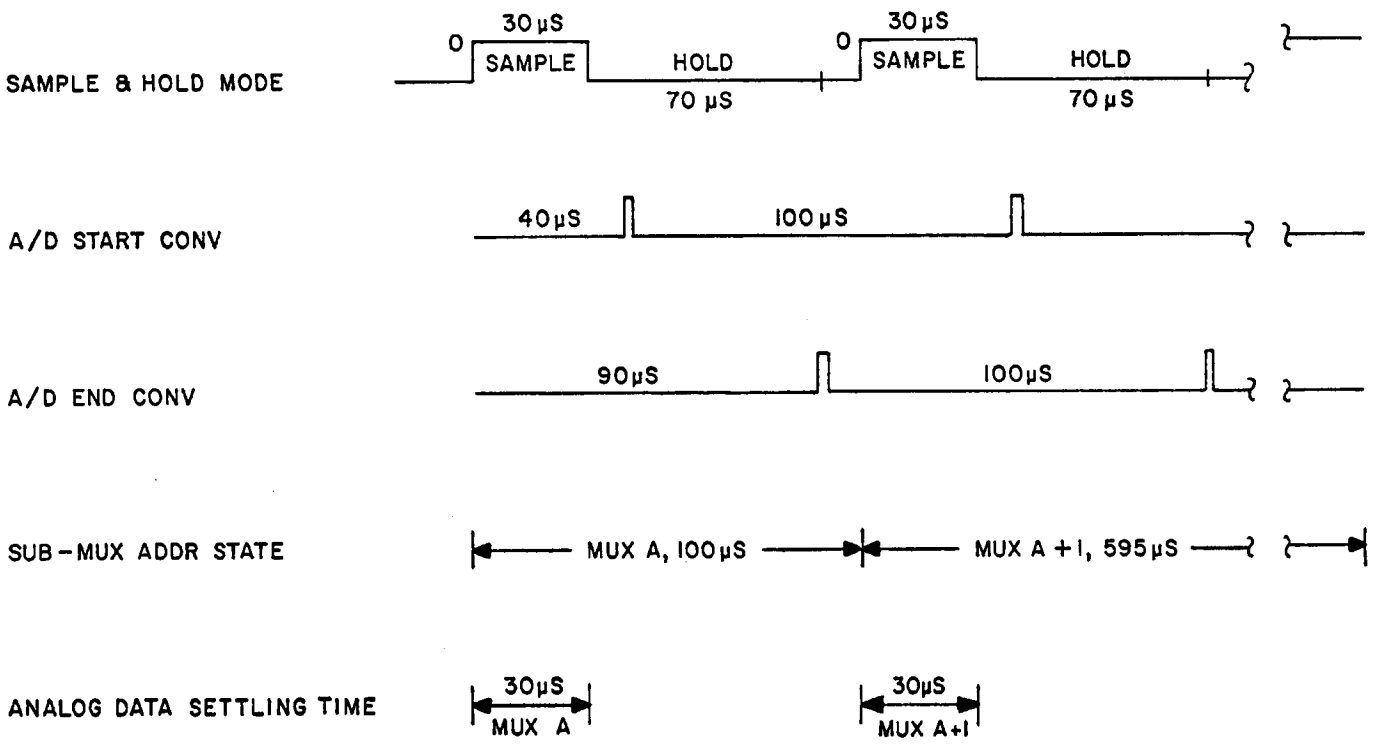
TIMING DIAGRAM 8 — CONTROLLER COMMAND LOAD TIMING



S⇒ DATA SET SAMPLES DATA AT THIS POINT

* THERE ARE 3 PAUSES IN CLKI-X AT 9 BIT INTERVALS TO PERMIT DATA SET TO MERGE PARITY DATA INTO MONITOR DATA WAVEFORM.

TIMING DIAGRAM 9: CONTROLLER BINARY MONITOR DATA UNLOAD TIMING



TIMING DIAGRAM 10 – CONTROLLER ANALOG DATA TIMING

7.0 DATA SET DOCUMENTATION

Figure 9 is the Revision "D" Data Set documentation file and relates all the Data Set drawings in the assembly hierarchy.

TOP ASSEMBLY DRAWING - D13720P73
TOP BILL OF MATERIAL - A13720Z99

LED DISPLAY SUB ASS'Y.

Ass'y Dwg. - C13720P38
BOM - A13720Z83
Drill Dwg. - C13720M33
Artwork Dwg. - B13720AB36

A/D CONVERTER SUB ASS'Y.

Ass'd Dwg. - D13720P58
BOM - A13720Z85
Drill Dwg. - D13720M45
Artwork Dwg. - D13720AB11

IC MODULE PANEL

Ass'y Dwg. - C13720P57
Ass'y BOM - A13720Z84

DIP HEADER SUB ASS'YS.

Ass'y Dwg. - Ass'y BOM
A13720P62 - A13720Z89
A13720P63 - A13720Z90
A13720P60 - A13720Z87
A13720P59 - A13720Z86
A13720P6 - A13720Z88
B13720P16 - A13720Z39
B13720P17 - A13720Z9
A13720P69 - A13720Z95
B13720P14 - A13720Z10

MECHANICAL PARTS

Front Panel, Engrvd. - B13720M22
Filter, Red Pol. - B13720M18-1
Filter, Clr - B13720M18-2
Rail Modified - C13720M15-1
Rail Modified - C13720M15-2
Rear Panel - B13450M32
Guide Blocks - B13050M4
Perf Cover - C13050M7
Side Plate - C13720M50
Bracket, Conn. - B13720M46
Spacer - B13720M47
Side Plate Insul. - B13720M49

MASTER WIRE LIST A13720W61

HAND WIRE LIST	MACHINE WIRE LIST	CONNECTOR I/O LIST	POWER WIRING DIAGRAM
A13720W62	A13720W63	A13720W64	D13720L44, SH7

LOGIC DIAGRAMS D13720L44

FIGURE 9: REV. "D" DATA SET DOCUMENTATION TREE

8.0 I/O SIGNAL PIN ASSIGNMENTS

Figure 5 shows the Data Set vital, address and signal I/O pin assignments. Figure 6 shows the command/data channel I/O pin assignments.

VITAL INPUTS		ADDRESS INPUTS		SIGNAL INPUTS		SIGNAL OUTPUTS
+5 V Logic Pwr	J4-10	Anta-4 ("16")	J4-18	CMD Inp-HI	J4-25	CMD/Data to DT, HI - J4-8
5 V Common	J4-34	Anta-3 ("8")	J4-24	CMD Inp-Ret	J4-26	CMD/Data to DT,Ret - J4-9
+15 V Pwr	J4-16	Anta-2 ("4")	J4-20			Data to Buffer,HI - J4-15
-15 V Pwr	J4-17	Anta-1 ("2")	J4-13			Data to Buffer,Ret - J4-27
Analog Gnd	J4-42	Anta-0 ("1")	J4-2			
5 MHz-HI	J3-MM	DSA-2 ("4")	J4-29			
5 MHz-Ret	J3-NN	DSA-1 ("2")	J4-28			
		DSA-0 ("1")	J4-11			

FIGURE 5: DATA SET VITAL, ADDRESS AND SIGNAL I/O PIN ASSIGNMENTS

DIGI/O	#0	#1	#2	#3
ADDR$_8$	200_8-217_8	220_8-237_8	240_8-251	260_8-277_8
Signal	⟵ J3-34 Pin ⟶		⟵ J4-42 Pin ⟶	
DIGIX	J3-B	J3-R	J4-01	J4-19
DIGIX RET	J3-D	J3-T	J4-04	J4-22
CLKIX	J3-F	J3-V	J4-03	J4-21
CLKIX RET	J3-J	J3-X	---	---
STRIX	J3-L	J3-Z	J4-12	J4-23
STRIX RET	J3-N	J3-BB	---	---
ADDR$_8$	320_8-337_8	340_8-357_8	360_8-377_8	
DIGOX	J3-C	J3-S	J4-35	
DIGOX RET	J3-A	J3-P	J4-36	
CLKOX	J3-H	J3-W	J4-37	
CLKOX RET	J3-E	J3-U	---	
STROX	J3-M	J3-AA	J4-30	
STROX RET	J3-K	J3-Y	---	

J3 J4

	ALGI-X	
00_8	ALGI-0+	J4-14
	ALGI-0-	J4-32
20_8	ALGI-1+	J4-33
	ALGI-1-	J4-41
40_8	ALGI-2	J4-7
60_8	ALGI-3	J4-40
100_8	ALGI-4	J4-6
120_8	ALGI-5	J4-39
140_8	ALGI-6	J4-5
160_8	ALGI-7	J4-38

J4

	SUB-MUX ODR	
"1"	SMA-0	J3-EE
	SMA-02	J3-CC
"2"	SMA-1	J3-KK
	SMA-1R	J3-HH
"4"	SMA-2	J3-DD
	SMA-2R	J3-FF
"8"	SMA-3	J3-JJ
	SMA-3R	J3-LL

J3

FIGURE 6: COMMAND/DATA CHANNEL I/O PIN ASSIGNMENTS

9.0 SPECIAL MODULE DATA SHEETS

Four special purpose modules are used in the Data Set. These are:

1. A/D Converter - Datel K12BE
2. Analog Multiplexer - Datel MMD-8
3. Sample and Hold - Burr-Brown SHC-85
4. PROM - Intel 1702A

All four of these items are contained on the Analog Multiplexer - A/D Converter PC board and are removeable for replacement. The PROM is installed on the A/D board because of its 24 pin physique which would be awkward to mount anywhere else in the Data Set. The PROM address programs are particularized for the data sampling requirements of each application so be sure the appropriate PROM is installed before you leave for an antenna with a Data Set under your arm. Be sure to use a PROM carrier when installing a PROM as the chip leads are very delicate and PROM's are very expensive.

Data Sheets for these four modules are bound in the next few pages.

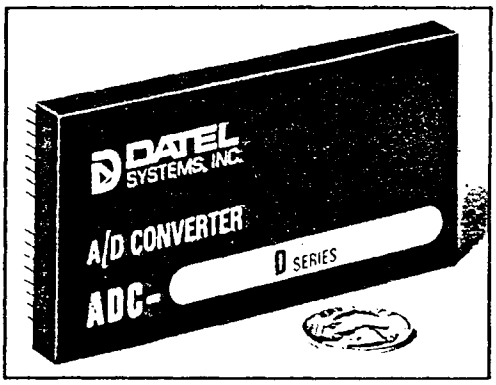
The A/D Converter data sheet shows only a ±5 volt input signal range. The A/D Converter used by the Data Set is a specially ordered version which has an input signal range of ±10 volts (actually +10.235 to -10.240 or 5 MV/bit).

The A/D is configured for bipolar operation and uses the offset adjustment configuration of Note 2 on the data sheet.

The A/D converter output code for bipolar operation is Offset Binary as shown on the data sheet. Inverter D2512 on the MSB transforms the code to 2's complement format as shown below:

Analog Input	2's Complement Code
+10.235, +FS	0 1 1 1 1 1 1 1 1 1 1 1
+10.230, +FS-1 bit	0 1 1 1 1 1 1 1 1 1 1 0
+5.000, +½FS	0 0 1 1 1 1 1 0 0 1 1 1
+0.005, CS+1 bit	0 0 0 0 0 0 0 0 0 0 0 1
0.000, CS	0 0 0 0 0 0 0 0 0 0 0 0
-0.005, CS-1 bit	1 1 1 1 1 1 1 1 1 1 1 1
-5.000, -½FS	1 0 1 1 1 1 1 0 0 1 1 1
-10.235, -FS+1 bit	1 0 0 0 0 0 0 0 0 0 0 1
-10.240, -FS	1 0 0 0 0 0 0 0 0 0 0 0

DATEL SYSTEMS, INC.



ANALOG-TO-DIGITAL CONVERTERS

ADC-D SERIES
ADC-K SERIES

GENERAL DESCRIPTION

Modern accuracy, medium conversion speed and relatively low cost is the theme behind the ADC-D and K Series Both use the successive approximation conversion technique. This encoding method is the most popular of all the A/D conversion techniques because it offers a favorable combination of a full monotonic conversion with excellent linearity over the full scale input range.

ADC-D and K series have total conversion speeds of 10 KHz (100 μsec) and 20 KHz (50 μsec) respectively. Voltage input can be unipolar (0 to +10V) or bipolar (±5V) by external pin strapping. Output coding can be straight binary, offset binary or two's complement with word lengths of 8, 10 and 12 binary bits.

Specified accuracy is ±0.05% for ADC-D series and ±0.025% for ADC-K series. Model ADC-D and ADC-K feature 50 ppm/°C and 30 ppm/°C temperature coefficients respectively and need not be adjusted over an operating tem-perature range of 0° to +70°C. Digital outputs include up to 12 parallel lines, serial output and an end of conversion status.

Overall dimensions are 2"W x 4"L x 0.4"H. Input power requirements are ±15VDC and +5VDC and all input control lines and digital outputs are DTL/TTL compatible.

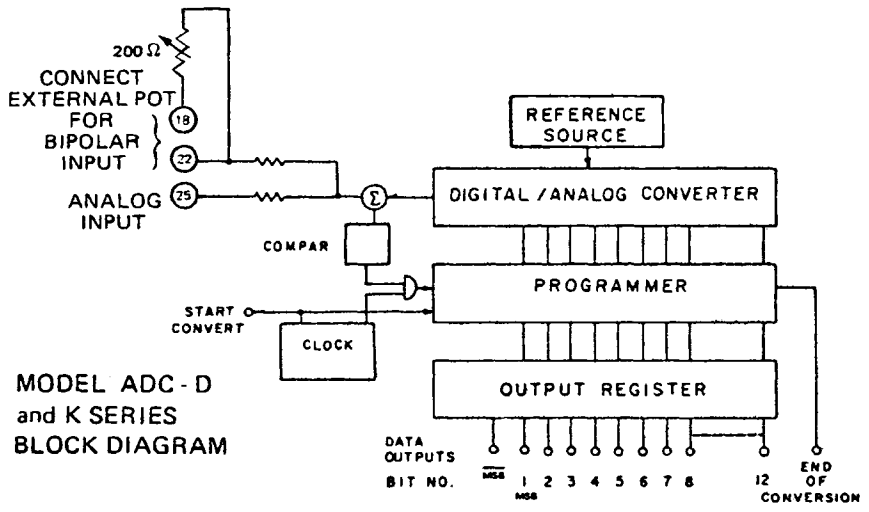
Basic ingredients of each series is a temperature compensated voltage reference source, successive approximation logic, output storage register/programmer, a low noise voltage comparator and a precision digital to analog converter.

All models feature dual-in-line pinning compatibility on .100" grid pin spacing.

MODERATE ACCURACY AND SPEED AT LOW COST
PRICED FROM $79.00

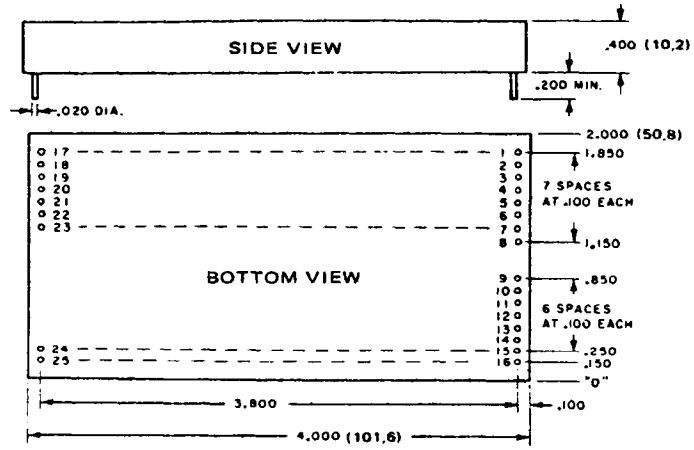
FEATURES

- ☐ Highly accurate . . . . . ±0.025%
- ☐ Moderate conversion rate . . . . 20 KHz word rate
- ☐ High resolution . . . . . Up to 12 binary bits.
- ☐ Ultra-Stable . . . . . ±0.003%/°C
- ☐ Adjustment-Free . . . . . From 0°C to +70°C
- ☐ Small size . . . . . 3.2 cubic inches.
- ☐ Low profile package . . . . . 0.4 inches
- ☐ Completely self-contained . . . . *Simply apply D.C. power.
- ☐ Hardware compatible . . . . . Will mount on 0.5" card file centers. Compatible with dual in-line pinning.
- ☐ OEM designed . . . . . Generous discounts available.



MODEL ADC-D and K SERIES BLOCK DIAGRAM

MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	E.O.C. (STATUS)	17	+ 5 VDC POWER IN
2	MSB OUTPUT	18	+ 15 VDC POWER IN
3	START CONVERT	19	- 15 VDC POWER IN
4	SERIAL OUTPUT	20	POWER GROUND
5	BIT 1 OUT (MSB)	21	OFFSET (NOTE 1)
6	BIT 2 OUT	22	OFFSET (NOTE 2)
7	BIT 3 OUT	23	GAIN ADJUST
8	BIT 4 OUT	24	ANALOG GND
9	BIT 5 OUT	25	ANALOG INPUT
10	BIT 6 OUT		
11	BIT 7 OUT		
12	BIT 8 OUT		
13	BIT 9 OUT		
14	BIT 10 OUT		
15	BIT 11 OUT		
16	BIT 12 OUT (LSB)		

SEE NOTES ON REVERSE SIDE

SPECIFICATIONS (typical @ 25°C unless otherwise noted)

ELECTRICAL

Inputs:

Analog input voltage range . . Standard ranges of 0V to +10V FS, ±5V FS via ext. pin strapping.
Input Overvoltage . . . . . ±15V DC without damage of unit.
Input Impedance . . . . . Standard 10K ohms ±1% shunted with 10 pf single-ended to ground.
Start of Conversion . . . . . 2V min. to 7V max. positive pulse with duration of 100 nsec min. 500 nsec max rise and fall times
"1" resets the converter.
"0" initiates conversion.
Loading of one TTL load.

Outputs:

Parallel output data . . . . . Up to 12 parallel lines of data held until next conversion command.
Vout ("0") ≤ +0.4V
V out ("1") ≥ +2.4V
Each output capable of driving up to 6 TTL loads.
Coding . . . . . Straight Binary (Unipolar Input)
Offset Binary (Bipolar Input)
Two's Complement (Bipolar Input)
Serial Output . . . . . NRZ successive decision pulse output generated during conversion, with MSB first.
End of Conversion . . . . . Conversion Status Signal
Vout ("0")≤ +0.4V conversion complete
Vout ("1") ≥ +2.4V during reset and conversion period.

Performance:

Resolution . . . . . One part in 2^n (max. resolution 12 binary bits or 3 digit BCD). (n= number of binary bits).
Accuracy (@25°C) . . . . . **ADC-D Series**
8 Binary Bits – ±0.05% of FS ±½ LSB
10 Binary Bits – ±0.05% of FS ±½ LSB
12 Binary Bits – ±0.025% of FS ±½ LSB
ADC-K Series
8 Binary Bits, 10 Binary Bits, 12 Binary Bits } ±0.025% of FS ±½ LSB
Temperature Coefficient . . . ±50 ppm/°C – ADC-D Series
±30 ppm/°C – ADC-K Series
Total Conversion Time . . . . 50 µsec
Input Power Requirements . ±15VDC, ±0.5VDC @ ±35 ma
+5VDC, ±0.5VDC @ 300 ma (3)

PHYSICAL-ENVIRONMENTAL

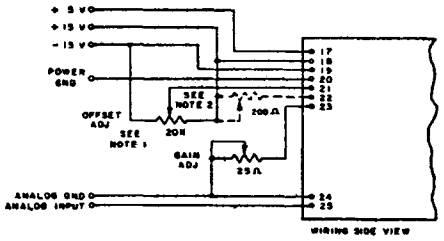
Operating temperature range . . . . . 0°C to +70°C
Storage temperature range . . −55°C to +85°C
Relative Humidity . . . . . Up to 100% Non-condensing
Size . . . . . 2"W x 4"L x 0.4"H
Pins . . . . . 0.020" round gold plated 0.250" long min.
Case Material . . . . . Black Diallyl Phthalate Per MIL-M-14.
Weight . . . . . 4 oz.
Mating Socket . . . . . DILS-2, 2 req'd per module, $4/pr.

Model ADC-D and K Series A/D converter modules are fully encapsulated and feature dual in-line pinning compatibility (i.e. 0.100" grid pin spacing).

Note 3: See power supply catalog #PSC 3-73-1

GAIN & OFFSET EXTERNAL ADJUSTMENT CONNECTIONS

ALL TRIM POTS ARE ≤ 100 PPM/°C
TRIM POTS AVAILABLE FROM DATEL, $3 EA. SPECIFY RESISTANCE
NOTES 1 OFFSET ADJUSTMENT FOR UNIPOLAR 0V TO +10V USE. WHEN NOT IN USE, CONNECT PIN 21 TO GROUND.
2 OFFSET ADJUSTMENT FOR BIPOLAR ±5V FS USE. WHEN NOT IN USE, PIN 22 REMAINS OPEN.



ORDERING INFORMATION

ADC-D
or
ADC-K

NUMBER OF BITS AND CODING
8B = 8 BINARY BITS
10B = 10 BINARY BITS
12B = 12 BINARY BITS

CODING FOR ADC-D AND K SERIES CONVERTERS

BIPOLAR			UNIPOLAR	
Analog Input Range ±5V, FS	Offset Binary	2's Complement	Analog Input Range (0 to +10V, FS)	Straight Binary
+4.9975	111111111111	011111111111	+9.9975	111111111111
+4.3750	111100000000	011100000000	+8.7500	111000000000
+3.7500	111000000000	011000000000	+7.5000	110000000000
+2.5000	110000000000	010000000000	+5.0000	100000000000
0.0000	100000000000	000000000000	+2.5000	010000000000
–2.5000	010000000000	110000000000	+1.2500	001000000000
–3.7500	001000000000	101000000000	0.0000	000000000000
–4.3750	000100000000	100100000000		
–4.9975	000000000001	100000000001		
–5.0000	000000000000	100000000000		

PRICES (1-9)

ADC-D8B – $ 79.00 ea.
ADC-D10B – $105.00 ea.
ADC-D12B – $129.00 ea.
ADC-K8B – $109.00 ea.
ADC-K10B – $129.00 ea.
ADC-K12B – $139.00 ea.

Mating Connector – DILS-2, 2 per module, $5.00/pair.

DATEL SYSTEMS, INC.
PRINTED IN U.S.A.
1020 TURNPIKE STREET, CANTON, MASS. 02021 TEL. (617) 828-8000 TWX: 710-348-0135 TELEX: 924461
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Bulletin ADKDT15404

DATEL SYSTEMS, INC.

Datel Systems' products are manufactured to high standards of workmanship and are carefully tested to ensure reliable operation. Our delivered products have experienced exceptionally low failure rates. In the event that you experience a malfunction with this product, first carefully check the connections and calibration of the device against the enclosed data sheet. If the problem persists and appears to be an internal malfunction, call the nearest Datel Sales Office for instructions on how to return the unit. Returns must be authorized by the factory and must be shipped prepaid.

8 CHANNEL DIFFERENTIAL ANALOG MULTIPLEXER

MODEL MMD-8

DESCRIPTION

The Datel Systems Model MMD-8 is a complete analog multiplexer with buffer amplifiers and a differential output amplifier for selectively switching one of eight differential input channels.

The MMD-8 exhibits excellent transfer characteristics with high speed break-before-make switching. A channel select inhibit (all channels off) is provided so that two MMD-8 multiplexers can be stacked to provide 16 differential input channel multiplexing with a four bit binary address.

The 1.6 cubic inch module contains an electronic switch array with an associated decoder and digital input buffers, two analog buffer amplifiers and a differential output amplifier. The common differential pair from the switch is brought out through an I/O pin along with the inputs and outputs of the two buffer amplifiers and the differential amplifier.

The MMD-8 can accept differential analog inputs of up to ±10 volts with a transfer accuracy of 0.01%. Without the amplifiers, the switching time is typically 500 nanoseconds. With the amplifier, the settling time is only 4 microseconds to 0.01% of full scale.

The differential output amplifiers will deliver ±10 milliamps at ±10 volts full scale. Linearity of this amplifier is 0.01% with an offset adjustable to less than 1 millivolt and an offset vs. temperature of 60 microvolts per degree centigrade. The amplifiers can be slewed at a rate of 100 volts per microsecond.

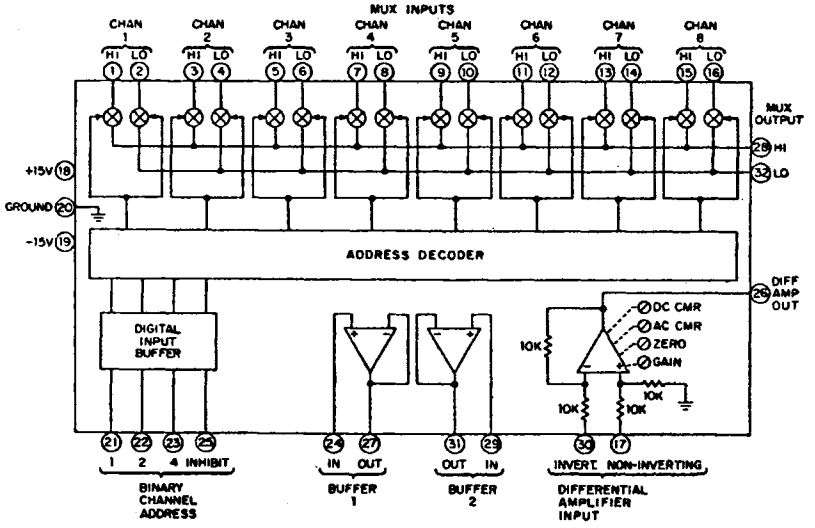
The entire 8-channel differential multiplexer is completely encapsulated in a 2"X2"X.375" module with dual in-line pinning (0.1" grid) and requires only ±15 volts at ±20 mA max for power.

8 CHANNEL DIFFERENTIAL–ANALOG TIME SHARING, WITH THREE OUTPUT AMPLIFIERS

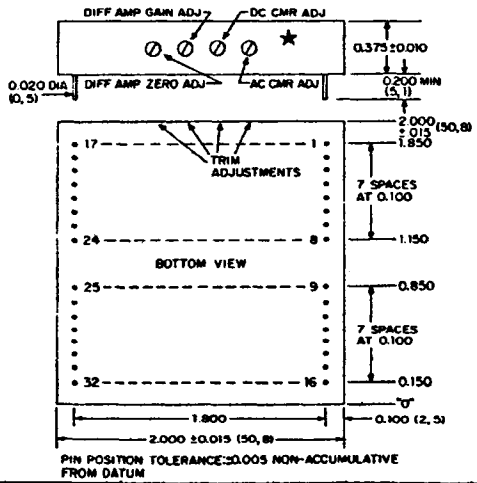
FEATURES

- ☐ Differential Output Amplifier . . . . . ±10mA Drive
- ☐ High Transfer Accuracy 0.01%
- ☐ Fast Settling Time . . . . . 4μsec, incl. ampl.
- ☐ Break-Before-Make Switching
- ☐ Parallel Pin alignment with MM-16 16 channel multiplexer for simple PC board dual pinning as a single-ended option.

BLOCK DIAGRAM



MECHANICAL DIMENSIONS — INCHES (MM)



★ **Note:**

Correct sequence of adjustments should read (left to right):

AC CMR ADJ
DIFF AMP ZERO ADJ
DIFF AMP GAIN ADJ
DC CMR ADJ

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	CHANNEL 1 HI INPUT	17	DIFF. AMP. POS. IN
2	CHANNEL 1 LO INPUT	18	+15V POWER
3	CHANNEL 2 HI INPUT	19	–15V POWER
4	CHANNEL 2 LO INPUT	20	PWR & SIG. GND
5	CHANNEL 3 HI INPUT	21	ADDRESS INPUT 1
6	CHANNEL 3 LO INPUT	22	ADDRESS INPUT 2
7	CHANNEL 4 HI INPUT	23	ADDRESS INPUT 4
8	CHANNEL 4 LO INPUT	24	BUFFER 1 INPUT
9	CHANNEL 5 HI INPUT	25	ADDRESS INHIBIT
10	CHANNEL 5 LO INPUT	26	DIFF. AMP. OUTPUT
11	CHANNEL 6 HI INPUT	27	BUFFER 1 OUTPUT
12	CHANNEL 6 LO INPUT	28	MUX. HI OUTPUT
13	CHANNEL 7 HI INPUT	29	BUFFER 2 INPUT
14	CHANNEL 7 LO INPUT	30	DIFF. AMP. NEG. IN
15	CHANNEL 8 HI INPUT	31	BUFFER 2 OUTPUT
16	CHANNEL 8 LO INPUT	32	MUX. LO OUTPUT

SPECIFICATIONS (Typical @ 25°C)

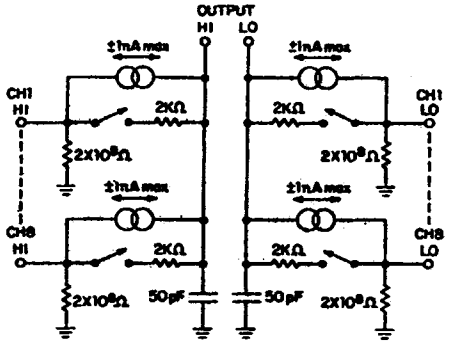
INPUT	
No.# of Inputs	8 channel differential
Input Voltage Range	±10V
Input Overvoltage	±35V max.
Input Impedance	
Without Buffer or Differential amplifier 2k Ohm switch Res. with 50 pf to Gnd. (High & Low inputs)	
With Buffer Amplifier	100 meg Ohms (Channel on) 200 meg Ohms (Channel off)
Leakage	.03 nA typ. from off channels into source (±20V differential)
Channel Select	3 lines straight binary code (1 through 8 channel select)
Inhibit (All channels off)	Logical "0" (negative true)
Input Logic Levels DTL/TTL/CMOS compatible (For TTL compatability use an open collector device with resistor pull up to +5V).	

INPUT CODE	V INPUT MIN.	V INPUT MAX.
"0"	0V	+0.8V
"1"	+4V	+15V

SWITCHING CHARACTERISTICS **(Independent of Amplifier)**	
Switching Time	500 ns typ., 1μSec max.
Sequence Rate	500kHz
Crosstalk	@ 10kHz 1 mv p-p @100kHz 4 mv p-p @1MHz 40 mv p-p

Enable/Inhibit Delay	300 ns Typ.
Break Time (Break before make)	80 ns Typ. to 50% points
Common mode Voltage	Ein Diff + CMV = ±10Vpk
Common mode rejection ratio, At 0 to 100 Hz	Adjustable for both AC & DC to: 110dB with 1KΩ unbalance (Adjustable DC & AC)
OUTPUT AMPLIFIER CHARACTERISTICS	
Output Voltage	±10V max.
Output Current	±10mv. max.
Output Loading	1kΩ in parallel with 1000 pf max.
Gain	1.000 adjustable
Linearity	0.01% of Full Scale
Offset (Vout–Vin)	Adjustable to <±1mV
Offset –VS– Temperature	±60μV/°C
Slew rate	100 V/μs
Settling Time (20 V step in)	4μs to 0.01% of Full Scale
Input Power Requirements	±15V @ ±20 mA max.
PHYSICAL ENVIRONMENTAL	
Operating Temperature	0° to + 70°C
Storage Temperature	–55°C to +85°C
Relative humidity	Up to 100% non-condensing
Size	2" L x 2" W x .375" H
Price (1–9)	$169.00
Mating Socket	DILS-2, 2 req'd per module, $5/pr.

MULTIPLEXER SWITCH EQUIVALENT CIRCUIT

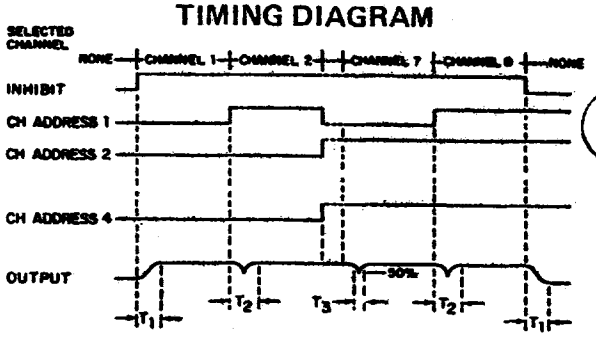


CHANNEL ADDRESSING

4	2	1	INHIB	"ON" CHANNEL
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

FOR EXPANDER OPERATION, CONSULT FACTORY

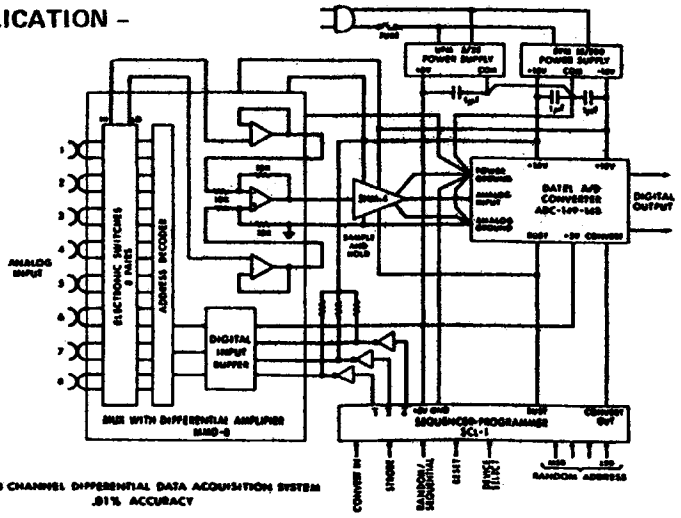
TIMING DIAGRAM



T_1 ENABLE/INHIBIT DELAY	500nsec typ.
T_2 SWITCHING TIME	500nsec typ. 1μsec max.
T_3 BREAK TIME (BREAK-BEFORE-MAKE)	80nsec typ. to 50% points.

TYPICAL SYSTEM APPLICATION –

An 8 Channel, Differential, Noninverting Data Acquisition System, using the MMD-8 along with other off-the-shelf Modules from Datel Systems.



14 BIT, 8 CHANNEL DIFFERENTIAL DATA ACQUISITION SYSTEM .01% ACCURACY

DIFFERENTIAL AMPLIFIER CALIBRATION PROCEDURE

1. Ground both the differential amplifier inverting and non-inverting inputs. Adjust the output to zero volts using the ZERO trim as seen on a DC-coupled scope.
2. Connect both the inverting and non-inverting inputs to a 100 Hz, 20V pk-pk squarewave source referenced to ground. Adjust the DC CMR trim for minimum output on a DC scope.
3. Repeat step 2 but use a 1 kHz sinewave source and adjust the AC CMR for minimum output.
4. Ground the inverting input. Connect the non-inverting input to a 20V pk-pk, 100 Hz sinewave source. Connect the differential inputs of a calibrated scope between the amplifier's non-inverting input and the amplifier output. Adjust the GAIN trim for minimum output on the scope. Note that the GAIN trim is essentially independent of CMR adjustment but the CMR is affected by GAIN adjustments.

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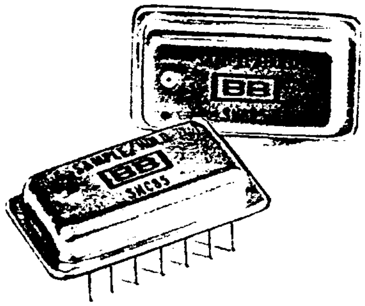


SHC85/SHC85ET

FAST IC SAMPLE-HOLD AMPLIFIERS

FEATURES

- 14 PIN DIP PACKAGE
- 5 μsec ACQUISITION TIME
- COMPLETE WITH HOLDING CAPACITOR
- ±0.01% ACCURACY
- -55°C to +125°C TEMPERATURE RANGE (SHC85ET)

DESCRIPTION

The SHC85 is designed to acquire and hold up to ±10 volt analog signals to an accuracy of ±0.01% of full scale range in 5.0 microseconds for a 20 volt step or 4.5 microseconds for a 10 volt step. Featuring internally compensated circuits normally found only in more expensive and larger sample/holds, the SHC85 offers ultra-linear performance and fast acquisition speeds for the most demanding data acquisition and control applications.

Two models are available; the SHC85 is specified for 0°C to 70°C operation, and the SHC85ET is specified for -55°C to +125°C operation.

The SHC85/SHC85ET are well suited for use in:

Data Acquisition Systems
Data Distribution Systems
Analog Delay Circuits
Pulse Amplitude Modulation Circuits
Waveform Amplitude Measurement

BURR-BROWN
RESEARCH CORPORATION
International Airport Industrial Park • Tucson, Arizona 85734
TEL: 602-294-1431 • TWX: 910-952-1111 • CABLE: BBRCORP

SPECIFICATIONS

Typical at 25°C with rated supply and a 1000 pF internal capacitor unless otherwise noted.

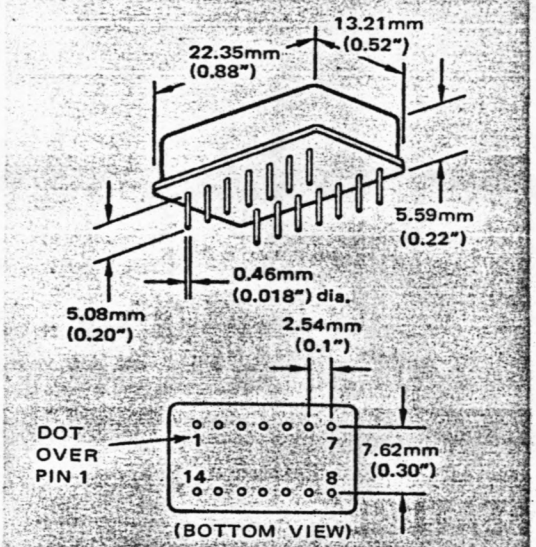
ELECTRICAL

MODELS	SHC85	SHC85ET	UNITS
INPUT			
ANALOG INPUT			
Voltage Range	±10	±10	V
Maximum Safe Input Signal	±15	±15	V
Resistance	10^8	10^8	Ω
Bias Current	50	50	nA
DIGITAL INPUT (TTL Compatible)			
Mode Control	Voltage	Current	
"Sample" - Logic "1"	+2.0V < e < +8V	50 nA	
"Hold" - Logic "0"	0V < e < +0.8V	-50 µA	
TRANSFER CHARACTERISTICS			
ACCURACY (25°C)			
Dynamic Nonlinearity (max)	±0.01	±0.01	% of 20V
@ min. "Hold" Time	1000	1000	µs
Gain	+1.0	+1.0	V/V
Gain Error	±0.01	±0.01	% of 20V
Throughput Offset (max)(adj to zero)	2	2	mV
Droop Rate (max)	0.5	0.5	mV/ms
Droop Rate (typical)	0.125	0.125	mV/ms
Throughput Nonlinearity	±0.005	±0.005	% of 20V
Noise (rms) (10 Hz to 100 kHz)	100	100	µV
Supply Rejection (0 to 50 kHz)	100	100	µV/V
ACCURACY DRIFT			
Gain Drift	±2	±2	ppm of 20V/°C
Offset Drift	±25	±25	µV/°C
Droop Rate(1)			
@ 70°C (max)	10	10	mV/ms
@ +125°C (max)	---	200	mV/ms
DYNAMIC CHARACTERISTICS			
Bandwidth (Full Power)(2)	200	200	kHz
Output Slew Rate	20	20	V/µs
Aperture Time	30	30	ns
Acquisition Time (to ±0.01%)			
10 V Step (max)	4.5	4.5	µs
20 V Step (max)	5.0	5.0	µs
Feedthrough in Hold Mode	±0.005	±0.005	% of step change
Charge Offset (max) @ 0V Input	±2	±2	mV
Sample-to-Hold Transient			
Peak Amplitude	50	50	mV
Settling to 1 mV	0.5	0.5	µs
OUTPUT			
ANALOG OUTPUT			
Voltage Range	±10	±10	V
Current Range	±10	±10	mA
Impedance	0.1	0.1	Ω
TEMPERATURE			
Specification	0 to +70	-55 to +125	°C
Storage	-55 to +125	-55 to +125	°C
POWER SUPPLY			
Rated Voltage	±15	±15	VDC
Range	±14.5 to ±15.5	±14.5 to ±15.5	VDC
Current	±13	±13	mA
PRICES (1 - 9)	$65.00	$89.00	
(100 up)	49.00	67.00	

Prices and specifications subject to change without notice.

(1) Doubles every 10°C over temperature.
(2) Small signal bandwidth is 3 MHz.

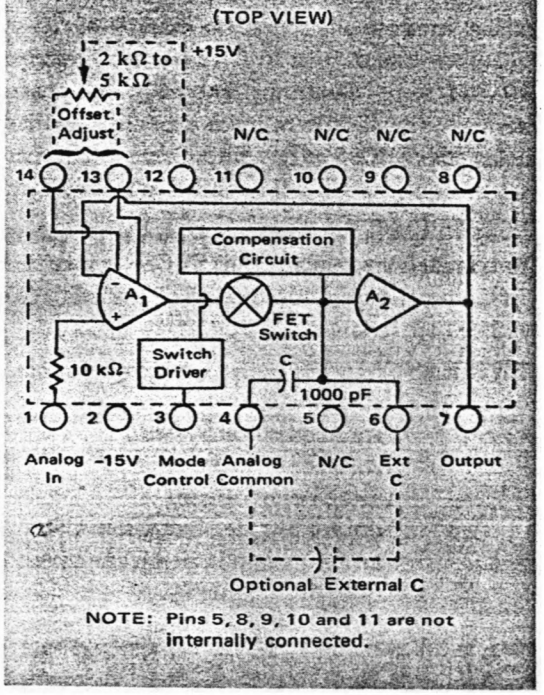
MECHANICAL



Case: Kovar
Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883, (except paragraph 3.2)

Mating Connector: 0145 MC

CONNECTION DIAGRAM



NOTE: Pins 5, 8, 9, 10 and 11 are not internally connected.

DEFINITION OF SPECIFICATIONS

DYNAMIC NONLINEARITY

This is the total nonadjustable input to output error. This specification includes throughput nonlinearity and errors due to droop, thermal transients and feedthrough, in short, all errors that cannot be adjusted to zero for a 10 volt input change after a 5 μsecond acquisition time and a one millisecond hold time. Offset errors must be adjusted to zero by the offset control and gain errors must be adjusted to zero by a gain adjustment elsewhere in the system (gain adjust not included in SHC85).

GAIN ACCURACY

The difference due to amplifier gain errors between INPUT and OUTPUT voltage when in the "sample" mode.

DROOP RATE

The voltage decay at the output when in the "hold" mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH

The amount of the input voltage change that appears at the output when the amplifier is in the "hold" mode.

THROUGHPUT - NONLINEARITY

The total charge offset and gain nonlinearity. That is, the inaccuracy due to these two errors that cannot be corrected by gain and offset adjustments. Throughput - nonlinearity is specified over the 20 volt input range.

THROUGHPUT OFFSET

The sum of sample offset and charge offset.

CHARGE OFFSET

The offset that results from charge transferred from the holding capacitor to the gate capacitance of the switching FET. This charge is partially restored by a special compensation circuit when the unit goes into the "hold" mode.

ACQUISITION TIME

The time required for the output to settle to its final value within a given error band, when the Mode control is switched from "hold" to "sample". See Figure 2.

APERTURE TIME

The time required to switch from "sample" to "hold". The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

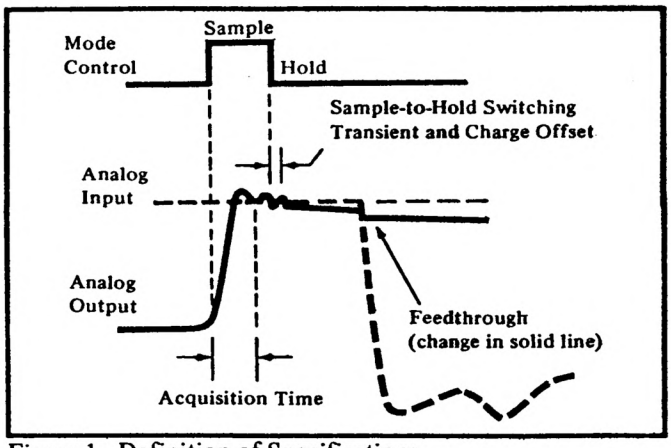


Figure 1. Definition of Specifications.

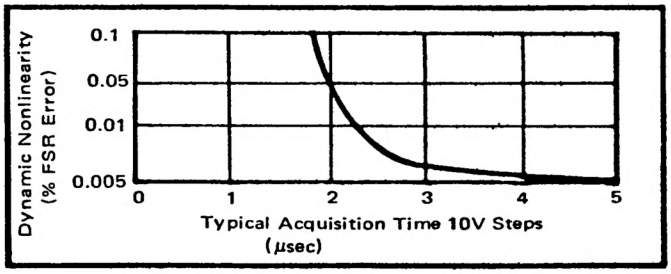


Figure 2. Acquisition Time vs. Full Scale Range Error.

OPERATING INSTRUCTIONS

OPTIONAL EXTERNAL CAPACITOR SELECTION

The value of the external capacitor determines the droop, charge offset and acquisition time of the sample/hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table.

Fig.3 shows the behavior of acquisition time with added external capacitance. The behavior of droop with external C is determined by:

$$\text{Droop} = \frac{dv}{dt} = \frac{0.5 \times 10^{-9}}{1000\ \text{pF} + C_{ext}}$$

Capacitors with high insulation resistance and low dielectric absorption, such as teflon or polystyrene should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize leakage currents from the capacitor; this will minimize droop errors.

OFFSET ADJUSTMENT

Connect a 2k to 5k ohm multi-turn potentiometer with a TCR of 150 ppm/°C or less as shown in the Connection Diagram. The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the "sample" and the "hold" mode. The error should then be adjusted to zero where the unit is in the "hold" mode. In this way, charge offset as well as amplifier offset will be adjusted.

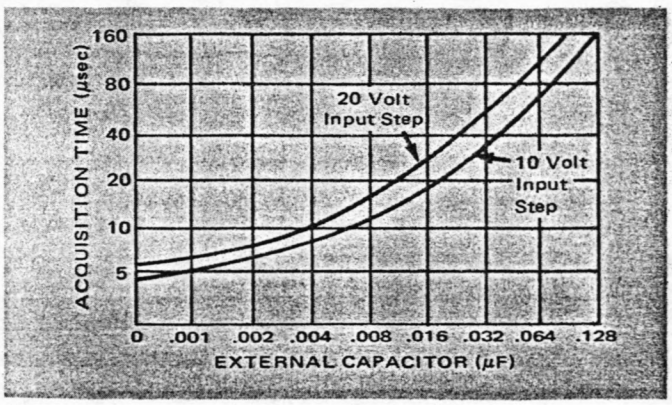
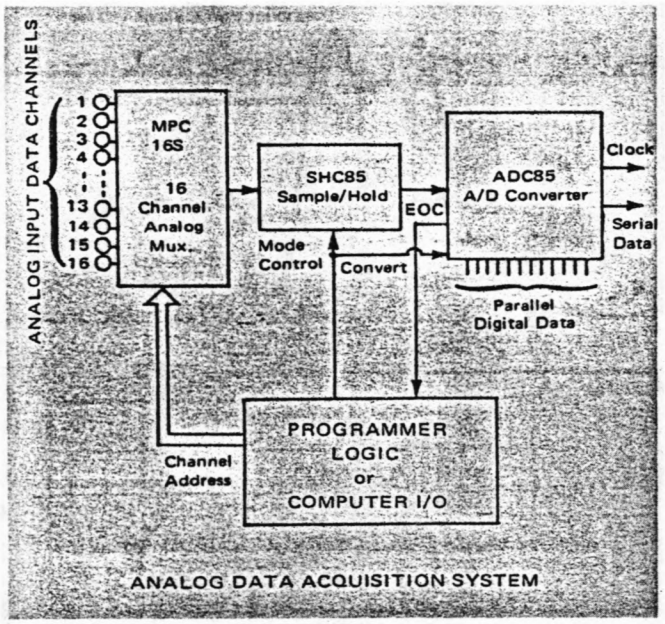


Figure 3. Acquisition Time vs. External Capacitor.

APPLICATIONS

DATA ACQUISITION SYSTEM

The SHC85 makes an excellent device for reducing aperture time in a data acquisition system. When combined with Burr-Brown's 16 channel MPC-16S Analog Multiplexer and ADC85 10 or 12 bit A/D Converter, you can have a compact 16 channel data acquisition system with 50 kHz to 65 kHz throughput sampling rates and 0.02 percent (RSS) system accuracy.



SIMULTANEOUS SAMPLE/HOLD

Time correlation of sampled data signals may be implemented by using one sample/hold for each analog signal prior to input to an analog multiplexer. The SHC85 low aperture time of 30 nanoseconds practically eliminates channel-to-channel time slew. The throughput sampling rate and the number of data channels will determine the maximum HOLD time and hence, the worst case droop error of the sample/hold in the last channel to be sampled prior to the next "refresh" or sample/hold command. This droop error may be minimized by adding external capacitance to the SHC85 as shown in Figure 3, page 3.

The droop error is computed by:

$$\text{MAX DROOP ERROR (CHANNEL N)} = (T \times n)(\text{Droop rate})$$

$$\text{Where } T = \frac{1}{\text{System Sampling Rate}} \text{ and}$$

n = number of multiplexer data channels

EXAMPLE:

For a 10 bit, 32 channel system with throughput sample rate of 50 kHz, assuming no external capacitance, the droop error of channel N is:

$$\text{Droop Error}(E_D) = \left(\frac{1}{50k} \times 32\right)(500 \times 10^{-3}) = 320\,\mu V$$

For ±10 volt input signal range and 10 bit resolution, the resolution of ±½ LSB is ±9.77 mV. This droop error is less than 0.016 LSB (negligible), and no external C need be added to reduce the droop of the SHC85.

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Printed in U.S.A.

1702A

2K (256 x 8) UV ERASABLE PROM

1702A-2	0.65 us Max.
1702A	1.0 us Max.
1702A-6	1.5 us Max.

- **Fast Access Time: Max. 650 ns (1702A–2)**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **All 2048 Bits Guaranteed* Programmable: 100% Factory Tested**
- **Static MOS: No Clocks Required**
- **Inputs and Outputs DTL and TTL Compatible**
- **Three-State Output: OR-tie Capability**

The 1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The 1702A undergoes complete programming and functional testing prior to shipment, thus insuring 100% programmability.

Initially all 2048 bits of the 1702A are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit location. The 1702A is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the 1702A to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

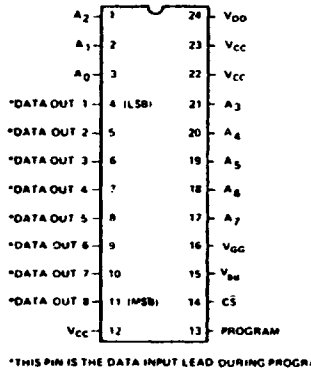
The circuitry of the 1702A is completely static. No clocks are required. Access times from 650ns to 1.5μs are available. A 1702AL family is available (see 1702AL data sheets for specifications) for those systems requiring lower power dissipation than the 1702A.

A pin-for-pin metal mask programmed ROM, the Intel 1302, is also available for large volume production runs of systems initially using the 1702A.

The 1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONFIGURATION

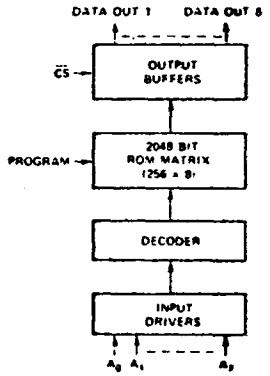


*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

PIN CONNECTIONS

The external lead connections to the 1702A differ, depending on whether the device is being programmed or used in read mode (see following table). In the programming mode, the data inputs 1-8 are pins 4-11 respectively. *The programming voltages and timing are shown in the ROM and PROM Programming instructions section, page 3-55.*

MODE \ PIN	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})	24 (V_{DD})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}	V_{DD}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG}	GND	GND	Pulsed V_{DD}

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to -20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . -48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = -9V ±5%, V_{GG} = -9V ±5%, unless otherwise noted.

READ OPERATION

Symbol	Test	1702A, 1702A-6 Limits Min.	Typ.[1]	Max.	1702A-2 Limits Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			1			1	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1			1	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{IH2}
I_{DD1}[1]	Power Supply Current		35	50		40	60	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD2}	Power Supply Current		32	46		37	55	mA	$\overline{CS}$ = 0.0V, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD3}	Power Supply Current		38	60		43	65	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 0°C, Continuous
I_{CF1}	Output Clamp Current		8	14		7	13	mA	V_{OUT} = -1.0V, T_A = 0°C, Continuous
I_{CF2}	Output Clamp Current		7	13		6	12	mA	V_{OUT} = -1.0V, T_A = 25°C, Continuous
I_{GG}	Gate Supply Current			1			1	μA	
V_{IL1}	Input Low Voltage for TTL Interface	-1		0.65	-1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}-6	V_{DD}		V_{CC}-6	V	
V_{IH1}	Addr. Input High Voltage	V_{CC}-2		V_{CC}+0.3	V_{CC}-2		V_{CC}+0.3	V	
V_{IH2}	Chip Sel. Input High Volt.	V_{CC}-2		V_{CC}+0.3	V_{CC}-1.5		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	-2.0			-2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		-3	0.45		-3	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		3.5	4.5		V	I_{OH} = -200μA

Note 1: Typical values are at nominal voltages and T_A = 25°C.

A.C. Characteristics

T_A = 0° C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5% unless otherwise noted

Symbol	Test	1702A Limits Min.	1702A Limits Max.	1702A-2 Limits Min.	1702A-2 Limits Max.	1702A-6 Limits Min.	1702A-6 Limits Max.	Unit
Freq.	Repetition Rate		1		1.6		0.66	MHz
t_{OH}	Previous Read Data Valid		0.1		0.1		0.1	μs
t_{ACC}	Address to Output Delay		1		0.65		1.5	μs
t_{CS}	Chip Select Delay		0.1		0.3		0.6	μs
t_{CO}	Output Delay From $\overline{CS}$		0.9		0.35		0.9	μs
t_{OD}	Output Deselect		0.3		0.3		0.3	μs

Capacitance* T_A = 25°C

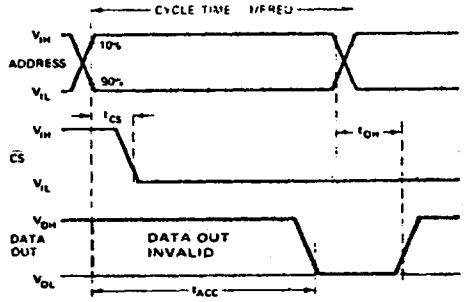
SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$ — All unused pins
C_{OUT}	Output Capacitance	10	15	pF	$V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — are at A.C. ground

*This parameter is periodically sampled and is not 100% tested.

Switching Characteristics

Conditions of Test:
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns
Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD}≤15 ns), C_L=15pF

A) READ OPERATION



B) DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION

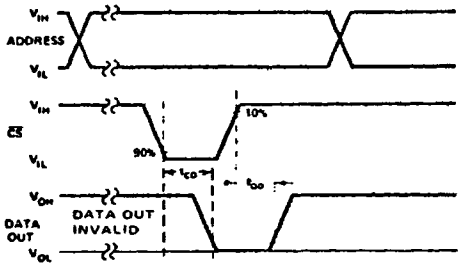
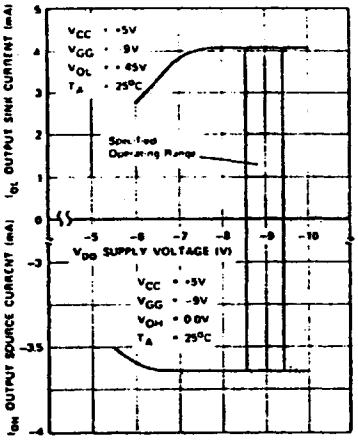


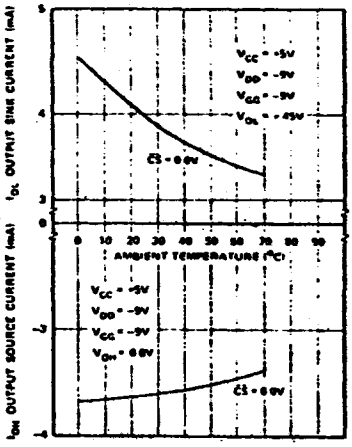
PHOTO ROM

Typical Characteristics

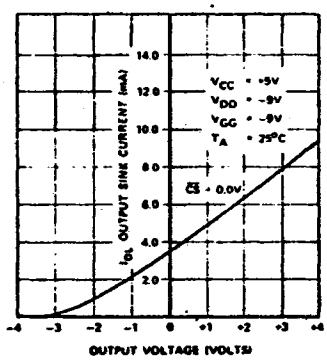
OUTPUT CURRENT VS.
V_{DD} SUPPLY VOLTAGE



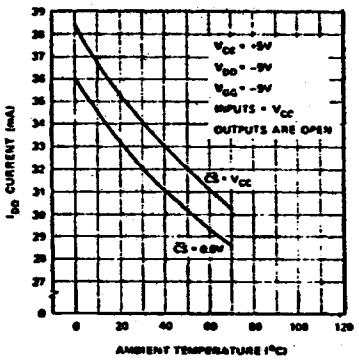
OUTPUT CURRENT VS.
TEMPERATURE



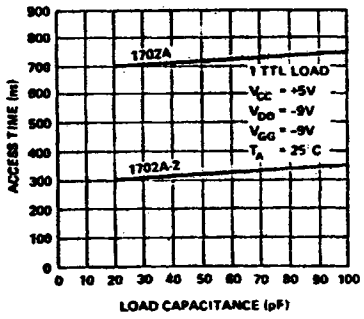
OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE



I_{DD} CURRENT VS. TEMPERATURE



ACCESS TIME VS.
LOAD CAPACITANCE



ACCESS TIME VS.
TEMPERATURE