VLA Technical Report No. 32

VLA ELECTRONICS SYSTEM MANUAL FOR THE VARIABLE PHASE SAMPLER TYPE D1

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1.4 Component Omissions

The following components must be disconnected during module test and may, therefore, be omitted during intial assembly:

Quadrature network - C23, C24, C25, C33, L1, L2, L3, L4, R45, R46, R52, and R53.

Subminiature cables - 4 cables from J5 and J6 to BR1 through BR4.

1.5 Test Adapters

1.5.1* A toggle switch adapter to provide manual control in place of U23 or a serial data generator and clock to generate commands into U23. Used in the Variable Phase Shifter tests.

1.5.2 A modified MC10231 to provide self-toggling. Pins 3 and 7 connected together and through a 470 ohm resistor to pin 8. Used in the Digital Retiming tests.

1.5.3* Output loads. The output signals on P1-5, 6, 38 and 39 are ECL levels requiring biased loads and a convenient connection for scope monitoring.

1.5.4* Heat sinks were required in lieu of forced air cooling on the MC 1650 comparators IC's. Failure rates were high on the first lot but a recent lot of chips (from Korea) have less dissipation and better reliability.

1.5.5 Four 50 ohm coax test cables with BNC connectors on one end. Two cables should have exposed conductors on one end and the other cables should have a 51 ohm resistor between the exposed conductors. Type RG 188/U cable preferred. Used for Quadrature Network Amplifier and Variable Phase shifter checks.

1.5.6* A divide-by-two circuit fed from the 100 MHz clock and providing a variable output of 5 to 50 mV. Required for Minimum Detectable Signal tests.

1.5.7* An adjustable reference voltage source that replaces U5 to provide a vernier controlled voltage of about -80 to +80 mV into pins 1, 7, 8 and 14. Required for Sampler and Minimum Detectable Signal checks.

1.5.8* An ECL AND -gate to accept a 100 MHz clock and an output from the unit under test. The gate output must drive a 50 MHz counter. This adapter is required for the Threshold Level Adjustment.

1.5.9* All items marked with * are not needed if the sampler test fixture is used.

* See step 1.5.9

2. OVERALL DESCRIPTION

The Variable Phase Sampler receives on IF band of 1 to 50 MHz or less from an IF Amplifier module, generates two signals having a 90^{o} phase difference, detects the polarity of both signals with respect to a positive and negative reference voltage at the time of sampling and transmits this information in the form of logic levels to the digital delay system. The sampling pulse is adjustable in 16 time increments over a 10 ns clock period on command from the system controller. The sampled levels are retimed in the digital section to remove the timing variations. Figure 1. shows a block diagram.

The nominal IF input level to J1 is 1.5 V rms, and from this level an ALC signal is generated for controlling an attenuator located in the IF Amplifier module. A dc level of 5 V nominal is also fed to the output plug for monitoring the IF level. Trim pots are provided for setting both levels. The IF input also feeds amplifiers driving a quadrature network to generate sine and cosine components. Each component is sampled by two diode switches driven by the gating pulse. The sampled levels enter A-to-D comparators where comparisons are made with a plus or minus reference level. The ECL outputs are determined by the polarity of the sampled signal with respect to the reference. The dc reference levels are set by trim pots to produce threshold voltages at 61% of the rms noise voltage.

The 100 MHz sine wave clock input to J2 should be between +5 and +15 dBm into 50 ohms. This clock feeds the output logic directly and is also phase shifted to provide a variable phase sampling pulse. The phase shift input data is in TTL serial form and is clocked in at a 2.5 MHz rate. Logic zero commands produce maximum delay of the sampling pulse so that increasing logic numbers are equivalent to increasing signal delay. The LSB is fed back to the Controller for verification.

The digital portion of the unit performs the functions of retiming the variable timed logic signals from the comparators, allows interchanging of the positive and negative threshold data for both sine and cosine signals, and permits disabling both positive and/or negative threshold data for system tests. The polarity data is interchanged in synchronism with phase switching at the antennas to reduce modem and sampler errors. The four ECL logic level outputs, one for each reference level discriminator, drive 50 ohm lines to the delay and multiplier system. Pull-down loads must be

provided externally. A delay monitor circuit produces a dc level proportional to the time between delayed and non-delayed clocks. This output to P1 permits a check of the unit's response to phase shift commands.

2.1 Input-Output Connections

J1 - IF Input
J2 - 100 MHz Clock Input

P1- 1 Gnd
2 LSB out
3 Serial clock in
4 Serial delay data in
5 Sin - out
6 Sin + out
8 Leveler out
9 Gnd
10 +5 V
11 -5.2 V
14 Level monitor out
15 Gnd
19 -12 V
29 +28 V
34 Gnd
36 Delay monitor out
37 Gnd
38 Cos - out
39 Cos + out

2.2 Power Supply Requirements

V	+28	+5	-5.2	-12	volts
I	580	150	1400	50	mA

2.3 Control Word Input (P1-4)

1 22.5^{o} LSB
2 45^{o}
3 90^{o}
4 180^{o} MSB
5 -Disable
6 + Disable
7 Invert

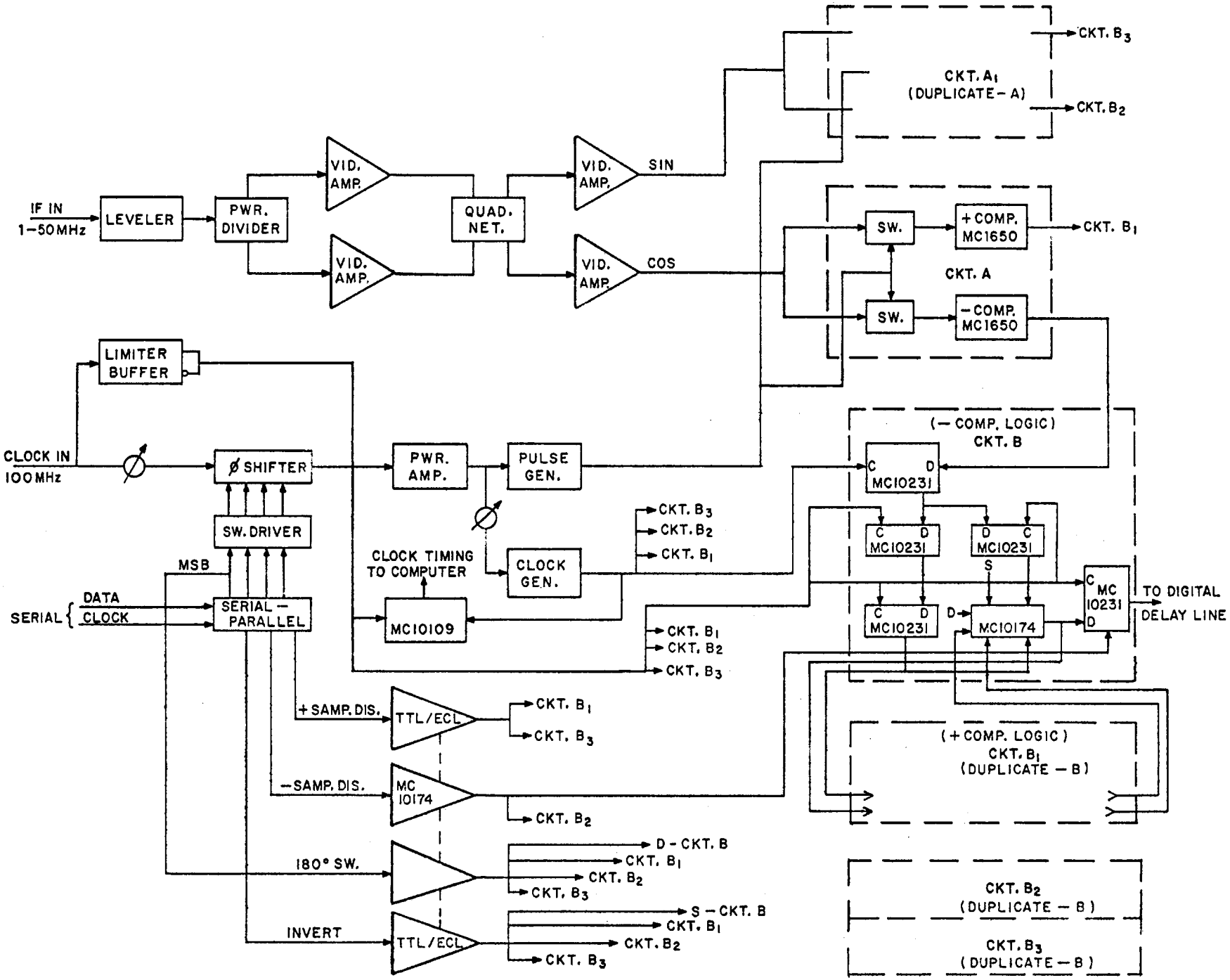


FIG.-1 VARIABLE PHASE SAMPLER

3. CIRCUIT DESCRIPTION

An IF input signal of 1.5 V rms feeds a leveling detector and inverting transformer. Refer to the schematic. The detector (CR1) develops 1 V dc into two op amps. One amplifier (U2A) generates a 5 V output for level monitoring. The second amplifier (U2B) is an integrator to produce a gain control voltage fed back to a buffer and attenuator in the IF Amplifier module. The IF level is set by adjusting R19, the reference input to U2B. R47 is then set for a 5 V monitor level.

Input transformer T1 has a floating secondary winding so that the two amplifier input impedances determine the relative amplitude and phase. The resulting voltages are 2:1 in amplitude ratio and 180^{o} in phase. This is the requirement for the quadrature network drive following the amplifiers. The amplifiers are Darlington circuits with complementary output drivers. Flatness, stability, phase match, low distortion and low output impedance are important in these applications. These circuits provide less than 5 ohms output impedance up to 50 MHz. The in-band flatness is within a few tenths of a dB, rising to about 2 dB near 150 MHz. Harmonic components are at least 46 dB down at 1.5 V rms at 50 MHz. Distortion tends to increase with frequency and amplitude due to slew rate restrictions in the interstage circuit. The quadrature network (L1 to L4 and associated components) develops two signals having 90^{o} relative phase with a theoretical error of less than 0.2^{o} from 0.95 to 55 MHz. In practice the errors can normally be adjusted to less than 0.4^{o} between 1 and 50 MHz. Most of the components were set near the theoretical values before mounting. The error curve was measured using a modified HP 8405 vector voltmeter. See VLA Electronics Memorandum No. 132 for more details. The amplifiers following the network are similar to the previously described circuits. These require high input impedance and must drive two 50 ohm cables each.

A 100 MHz, +5.5 dBm sine wave clock input to J2 drives a squaring buffer, U13, in the digital section and the phase switching circuits following T2. A 50 ohm plug-in phase network is used for clock timing adjustment. A serial-to-parallel converter, U23, receives delay data and a 2.5 MHz clock from the System Controller. The data controls the phase shift, interchanges the digital outputs from the positive and negative samplers and permits disabling both positive and both negative samplers for tests. Following U23 is U1, a Norton input quad op amp used as a switch driver.

Low or "0" TTL inputs to U23 produce low inputs to U1 to generate +4 V drive to the diode switch circuitry, turning on the inductor side of the networks. Increasing serial numbers produce a phase advance in the clock, equivalent to a delay of the signal. The 180^{o} step is obtained from transformer T2. The remaining shifts are developed in parallel RL-RC circuits which have the advantages of constant resistive loading on the driving circuit and equal output levels. These networks should be accurate to less than 4^{o} and 0.6 dB per section and have less than 10^{o} and 1.1 dB error between the worst case combinations of phase settings.

The phase shift circuit drives a power amplifier to develop 0.5 W (5 V) into 50 ohms. A small amount of power is tapped off through a matching network and 75 ohm circuit to become the delayed clock. The plug-in phase network allows timing adjustment of the clock to the first flip-flops following the comparators with respect to the gate pulse.

The primary output of the power amplifier drives a matching network and two step recovery diodes, Cr 29 and 30. These diodes with appropriate biases convert the 100 MHz sine wave into a 1.8 ns, 9.6 V positive pulse loaded by two 95 ohm cables. Both pulse amplitude and width are controlled by the bias voltages. The voltages are set with R94 and R155 and regulated by the associated op amp circuits. Typical voltages are +10 V on CR 29 and -1.9 V on CR 30. The 95 ohm cables are of equal length to preserve timing accuracy. They terminate in the bridge switch circuits where each one is divided and fed through isolating transformers to provide a balanced drive to the diode bridges.

The sampling circuits consist of a diode bridge switch and MC 1650 high speed comparator. The cos + circuit will be used in the following references as an example of operation for all four parallel signal paths. The bridge (BR1) is turned on for about 1.8 ns by the gate pulse from the pulse generator. The gating is via a balancing transformer (T3) that supplies an isolated current pulse through the diodes. During conduction a charge accumulates on the .022 uf capacitors (C56 and 57) at the transformer input. After the pulse ends this charge flows through the self-bias circuit (R95, CR11, R96, R106, etc.) paralleling the bridge. The resulting voltage reverse biases the bridge by about $\pm$ 3.6 V to prevent diode conduction at peak signal level. A part of this voltage (approximately 3 V) is fed through the summing op amp U4A for monitoring at a front panel test point.

This allows a check on bias and indirectly on the gating pulse without disturbing operation. Some signal leakage through the bridge is possible due to diode capacitance. This problem is reduced by bypassing the center diode junctions via R95, R105, CR11, CR12, C64 and C70.

The gated signal out of the bridge feeds the MC 1650 comparator (U6A) where it is compared with a positive dc reference voltage set near 61% of the rms signal level. The reference level is set by R124 and regulated by op amp U5A. A recovery circuit (CR19, 20 and R164) on the signal line returns the voltage during gate off time to a level near threshold. This reduces errors due to a level far from threshold at one gate time influencing a small level on the other side of threshold at the next gate time; that is, the memory or hysteresis tendency is reduced. Large excursions toward signal peaks during gate time are limited by the switching current. The sampling pulse does not cancel out completely in the bridge due to a transformer characteristic. The result is a small 100 to 150 mV peak 1 ns wide leakage pulse into the comparator. This leakage is used to an advantage by setting the timing of the delayed clock to U8 to coincide with the appearance of the pulse or its effects at the comparator output. The MC 1650 has 15 mV of dc hysteresis at its input which limits the threshold detection accuracy. This error can be largely overcome by introducing a controlled amount of gate leakage.

The comparators detect signal polarity with respect to the threshold level at gate time. The gate, having been generated from the variable phase shifted clock, is out of step with the clock input at J2. To retime the digital signal the comparator output is first captured by delayed clock which is time fixed with respect to the gate pulse. The 75 ohm plug-in phase shift network sets this timing for the most sensitive capture by the U8A flip-flop. This occurs when the gate leakage residue arrives from the comparator. The following flip-flops, U8B and U14, are clocked by the reference clock. When the serial delay data into U23 is in the 0000 to 0111 range the signal path is selected through U8B and U14B by U18A. For delays of 1000 through 1111 the path is through U14A. Path selection is made by the MSB data through U23 and U22A.

The positive and negative sampler data can be interchanged by U18. The command for this function also comes into the unit as part of the serial

data, out of U23-4 and is converted to ECL by U22B. This function permits phase switching at the antenna and in this circuit to reduce spurious IF and sampler offset errors.

FOR L35 to 40:
ONE FERROX CUBE
56 590 65/4B
BEADS ON TRANSISTOR EMITTER LEADS.

SIGNAL INPUT J1

T1
5 TURNS # 37 TRIFILAR
STACKPOLE 57-0372
GRADE 24 CORE

75Ω CABLE

150Ω CABLE

*VARIABLE CAPACITOR C24,C23,C25,C33 HAVE CAPACITOR IN PARALLEL TO BE SELECTED DURING TESTING

+28V

AB BEAD L41

Q1 2N6305
Q3 2N5109
Q4 2N5583

AB BEAD L42
Q10 2N5109
Q11 2N5583

AB BEAD L43
Q5 2N5109
Q6 2N5583

AB BEAD L44
Q12 2N5109
Q13 2N5583

OSM TEST POINT J5

OSM TEST PT J6

12"CABLE

50Ω

330 L22

330 L23

L59 L3

574 L4

BR1 A2X919 (4)
BR2 A2X919 (4)
BR3 A2X919 (4)
BR4 A2X919 (4)

COS+
COS−
SIN+
SIN−

HP 2810 (2)

LM324 U4A
LM324 U4B
LM324 U4C
LM324 U4D

TP1 ON FRONT PANEL
TP2 ON FRONT PANEL
TP3 ON FRONT PANEL
TP4 ON FRONT PANEL

HP2835 (2)
CR19 CR20
CR21 CR22
CR23 CR24
CR25 CR26

1650 COMPARATOR
U6A U6B U7A U7B

TRANSFORMERS T3−T6
8 TURNS # 38 BIFILAR
STACKPOLE 570184
GRADE 5N CORE

LM324 U5A
LM324 U5B
LM324 U5C
LM324 U5D

HP-2810 (2)
Q21 MM8001

U8A U8B U16A U16B U17A U17B U18A U18B U19A U19B U1A U1B U12

U23-10 180° BIT
U23-4
U23-8
U23-5

DELAY MON PI-36

75Ω Ø SHIFT NET

TRW CA860 RF AMPLIFIER

3 TURNS #24 L21 .125 DIA.

CLOCK IN J2

U13 Q22 MM8001

U20A U20B U21A U21B U22A U22B U22C U22D

COS+ PI-39
COS− PI-38
SIN+ PI-6
SIN− PI-5

PI-39 PI-38 PI-6 PI-5

PI	
1	GND
2	LSB OUT
3	CLK IN
4	SERIAL IN
5	DIG SIG OUT
6	DIG SIG OUT
7	
8	LEVELER OUT
9	GND
10	+5V
11	−5.2V
12	
13	
14	MON LEVEL OUT
15	GND
16	
17	
18	
19	−12V
20	
21	
22	
23	
24	
25	
26	
27	
28	+28V
29	
30	
31	
32	
33	
34	GND
35	
36	DELAY MON
37	GND
38	DIG SIG OUT
39	DIG SIG OUT
40	
41	
42	

LEVEL MONITOR OUT PI-14 PI-15

LEVEL CONTROL VOLTAGE TO ATTEN IN I.F. MODULE PI-8

CR6 IN4742 12V ZENER

+12V PI-9

50Ω Ø SHIFT NET
8 TURNS #36 TRIFILAR
1041T060/4C4 CORE

U22A-7 MSB
U22C-10 NEG DISABLE
U22D-11 POS DISABLE
U22B-5 SERIAL IN
CLOCK IN
PI-4
PI-3
PI-1
74164 U23

LSB PI-2 (BACK CONN)

22.5° PHASE SHIFT
180° PHASE SHIFT
90° PHASE SHIFT
45° PHASE SHIFT

LM 3900 U1A U1B U1C U1D

10V IN4740 ZENER

Q18 2N3904
Q26 2N3906

A4X288 (2)

NOT USED: Rs 83, 107, 99, 112, 115

LAST REF DESIG USED							
C	CR	L	Q	R	T	U	
140	31	30	22	237	7	22	

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
B	8/1/77	D.D. Rouse	CRP	CHANGED CLOCK PULSE AMPLIFIER TO TRW CA860 AND INPUT CIRCUIT AT U8A.
A	6/28/76	D.D. Rouse	CRP	REMOVED R88, R86, R87, R113, R115 ADDING R68, R2, R90, R124, R125, R126, R127 & R117. ALL OF THE ABOVE.

VLA SAMPLER

VARIABLE PHASE SAMPLER

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

DRAWN BY C. PACE, S. ROUSE — DATE 11/17/75
DESIGNED BY Bob MAUZY — DATE
APPROVED BY CRP — DATE 5-3-76

SHEET NUMBER
DRAWING NUMBER D13500S2 REV. A
SCALE

4. TEST AND ADJUSTMENT PROCEDURE *

4.1 Leveler

Apply a 1.5 V rms (+16.5 dBm) noise signal of 1 to 50 MHz bandwidth to J1. Adjust IF level control, R19, until the output of U2B (P1-8) comes out of saturation. The amplifier will remain unsaturated only a short time because of the very high gain and absence of feedback. Set R47 for 5 V out U2A (P1-14).

4.2 Quadrature Network Amplifiers

Attach temporary test cables to the driving amplifier outputs at C15 and C18. Feed a sweep generator into J1. The level out of the 75 ohm amplifier will be -3.5 dB and out of the 150 ohm amplifier +2.5 dB. Observe and record the shape of these gain curves out to about 200 MHz. The shapes should be within $\pm$ 0.2 dB from 1 to 50 MHz and $\pm$ 0.4 dB to 100 MHz.

Attach terminated cables to the inputs of the output amplifiers at C37 and C39. The output levels at J5 and J6 should show 0 dB gain in the 1 to 50 MHz range and have similar shapes. The responses should meet the same requirements for match as the input amplifiers.

(If a rapid automated procedure is developed for adjusting the quadrature network, it may be reasonable to omit the amplifier checks except in those cases where the network cannot be adjusted to the required accuracy.)

4.3 Quadrature Network Components

On the first units built network components were set to calculated values derived from the theoretical values with corrections for inductor shunt capacitance and p.c. land capacitance. When installed and measured the components required some changes to shift the phase curve and reduce ripple. The method used for checking phase was not considered satisfactory for future testing because of the time involved though accuracy was good. A vector voltmeter was connected to J5 and J6 for the measurements. More information is available in VLA Electronics Memorandum No. 132. Even with an automated measurement procedure it is believed to be very desirable, possibly necessary to measure, adjust, and/or select components to match standards before installation.

* See section 5 for description and use of the automatic test fixture.

An important, unsolved problem concerning phase accuracy is the error introduced by the sampling circuits. Errors introduced there degrade the performance of the network considerably. An automated measurement system making use of the digital outputs should give a better indication of overall performance but may lead to misadjustment and condemnation of the network for errors introduced elsewhere.

The network components should now be mounted and the 12-inch 50 ohm subminiature cables installed.

4.4 Variable Phase Shifter

Install a jumper plug-in (0^{o} phase shift) in the 50 ohm phase shift network socket. Disconnect one end of C63 and connect a coax test cable to Q15 collector. Provide a 100 MHz sine wave +5.5 dBm clock into J2. The clock should come through a vector voltmeter (VVM) reference tee probe (A) and a fixed attenuator of at leat 10 dB (attenuator between probe and J2 to reduce reflections). Install a manual switch adapter in place of U23 or provide for external control of commands into U23. Connect the coax test cable to the terminated test probe (B) of the VVM. Insert and remove each phase step, verify that logic "1" inputs produce a phase advance, and record the phase and amplitude errors including polarity. The errors for any one step should not exceed 4^{o} and 0.6 dB. The worst case combinations of settings should produce error differences of less than 10^{o} and 1.1 dB. The average output level should be between -8 and -9 dBm. Remove the test cable and connect C63.

4.5 Pulse Generator

Apply power and adjust R155 for 10 V at the junction of R140 and R141. Set R94 for -1.9 V at the junction of R170 and R171. Apply the 100 MHz clock to J2. Using a sampling scope with a 500 or 5 K ohm probe held at the junction of the two 95 ohm cables observe the sampling pulse. It should be about 9.6 V in amplitude and 1.8 ns wide. Change R94 and R155 to change width and amplitude. See Figure 3.

4.6 Samplers

The following tests will refer to the cos +circuit but apply to all samplers:

4.6.1 Remove U5 and insert a test fixture to supply an adjustable reference voltage of about +80 to -80 mV to pins 1, 7, 8 and 14. The pins can be connected and fed simultaneously. With the sampling pulse

present measure the self-bias voltages at R96 and R106. They snould be positive and negative, respectively, and between 2.7 and 3.3 V. Check that the voltage at TP1 is their absolute sum within 7%.

4.6.2 Remove U8. Using a sampling scope with a probe of 500 ohms or more, check the output of U6 pin 2 while varying the reference voltage from the test fixture. The level may change state smoothly or with some snapping action. If the output changes state suddenly, the control voltages required to produce the positive and negative transitions should not differ by more than 10 mV. When near the threshold region a positive pulse due to gate leakage should appear at U6-2 (negative at U6-14). See Figure 4. Set the reference voltage so that the peak of this pulse is about 1/3 the transition amplitude. Replace U8 and select a 75 ohm phase shift network that places the positive transition of delayed clock at U8-6 about 2 ns following the peak of the gate leakage previously observed. (The scope must be externally triggered from the clock for these tests.)

Note: During recent tests on a very similar circuit operating at 70 MHz clock rate but having the same sampling pulse amplitude, width and same gate leakage into the comparator the output pulse was less dominant. When the leakage peak was adjusted to 1/3 the transition voltage the trailing part of the pulse frequently did not return all the way to the original state. With the reference moved to increase the pulse peak to 1/2 the transition, the level would part-time continue on to the high state rather than trail off toward the low state. No snap action or hysteresis was present in any of the 20 comparators. Clock time was set about 2 ns ahead of the leading edge of the pulse and minimum detectable signal was somewhat lower. Less dissipation was noticed in the comparator chips, so it is believed that the MC 1650's have been changed.

4.7 Minimum Detectable Signal

Apply a 50 MHz signal to J1 that is locked to the 100 MHz clock. Set the level for about 20 mV rms. Set the variable phase shifter delay so that the gate pulse leakage at R231 is centered on the peaks of the input signal also observed at that point. Do not confuse leakage

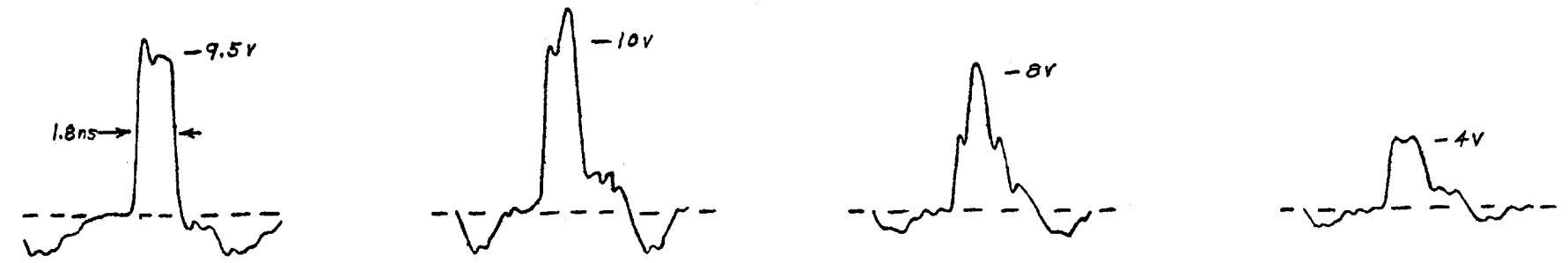
with delayed leakage from BR2 which is 2.8 ns later. While monitoring U8-2 reduce the signal input level until capture is occurring about half the time. (The test adapter reference voltage may be changed to improve sensitivity.) The signal input level shall be less than 15 mV.

4.8 Digital Retiming

Replace U8 with a toggling chip (an MC 10231 with a jumper between pins 3 and 7 and 470 ohms from 3 to 8). Provide enable signals through U23-5 and 6. With the 180° bit in the "0" position select a 50 ohm phase shift network that provides more than 2 ns setup time and more than 1 ns hold time at U8-10 with respect to U8-11 over the delay control range of 0000 to 0111. Also check that for the delay range from 1000 to 1111 the same limits are met for the signal at U14-7 with respect to U14-9. With a pull-down load provided on the logic output, P1-39, a toggling signal should be present at P1-39 for both states of the 180° command. With the invert command initiated at U23 the output should cease toggling. Moving the toggle IC from position U8 to U9 should again provide an output signal. Generate a positive disable command through U23 and see that the output signal is not present. Using the toggling IC, repeat the 180°, invert and disable checks on the remaining channels.

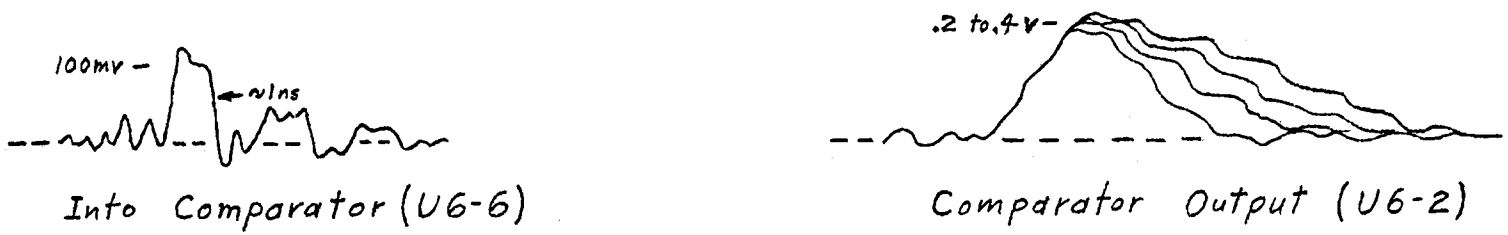
4.9 Threshold Level Adjustment

Replace the test fixture in U5 with the proper IC. Provide a 1.5 V rms 1 to 50 MHz noise spectrum into J1 (the level at which the output of Level Control Amplifier U2B is not saturated momentarily in an open loop condition). Provide an and-gate test fixture with two inputs, one being the 100 MHz clock and the other a logic signal output from P1-39. Adjust the timing by cable length change on one of the inputs so that the minimum width output pulses have maximum width, or set the positive slope of the clock pulse about 2.5 ns after the positive slope of the output signal at the gate input. Feed the test fixture output to a counter. Adjust the threshold level, R124, for a counter reading of 27.024 MHz. Repeat the test for the three remaining outputs.



SAMPLING PULSE WAVEFORMS

FIGURE 3



GATE LEAKAGE

FIGURE 4

5. AUTOMATIC SAMPLER TEST FIXTURE

5.1 Fixture Description

The Automatic Sampler Test Fixture will aid in the test and adjustment of The D-1 sampler. This unit contains:

(1) The power amplifier and filter portion of an IF receiver with a manual gain adjustment.

(2) A mixer used to obtain a 1 to 50 MHz sweep signal of required low distortion level and amplitude flatness.

(3) A digital program word generator.

(4) A digital phase meter.

(5) A digital duty cycle meter.

(6) A wide band noise source.

The top panel of this unit is self explanatory in displaying how to drive the sampler with:

(1) A 1 to 50 MHz flat sweep.

(2) A 1 to 50 MHz wide band noise signal.

(3) A signal from an external source.

The front panel of the test fixture contains these features:

(1) A delay program section to select the 7 bits of the sampler program word via switches. This program word can be either sent automatically each 50 ms or on a push button one shot basis.

(2) Test jacks for a high impedance scope probe to view each of the four sampler ECL digital outputs.

(3) A test meter with function and range controls to display either the duty cycle of any digital output or the phase between the positive or negative bits of the sine and cos digital outputs. An analog jack with the meters driving signal is provided. The overrange lamp must be off for the meter reading to be valid.

(4) Hi and lo ALC lamps that display the conditions of the ALC integrating amplifier.

5.2 Meter Section Switch Functions

5.2.1 Range and Functions These switches determine the scale factor of the meter and meter analog output. With the function switch in sin +, sin-, cos+, or cos- positions only

± 5% and 0 - Vs positions of the range switch are valid. In ± 5% position the meter center position represents a digital duty cycle of 27.0% which is the correct duty cycle for correct threshold adjustment with a wideband input of +16.5 dBm or a sinewave input of +12.9 dBm. An error of 5% in the threshold setting with these inputs will deflect the meter full scale. In 0 and Vs position a constant logic one at a digital output will yield a full scale right meter deflection.

With the function switch in $\phi+$, $\phi-$, or $\phi\pm$ positions the range switch must be in 0 - Vs or $\pm 5^{o}$ positions. The 0 - Vs position will provide meter extremes of 0^{o} and 180^{o} phase and the $\pm 5^{o}$ position puts 90.0^{o} at the meter center position with a $\pm 5^{o}$ range. The $\phi+$ position drives the meter with the phase as measured by comparing the sin+ and cos+ digital outputs whereas the $\phi-$ uses the two negative sampler outputs. The $\phi\pm$ position alternated phase measurement integrations between the two, thus if a sweep generator is driving the sampler input a scope driven from the meter analog jack will display two traces, one for a phase measurement using the positive bits and one using the negative bits.

5.2.2 Long Integration/Short Integration Switch This switch determines the integration time of the phase or duty cycle measurements. Short integration will average measurements over 81.92 µs and long integrations over 655 µs. When sweeping the short integration will yield 200 samples across the scope screen with a 60 cycle sweep rate.

5.2.3 Overrange Lamp In ± 5% or $\pm 5^{o}$ range switch positions the lamp must be out for the meter reading to be valid.

5.3 Test Procedure

5.3.1 Leveler Apply a 1.5 V rms (+ 16.5 dBm) noise signal of 1 to 50 MHz bandwidth to the sampler input. The top panel bnc connectors need only be jumpered correctly and the gain adjustment made with power meter. Adjust IF level control, R19

until the ALC hi and lo lamps just switch between themselves. The longer both lamps remain off when switching from one on to the other on the closer to correct the adjustment is. Adjust R 47 for 5 V out of V2A (P1-14).

5.3.2 Variable Phase Shifter and Pulse Generator Install a jumper plug-in (0^{o} phase shift) in the 50 ohm phase shift network socket, trigger a scope from the signal on pin 16 of plug-in (100 MHz sinewave).

Apply power and adjust R155 for 10 V at the junction of R140 and R141. Set R94 for -1.9 V at the junction of R170 and R171. Using scope with a 500 or 5 K ohm probe held at the junction of the two 95 ohm cables observe the sampling pulse. It should be about 9.6 V in amplitude and 1.8 ns wide. Change R94 and R155 to change width and amplitude. See Figure 3.

Step thru all 16 delays in order 0000 to 1111 using the 4 program bits on front panel of test fixture. Each step should move the pulse by .625 ns $\pm$ .1 ns.

5.3.3 Samplers The following tests will refer to the cos +circuit but apply to all samplers:

5.3.3.1 Remove U5 and insert a test fixture to supply an adjustment reference voltage of about +80 to -80 mV to pins 1, 7, 8 and 14. The pins can be connected and fed simultaneously. With the sampling pulse present measure the self-bias voltages at R96 and R106. They should be positive and negative, respectively, and between 2.7 and 3.3 V. Check that the voltage at TP1 is their absolute sum within 7%.

5.3.3.2 Remove U8. Using a scope with a probe of 500 ohms or more, check the output of U6 pin 2 while varying the reference voltage from the test fixture. The level may change state smoothly or with some snapping action. If the output changes state suddenly, the control voltages required to produce the positive and negative transitions should not differ by more than 10 mV. When near the threshold region a positive pulse due to gate leakage should appear at U6-2 (negative at U6-14). See Figure

4. Set the reference voltage so that the peak of this pulse is about 1/3 the transition amplitude. Replace U8 and select a 75 ohm phase shift network that places the positive transition of delayed clock at U8-6 about 2 ns following the peak of the gate leakage previously observed. (The scope must be externally triggered from the clock for these tests.)

Note: During recent tests on a very similar circuit operating at 70 MHz clock rate but having the same sampling pulse amplitude, width and same gate leakage into the comparator the output pulse was less dominant. When the leakage peak was adjusted to 1/3 the transition voltage the trailing part of the pulse frequently did not return all the way to the original state. With the reference moved to increase the pulse peak to 1/2 the transition, the level would part-time continue on to the high state rather than trail off toward the low state. No snap action or hysteresis was present in any of the 20 comparators. Clock timing was set about 2 ns ahead of the leading edge of the pulse and minimum detectable signal was somewhat lower. Less dissipation was noticed in the comparator chips, so it is believed that MC 1650's have been changed.

5.3.4 Minimum Detectable Signal Apply a sinewave input to the sampler Adjust the signal level until all digital outputs just come out of fixed logic zero (indicating some capturing of samples above the threshold level). The input signal level shall be less than 15 mV.

5.3.5 Digital Retiming Replace U8 with a toggling chip (an MC 10231 with a jumper between pin 3 and 7 and 470 ohms from 3 to 8). Provide enable signals through U23-5 and 6. With the 180^{o} bit in the "O" position select a 50 ohm phase shift network that provides more than 2 ns setup time and more than 1 ns hold time U8-10 with respect to U8-11 over the delay control range of 0000 to 0111. Also check that for the delay range from 1000 to 1111 the same limits are met for the signal at U14-7 with respect to U14-9. With a pull-down load provided on the logic output, P1-39, a toggling signal should be present at P1-39 for both states of the 180^{o} command. With the invert command initiated at U23 the output should cease toggling. Moving the toggle IC from position U8 to U9 should again provide an output signal. Generate a positive disable command through U23 and see that the output signal is not present. Using the toggling IC, repeat the 180^{o}, invert and disable checks on the remaining channels.

5.3.6 Threshold Level Adjustment Replace the test fixture in U5 with the proper IC. Provide a 1.5 V rms 1 to 50 MHz noise spectrum into J1 (the level at which the output of Level Control Amplifier U2B is not saturated momentarily in an open loop condition).

Put test fixture range switch in ± 5% position and with function switch alternately in sin +, sin-, cos +, and cos- position adjust respective threshold pots for a center of screen meter reading with overrange lamp off. Long integration should be used.

5.3.7 Quadrature Network Adjustment Connect the test fixture, VHF oscillator, and sweep oscillator so as to provide the sampler with a 12.9 dBm (2.80 Vpp) 1 to 50 MHz input. Connect a high impedance probe to the meter analog jack and adjust sweep rate (using short integrating) for little or no scope trace flicker. Function switch to

$\phi\pm$, range switch to ±5%. Two traces of dots should be seen on the scope face where 1 volt equals one degree and zero volts is 90^{o}. Adjust all the various network components to obtain best overall overlay of the two traces with minimum deviation from 90^{o} over the 1 to 50 MHz band. Ignore very narrow "blips" along traces that indicate large errors from 90^{o} as these points occur at frequencies where the digital phase measuring technique fails to average out systematic erros. (As for instance where the signal is at 100/N MHz for any interger N).

It may be necessary to change some components in the network to obtain best adjustment. In any event the adjustment has not proven to be difficult and only rare components changes needed. One quickly learns the area's effect of each adjustment and overall adjustment, if the unit is free of problems, should not take over 5 to 10 minutes.

5.3.8 Repeat entire test procedure to eliminate interacting effects.

6. REFERENCE MATERIAL

Data Sheets

50-75 Ω Phase Shift Networks . . . C13500S6*

Motorola MC-1650 Dual A-D Converter

National LM324 Quad Op Amp

National LM3900 Quad Amp

TRW CA860/CA830 Power Amp

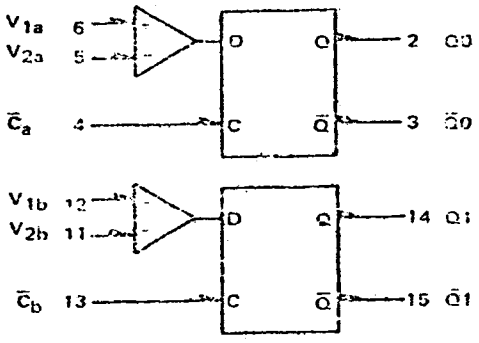
*Not included in Technical Report No. 32 as an attachment. Available through VLA Site Drafting Department.

DUAL A/D COMPARATOR

MC1650 • MC1651

ISSUE

Positive Logic



V_{CC} = +5.0 V = Pin 7,10
V_{EE} = -5.2 V = Pin 8
Gnd = Pin 1,16

- P_D = 330 mW typ/pkg (No Load)
- t_{pd} = 3.5 ns typ (MC1650)
  = 3.0 ns typ (MC1651)
- Input Slew Rate = 350 V/μs (MC1650)
  = 500 V/μs (MC1651)
- Differential Input Voltage:
  -5.0 V to +5.0 V (-30°C to +85°C)
- Common Mode Range:
  -3.0 V to +2.5 V (-30°C to +85°C) (MC1651)
  -2.5 V to +3.0 V (-30°C to +85°C) (MC1650)
- Resolution: ≤20 mV (-30°C to +85°C)
- Drives 50 Ω lines

The MC1650 and the MC1651 are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The MC1650 provides high impedance Darlington inputs, while the MC1651 is a lower impedance option, with higher input slew rate and higher speed capability.

Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection, transmitters, receivers, memory translation, sense amplifiers and more.

The clock inputs ($\bar{C}_a$ and $\bar{C}_b$) operate from MECL 5 or MECL 10,000 digital levels. When $\bar{C}_a$ is at a logic high level, Q0 will be at a logic high level provided that V_1 > V_2 (V_1 is more positive than V_2). $\bar{Q}0$ is the logic complement of Q0. When the clock input goes to a low logic level, the outputs are latched in their present state.

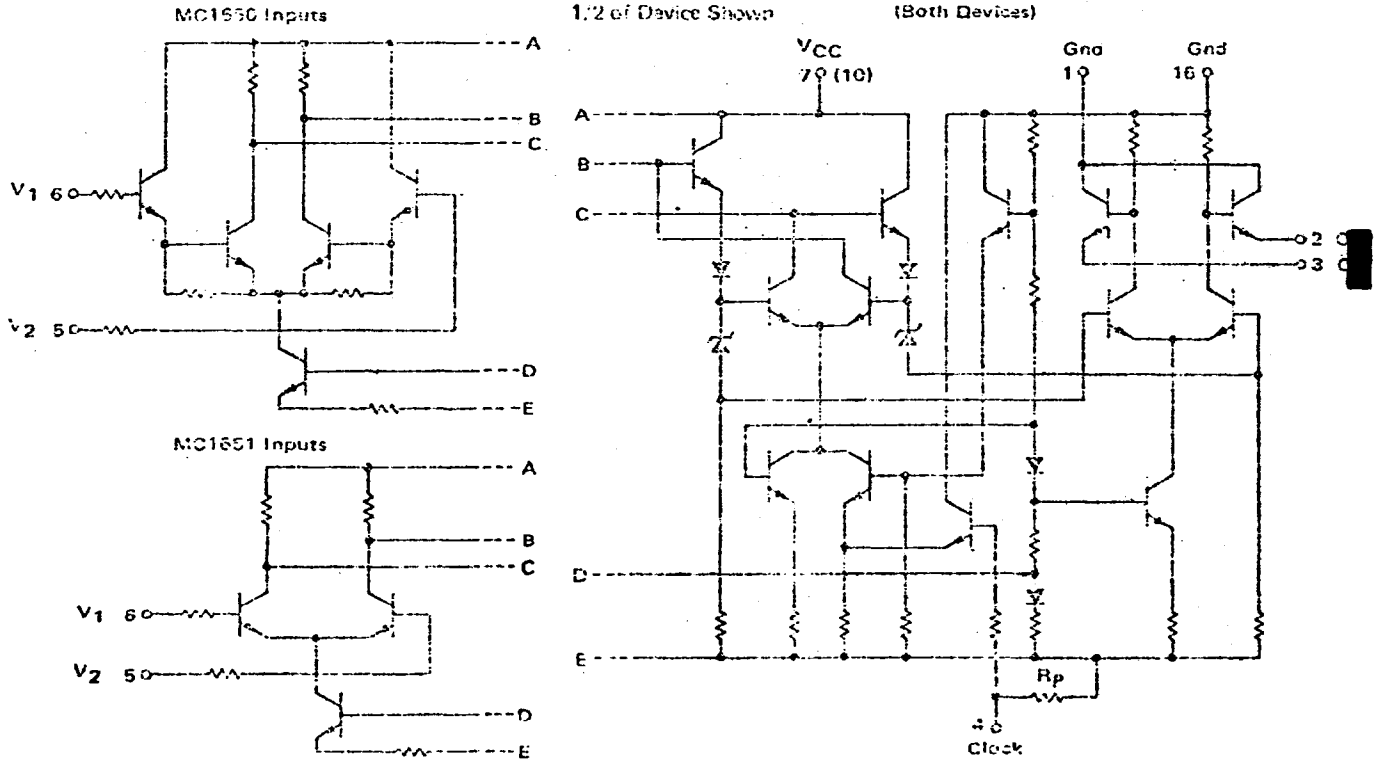
Assessment of the performance differences between the MC1650 and the MC1651 may be based upon the related behaviors shown in Figures 3 and 6.

TRUTH TABLE

$\bar{C}$	V_1, V_2	$Q0_{n+1}$	$\bar{Q}0_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	$Q0_n$	$\bar{Q}0_n$

ϕ = Don't Care

CIRCUIT SCHEMATIC
1/2 of Device Shown (Both Devices)

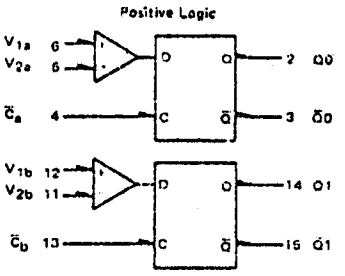


See General Information section for packaging information.

ELECTRICAL CHARACTERISTICS

Each MECL III series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm register to -2.0 volts.

Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.



L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	V_{IHmax}	$V_{IL\,min}$	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③
	TEST VOLTAGE VALUES (Volts)											
-30°C	-0.875	-1.600	-1.180	-1.515	+0.020	-0.020	+2.500	+2.480	-2.500	-2.480	+5.0	-5.2
+25°C	-0.810	-1.650	-1.005	-1.485	+0.020	-0.020	+2.500	+2.480	-2.500	-2.480	+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020	+2.500	+2.480	-2.500	-2.480	+5.0	-5.2

Characteristic	Symbol	Pin Under Test	MC1650L/1651L Test Limits ① -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	$V_{IL\,min}$	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③	Gnd
Power Supply Drain Current																						
Positive	I_{CC}	7,10	–	–	–	25*	–	–	mAdc	–	4,13	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
Negative	I_E	8	–	–	–	55*	–	–	mAdc	4,13	–	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
Input Current	I_{in}																					
MC1650		6	–	–	–	10	–	–	μAdc	4	13	–	–	12	–	6	–	–	–	7,10	8	1,5,11,16
MC1651		6	–	–	–	40	–	–	μAdc	4	13	–	–	12	–	6	–	–	–	7,10	8	1,5,11,16
Input Leakage Current	I_R																					
MC1650		6	–	–	–	7	–	–	μAdc	4	13	–	–	12	–	–	–	6	–	7,10	8	1,5,11,16
MC1651		6	–	–	–	10	–	–	μAdc	4	13	–	–	12	–	–	–	6	–	7,10	8	1,5,11,16
Input Clock Current	I_{inH}	4	–	–	–	350	–	–	μAdc	4	13	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
	I_{inL}	4	–	–	0.5	–	–	–	μAdc	–	13	–	–	6,12	–	–	–	–	–	7,10	4,8	1,5,11,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4,13	–	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
		2									–	–	–	–	5,11	–	–	–	–			1,6,12,16
		2									–	–	–	–	–	6,12	5,11	–	–			1,16
		2									–	–	–	–	–	–	–	5,11	6,12			1,16
		3									–	–	–	–	6,12	–	–	–	–			1,5,11,16
		3									–	–	–	5,11	–	–	–	–	–			1,6,12,16
		3									–	–	–	–	–	5,11	6,12	–	–			1,16
		3									–	–	–	–	–	–	–	6,12	5,11			1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4,13	–	–	–	–	6,12	–	–	–	–	7,10	8	1,5,11,16
		2									–	–	–	5,11	–	–	–	–	–			1,6,12,16
		2									–	–	–	–	–	5,11	6,12	–	–			1,16
		2									–	–	–	–	–	–	–	6,12	5,11			1,16
		3									–	–	–	6,12	–	–	–	–	–			1,5,11,16
		3									–	–	–	–	5,11	–	–	–	–			1,6,12,16
		3									–	–	–	–	–	6,12	5,11	–	–			1,16
		3									–	–	–	–	–	–	–	5,11	6,12			1,16
Logic "1" Threshold Voltage ②	V_{OHA}	1	-1.065	–	-0.980	–	-0.910	–	Vdc	–	13	4	–	6	–	–	–	–	–	7,10	8	1,5,16
		2		–		–		–		–		–	4	–	6	–	–	–	–			
		3		–		–		–		–		4	–	–	6	–	–	–	–			
		4		–		–		–		–		–	4	6	–	–	–	–	–			
Logic "0" Threshold Voltage ②	V_{OLA}	1	–	-1.630	–	-1.600	–	-1.555	Vdc	–	13	4	–	6	–	–	–	–	–	7,10	8	1,5,16
		2	–		–		–			–		–	4	–	6	–	–	–	–			
		3	–		–		–			–		4	–	–	6	–	–	–	–			
		4	–		–		–			–		–	4	6	–	–	–	–	–			

NOTES: ① All data is for ½ MC1650 or MC1651, except data marked (*) which refers to the entire package.
② These tests done in order indicated. See Figure 4.
③ Maximum Power Supply Voltages (beyond which device life may be impaired):
$|V_{EE}| + |V_{CC}| \leq 12$ Vdc.

ELECTRICAL CHARACTERISTICS (continued)

MOTOROLA Semiconductor Products Inc.
ROBERT M. LIGGETT
PRODUCT MARKETING ENGINEER
DIGITAL INTEGRATED CIRCUITS

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PHONE (602) 962-2011

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①
-30°C	+2.000	+4.400	-0.400	+1.190	+2.00	+7.00	-3.20
+25°C	+2.000	+4.400	-0.400	+1.190	+2.00	+7.00	-3.20
+85°C	+2.000	+4.400	-0.400	+1.190	+2.00	+7.00	-3.20

See Figure 2

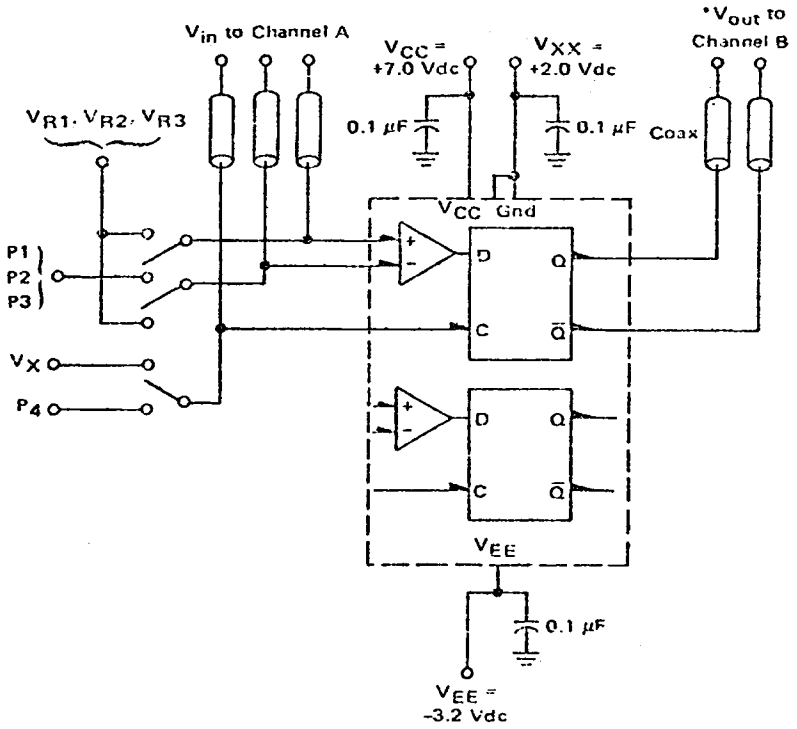
Characteristic	Symbol	Pin Under Test	MC1650L/1651L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①	P1	P2	P3	P4
Switching Times Propagation Delay (50% to 50%) V-Input to Output	t_{6+2+}	2	2.0	5.0	2.0	5.0	2.0	5.7	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{6+2+}	2								–	5	–					–	6	–	–
	t_{6+2+}	2								–	–	5					–	–	6	–
	t_{6+3-}	3								5	–	–					6	–	–	–
	t_{6+3-}	3								–	5	–					–	6	–	–
	t_{6+3-}	3								–	–	5					–	–	6	–
	t_{6-2-}	2								5	–	–					6	–	–	–
	t_{6-2-}	2								–	5	–					–	6	–	–
	t_{6-2-}	2								–	–	5					–	–	6	–
	t_{6-3+}	3								5	–	–					6	–	–	–
	t_{6-3+}	3								–	5	–					–	6	–	–
	t_{6-3+}	3								–	–	5					–	–	6	–
Clock to Output ②	t_{4+2+}	2	2.0	4.7	2.0	4.7	2.0	5.2	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
	t_{4+2-}	2								6	–	–	–				5	–	–	
	t_{4+3+}	3								6	–	–	–				5	–	–	
	t_{4+3-}	3								5	–	–	–				6	–	–	
Clock Enable Time ③	t_{setup}	6	–	–	2.5	–	–	–	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
Clock Aperture Time ③	t_{ap}	6	–	–	1.5	–	–	–	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
Rise Time (10% to 90%)	t_{2+}	2	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3+}	3	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
Fall Time (10% to 90%)	t_{2-}	2	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3-}	3	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–

NOTES: 1 Maximum Power Supply Voltages (beyond which device life may be impaired:
$|V_{CC}| + |V_{EE}| \leq 12$ Vdc.

2 Unused clock inputs may be tied to ground.

3 See Figure 8.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



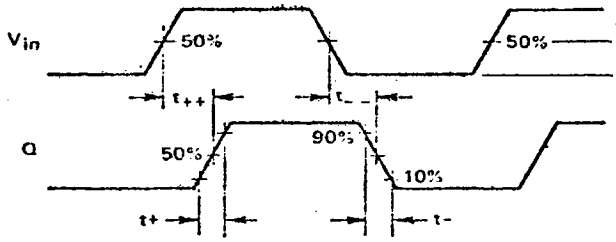
50-ohm termination to ground located in each scope channel input
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

Complement of output under test should always be loaded with 50-ohms to ground.

FIGURE 2 – SWITCHING AND PROPAGATION WAVEFORMS @ 25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

V – Input to Output

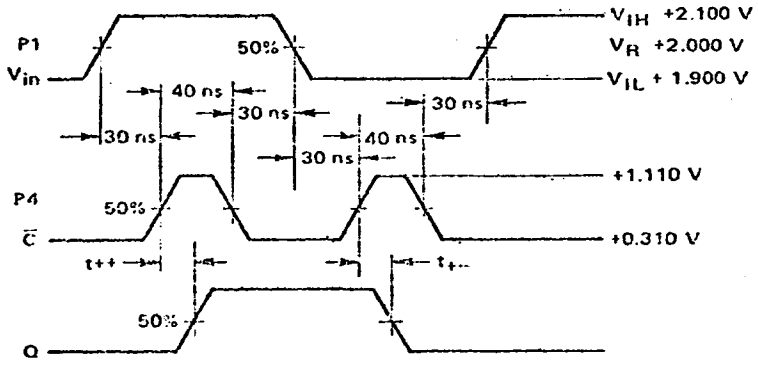


TEST PULSE LEVELS

	P1	P2	P3
V_{IH}	+2.100 V	+4.500 V	-0.30 V
V_R	+2.000 V	+4.400 V	-0.40 V
V_{IL}	+1.900 V	+4.300 V	-0.50 V

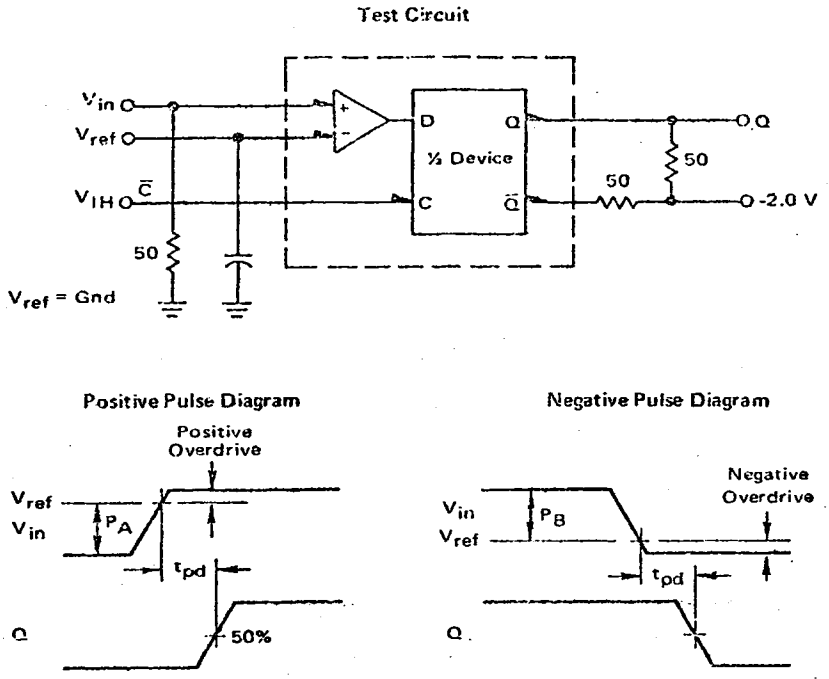
Test pulses: $t_+, t_- = 1.5 \pm 0.2$ ns (10% to 90%)
f = 5.0 MHz
50% Duty Cycle
V_{IH} is applied to $\overline{C}$ during tests.

Clock to Output



P4: $t_+, t_- = 1.5 \pm 0.2$ ns.

FIGURE 3 – PROPAGATION DELAY (t_{pd}) versus INPUT PULSE AMPLITUDE AND CONSTANT OVERDRIVE



Input switching time is constant at 1.5 ns (10% to 90%).

Propagation Delay versus Pulse Amplitude

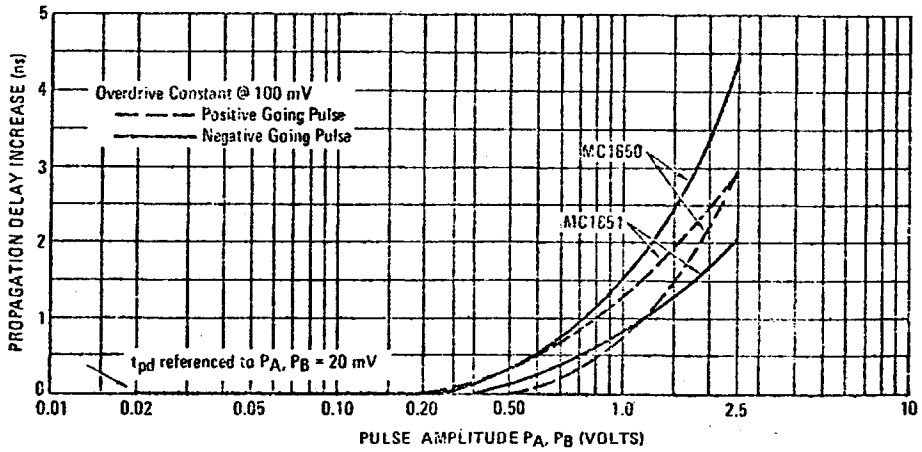


FIGURE 3 (continued)

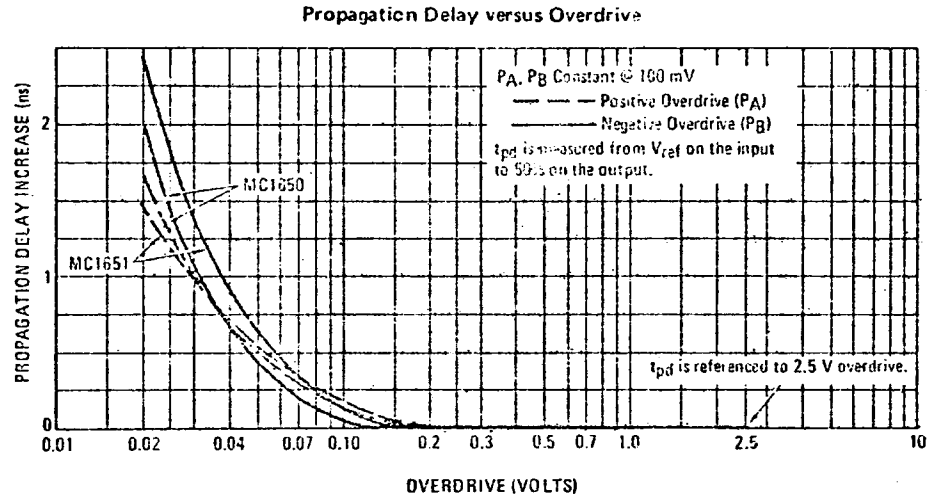


FIGURE 4 -- LOGIC THRESHOLD TESTS (WAVEFORM SEQUENCE DIAGRAM)

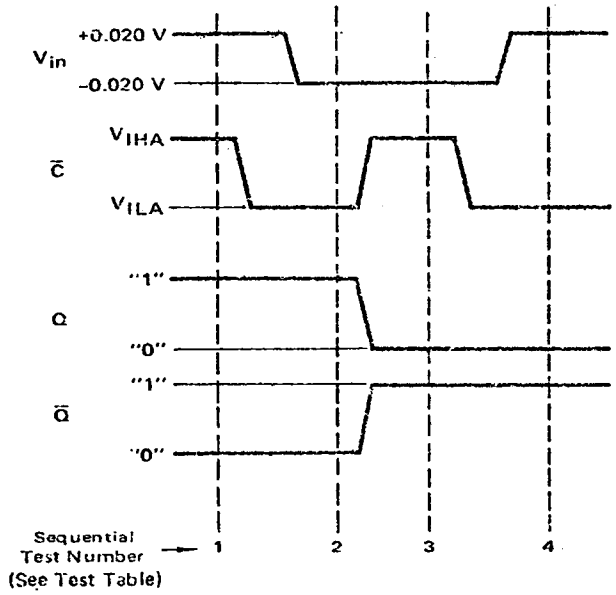
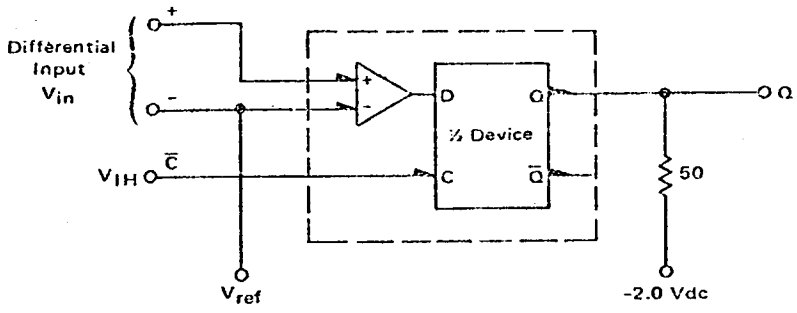


FIGURE 5 – TRANSFER CHARACTERISTICS (Q versus V_{in})

Test Configuration



$-2.5\ Vdc \leqslant V_{ref} \leqslant +2.5\ Vdc$

Typical Transfer Curves

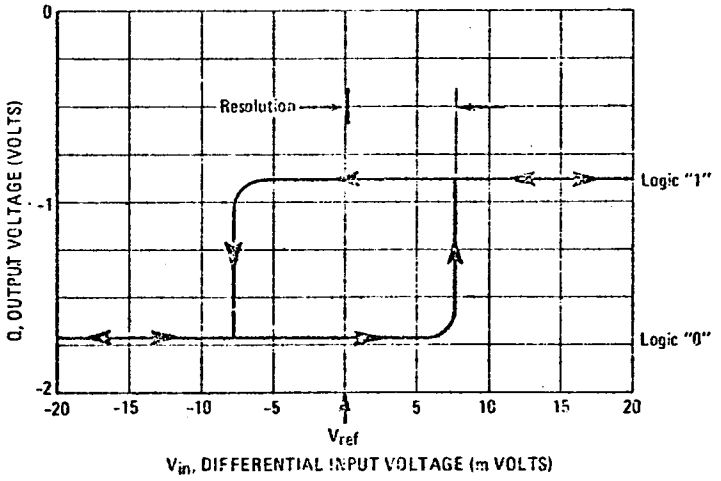
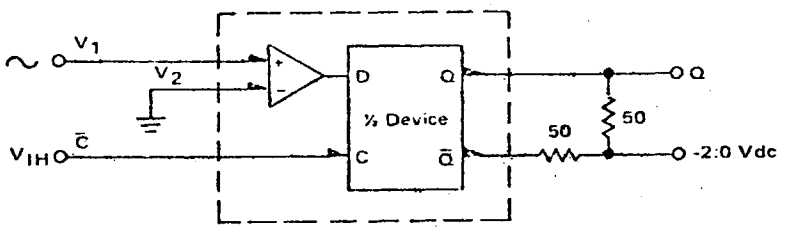
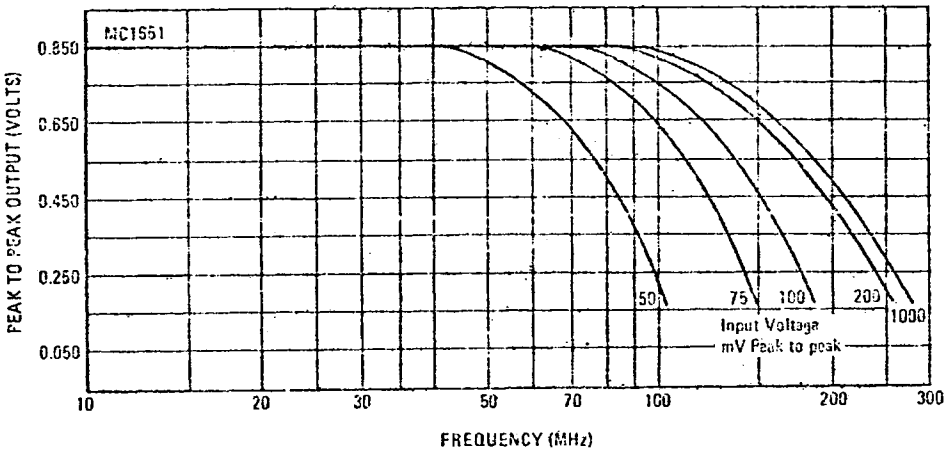


FIGURE 6 – OUTPUT VOLTAGE SWING versus FREQUENCY

(A) Test Circuit



(B) Typical Output Logic Swing versus Frequency



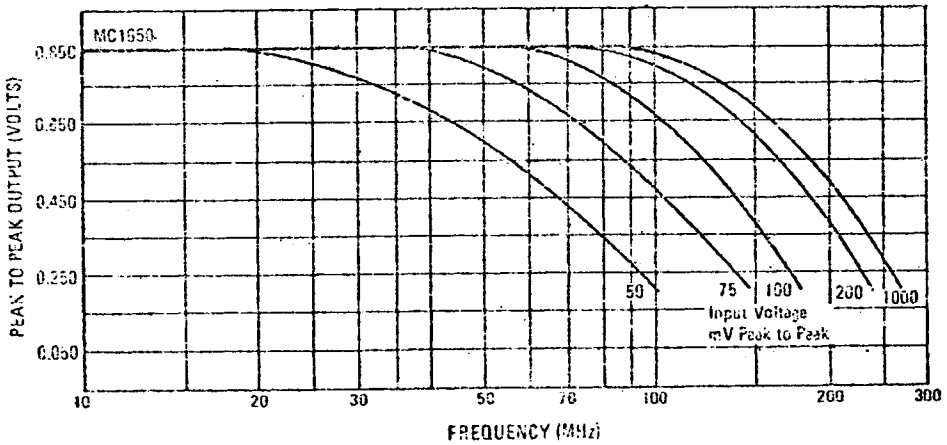
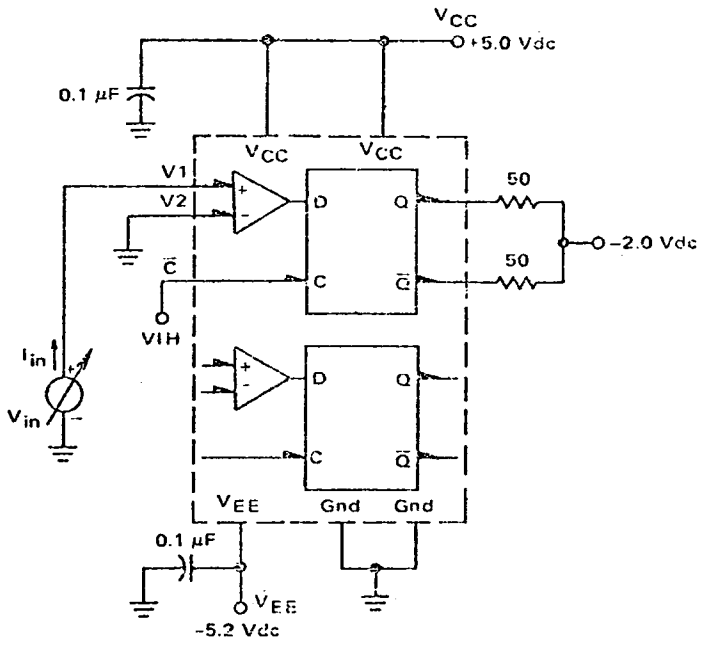
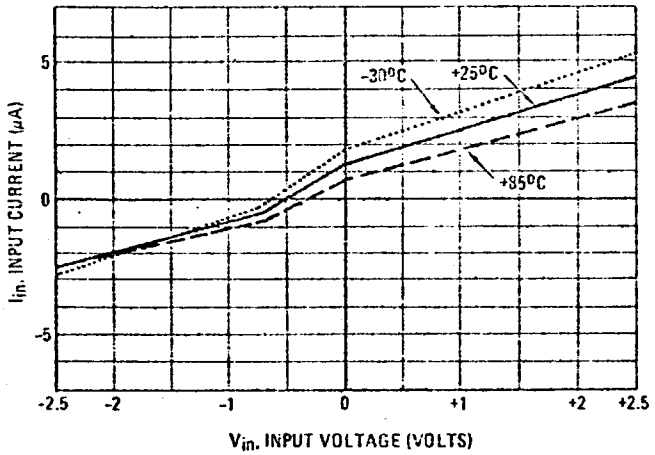


FIGURE 7 – INPUT CURRENT versus INPUT VOLTAGE

TEST CIRCUIT



Typical MC1650 (Complementary Input Grounded)



Typical MC1651 (Complementary Input Grounded)

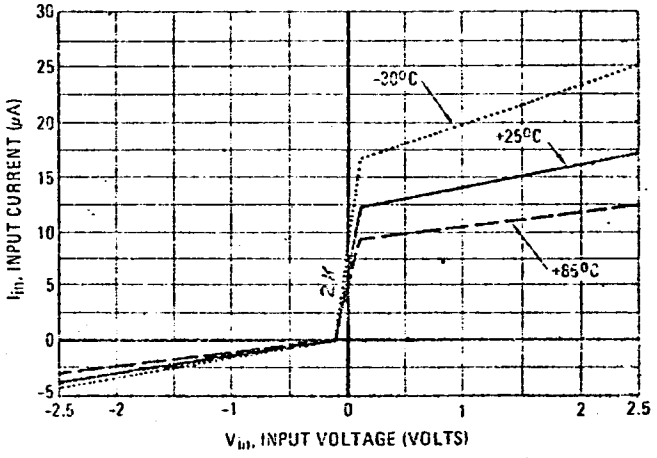
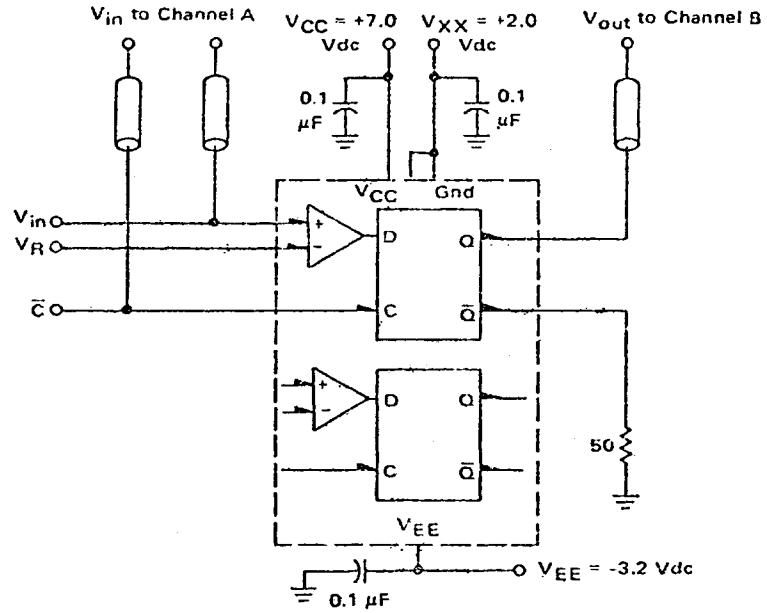


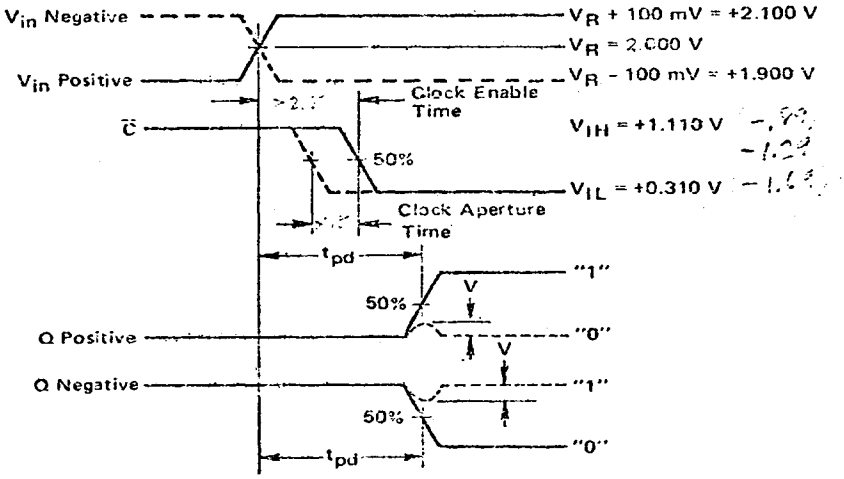
FIGURE 8 – CLOCK ENABLE AND APERTURE TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable.

Analog Signal Positive and Negative Slew Case



——— Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200 ps.

– – – – – – Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.

MAY 1974

LM124/LM224/LM324 quad op amps

general description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

unique characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

advantages

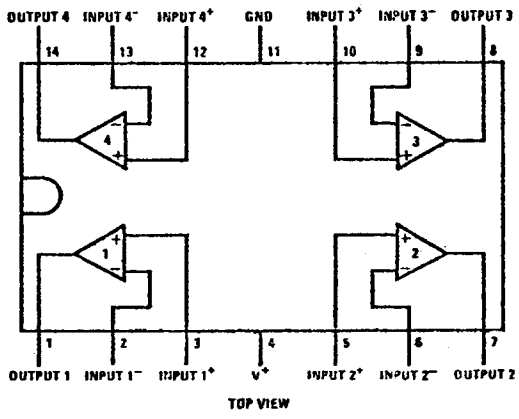
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

features

Internally frequency compensated for unity gain	
Large dc voltage gain	100 dB
Wide bandwidth (unity gain) (temperature compensated)	1 MHz
Wide power supply range:	
Single supply	3 V_{DC} to 30 V_{DC}
or dual supplies	±1.5 V_{DC} to ±15 V_{DC}
Very low supply current drain (800μA) — essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})	
Low input biasing current (temperature compensated)	45 nA_{DC}
Low input offset voltage	2 mV_{DC}
and offset current	5 nA_{DC}
Input common-mode voltage range includes ground	
Differential input voltage range equal to the power supply voltage	
Large output voltage swing	0 V_{DC} to V^+ − 1.5 V_{DC}

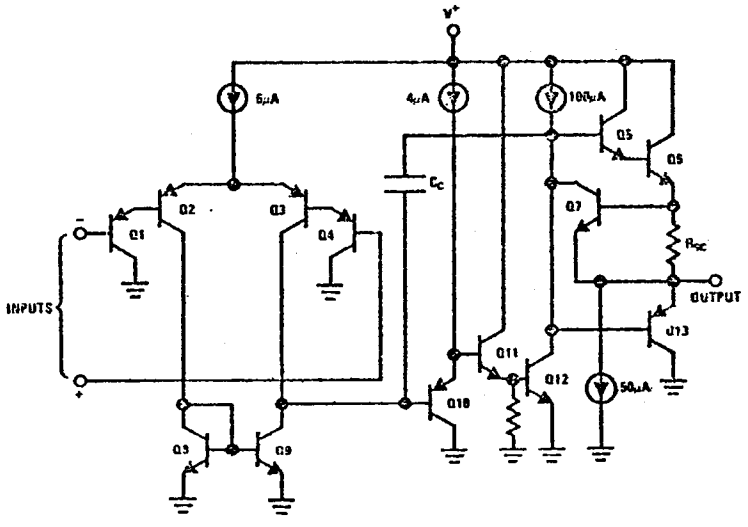
connection diagram

Dual-In-Line and Flat Package



TOP VIEW

schematic diagram (Each Amplifier)



absolute maximum ratings

Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}
Differential Input Voltage	32 V_{DC}
Input Voltage	−0.3 V_{DC} to +32 V_{DC}
Power Dissipation (Note 1)	
Molded DIP (LM324N)	570 mW
Cavity DIP (LM124D, LM224D & LM324D)	900 mW
Flat Pack (LM124F)	800 mW
Output Short-Circuit to GND (Note 2) (One Amplifier)	Continuous
$V^+ \leq 15$ V_{DC} and $T_A = 25°C$	
Input Current ($V_{IN} < -0.3$ V_{DC}) (Note 3)	50 mA
Operating Temperature Range	
LM324	0°C to +70°C
LM224	−25°C to +85°C
LM124	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics ($V^+ = +5.0$ V_{DC}, Note 4) LM124

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = +25°C$ (Note 5)		±2	±5	mV_{DC}
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = +25°C$		45	150	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = +25°C$		±3	±30	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30$ V_{DC}, $T_A = +25°C$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$ On All Op Amps Over Full Temperature Range		0.8	2	mA_{DC}
Large Signal Voltage Gain	$V^+ = +15$ V_{DC} (For Large V_O Swing) $R_L \geq 2$ kΩ, $T_A = +25°C$	50	100		V/mV
Output Voltage Swing	$R_L = 2$ kΩ, $T_A = +25°C$	0		$V^+-1.5$	V_{DC}
Common-Mode Rejection Ratio	DC, $T_A = +25°C$	70	85		dB
Power Supply Rejection Ratio	DC, $T_A = +25°C$	65	100		dB
Amplifier-to-Amplifier Coupling (Note 8)	f = 1 kHz to 20 kHz, $T_A = +25°C$ (Input Referred)		−120		dB
Output Current					
Source	$V_{IN}^+ = +1$ V_{DC}, $V_{IN}^- = 0$ V_{DC}, $V^+ = 15$ V_{DC}, $T_A = +25°C$	20	40		mA_{DC}
Sink	$V_{IN}^- = +1$ V_{DC}, $V_{IN}^+ = 0$ V_{DC}, $V^+ = 15$ V_{DC}, $T_A = +25°C$	10	20		mA_{DC}
	$V_{IN}^- = +1$ V_{DC}, $V_{IN}^+ = 0$ V_{DC}, $T_A = +25°C$, $V_O = 200$ mV_{DC}	12	50		μA_{DC}
Input Offset Voltage	(Note 5)			±7	mV_{DC}
Input Offset Voltage Drift	$R_S = 0\Omega$		7		μV/°C
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±100	nA_{DC}
Input Offset Current Drift			10		pA_{DC}/°C
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$			300	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30$ V_{DC}	0		V^+-2	V_{DC}
Large Signal Voltage Gain	$V^+ = +15$ V_{DC} (For Large V_O Swing) $R_L \geq 2$ kΩ	25			V/mV
Output Voltage Swing					
V_{OH}	$V^+ = +30$ V_{DC}, $R_L = 2$ kΩ	26			V_{DC}
	$R_L \geq 10$ kΩ	27	28		V_{DC}
V_{OL}	$V^+ = +5$ V_{DC}, $R_L \leq 10$ kΩ		5	20	mV_{DC}
Output Current					
Source	$V_{IN}^+ = +1$ V_{DC}, $V_{IN}^- = 0$ V_{DC}, $V^+ = 15$ V_{DC}	10	20		mA
Sink	$V_{IN}^- = +1$ V_{DC}, $V_{IN}^+ = 0$ V_{DC}, $V^+ = 15$ V_{DC}	5	8		mA
Differential Input Voltage (Note 7)				V^+	V_{DC}

electrical characteristics (V^+ = +5.0 V_{DC}, Note 4) LM224, LM324

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	T_A = +25°C (Note 5)		±2	±7	mV_{DC}
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, T_A = +25°C		45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = +25°C		±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	V^+ = 30 V_{DC}, T_A = +25°C	0		V^+–1.5	V_{DC}
Supply Current	$R_L = \infty$ On All Op Amps Over Full Temperature Range		0.8	2	mA_{DC}
Large Signal Voltage Gain	V^+ = +15 V_{DC} (For Large V_O Swing) $R_L \geq 2\ k\Omega$, T_A = +25°C	25	100		V/mV
Output Voltage Swing	R_L = 2 kΩ, T_A = +25°C	0		V^+–1.5	V_{DC}
Common-Mode Rejection Ratio	DC, T_A = +25°C	65	70		dB
Power Supply Rejection Ratio	DC, T_A = +25°C	65	100		dB
Amplifier-to-Amplifier Coupling (Note 8)	f = 1 kHz to 20 kHz, T_A = +25°C (Input Referred)		–120		dB
Output Current					
Source	V_{IN}^+ = +1 V_{DC}, V_{IN}^- = 0 V_{DC}, V^+ = 15 V_{DC}, T_A = +25°C	20	40		mA_{DC}
Sink	V_{IN}^- = +1 V_{DC}, V_{IN}^+ = 0 V_{DC}, V^+ = 15 V_{DC}, T_A = +25°C	10	20		mA_{DC}
	V_{IN}^- = +1 V_{DC}, V_{IN}^+ = 0 V_{DC}, T_A = +25°C, V_O = 200 mV_{DC}	12	50		μA_{DC}
Input Offset Voltage	(Note 5)			±9	mV_{DC}
Input Offset Voltage Drift	R_S = 0Ω		7		μV/°C
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±150	nA_{DC}
Input Offset Current Drift			10		pA_{DC}/°C
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$			500	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	V^+ = 30 V_{DC}	0		V^+–2	V_{DC}
Large Signal Voltage Gain	V^+ = +15 V_{DC} (For Large V_O Swing) $R_L \geq 2\ k\Omega$	15			V/mV
Output Voltage Swing					
V_{OH}	V^+ = +30 V_{DC}, R_L = 2 kΩ	26			V_{DC}
	$R_L \geq 10\ k\Omega$	27	28		V_{DC}
V_{OL}	V^+ = +5 V_{DC}, $R_L \leq 10\ k\Omega$		5	20	mV_{DC}
Output Current					
Source	V_{IN}^+ = +1 V_{DC}, V_{IN}^- = 0 V_{DC}, V^+ = 15 V_{DC}	10	20		mA
Sink	V_{IN}^- = +1 V_{DC}, V_{IN}^+ = 0 V_{DC}, V^+ = 15 V_{DC}	5	8		mA
Differential Input Voltage (Note 7)				V^+	V_{DC}

Note 1: For operating at high temperatures, the LM324 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224 and LM124 can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than –0.3 V_{DC}.

Note 4: These specifications apply for V^+ = +5 V_{DC} and –55°C ≤ T_A ≤ +125°C, unless otherwise stated. With the LM224, all temperature specifications are limited to –25°C ≤ T_A ≤ +85°C and the LM324 temperature specifications are limited to 0°C ≤ T_A ≤ +70°C.

Note 5: $V_O \cong 1.4\ V_{DC}$, R_S = 0Ω with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to V^+ – 1.5 V_{DC}).

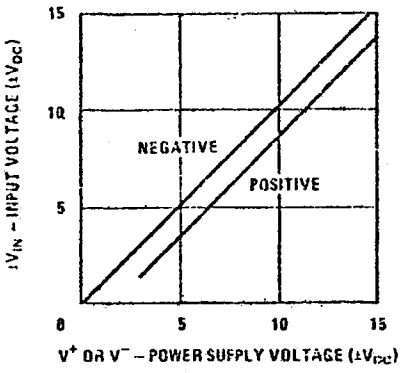
Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ – 1.5V, but either or both inputs can go to +32 V_{DC} without damage.

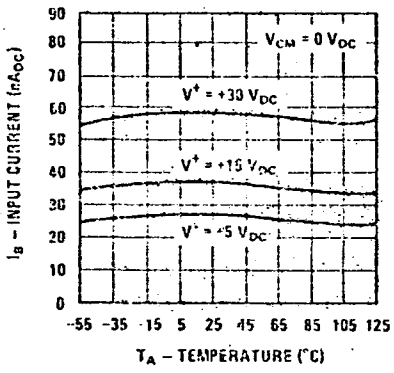
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

typical performance characteristics

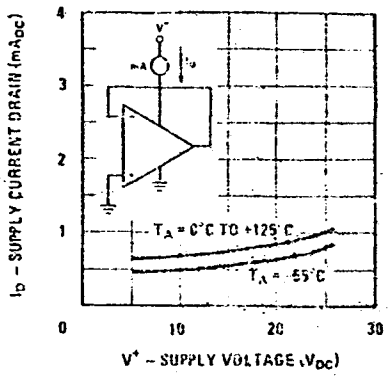
Input Voltage Range



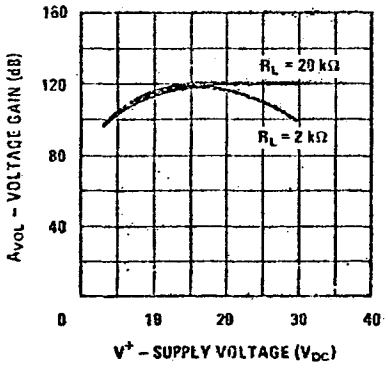
Input Current



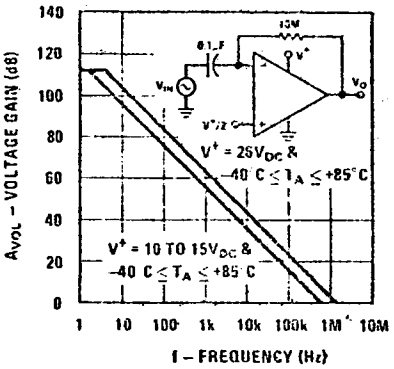
Supply Current



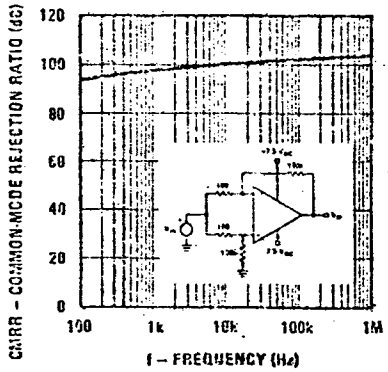
Voltage Gain



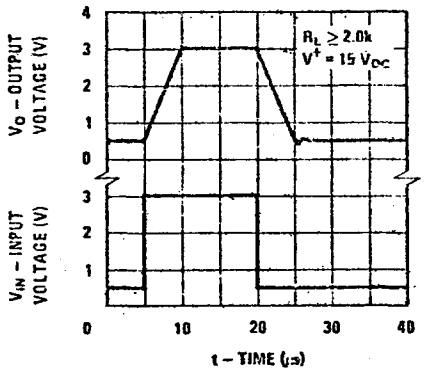
Open Loop Frequency Response



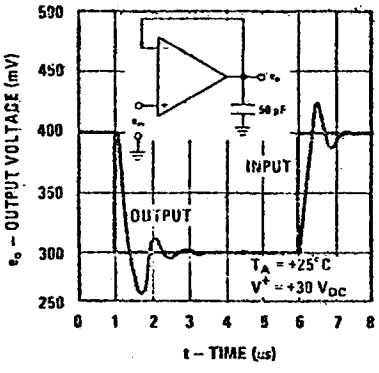
Common Mode Rejection Ratio



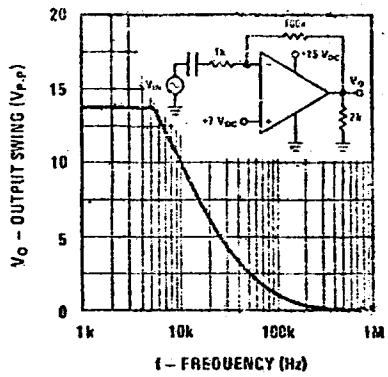
Voltage Follower Pulse Response



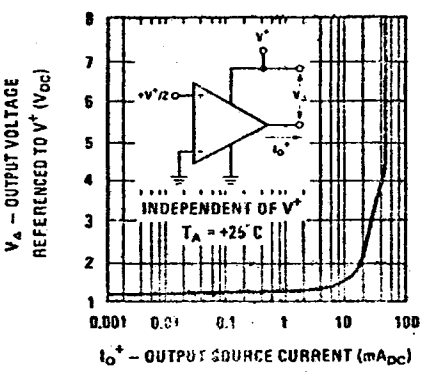
Voltage Follower Pulse Response (Small Signal)



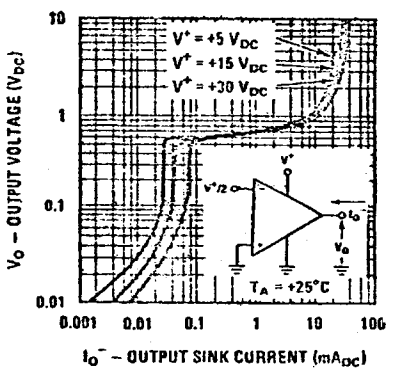
Large Signal Frequency Response



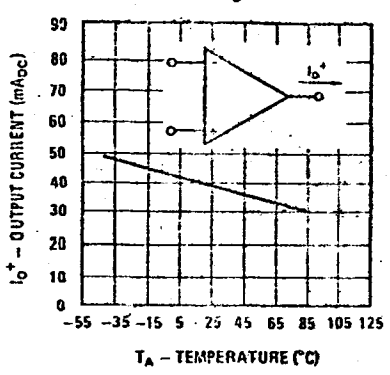
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



Current Limiting



MAY 1972

LM3900 quad amplifier

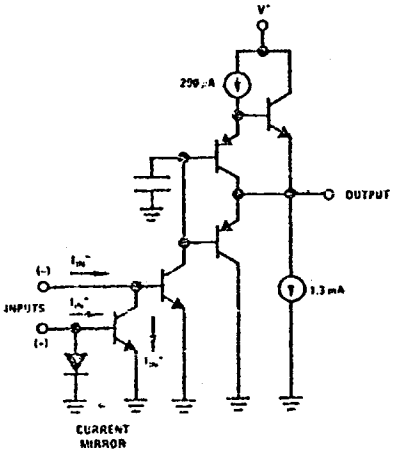
general description

The LM3900 consists of four independent, dual input, internally compensated amplifiers which were designed specifically to operate off of a single power supply voltage and to provide a large output voltage swing. These amplifiers make use of a current mirror to achieve the non-inverting input function. Application areas include: AC amplifiers, RC active filters; low frequency triangle, squarewave and pulse waveform generation circuits, tachometers and low speed, high voltage digital logic gates.

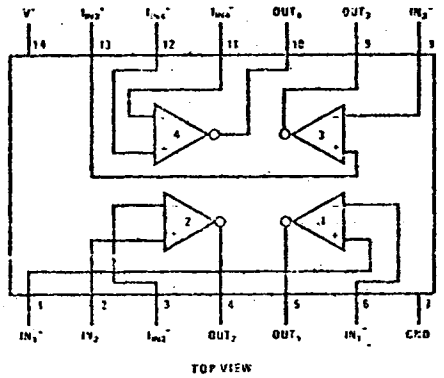
features

- Wide single supply voltage range — 4 V_{DC} to 36 V_{DC}
  or dual supplies — ±2 V_{DC} to ±18 V_{DC}
- Supply current drain independent of supply voltage
- Low input biasing current — 30 nA
- High open-loop gain — 70 dB
- Wide bandwidth — 2.5 MHz (Unity Gain)
- Large output voltage swing — $(V^+ - 1)$ V_{pp}
- Internally frequency compensated for unity gain
- Output short-circuit protection

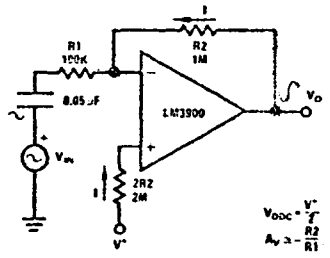
schematic and connection diagrams



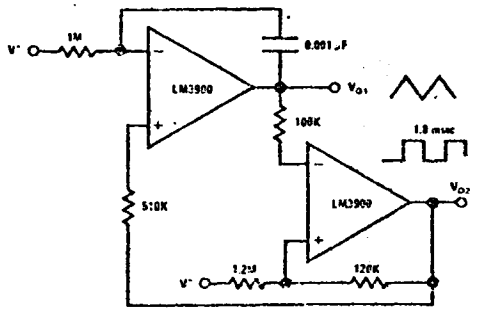
Dual-In-Line Package



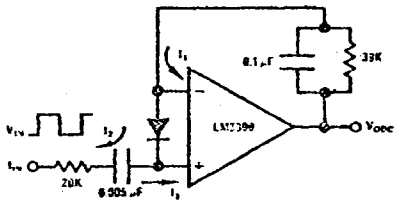
typical applications ($V^+ = 15V_{DC}$)



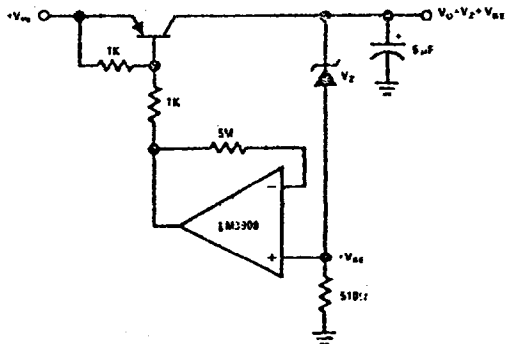
Inverting Amplifier



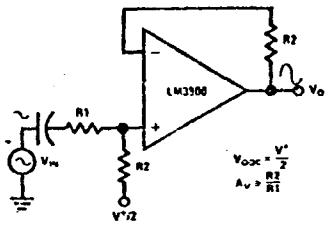
Triangle/Square Generator



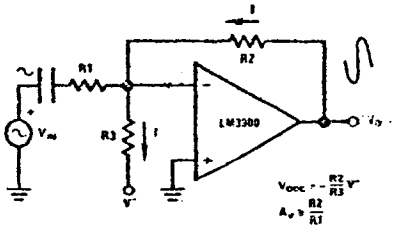
Frequency-Doubling Tachometer



Low V_{IN}–V_{OUT} Voltage Regulator



Non-Inverting Amplifier



Negative Supply Biasing

absolute maximum ratings

Supply Voltage	+36 VDC ±18 VDC
Power Dissipation (T_A = 25°C) (Note 1)	570 mW
Input Currents, $I_{IN}+$ or $I_{IN}-$	20 mA DC
Output Short Circuit Duration – One Amplifier T_A = 25°C (See Application Hints)	Continuous
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

electrical characteristics (V^+ = +15 VDC and T_A = 25°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Open Loop					
Voltage Gain	f = 100 Hz	1200	2800		V/V
Input Resistance	Inverting Input		1		MΩ
Output Resistance			8		kΩ
Unity Gain Bandwidth	Inverting Input		2.5		MHz
Input Bias Current	Inverting Input		30	200	nA
Slew Rate	Positive Output Swing		0.5		V/μs
	Negative Output Swing		20		V/μs
Supply Current	$R_L = \infty$ On All Amplifiers		6.2	10	mA DC
Output Voltage Swing	R_L = 5.1k				
V_{OUT} High	$I_{IN}- = 0$, $I_{IN}+ = 0$	13.5	14.2		VDC
V_{OUT} Low	$I_{IN}- = 10\ \mu A$, $I_{IN}+ = 0$		0.09	0.2	VDC
Output Current Capability					
Source		3	10		mA DC
Sink	(Note 2)	0.5	1.3		mA DC
Power Supply Rejection	f = 100 Hz		70		dB
Mirror Gain	$I_{IN}+ = 200\ \mu A$ (Note 3)	0.90	1	1.1	μA/μA
Mirror Current	(Note 4)		10	500	μA DC
Negative Input Current	(Note 5)		1.0		mA DC

Note 1: For operating at high temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient.

Note 2: The output current sink capability can be increased for large signal conditions by overdriving the inverting input. This is shown in the section on Typical Characteristics.

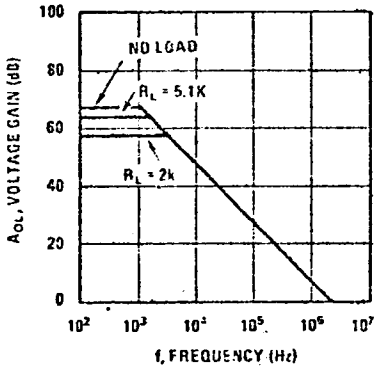
Note 3: This spec indicates the current gain of the current mirror which is used as the non-inverting input.

Note 4: Input V_{BE} match between the non-inverting and the inverting inputs occurs for a mirror current (non-inverting input current) of approximately 10 μA. This is therefore a typical design center for many of the application circuits.

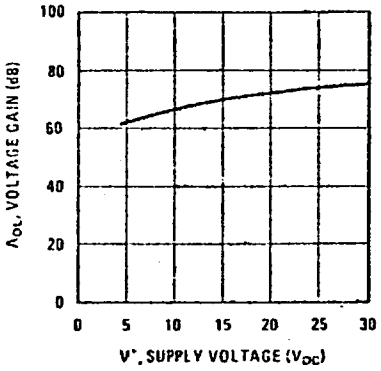
Note 5: Clamp transistors are included on the IC to prevent the input voltages from swinging below ground more than approximately −0.3 VDC. The negative input currents which may result from large signal overdrive with capacitance input coupling need to be externally limited to values of approximately 1 mA. Negative input currents in excess of 4 mA will cause the output voltage to drop to a low voltage. This maximum current applies to any one of the input terminals. If more than one of the input terminals are simultaneously driven negative smaller maximum currents are allowed. Common-mode current biasing can be used to prevent negative input voltages; see for example the "Differentiator Circuit" in the applications section.

typical performance characteristics

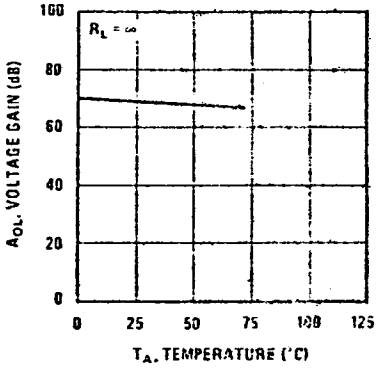
Open-Loop Gain



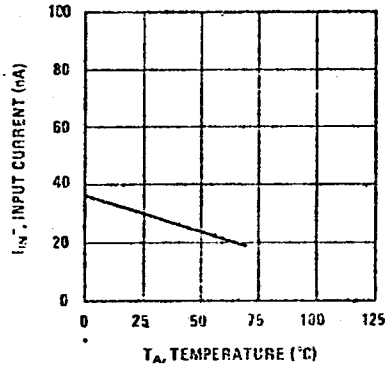
Voltage Gain



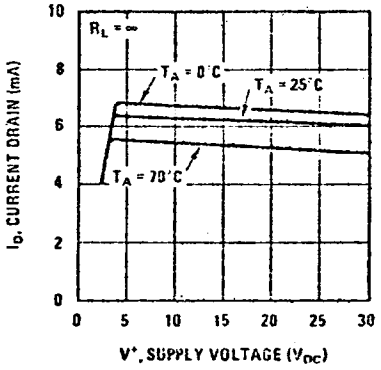
Voltage Gain



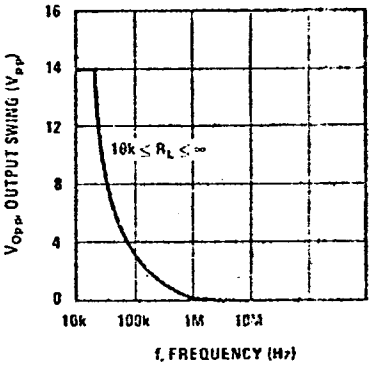
Input Current



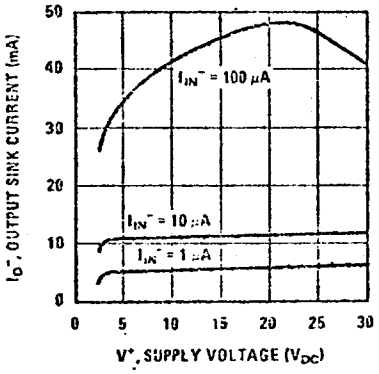
Supply Current



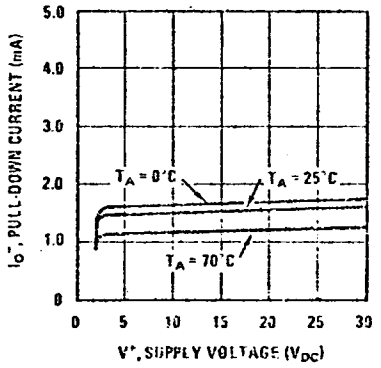
Large Signal Frequency Response



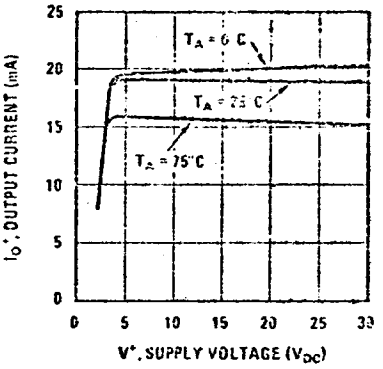
Output Sink Current



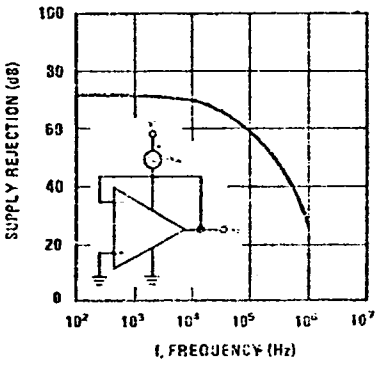
Output Class-A Bias Current



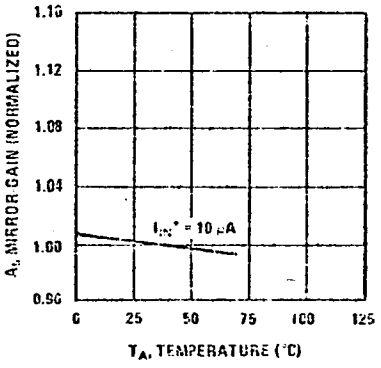
Output Souce Current



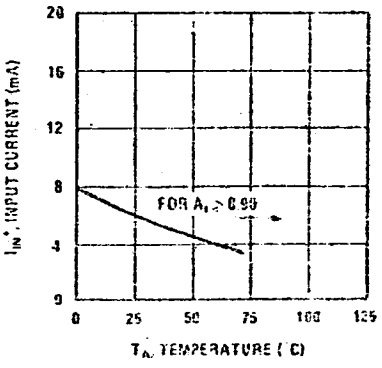
Supply Rejection



Mirror Gain



Maximum Mirror Current



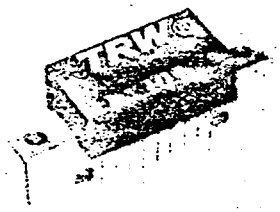
DATA SHEET

TRW SEMICONDUCTORS

RF Hybrid Amplifiers

CA860 10-200MHz, 500mW

CA870 100-400MHz, 400mW



Broadband Reliable Performance, ±1.0 dB

The CA860 and CA870 amplifiers are hybrid microelectronic circuits. They are miniature, low cost, high gain modules with built-in provisions for amplitude leveling. The two circuits cover the 10-200MHz and 100-400MHz ranges. Two B+ inputs, one for the preamplifier and one for the final stage, provide a convenient means of RF leveling by variation of the final stage B+ voltage. Load variations on the preceding stage are kept to a minimum by this provision. Although the uncorrected flatness of both modules is superb (±1dB), the leveling provisions provide convenient means of correcting for the frequency response of succeeding stages and injection of AM modulation.

The modules find wide application in military and industrial service as gain blocks in RF amplifiers for HF, VHF and UHF transmitters.

SPECIFICATIONS

Parameter	CA860	CA870
Frequency	10-200MHz	100-400MHz
Power Output (V_{CC} = 24V) @ 25°C	500mW Min	400mW Min
Unleveled Broadband Response	±1dB	±1dB
Input/Output Impedance	50 Ohms	50 Ohms
Input/Output VSWR	1.5:1	1.5:1
$B+_1$ and $B+_2$	24V Max	24V Max
Gain (V_{CC} = 24V)	32dB Typ	32dB Typ
P_{in} (for saturation output)	1mW Min	1mW Min
Storage Temperature*	-40 to 100°C	-40 to 100°C
Operating Temperature*	-20 to 90°C	-20 to 90°C
Noise Figure	12dB	12dB
Reverse Isolation (due to variation of V_{CC2})	40dB Min	40dB Min

*Measured under head of mounting screw.

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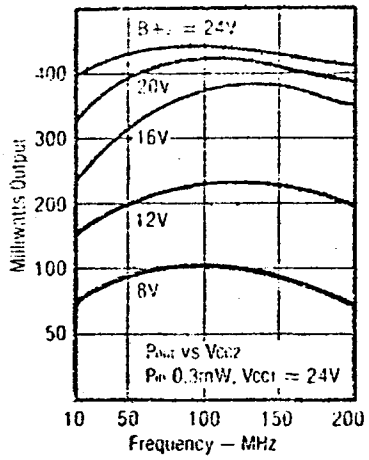
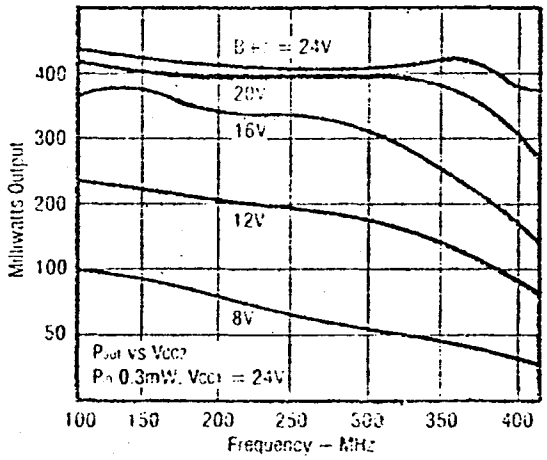
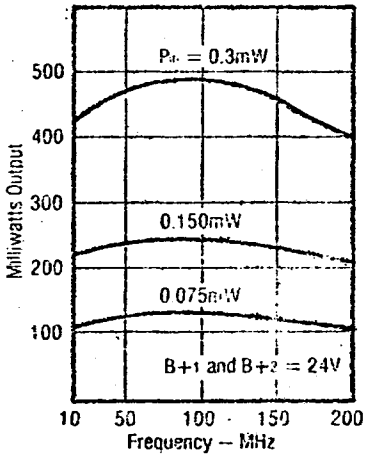
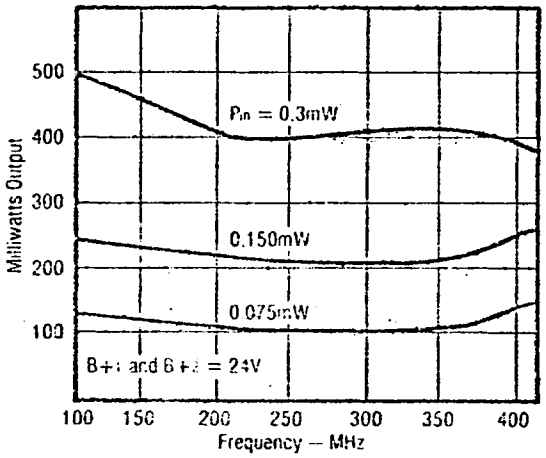
CA860
TYPICAL PERFORMANCE
10-200MHz



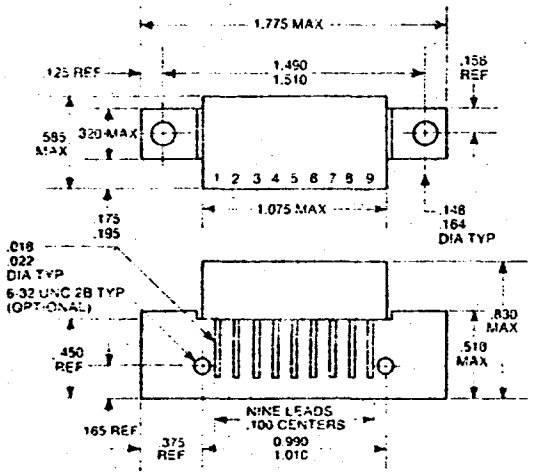
CA870
TYPICAL PERFORMANCE
100-400MHz

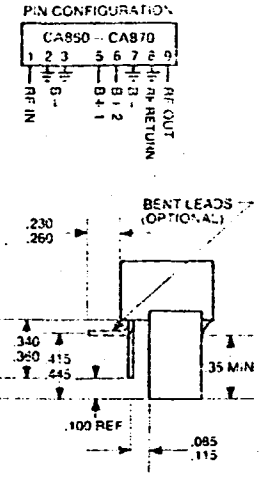


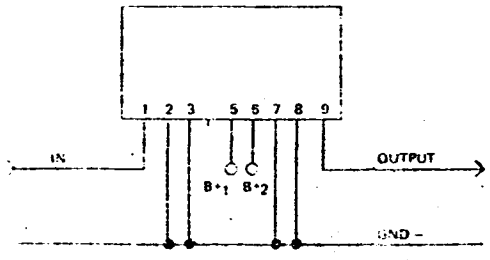




PACKAGE OUTLINE AND PIN DIAGRAM







TRW RF SEMICONDUCTORS

PRELIMINARY SPECIFICATIONS FOR THIN FILM HYBRID AMPLIFIERS

CA2830 PUSH PULL RF AMPLIFIER

34.5dB GAIN

1 TO 150MHz

WIDE DYNAMIC RANGE

LOW ENVELOPE DISTORTION

PARAMETERS @ V_{CC}=24V	CA2830
GAIN @ 10MHz	34.5 ± 1.0dB
FREQUENCY RESPONSE	1 - 150MHz (± 1.0dB)
POWER OUTPUT @ 1dB COMPRESSION	28dBm
THIRD ORDER INTERCEPT	45dBm
SECOND ORDER INTERCEPT	65dBm
NOISE FIGURE	7dB
VSWR (50Ω) IN/OUT	2:1
POWER REQUIREMENTS	330mA
OPERATING TEMPERATURE (CASE)	-40°C to +100°C
STORAGE TEMPERATURE	-55°C to +125°C

TRW RF Semiconductors, An Electronic Components Division of TRW, Inc.
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7. BILL OF MATERIAL

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☑ MECHANICAL BOM # A13800Z8 REV _____ DATE 1/24/78 PAGE 1 OF 3

MODULE # D1 NAME VARIABLE PHASE SAMPLER DWG # _____ SUB ASMB _____ DWG # _____

SCHEMATIC DWG # _____ LOCATION _____ QUA/SYSTEM _____ PREPARED BY J. Osborne APPROVED _____

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
		NRAO	A13500Z1	VARIABLE PHASE SAMPLER	—	
		NRAO	A13500Z2	VARIABLE PHASE SAMPLER PC BD ASSY	1	
		NRAO	A13500Z14	COAXIAL CABLE ASSEMBLY	1	
		NRAO	A13500Z15	COAXIAL CABLE ASSEMBLY	1	
		NRAO		" " "	1	
		NRAO		" " "	1	
		NRAO		" " "	1	
		NRAO		" " "	1	
		NRAO		" " "	1	
		NRAO		" " "	1	
		NRAO		" " "	1	
		NRAO	B13500M29	PANEL, FRONT	1	
		NRAO	B13500M30	PANEL, REAR	1	
		NRAO	B13500M31-1	BAR SUPPORT, LEFT	2	
		NRAO	B1350M31-2	BAR SUPPORT, RIGHT	2	

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☐ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 2 OF 3

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA
		NRAO	C13500M32	COVER, PERFORATED.	2
		NRAO	B13050M4	GUIDE	2
		SOUTHCO	47-10-204-10	FASTNER, CAPTIVE	2
			6-32x0.25	ST.ST'L., FLT HEAD, FOR FRONT PANEL	4
			4-40 x .5	ST. ST'L., PAN HEAD, FOR SPACER BARS	2
			6-32 x 0.25	ST. ST'L., PAN HEAD, FOR SOCKET SUPER PAN HEAD	4
			6-32 x .25	ST. ST'L., HEX SOC. HD. CAP. SCR.	2
		NRAO	B1350M31-3	SPACER, BAR	2
		AMP SPEC IND	204186-5	PIN BLOCK, 42 PIN MIXED	1
		AMP SPEC IND	202394-2	HOOD	1
	J5, J6		OSM 244-2	TEST POINTS	2
		OMNI-SPECTRA	OMQ3043-75	CONNECTOR, RIGHT ANGLE PC MOUNT	2
		HH SMITH	15.01 - RED	TIP JACK NYLON	1
		"	1501 - BROWN	"	1
		"	1501 - YELLOW	"	1
		"	1501 - ORANGE	"	1
		"	1501 - BLACK	"	1

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☐ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 3 OF 3

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
		NRAO	D13500AR3	ARTWORK, PC	1	
		NRAO		DRILL DWG	1	
			4-40x.25	ST.ST'L., BINDING HD. FOR PC BOARD	8	
			2-56 x .125	B/S, FOR OSM244-2 T.P.	4	
			2-56	H N S, NUTS FOR ABOVE	4	
		AMP SPEC IND	203964-6	SOCKET GUIDE	2	
		"	201578-1	PIN, CRIMP	15	
		"	201143-5	PIN, COAX	4	
		"	200833-4	PIN, GUIDE	1	
		"	202514-1	PIN, GUIDE (GOLD PLTD.)	1	

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☑ ELECTRICAL ☐ MECHANICAL BOM # A1380079 REV _____ DATE 1/24/78 PAGE 1 OF 8

MODULE # D1 NAME VARIABLE PHASE SAMPLER DWG # _____ SUB ASMB _____ DWG # _____

SCHEMATIC DWG # _____ LOCATION _____ QUA/SYSTEM _____ PREPARED BY J. Osborne APPROVED _____

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA
		ALLEN BRADLEY or EQUIV.	RCR07G270JS	27Ω ¼w	1
		"	RCR07G470JS	47Ω ¼w	3
		"	RCR07G510JS	51Ω ¼w	4
		"	RCR07G680JS	68Ω ¼w	10
		"	RCR07G101JS	100Ω ¼w	8
		"	RCR07G151JS	150Ω ¼w	2
		"	RCR07G201JS	200Ω ¼w	9
		"	RCR07G221JS	220Ω ¼w	27
		"	RCR07G241JS	240Ω ¼w	2
		"	RCR07G271JS	270Ω ¼w	8
		"	RCR07G331JS	330Ω ¼w	5
		"	RCR07G391JS	390Ω ¼w	1
		"	RCR07G431JS	430Ω ¼w	5
		"	RCR07G511JS	510Ω ¼w	1
		"	RCR07G621JS	620Ω ¼w	1

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☑ ELECTRICAL ☐ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 2 OF 8

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
		ALLEN BRADLEY or EQUIV	RCR07G751JS	750Ω ¼w	1	
		"	RCR07G911JS	910Ω ¼w	1	
		"	RCR07G102JS	1000Ω ¼w	7	
		"	RCR07G112JS	1.1K ¼w	7	
		"	RCR07G122JS	1.2K ¼w	11	
		"	RCR07G152JS	1.5K ¼w	1	
		"	RCR07G182JS	1.8K ¼w	3	
		"	RCR07G202JS	2K ¼w	1	
		"	RCR07G272JS	2.7K ¼w	3	
		"	RCR07G302JS	3K ¼w	8	
		"	RCR07G332JS	3.3K ¼w	2	
		"	RCR07G362JS	3.6K ¼w	1	
		"	RCR07G512JS	5.1K ¼w	2	
		"	RCR07G682JS	6.8K ¼w	1	
		"	RCR07G103JS	10K ¼w	12	
		"	RCR07G153JS	15K ¼w	4	
		"	RCR07G513JS	51K ¼w	10	

[redacted] OF [redacted]

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☐ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 3 OF 8

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
		ALLEN BRADLEY or EQUIV	RCR07G753JS	75 K ¼ w	1	
		"	RCR07G104JS	100 K ¼ w	26	
		"	RCR07G244JS	240 K ¼ w	1	
		"	RCR07G474JS	470 K ¼ w	2	
		"	RCR05G101JS	100 Ω ⅛ w	4	
		"	RCR20G271-JS	270 Ω ½ w	1	
		"	RCR20G391-JS	390 Ω ½ w	6	
	R36, R37		RC742G101JS	10Ω 2w	2	
		TRW/IRC	RNR55D2000F	RESISTOR 200 Ω 1%	2	
		"	RNR55D2100F	210Ω 1%	2	
		"	RNR55D1540F	154Ω 1%	1	
		"	RNR55D76R8F	76.8Ω 1%	1	
		"	RNR55D2370F	237Ω 1%	1	
		"	RNR55D2431F	2.43K 1%	1	
		SPECTROL	64W102	POTENTIOMETER, PC. 25T	4	
		BECKMAN	66WR10.0K	POT, 10K 20T	3	
		SPECTROL	64W102	POT, 1K 25T	1	

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☐ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 4 OF 8

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
		TEXAS INSTR	SN74164	IC	1	
		NAT SEMICOND.	LM3900	AMP, OP QUAD	1	
		RCA	CA3102	IC	1	
		MOTOROLA	MC10109	MECL, IC	1	
		"	MC10124	MECL, IC	1	
		"	MC10174	MECL, IC	2	
		"	MC10231	MECL, IC	10	
		NAT SEMICOND	LM324N	IC	4	
		MOTOROLA	MC1650	IC	2	
		"	2N4996	TRANSISTOR	2	
		"	MM8001	TRANSISTOR	2	
		"	2N3906	TRANSISTOR	1	
		"	2N3904	"	1	
		RCA	2N5109	"	4	
		MOTOROLA	2N5583	"	4	
		"	2N6305	"	4	
		"	1N4742A	DIODE, ZENER 12V 1W	1	

BILL OF MATERIAL

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☐ ELECTRICAL ☐ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 5 OF 8

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA
		AERTECH	A2X919	DIODE BATCH MATCHED	16
		"	A4X988U	DIODE	2
		MOTOROLA	1N4740A	DIODE, ZENER 10V 1W	1
		HEWLETT PACKARD	HP5082-3077	DIODE	8
		"	" -2835	"	8
		"	" -2810	"	11
		NYTRONICS	WEE V-L 1.5	INDUCTOR, VAR 1.5uh	1
		"	" " 0.68	" " 68uh	1
		"	" " 18.0	" " 18uh	1
		"	" " 56.0	" " 56uh	1
		"	DD-47.0	INDUCTOR, RF 47uh	4
		"	" -0.15	" " .15uh	2
		"	" -330	" " 330uh	2
		"	" -6.80	" " 6.8uh	6
		"	" -0.47	" " .47uh	1
		"	" -470	" " 470uh	1
		"	" -0.33	" " .33uh	1

BILL OF MATERIAL

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☐ ELECTRICAL ☐ MECHANICAL BOM # _____ REV _____ DATE _____ PAGE 6 OF 8

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
		NYTRONICS	OD-0.22	INDUCTOR, RF 0.22μh	1	
		"	" -0.18	" " 0.18μh	1	
		"	" -1.50	" " 1.50μh	1	
		SPRAGUE	TG-S10	CAPACITOR, CERAMIC .01μf	24	
		"	" -D50	" " .005μf	44	
		"	10TCC-Q10	CAPACITOR, TC 10Pf	1	
		"	5GA-D10	CAPACITOR, CERAMIC .001μf	13	
		"	10TCC-V47	" " 4.7Pf	5	
		"	7C093104X7500D	CAPACITOR MONOLYTHIC .1μf	3	
		"	5GA-Q30	CAPACITOR, CERAMIC 30Pf	2	
		AVX	3420-050E-224M	CAPACITOR 0.22μf	6	
		ELECTRO MATERIALS	502ES50RD473Z	" 0.047μf	16	
		SPRAGUE	10TCC-V10	CAPACITOR, TC 1 Pf	2	
		"	10TCC-Q15	CAPACITOR, CERAMIC 15Pf	1	
		CORNELL DUBILIER	CD7FA331J03	CAPACITOR, MICA 330 Pf	1	
		"	CD7FA681J03	" " 680 Pf	1	
		"	CD6EA510J03	" " 51.0 Pf	1	

BILL OF MATERIAL

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ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA
				CAPACITOR, MICA 22.0pf	1
		ARCO	CM05ED300J03	" " 30 pf	2
		E.F. JOHNSON	9312	CAPACITOR, VAR 3-10pf	2
		E.F JOHNSON	274-0020-250	" " 3.5-20pf	1
	C23	"	274-0009-250	" " 2.5-9 pf	1
		SPRAGUE	CS13BF56K	CAPACITOR 5.6uf Tant	1
		"	T21202	CAPACITOR 5uf /25V	2
	L35-L40	FERROXCUBE	56 590 65/4B	BEAD, FERRITE FOR TRANSISTOR EMMITTER LEADS	6
	L33, L41, 42, 43, 44	ALLEN BRADLEY	To 140A303B	BEAD, FERRITE	5
	L31, L32	"	To 140A303B	" "	2
		FERROXCUBE	VK211-07/3B	CORE, FERRITE	1
	T2	"	104T060/4C4	CORE, FERRITE, TOROID	1
	T3, 4, 5, 6	STACKPOLE	57-0184	CORE, TOROID, FERRITE	4
		STACKPOLE	57-0372	CORE, TOROID, FERRITE	1
		CENTRALAB	W05011J184M	CAPACITOR, CHIP. 0.1uf	8
		"	W05OFH223M	" " .022uf	8
		"	W05OFH223M	" " .022uf	2

BILL OF MATERIAL

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ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
		CENTRALAB	W050FH103M	CAPACITOR, CHIP .01uF	1	
	L21			#24 BUS WIRE 3 TURNS .125 DIA.	1	
		THERMALLOY	2254B	HEATSINK	1	
				SPACING BLOCK	1	
		TEXAS INSTR.	C931402	SOCKET, IC 14 PIN	7	
		"	C931602	SOCKET, IC 16 PIN	18	