VLA Technical Report No. 38

MODULE TYPE M2 DATA TAP MANUAL

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1.0 INTRODUCTION AND FUNCTIONAL DESCRIPTION

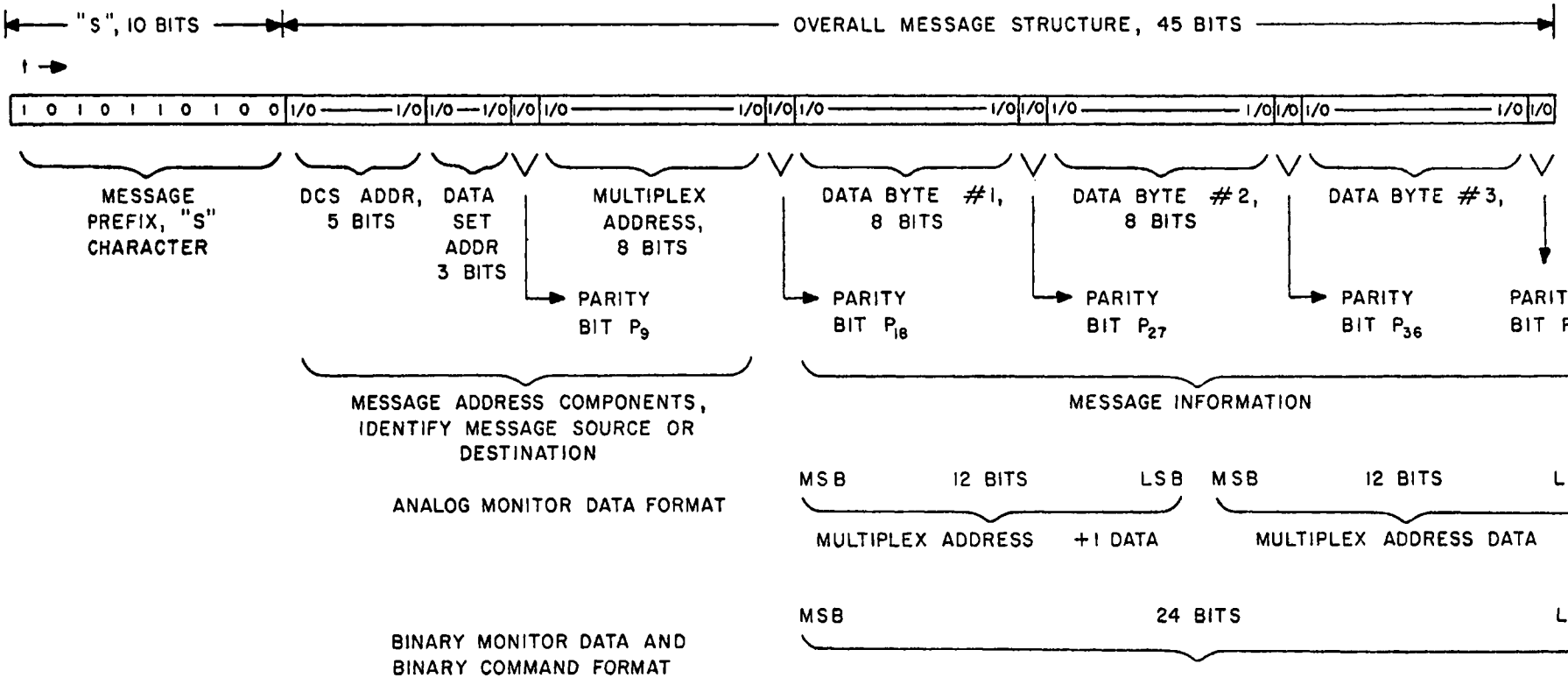
This manual describes the Data Tap (M2) Monitor and Control System module and is intended to serve as the principle repair and maintenance guide for this unit. It may also be useful for those who are interested in the Data Tap Message storage logic.

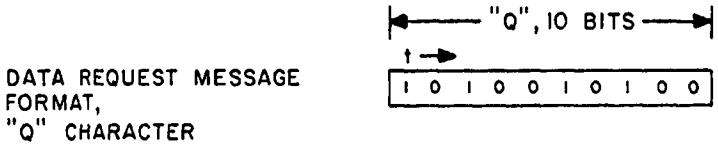
The Data Tap provides the facility to conveniently detect, store and display Command and Monitor Data messages without the participation of the control computers. The Data Tap may also be used for analog recording as it has two D/A converters which convert Analog Monitor Data messages back to two analog voltages which may be patched to analog recorders. The reader is referred to the Data Set Manual for details on the conversion and packing of two analog voltages into one Analog Monitor Data message.

Figure 1 depicts the Command and Monitor Data message format.

The Data Tap is not a serial element in the distribution of Command and Monitor Data messages but is "Tapped" onto the message flow as they are distributed through the system.

The operator may cause message trapping to be conditional on the occurrence of messages which match the front panel address switch settings or the occurrence of messages which have been tainted by errors. Message trapping on the basis of message information content is not normally possible with the present design but has been done on an improvised basis. The Data Tap may be connected to any Data Set in the system, to the Central Buffer or to the Serial Line Controller. When connected to a Data Set the Data Tap detects and displays messages which have a 10 μsec/bit rate and when connected to either the Central Buffer or SLC the Tap detects and displays messages which have a 1 μsec/bit rate. The Central Buffer/SLC connection provides access to <u>all</u> Command and Monitor Data messages which are circulated around the Electronics/Control Room environment. When the Data Tap is connected to a Data Set in the antenna it is able to trap and display all messages locally available in the





MESSAGE DATA RATES

PATH	MSG	"S" & "Q" BIT RATE	MESSAGE BIT RATE
CB/SLC	CMD/MON/Q	.5 μs	1 μs
CB/DS	CMD/MON/Q	5 μs	10 μs
CB/AB	CMD	2 μs	4 μs
AB/DS	CMD/MON/Q	5 μs	10 μs
AB/CB	MON	10 μs	20 μs

FIGURE 1: COMMAND AND MONITOR DATA MESSAGE FORMATS

antenna which consist of commands addressed to the antenna and data from the antenna Data Sets. A connection to the Central Data Set is a trivial connection as it is exposed to only the Command Messages directed to the Data Set and no other messages.

The reader is referred to the Monitor and Control System manual for a description of the system usage of the Data Tap.

2.0 FRONT PANEL CONTROLS AND DISPLAYS

Figure 2 shows the location and marking of the front panel controls and displays. Figure 3 depicts the message storage logic. The Parity/Address switch determines whether the tap stores parity error tainted messages or messages based upon the address content. In the parity position only parity tainted messages will be stored and the message address and information components displayed for interpretation of the malfunction. Since the address components of an error tainted message may be in error one should be cautious in the inferences drawn from this displayed information. The red parity error LED is illuminated for each occurrence of a parity error irrespective of the position of the Parity/Address or any other switch.

When the Parity/Address switch is in the address position the tap will store and display messages in accordance with the settings of the address thumbwheel and sel/any toggle switches. When the sel/any toggle switches are in the sel position the tap will store and display only messages having address components identical to those set on the address thumbwheel switches. In the any position the sel/any switches substitute a "Don't Care" condition for the associated thumbwheel address comparison in the message decode logic. This variable address decode selectivity can enable one to view a "flow" of messages for an overview of the composition of data associated with a message source or destination. For example, by setting an antenna Data Tap to DCS Addr = 00, DS Addr = 2, Max Addr to "Any" the whole flow of Monitor Data messages from Data Set #2 may be observed on the display. Another interesting case is DCS Addr = actual, DS Addr = 2 and Max Addr = any. This setting allows the periodic bursts of fringe rate and phase and Walsh function commands to be trapped and displayed.

Whenever the tap detects a match of address conditions with message conditions and stores the message, the green update LED is

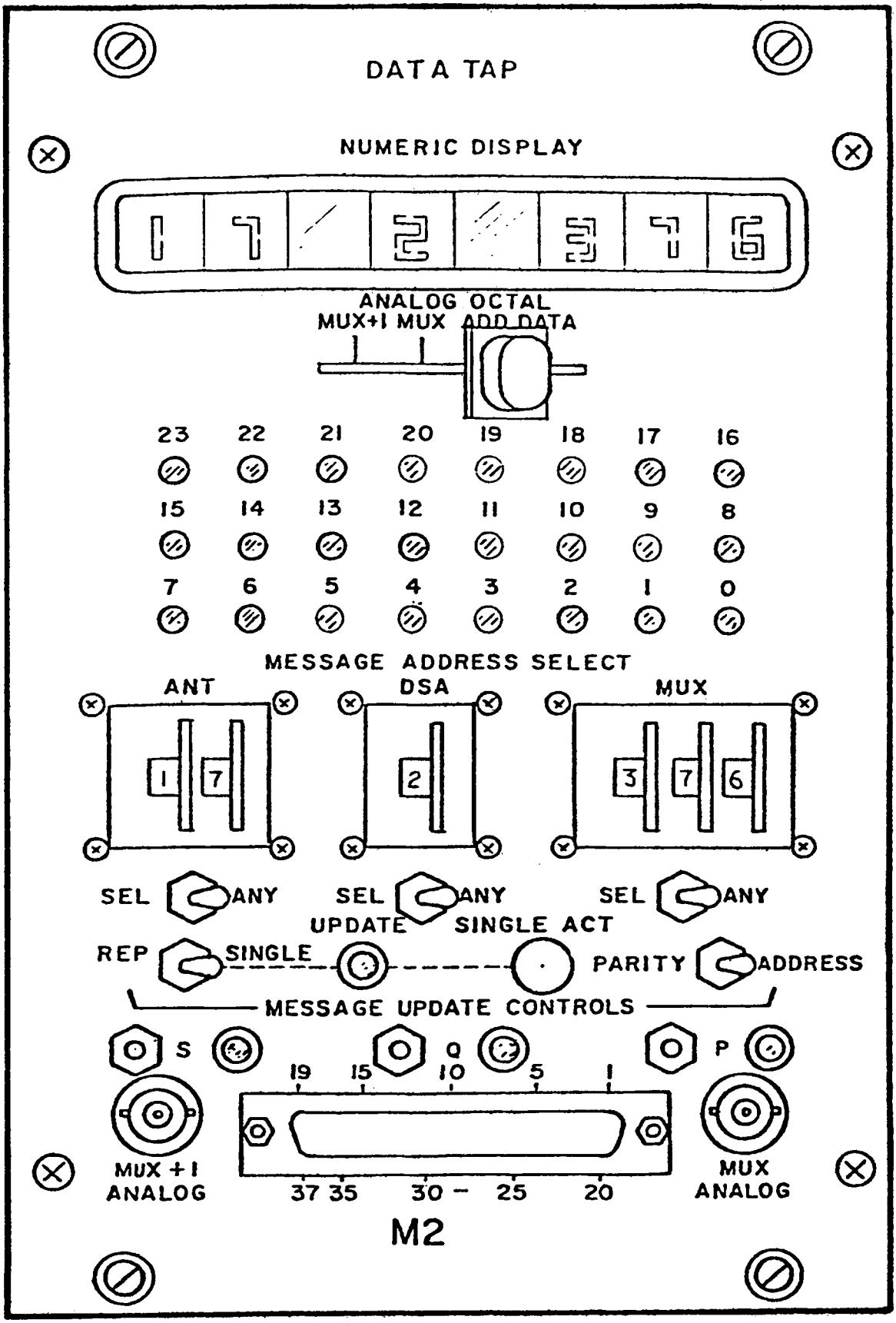


FIGURE 2: DATA TAP CONTROL/DISPLAY PANEL

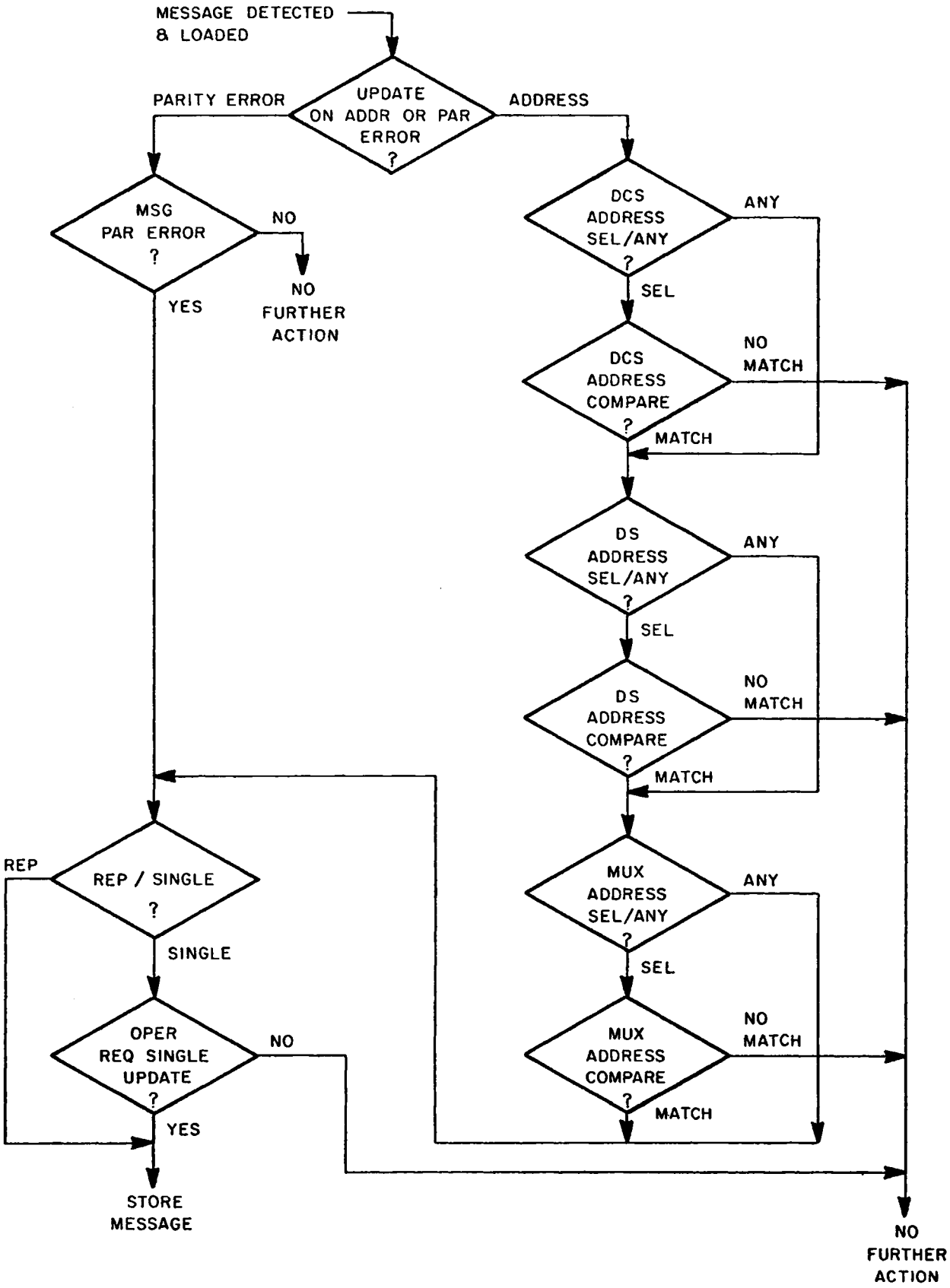


FIGURE 3: MESSAGE STORAGE LOGIC

briefly illuminated. The single/rep toggle switch controls the frequency of message updating. In the Rep (for repetitive) position the tap will update each time the message components match the switch settings. In the single position the tap will update once for each activation of the single activate push button switch. This mode is useful when the tapped message composition is highly variable and it is difficult to analyze a continuously changing display.

The numeric LED display can be used to display the trapped message in several formats. When the display control switch is in the octal position, the 24 information bits of the message are displayed in eight digit octal format. When the switch is in the address position, the message address components are displayed in six digit octal format. In the Mux and Mux + 1 position, the upper or lower half of the 24 bit message is selected, multiplied by five and converted to BCD so that the data is displayed in decimal bipolar format (i.e., + or -) volts with a decimal point. This operation rescales the digital data to the equivalent analog voltage. The resolution of this display is 5 milli-volts which is the Data Set A/D resolution. Of course, this display is only meaningful when the data is associated with an analog data message. Older data tap models (A and B) use the labels "Right" and "Left" to designate the Mux and Mux +1 analog data components respectively.

An array of 24 LED's displays the 24 message bits and is convenient for interpretation of Binary Monitor Data messages.

The Q and S LED's indicate the detection of these message components.

3.0 LOGIC CIRCUITRY DESCRIPTION

Figure 8 is the Data Tap Top Assembly Drawing. Figure 4 depicts the Data Tap Logic Block Diagram.

3.1 Message Loading Logic and Data Rates

The message loading logic is found on Sheet 1 of the logic diagrams.

Central Buffer and Serial Line Controller messages are input via the optical isolator A26. Data Set messages are input to the exclusive or gate A3003. When the Central Buffer/SLC input is used, pin J4-26 should be grounded.

Edge detector A3013 phase adjusts counter A24 and A22 which generates clocks to sample the input message which is shifted into shift register A14. The message preamble, the "S" character is detected by gate A1510 which resets flip flop B0805. This flip flop is clocked by the 10 MHz clock and is reset during the time that the "S" detector gate is true. B0805 turns on the format counter A13 and A12 by causing control flip flop A1811 to lift the counter's preset enable. Counter term A13-14 is used as a shift clock to serially load the incoming message into the Message Input Register. When the counter reaches a state of 99 the message is completely loaded in the register so the counter is turned off by gate B0910 which resets control flip flop A1811. The output of gate B0910 is also used as a strobe in the message parity and storage decision logic on Sheet 3.

Counter A24 and A25 operate with two radices: ÷ 5 and ÷ 50 which are selected by the Hi/Lo jumper wire on pin J4-01 on the rear I/O connector pin. When J4-01 is jumpered to J4-02 (grounding pin 3 on nor gate A22) the counter radix is 50 which produces a 200 kHz shift clock at A2211. This rate is used in the antenna when the Data Tap is connected to an antenna Data Set. If pin J4-01 is not jumpered to ground, counter A22 radix is ÷ 5 and produces a 2 MHz shift clock at A2211. The key to the radix control lies in gate B1704 which

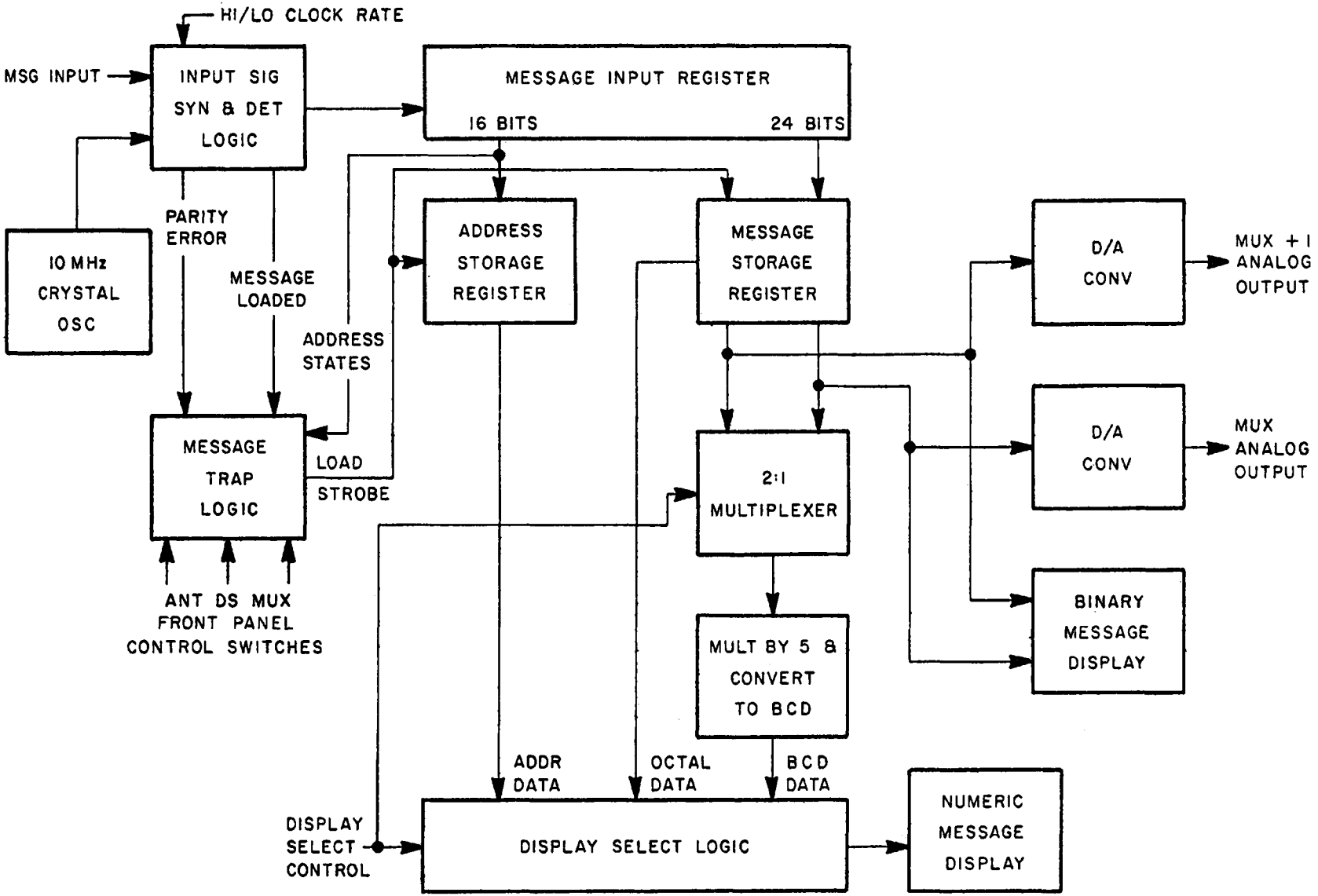


FIGURE 4: DATA TAP BLOCK DIAGRAM

passes the TC carries from A2415 through to A2207 in the ÷ 50 mode and permits A22 to count each 10 MHz clock in the ÷ 5 mode. The ÷ 5 mode is used in loading SLC/Central Buffer messages. When pin J4-01 is floating, A22 sequences through the states 5, 6, 7, 8, 9, 5, 6, etc., and when J4-01 is grounded A24 and A22 sequence through the states 41 to 90.

The "S" character and the "Q" character LEDs are illuminated to indicate the detection of command/monitor and data request messages respectively. Figure 5 depicts the message load timing.

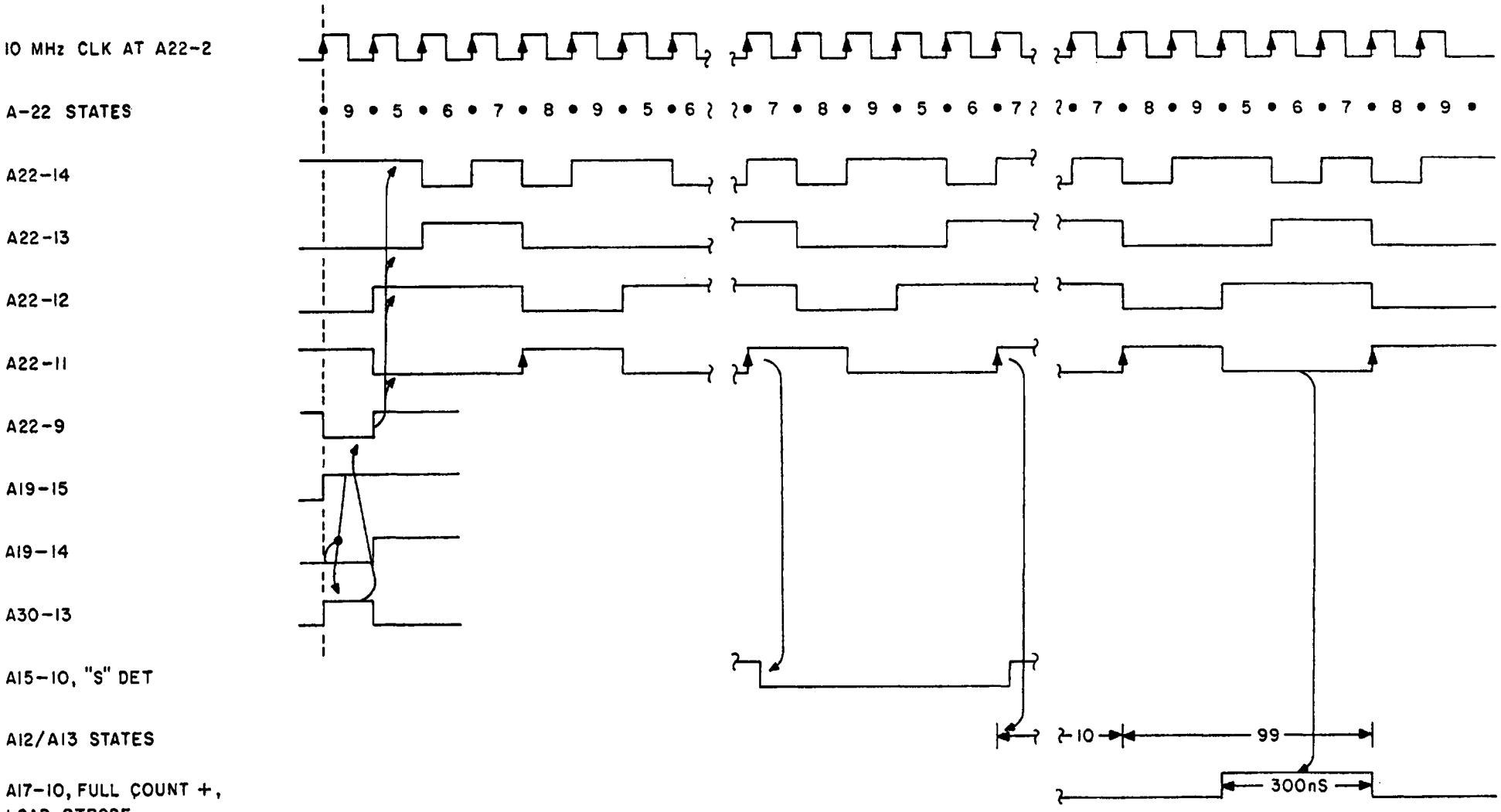
3.2 Storage Decision Logic

The message storage logic depicted in Figure 3 is found on sheet 3 of the logic diagrams.

Flip flop A1106 is the parity analysis flip flop and is toggled whenever a message bit is a "1." At the completion of the load sequence the full count term from A1710 tests the state of A1106 and sets flip flop B0811 if the message was tainted by a parity error.

If the Parity/Address switch is in the Parity position, gate A0903 causes the error tainted message to be parallel transferred from the Message Input Register B11, B12, B13, B20 on sheet 2 and A1 and A6 on sheet 3 to the Message and Address Storage Register's E1, E2, E6, E7, E11, E12 on sheet 2 and C1, C2, C6 and C11 on sheets 8 and 6. The Parity LED is illuminated whenever an error is detected.

When the Parity/Address switch is in the Address position the comparators A2, A4, A5 and B5 compare the address components set on the DCS, DS and MUX address thumbwheels with the message address components standing in registers A6 and A1. Nor gates B1406, B1410 and B1413 provide the "Don't Care" conditions for the DCS, DS and MUX Sel/Any switches respectively. Gate A0806 senses the equals (or associated "Don't Cares") condition of these



NOTE: THE TIMING RELATIONSHIPS DEPICTED IN THIS DIAGRAM ARE ASSOCIATED WITH CB/SLC MESSAGES.

FIGURE 5: MESSAGE LOAD TIMING DIAGRAM

comparators and causes contents of the Message Input Register to be loaded into the Message and Address Storage Registers. The message update LED is illuminated by the pulse stretching one-shot E2507.

3.3 Data Selection Logic

With the message address and information bits safely tucked away in the Message and Address Storage Registers (E1, E2, E6, E7, E11, E12 on sheet 2 and C1, C2, C6 and C11 on sheets 8 and 6) the data selection logic selects the data for display on the numeric display. The display selector switch controls two and three channel multiplexers on sheets 4, 6, 7 and 8 to select for display either the 24 data bits or the address components. The selector switch also conditions the display logic to display the negative sign, decimal point, suppresses leading zeros in the analog display and blanks unused digits in the address display. In the octal address and data positions the address and information components are displayed in octal format.

In the octal data or address position either the 24 message information bits or 16 address bits are selected for display in octal format on the eight digit numeric display. Two digits are blanked in the address display to improve readability. See Figure 2 for an example of a typical address display.

In the analog position either the upper or lower (Mux/Right or Mux +1/Left) 12 bits stored in the Message Storage Register are selected, multiplied by 5 and converted to BCD as described in section 3.4 of this manual.

3.4 Analog Data Multiplication/Conversion Logic

In the analog positions of the selector switch, either the 12 upper or lower bits of the 24 information bits stored in the Message Storage Register are selected, multiplied by 5 and converted to BCD for display. Two channel multiplexers B7, B18

and B19 on sheet 4 perform this upper/lower 12 bit selection. The output of these multiplexers drive the full adders B21, B26, B23, B27, B29, B24 and B25. These adders implement the multiply by 5 operation by a right shift 2 bits (multiply by 4) which is added to unshifted data. The adder outputs are thus scaled five times higher so that the data LSB now is weighted at 1 millivolt which is one-fifth of the weight of the Data Set A/D converter LSB (five millivolts). The MSB causes negative values to be complemented via exclusive or gates B6, B15 and B22. The adder output is routed to the binary to BCD conversion logic on sheet 5.

The 12 bit binary to BCD converter transforms the multiplied 16 bit binary value to a 5 digit BCD format for presentation to the data selection and display logic described in section 3.3 and 3.5. The converter operates as a parallel converter using 74185 binary to BCD converters in locations C7 through C29.

3.5 Display Logic

The logic and front panel display circuitry are depicted on sheet 3.

The data selected for display by the logic described in sections 3.3 and 3.4 is routed to an 8 channel, four bit multiplexer which sequentially scans the data on a digit by digit basis and converts the four BCD (or octal) data bits to a seven segment numeric LED drive format. The multiplexer consists of 9312 chips in locations D22, D23, D18 and D13 whose outputs are the 1, 2, 4 and 8 BCD bits respectively, which drive a 7447 BCD to seven segment decoder/driver on the display assembly pc board. The multiplexer 3 bit select lines are driven by counter D8 which is incremented by a 5 kHz (nominal frequency) oscillator D9. The 7 segment drive lines from the decoder are bussed to the segments of all eight LEDs. The LEDs are illuminated by switching transistors which sequentially switch on the LED anode voltage.

These transistors are driven by a 9301 1 of 10 decoder in E18 which is also driven by the 74161 sequencing counter D8. The synchronous decode/drive and anode enable of these two sets of circuits sequentially illuminate the eight digit display. The decimal point of digit 5 is illuminated by E15 (A DTL 944 open collector power nand) when the display is used for analog data. The two leading (DS1 and DS2) and last (DS7) digits of the display are also blanked in the analog display mode. In the address mode digits 3 and 5 (DS3 and DS5) are blanked.

The numeric display LED segments have a rather heavy pulse current (limited by 39 Ω, and the LED, 7447 and transistor drops) which can perturb the L.O. system through high frequency harmonics of the digit scanning clock. The display power is filtered to subdue these harmonics by an LC "pi" filter mounted in the front portion of the data tap.

The 24 bit LED display (bits 23 through 0) displays the 24 bits stored in the Message Storage Register. Bits 23 and 0 are the MSB and LSB of the information bits respectively. This display is most convenient for display of binary or discrete states.

3.6 D/A Conversion Logic

When the Data Tap updates by trapping a new message in the process described above, the 24 bit message storage register (E1, E2, E6, E7, E11 and E12) is parallel-loaded with the 24 bits of message information. Two digital-to-analog converters (on sheet 2) then convert the upper and lower halves of the stored data into equivalent analog voltages which are available at front panel BNC connectors and are also wired to the rear panel I/O connector.

The digital data stored in the Message Storage Register is 12 bits 2's complement format and is converted to offset binary by inversion of the MSB of each 12 bit byte.

Model A and B versions of the Data Tap use 12 bit D/A converters packaged on a detachable auxiliary chassis fastened to the module rails. The resolution of the DAC analog outputs is 5 millivolts/bit-identical to the Data Set, so that the range of the analog outputs is +10.235 to -10.240 volts corresponding to $(2^{11} - 1)$ x 5 mv and 2^{11} x 5 mv respectively (in 2's complement coding). The output impedance of these converters is 0.1 Ω, and they are capable of sourcing/sinking 5 MA. There are no provisions for changing the scaling of the DAC outputs; if scaling is required, it must be done in the recorder or meter circuitry and must be consistent with the DAC source impedance and current drive capabilities cited above. Data Taps serial numbers A1 through B24 use this DAC configuration.

The other (Model C) DAC configuration uses 10 bit multiplying DACs which are packaged in 16 pin dip's. These DAC's, associated operational amplifiers and a DAC reference supply are mounted on the logic connector board along with the Data Tap logic circuitry. This DAC configuration was chosen as it uses less expensive DACs, eliminates a clumsy DAC packaging physique which makes maintenance access difficult and reduces Data Tap fabrication and assembly costs.

This DAC configuration has a resolution of 20 mV per bit which is adequate for the average strip chart recorder application. If higher resolution is required the older models may be used. The upper 10 data bits of the Message Storage Register are input to the DACs. The DACs are current devices and use external operational amplifiers to provide a voltage output. The DACs require an external reference voltage supply of -10 volts which is provided by the LM299H precision reference in D27 and AD741KN operational amplifier in E29. The DAC is configured for bi-polar (4 quadrant) operation, see the AD7520 Data Sheet in the back of this manual for details on the usage of this device. The source impedance and current capability of this DAC configuration are .15 Ω and 4.5 ma respectively.

3.7 DAC and Binary-to-BCD Converter Alignment and Test

This section is based on Model C Data Taps, though Model A and B units may be aligned in a similar manner; however, all test points, voltage measurements and adjustments apply to Model C versions only.

The DAC and binary-to-BCD converter sections are aligned in a three step process - (a) alignment of the Reference Voltage Power Supply (RVPS) to establish a precision -10 V DAC reference voltage, (b) alignment of the associated operational amplifier circuits to compensate for offsets and establish full-scale gains, and (c) exercising the binary-to-BCD converter to determine proper operation. Refer to Figure 6 for test point and adjustment locations.

3.7.1 Reference Voltage Power Supply Alignment (Rev C Only)

The RVPS consists of an LM299H, a monolithic precision zener diode reference and an AD741KN OP AMP. The output of the LM299H at D27 is +6.95 V ± 2% and exhibits a long term stability of 20 parts per million/year insuring a stable precision reference. This +6.95 V is applied to the inverting input AD741KN at E29 and amplified to -10.000 V ± 10 mV. The gain is about 1.43 and fine adjusted by resistor E30-4, 5, 12.

Alignment of the RVPS is simply as follows:

Step 1 - Measure +6.95 V ± 2% at LM299 output at D-27-2 ⟨A1⟩ Figure 6.

Step 2 - Measure voltage at 741 output at E29-14 using a DVM with 1 mV accuracy and resolution. ⟨A2⟩ Figure 6

Setp 3 - Adjust trim-pot at E30-4,5,12 for -10.000 V ± 1 mV reading on DVM. ⟨A3⟩

If -10.000 ± 10 mV cannot be obtained and Step 1 voltage is normal, fine trimming of the coarse gain resistor may be required as follows:

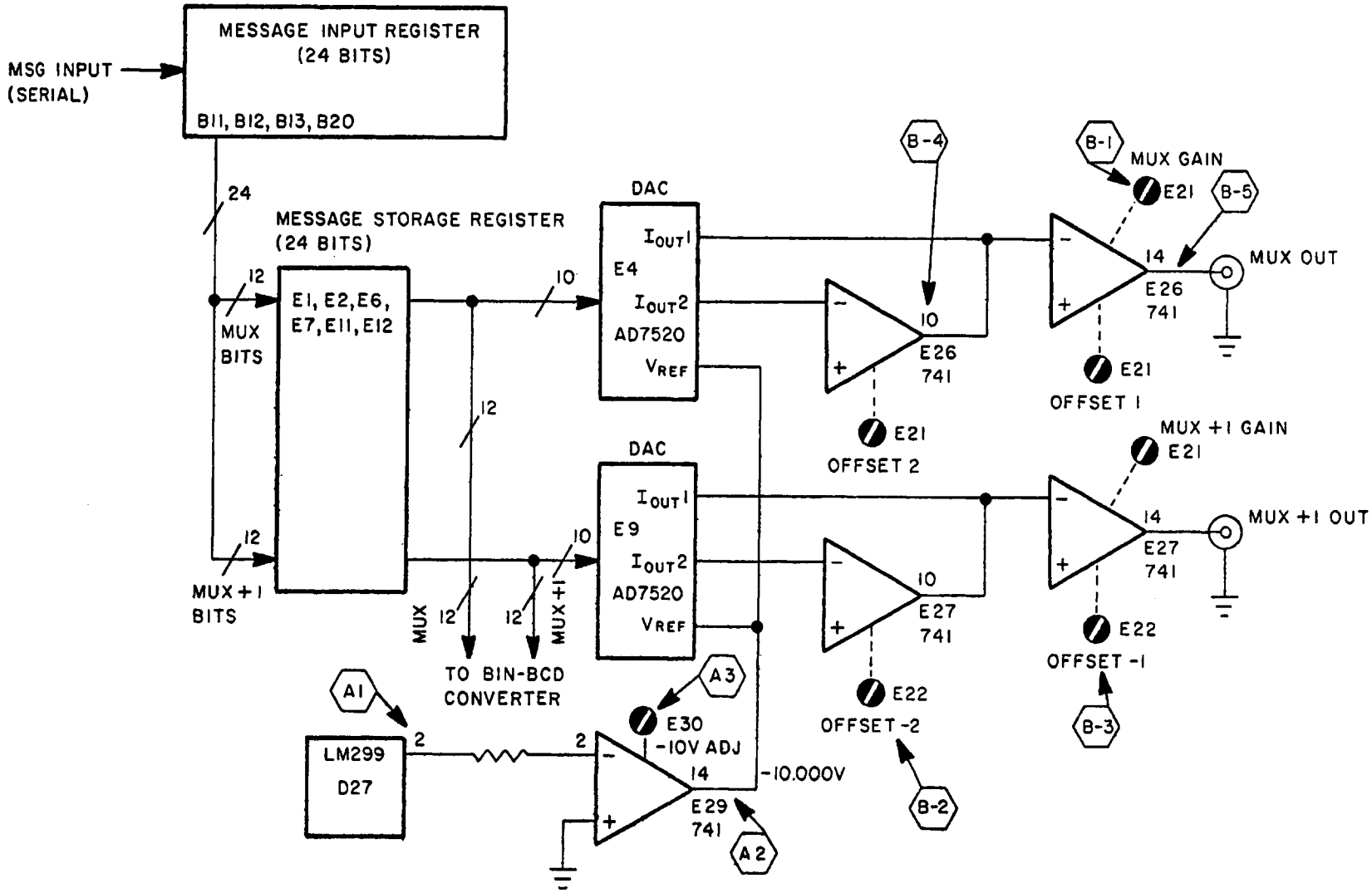


FIGURE 6: DAC ALIGNMENT SCHEMATIC

Step 2 - Voltage > -10.000 V (i.e., -9.8) INCREASE value of resistor at E30-6, 11.

Step 2 - Voltage < -10.000 V (i.e., -10.2) DECREASE value of resistor at E30-6, 11.

Resistor E30-6, 11 should be trimmed in increments of 500 ohms so that the range of the gain trim-pot E30-4,5, 12 is not exceeded.

3.7.2 DAC and OP AMP Alignment

A message source (typically the Monitor and Control System Test Bench) is applied to either the Data Tap messege input or internally to the DAC digital inputs to produce a series of bit patterns corresponding to plus full-scale (+FS), minus full-scale (-FS) and center-scale (CS). These three conditions are essential to properly adjust the full scale gains and to compensate for offsets in the output amplifiers.

As discussed in paragraph 3.6, the input binary bit pattern is converted to offset binary by inversion of the MSB of each 12 bit byte by the Data Tap logic. Hence, the bit patterns used for this alignment differs depending upon where this digital data is introduced to the logic. Table 1 shows the bit patterns and the relationship to the analog output.

Table 1 is the complete alignment procedure for the Model C DAC circuitry and basically consists of the following steps:

1) Insuring ± 15 V input is acceptable
2) Selecting FS and coarse set GAIN ADJ for about +10.3 V and then zeroing offset error in the I OUT 2 amplifier
3) Selecting CS and zeroing offset error in I OUT 1 amplifier

Table 1 - Model C Data Tap (AD7520) DAC Alignment Procedure

Cautions:

1. Do not remove or install the AD7520 DAC devices with power applied. The AD7520's are CMOS devices and should be handled accordingly.
2. Do not use "live" antenna data for alignment bit-pattern standard; i.e., comparing Analog Display voltages to DVM reading on front panel BNC output jacks.
3. Do not perform this alignment prior to alignment of Ref. Voltage Power Supply.

Step	Test Function	Correct Reading	Input Data	Test Point MUX	Test Point MUX +1	Adjustment MUX	Adjustment MUX +1	Figure Ref.
1.	Test +15 V input	+15.000 ± 50 mV	-	E26-15	E27-15			
	Test -15 V input	-15.000 ± 50 mV	-	E26-4	E27-4			
2.	Adjust GAIN	+10.3 V ± 0.1 V	+FS	E26-14	E27-14	E21-9,10	E22-9,10	B-1 ADJ
	Adjust OFFSET -2	0.000 V ± 5 mV	+FS	E26-10	E27-10	E21-1,3	E22-1,3	B-2 ADJ
								B-4 TEST
3.	Adjust OFFSET -1	0.000 V ± 1 mV	CS	E26-14	E27-14	E21-4,6	E22-4,6	B-3 ADJ
				or	or			B-5 TEST
4.	Adjust GAIN	-10.240 V ± 10 mV	-FS	MUX OUT	MUX +1	E21-9,10	E22-9,10	B-1 ADJ
				BNC	OUT BNC			B-5 TEST
5.	Adjust GAIN	+10.220 V ±	+FS			E21-9,10	E22-9,10	
6.	Adjust OFFSET -1	0.000 V ± 1 mV	CS			E21-4,6	E22-4,6	
7.	Insure...+FS =	+10.220 V ± 10 mV	+FS					
	+CS =	0.000 V ± 1 mV	CS					
	-FS =	-10.240 V ± 10 mV	-FS					

FIGURE 7: MODEL C DATA TAP (7520) DAC ALIGNMENT PROCEDURE

Table 1 (Cont'd)

Input Data Code States

(12 Bit Byte Patterns)

	+FS	CS	-FS
DATA TAP INPUT	011 111 111 111	000 000 000 000	100 000 000 000
DAC DIGITAL INPUT (Offset Binary Code)	111 111 111 1XX MSB	100 000 000 0XX MSB	000 000 000 0XX MSB
ANALOG OUTPUT	+10.220 V ± 10 mV	0.000 V ± 1 mV	-10.240 V ± 10 mV

FIGURE 7 (CONT.)

4) Selecting -FS and fine set GAIN ADJ for - 10.240 V ± 10 mV
5) Selecting +FS and insuring output is + 10.220 V ± 10 mV and correct if necessary
6) Selecting CS and insuring output has remained zeroed (0.000 V ± 1 mV) and correct if necessary

Models A and B applicability: This alignment procedure may be utilized on A and B which use the CY2235 DAC. Use front-panel BNC analog output jacks for voltage monitoring. Adjustments for OFFSET and GAIN are marked on the CY2235 DAC assembly.

3.7.2 Binary to BCD Converter Tests (Applies to all models)

The binary to BCD Converter section is tested in a manner similar to the DAC alignment by introducing established bit patterns in the Message Storage Register (E1, E2, E6 for MUX data and E7, E11 and E12 for MUX +1 data) to exercise the converter and check for proper operation.

As described in section 3.4, the Display Selector switch is placed in either the MUX or MUX +1 position to enable the converter, select the proper byte of the input message bits, and route the results in formatted form to the decimal LED display. The converter operation is tested by exercising the bits, one-by-one, to verify that the multiply by 5 and the array of 74185 binary-to-BCD converter devices are functioning.

A brief test is as follows:

Message Bit Pattern	Display (MUX or MUX +1 Position)
000 000 000 000	+ 0.000
000 000 000 001	+ 0.005
000 000 000 010	+ 0.010
000 000 000 100	+ 0.020
000 000 001 000	+ 0.040
000 000 010 000	+ 0.080
000 000 100 000	+ 0.160
000 001 000 000	+ 0.320
000 010 000 000	+ 0.640
000 100 000 000	+ 1.280
001 000 000 000	+ 2.560
010 000 000 000	+ 5.120
100 000 000 000 MSB	-10.240

This simplistic test will provide a confidence test of the logic; failure will require that the logic be tested in more detail to detect stuck bits. The multiply by 5 logic is tested first by setting in a single bit message in ascending order from a message state of 000 000 000 000. Each multiplication may be easily tested by examining the associated adder outputs.

When the multiplication logic operation has been verified the binary to BCD logic may be tested by repeating the ascending order single bit messages used above and examing the propagation of the converted code through the conversion tree. The 74185 chip algorithm is: a) examine the 3 most significant bits; if the sum is greater than 4, add 3 and

shift left 1 bit, b) otherwise, pass the data through unaltered. The reader is referred to logic data books for a more extensive discussion. The ascending order single bit messages will generally enable the stuck bit(s) to be isolated to a few chips. By examining the chip inputs and outputs the faulty chips may be identified by non-conformance to the above algorithm.

3.8 I/O Connector Pin Assignment

J4-10	+5 Logic Power
J4-34	Logic Common
J4-16	+15 Volts
J4-17	-15 Volts
J4-42	Hi-Q ground
J4-14	Central Buffer/SLC Data Input-Hi
J4-15	Central Buffer/SLC Data Input-Return
J4-26	Data Set Data Input (ground for use with LB/SLC)
J4-38	Mux Analog Output
J4-5	Mux +1 Analog Output
J4-1	Hi/Lo Select, (ground for use with Data Set)

3.9 Test Point Connector Pin Assignments

J2 Pin	Logic Tie	Function
1	D5-13	Message Storage Register Bit 23, (MSB)
2	D5-10	" " " " 22, "
3	D5-6	" " " " 21, "
4	D5-3	" " " " 20, "
5	D10-13	" " " " 19, "
6	D10-10	" " " " 18, "
7	D10-6	" " " " 17, "
8	D10-3	" " " " 16, "
9	D15-13	" " " " 15, "
10	D15-10	" " " " 14, "
11	D15-6	" " " " 13, "
12	D15-3	" " " " 12, "
13	D20-13	" " " " 11, "
14	D20-10	" " " " 10, "
15	D20-6	" " " " 9, "
16	D20-3	" " " " 8, "
17	D25-13	" " " " 7, "
18	D25-10	" " " " 6, "
19	D25-6	" " " " 5, "
20	D25-3	" " " " 4, "
21	D30-13	" " " " 3, "
22	D30-10	" " " " 2, "
23	D30-6	" " " " 1, "
24	D30-3	" " " " 0, (LSB)
25	N/U	
26	D29-3	Parity Error Detect
27	E25-9	Q Character Detect
28	E5-3	S Character Detect

J2 Pin	Logic Tie	Function
29	A26-2	LB/SLC Input
30	A30-3	Data Set Data, lo-true
31	E5-6	Input Shift Clock
32	N/U	
33	N/U	
34	N/U	
35	N/U	
36	N/U	
37	N/U	

4.0 DOCUMENTATION TREE

Top Ass'y Dwg - D13720P9
Top BOM - A13720Z3

LED MTG BD ASS'Y

Ass'y Dwg C13720P42

Ass'y BOM A13720Z13

Drill Dwg C13720M39

Artwork B13720AB4

LED DISPLAY ASS'Y

Ass'y Dwg D13720P33

Ass'y BOM A13720Z12

Drill Dwg C13720M40

Artwork B13720AB8

LED DISPLAY SUB-ASS'Y

Ass'y Dwg C13720P34

Ass'y BOM A13720Z11

Drill Dwg C13720M34

Artwork B13720AB7

D/A CONVERTER ASS'Y

Ass'y Dwg C13720P36

Ass'y BOM A13720Z5

PC Board Support C13720M11

DUAL 12 BIT CONV PC BD

Ass'y Dwg D13720P35

Ass'y BOM A13720Z7

Drill Dwg C13720M35

Artwork C13720AB10

IC MODULE PANEL

Ass'y Dwg-C13720P30

Ass'y BOM-A13720Z6

DIP HEADER SUB ASS'YS

ASS'Y DWG	ASS'Y BOM
B13720P16	A13720Z9
B13720P17	A13720Z8
B13720P13	A13720Z42
B13720P29	A13720Z45
B13720P14	A13720Z10

MECHANICAL PARTS

Front Cover-B13050M34-1
Top Support-B13050M34-2
Bottom Support-B13050M34-3
Left Side Plate-B13050M35
Support Power-B13050M38
Cover Perf-B13050M40
Panel Rear-B13050M41
Support Bottom-B13050M42
Rail Modification-C13720M9-1
Rail Modification-C13720M9-2
Rail Modification-C13720M10-1
Rail Modification-C13720M10-2
Spacer Rails-C13720M13
Guide Block-B13050M4
Engraved Panel-D13720M21
Spacer-B13720M47
Polarized Screen-B13720M8-1
Clear Filter-B13720M8-2

MASTER WIRE LIST

A13720W4 Rev B

HAND WIRE LIST

A13220W6 Rev B

MACHINE WIRE LIST

A13720W5 Rev B

POWER WIRING DIAGRAM

C13720W40 Rev B

CONNECTOR I/O LISTS

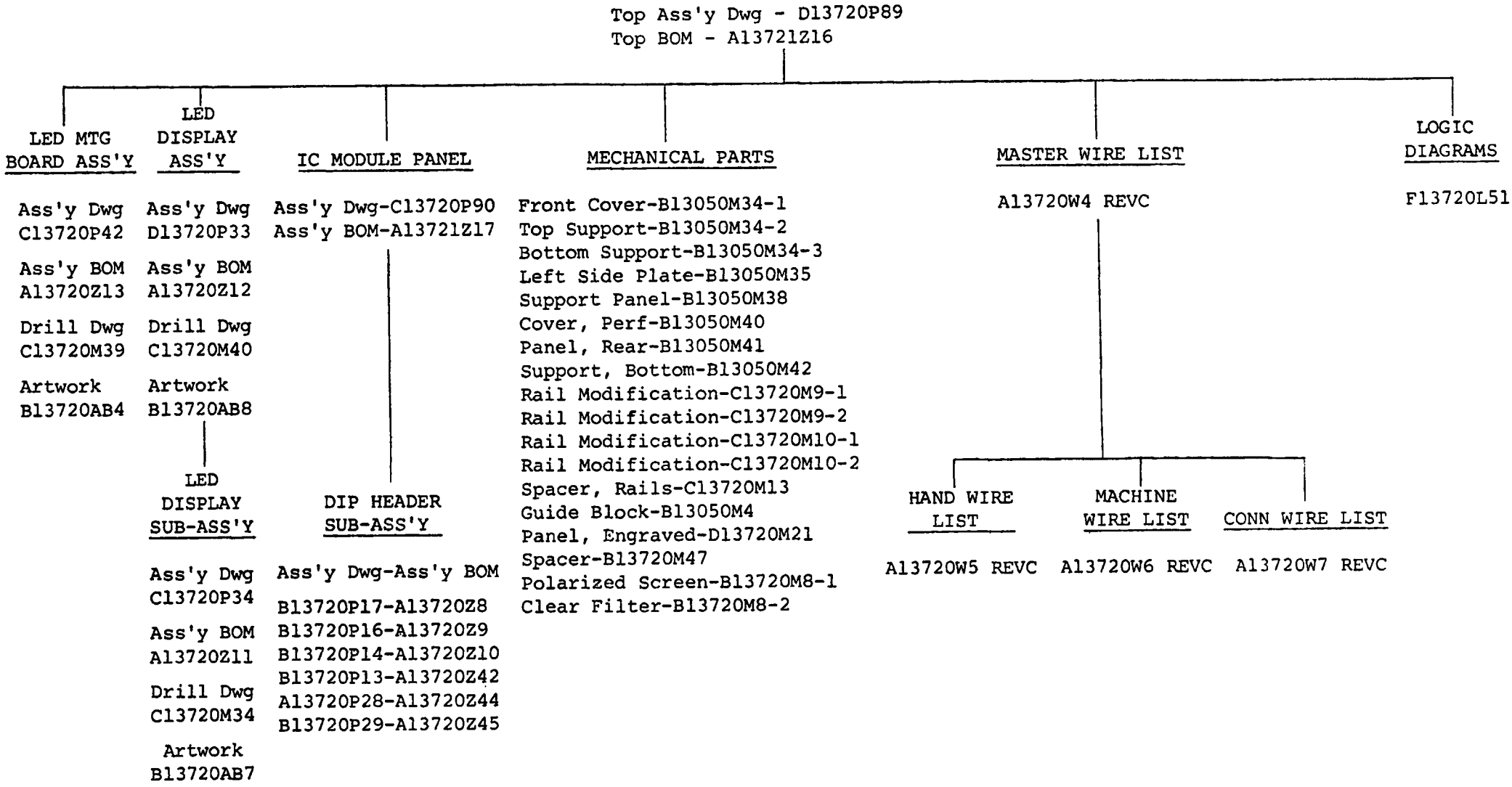
A13720W7 Rev B

LOGIC DIAGRAMS

F13720L38

DATA TAP MODEL B

DOCUMENTATION TREE



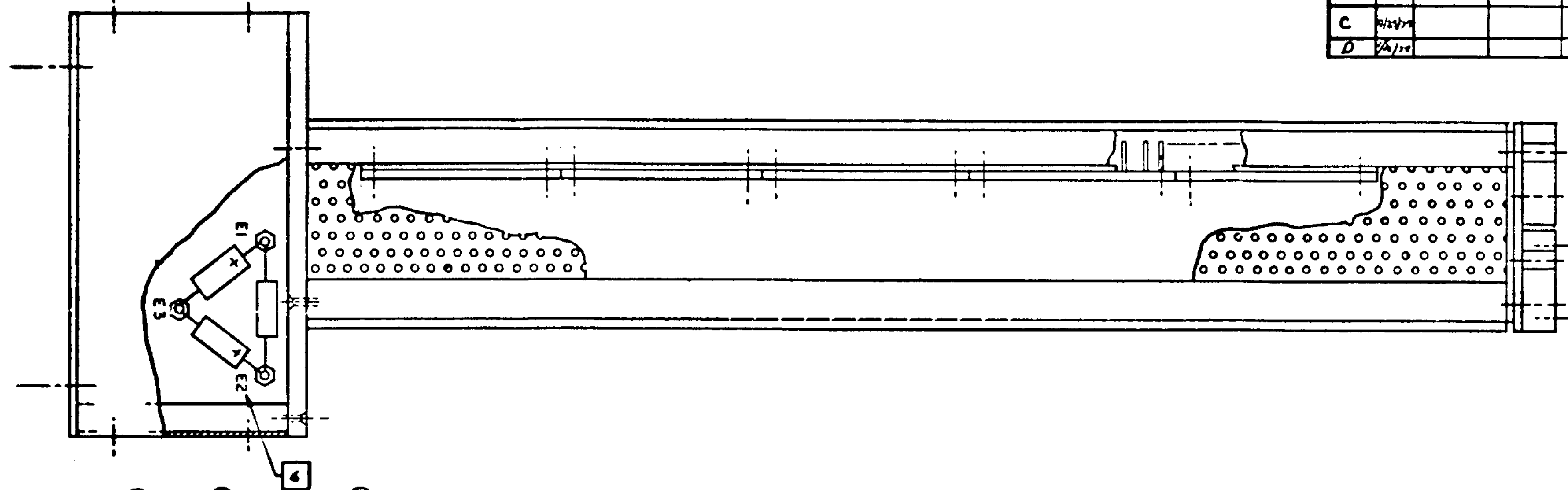
DATA TAP DOCUMENTATION TREE

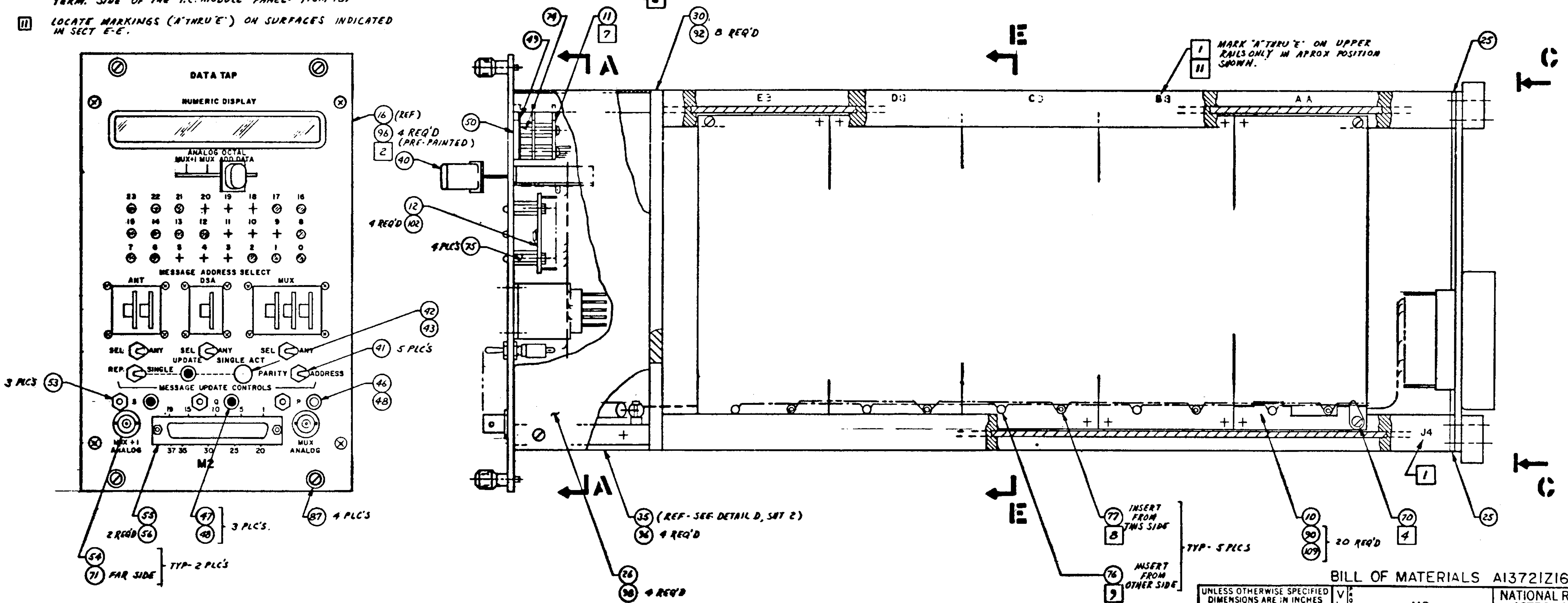
MODEL C

NOTES:

1. MARKING SHALL BE 1/8" HIGH, LEGIBLE AND PERMANENT. LOCATE APROX. AS SHOWN.
2. A WIRING SERVICE LOOP OF SUFFICIENT LENGTH TO ALLOW THE FRONT & REAR PANELS TO BE FOLDED FLAT MUST BE PROVIDED.
3. WHERE TWO WASHERS (ITEM 112) ARE REQ'D PLACE ONE UNDER THE SCREW HEAD AND THE OTHER BETWEEN THE GUIDE (ITEM 17) AND THE REAR PANEL (ITEM 34).
4. SOLDER "SOLDER LUG" (ITEM 70) TO "GND" PLANE AND PLACE UNDER SCREW HEAD APROX. AS SHOWN.
5. LEADS TERMINATING AT POS. 10, 34 & 42 USE ITEM NO. 64
   LEADS TERMINATING AT POS. 16 & 17 USE ITEM NO. 63
   LEADS TERMINATING AT POS. 5, 6, 7, 38, 39 & 40 USE ITEM NO'S 65, 66 & 67.
6. THE WIRE LIST REFERS TO TERMINALS E1, E2 & E3 AS FOLLOWS:
   E1 - TERM. "FLTOUT"
   E2 - TERM. "FLTIN"
   E3 - TERM. "FLTGND"
7. INSTALLATION OF THE L.E.D. DISPLAY ASSY (ITEM 11) REQUIRES THE DISCARDING OF THE FOUR HEX NUTS USED TO HOLD THE ASSY. TOGETHER PRIOR TO INSTALLATION.
8. SOLDER GND TERM. (ITEM 77) TO GND PLANE (COMPONENT SIDE OF I.C. MODULE PANEL - ITEM 10).
9. SOLDER PWR TERM. (ITEM 76) TO PWR PLANE (WIRE-WRAP TERM. SIDE OF I.C. MODULE PANEL - ITEM 10).
10. THE PWR & GND BUS WIRING SHALL BE ON THE WIRE-WRAP TERM. SIDE OF THE I.C. MODULE PANEL - ITEM 10.
11. LOCATE MARKINGS ("A" THRU "E") ON SURFACES INDICATED IN SECT E-E.

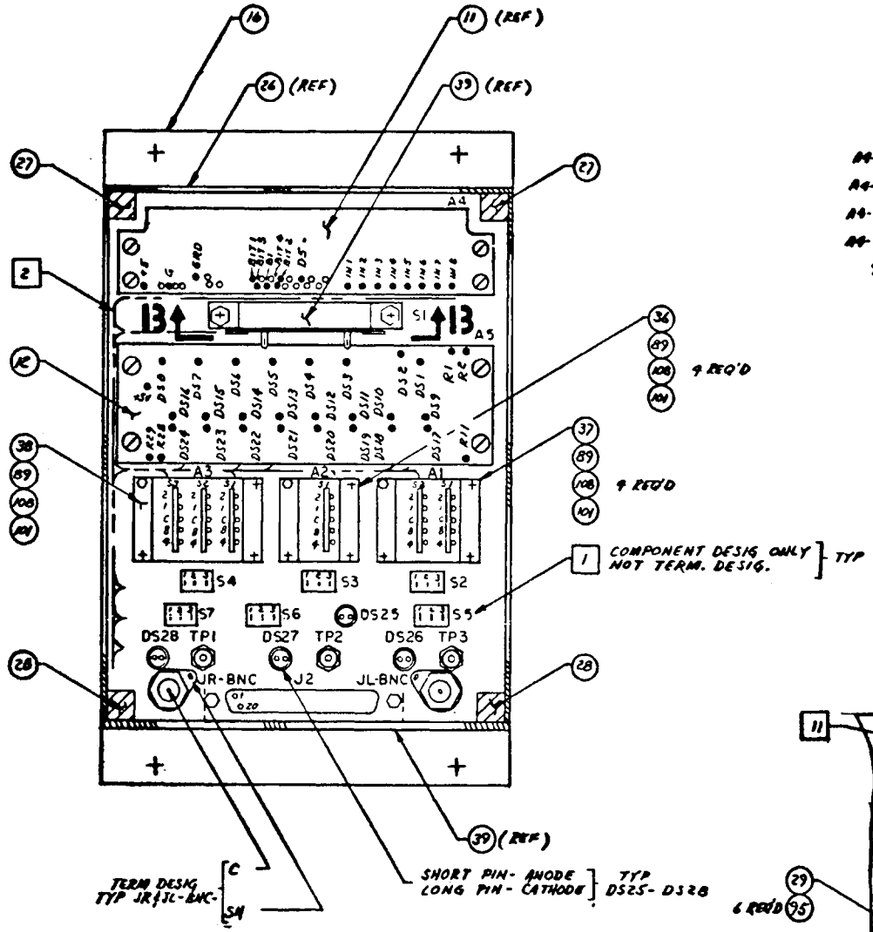
REV	DATE	DESCRIPTION
A	[illegible]	REDRAWN TO AS BUILT COND
B	[illegible]	REV TO AS BUILT
C	[illegible]	ADDED NOTE 11 & J4 MARKING.
D	[illegible]	CORRECTED HDWR REQ'D



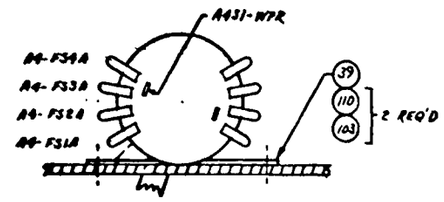


BILL OF MATERIALS A13721Z16

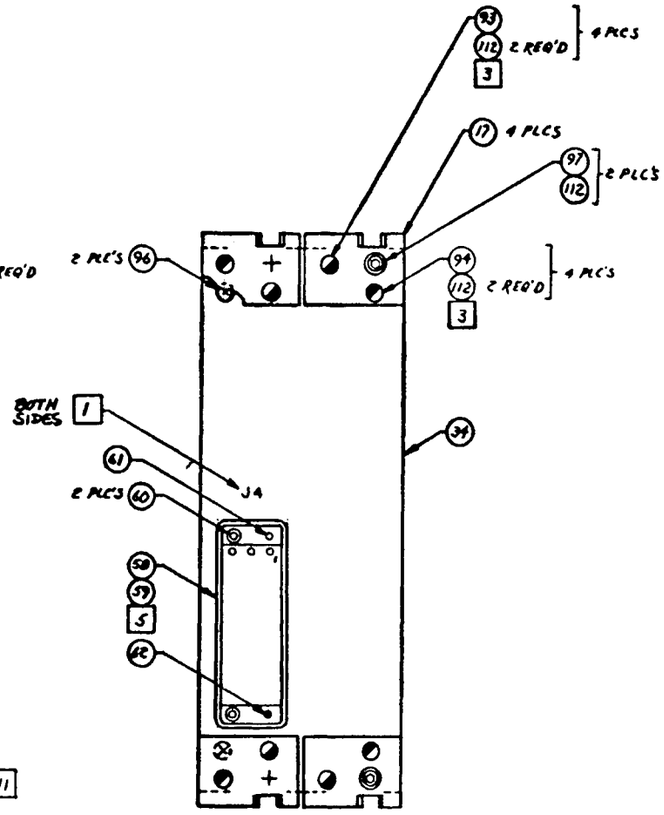
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	VLA PROJECT	M2 (MODEL C)	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801
TOLERANCES: ANGLES ±; 3 PLACE DECIMALS (.XXX): ±; 2 PLACE DECIMALS (.XX): ±; 1 PLACE DECIMALS (.X): ±	TITLE	DATA TAP MODULE	DRAWN BY / DATE 9/75; DESIGNED BY / DATE; APPROVED BY / DATE 7/1/76
MATERIAL:			
FINISH:			
NEXT ASSY / USED ON	SHEET NUMBER 1 of 2	DRAWING NUMBER D13720P89	REV D SCALE 1/1



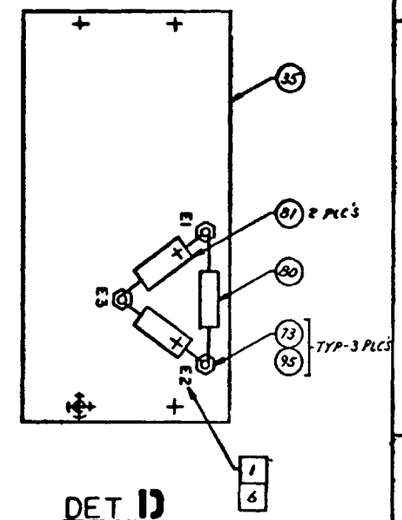
SECT A-A



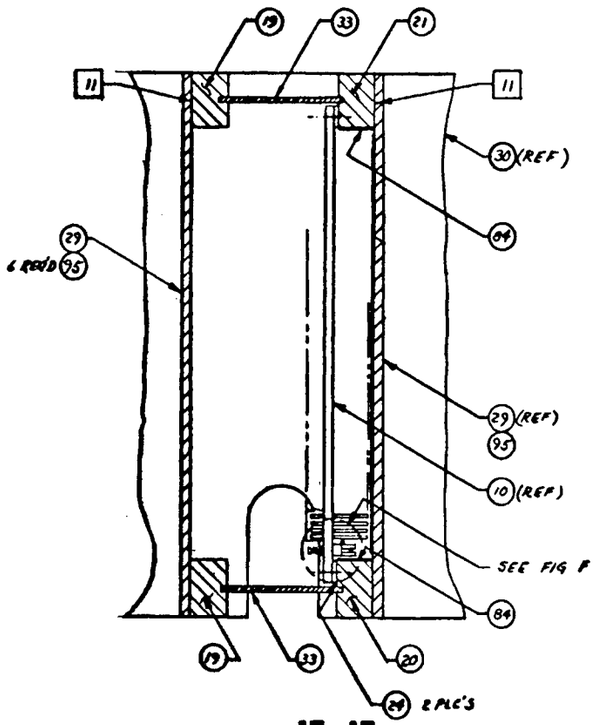
SECT B-B



VIEW C-C



DET D



SECT E-E

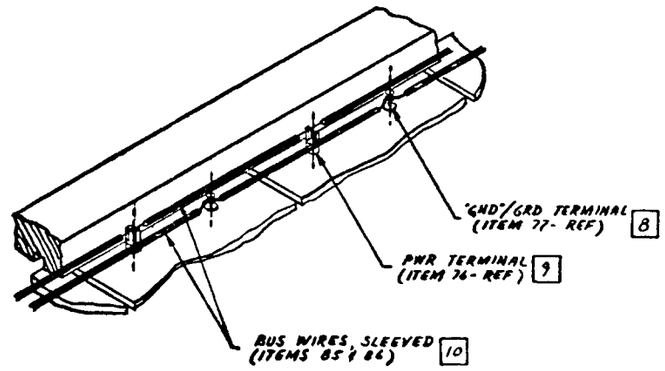


FIG F

PICTORIAL VIEW OF PWR-GRD BUS. (UNDERSIDE OF I.C. MODULE SUB-ASSY - ITEM 10)

REV	DATE	DRAWN BY	APPR'D BY	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

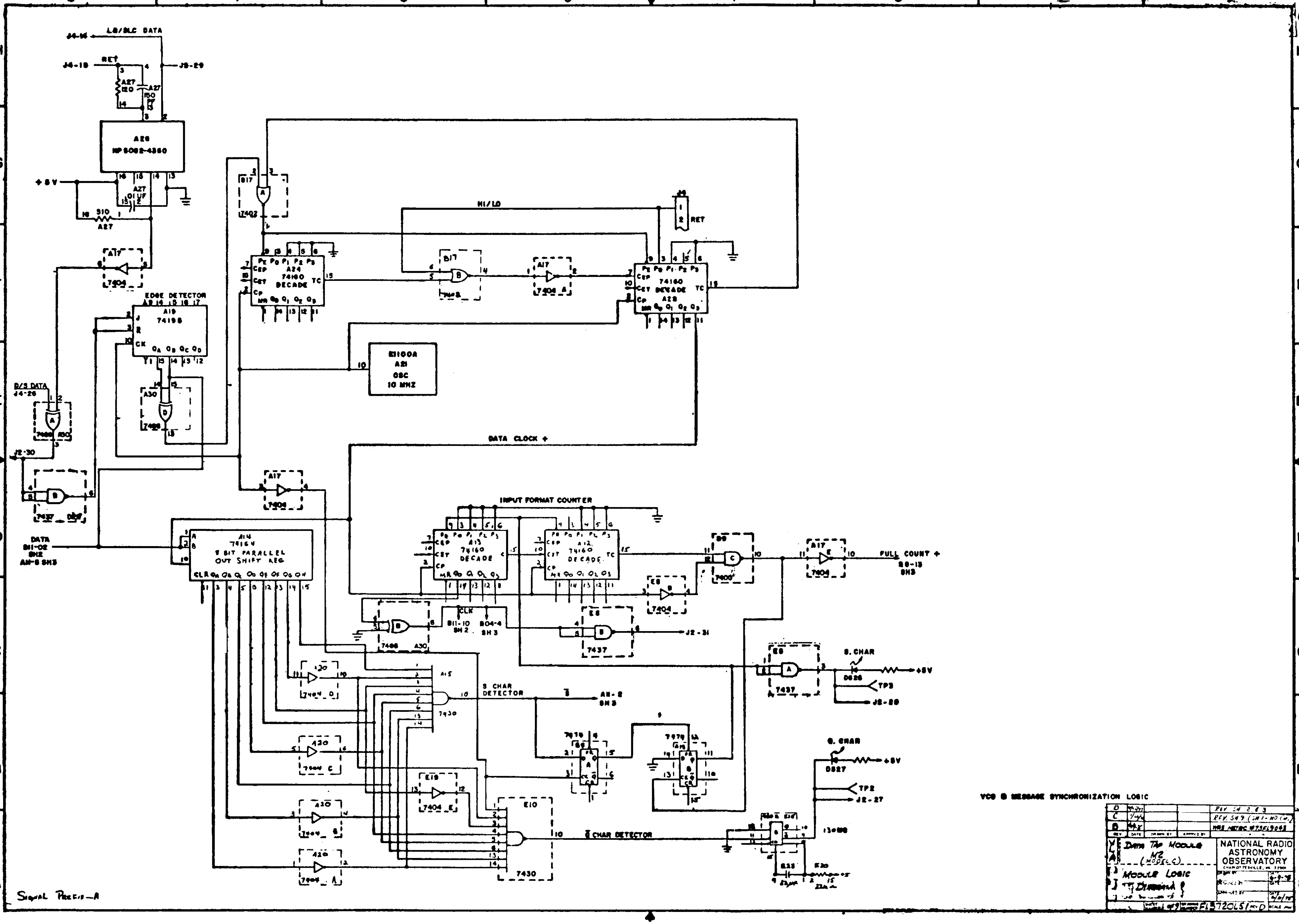
FINISH:

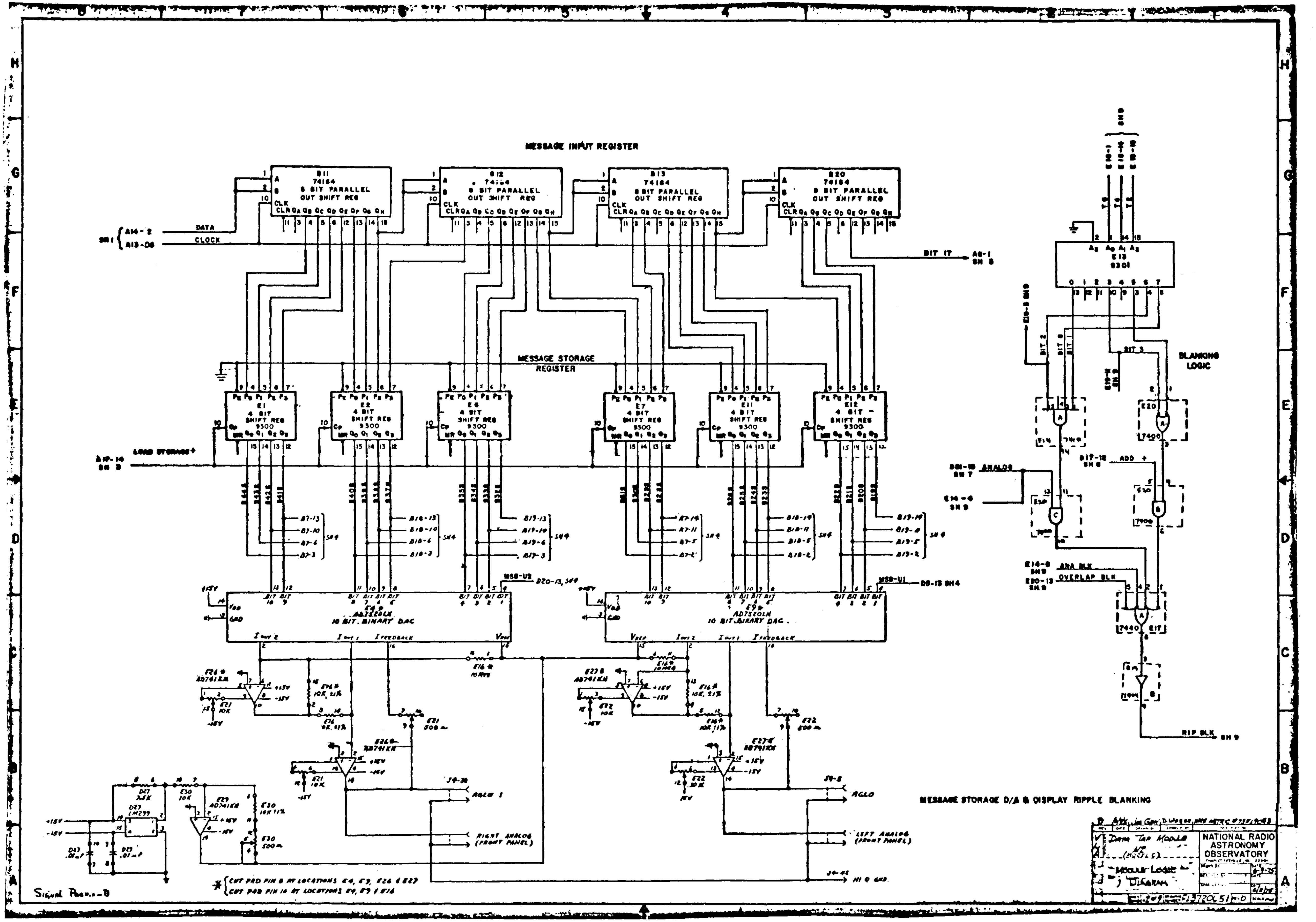
NEXT ASSY | USED ON

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

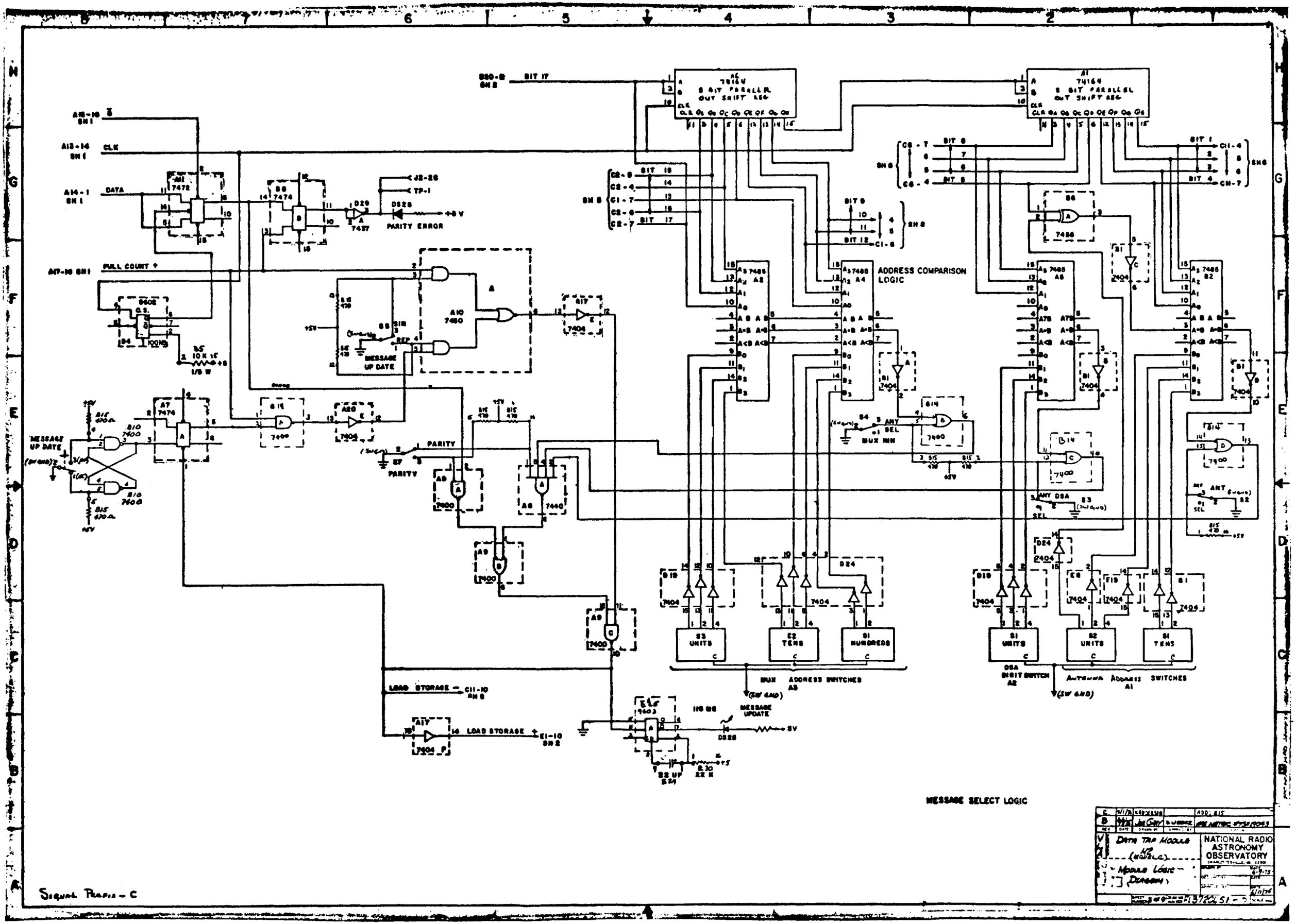
DRAWN BY | DATE
DESIGNED BY | DATE
APPROVED BY | DATE

SHEET NUMBER 2 OF 2 | DRAWING NUMBER D13720P89 | REV D | SCALE


LB/SLC DATA
RET
A28
HP5082-4360
+5V
EDGE DETECTOR
A19
74195
A24
74160
DECADE
HI/LO
A23
74160
DECADE
E100A
A21
OSC
10 MHZ
DATA CLOCK +
INPUT FORMAT COUNTER
A13
74160
DECADE
A12
74160
DECADE
FULL COUNT +
A14
74164
8 BIT PARALLEL
OUT SHIFT REG
DATA
S CHAR
DETECTOR
S̄ CHAR DETECTOR
S. CHAR
TP3
TP2
VCO B MESSAGE SYNCHRONIZATION LOGIC
NATIONAL RADIO
ASTRONOMY
OBSERVATORY
MODULE LOGIC
Signal Prefix—A



MESSAGE INPUT REGISTER
B11 74164 8 BIT PARALLEL OUT SHIFT REG
B12 74164 8 BIT PARALLEL OUT SHIFT REG
B13 74164 8 BIT PARALLEL OUT SHIFT REG
B20 74164 8 BIT PARALLEL OUT SHIFT REG
DATA
CLOCK
BIT 17
MESSAGE STORAGE REGISTER
E1 4 BIT SHIFT REG 9300
E2 4 BIT SHIFT REG 9300
E6 4 BIT SHIFT REG 9300
E7 4 BIT SHIFT REG 9300
E11 4 BIT SHIFT REG 9300
E12 4 BIT SHIFT REG 9300
LOAD STORAGE
E4 AD7520LN 10 BIT BINARY DAC
E9 AD7520LN 10 BIT BINARY DAC
E13 9301
BLANKING LOGIC
ANALOG
ADD
ANA BLK
OVERLAP BLK
RIP BLK
RIGHT ANALOG (FRONT PANEL)
LEFT ANALOG (FRONT PANEL)
HI Q GND
* CUT PAD PIN 8 AT LOCATIONS E4, E9, E26 & E27
CUT PAD PIN 16 AT LOCATIONS E4, E9 & E16
MESSAGE STORAGE D/A & DISPLAY RIPPLE BLANKING
NATIONAL RADIO ASTRONOMY OBSERVATORY


A10-16 SH 1
A13-14 SH 1
CLK
A14-1 SH 1
DATA
A17-10 SH 1
FULL COUNT +
MESSAGE UP DATE
PARITY ERROR
+5 V
PARITY
LOAD STORAGE — C11-10 SH 8
LOAD STORAGE — E1-10 SH 8
MESSAGE UPDATE
ADDRESS COMPARISON LOGIC
MUX ADDRESS SWITCHES A3
DSA DIGIT SWITCH A2
ANTENNA ADDRESS SWITCHES A1
(SW GND)
MESSAGE SELECT LOGIC
DATA TRP MODULE
MODULE LOGIC — (DESIGN)
NATIONAL RADIO ASTRONOMY OBSERVATORY
SIGNAL PROBE — C

BINARY LED DISPLAYS

SEL RIGHT +

SELECT & MULTIPLY ANALOG DATA X 5

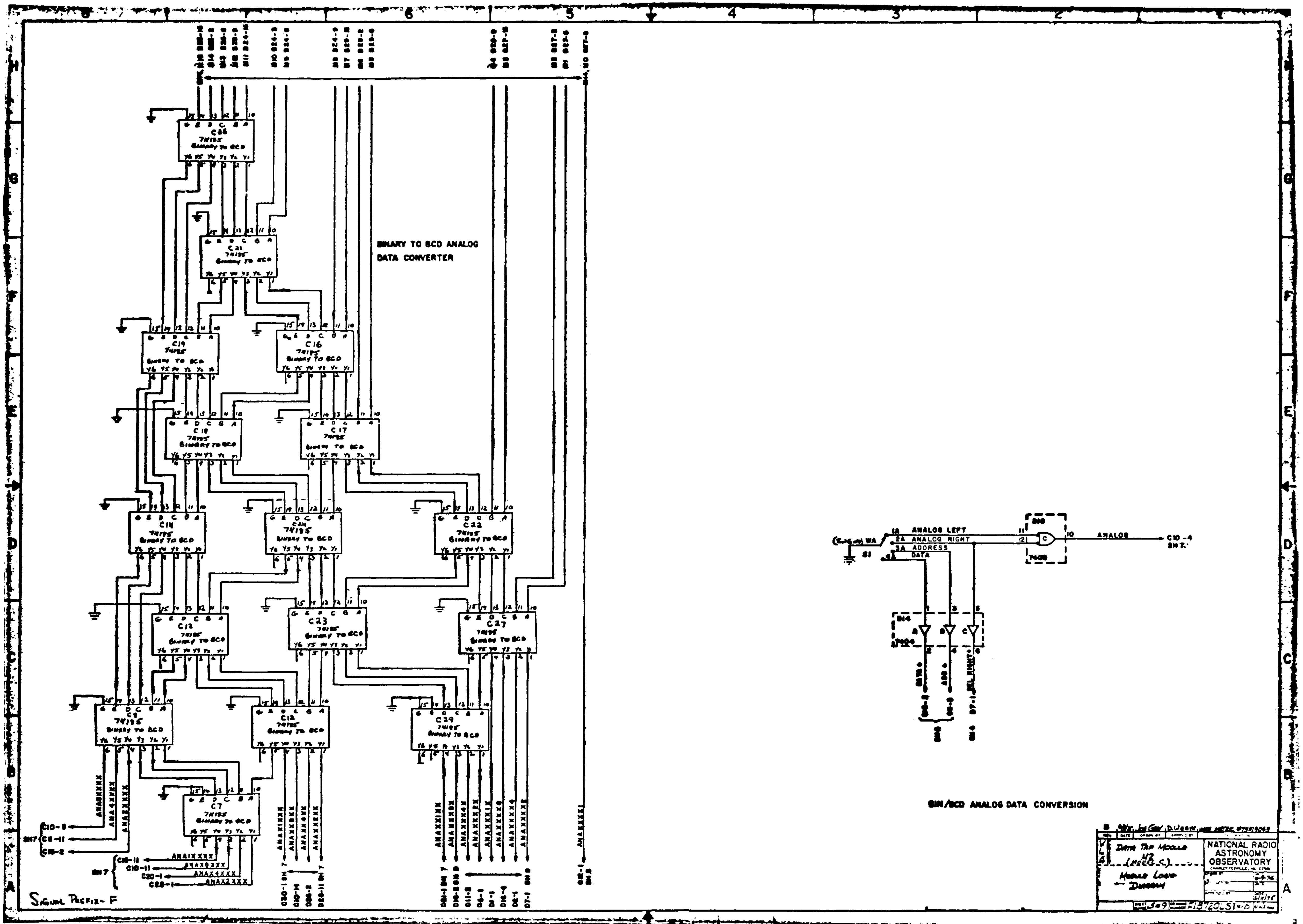
7483 FULL ADDER

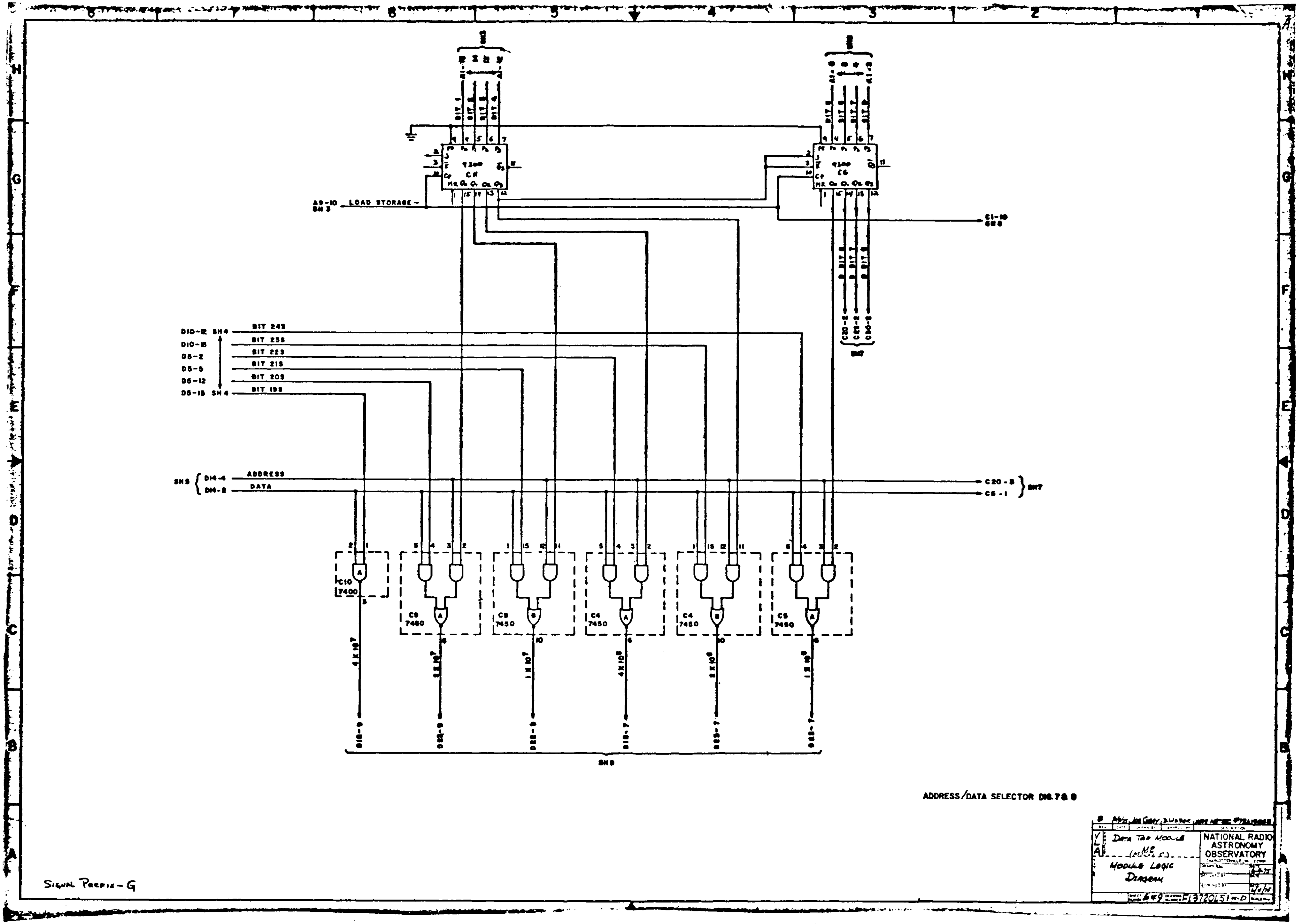
BINARY DATA DISPLAY & ANALOG DATA SELECT/MULTIPLY

NOTE:
1. REMOVE VCC FROM PIN 16 OF B21, B23, B24, B25, B27 & B29
2. REMOVE GND FROM PIN 8 OF B24, B27 & B29

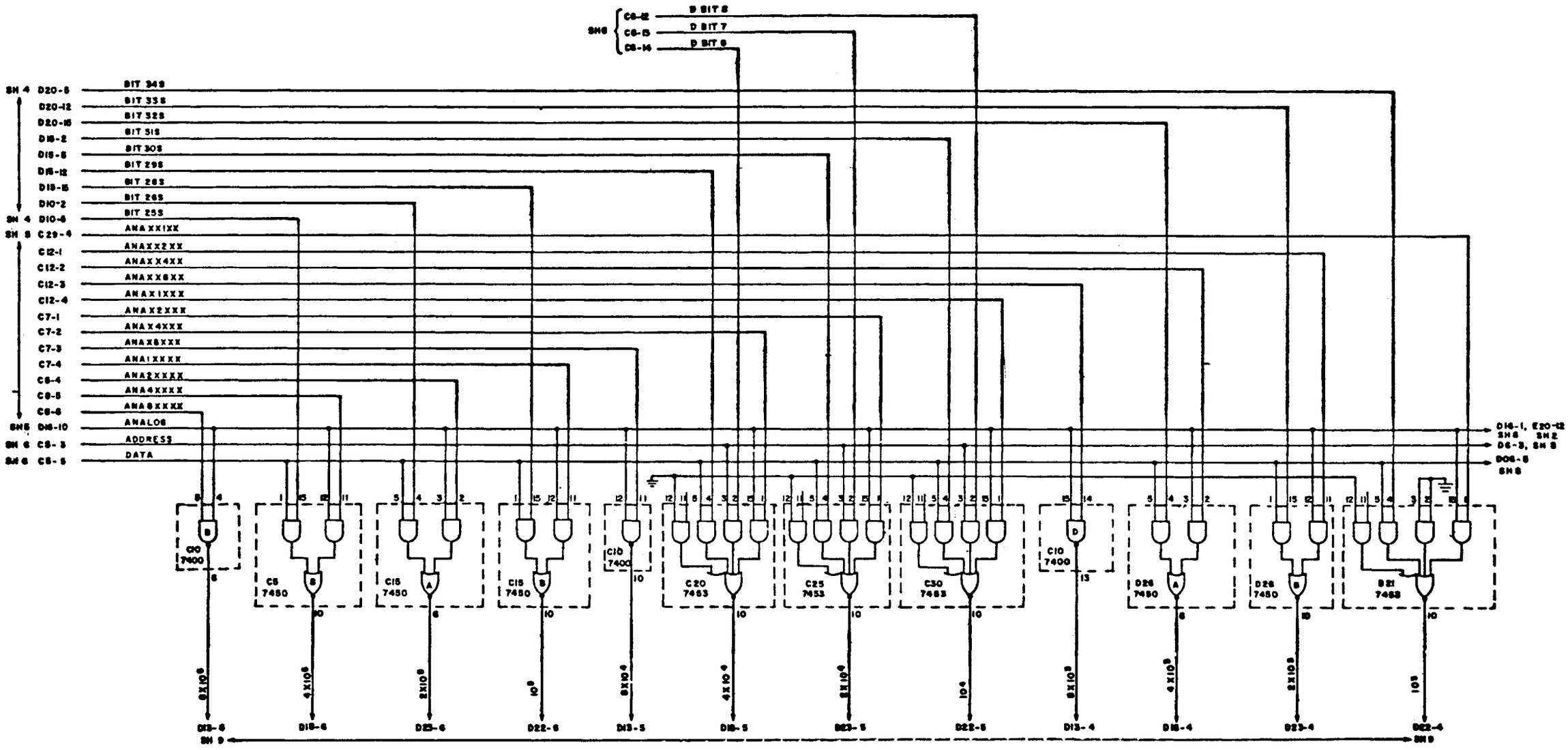
Signal Prefix—D

NATIONAL RADIO ASTRONOMY OBSERVATORY


BINARY TO BCD ANALOG DATA CONVERTER
ANALOG LEFT
ANALOG RIGHT
ADDRESS
DATA
ANALOG
BIN/BCD ANALOG DATA CONVERSION
SIGNAL PREFIX- F
NATIONAL RADIO ASTRONOMY OBSERVATORY



LOAD STORAGE
9300
C11
C6
BIT 24S
BIT 23S
BIT 22S
BIT 21S
BIT 20S
BIT 19S
ADDRESS
DATA
C10
7400
C9
7450
C4
7450
C5
7450
4 X 10^7
2 X 10^7
1 X 10^7
4 X 10^6
2 X 10^6
1 X 10^6
SH 9
SH 7
ADDRESS/DATA SELECTOR D16,7 & 8
DATA TAP MODULE
MODULE LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY
SIGNAL PREFIX - G



ADDRESS/DATA SELECTOR D18.4,5,8.6

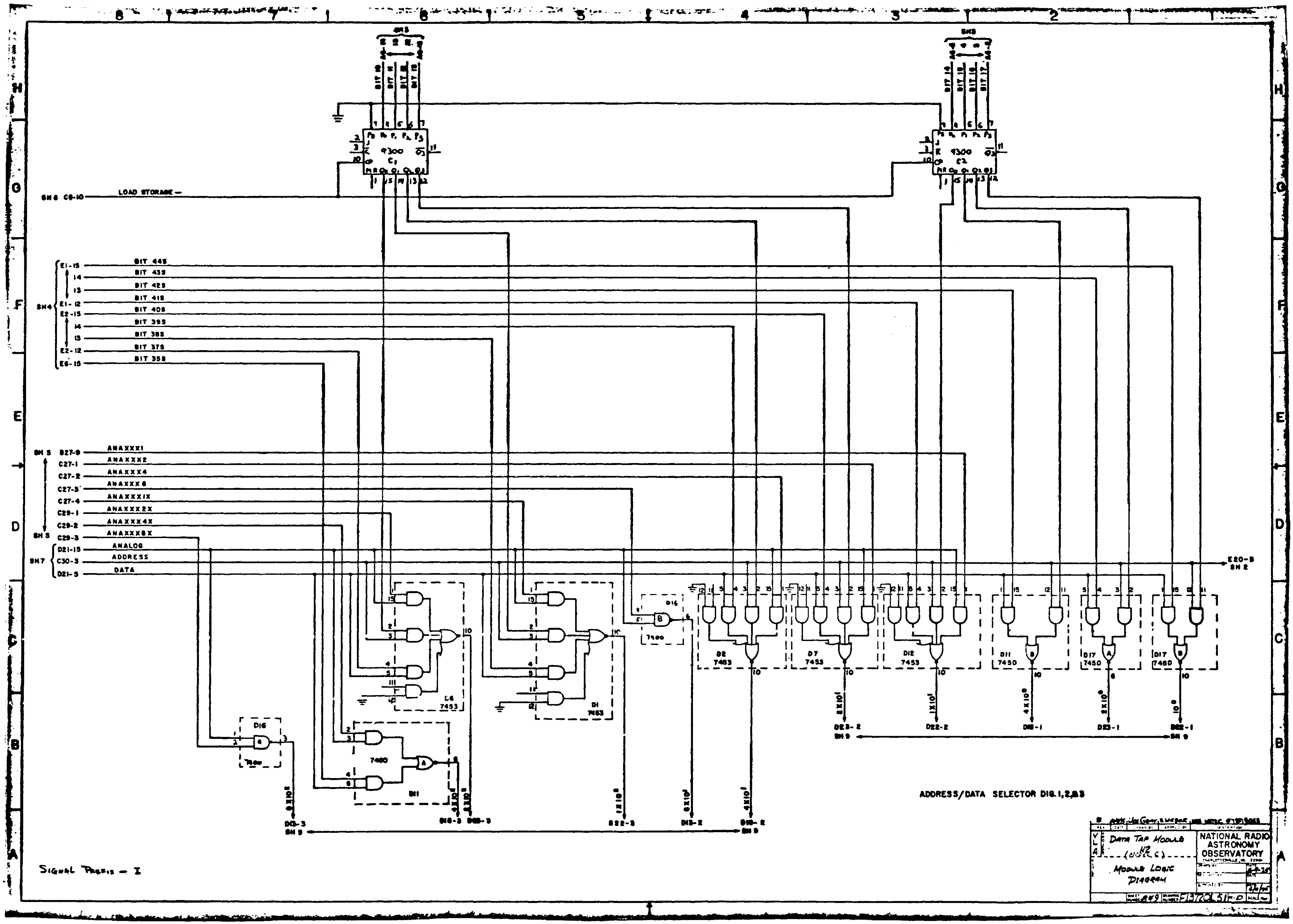
DATA TAP MODULE MP (MODEL C)

MODULE LOGIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY

SHEET NUMBER 7 OF 9 F13720.51 REV D

SIGNAL PREFIX - H


LOAD STORAGE
SH 6 C8-10
9300 C1
9300 C2
BIT 10
BIT 11
BIT 12
BIT 13
BIT 14
BIT 15
BIT 16
BIT 17
SH4
E1-15
E1-12
E2-15
E2-12
E6-15
BIT 44S
BIT 43S
BIT 42S
BIT 41S
BIT 40S
BIT 39S
BIT 38S
BIT 37S
BIT 35S
SH 5
B27-9
C27-1
C27-2
C27-3
C27-4
C29-1
C29-2
C29-3
ANAXXX1
ANAXXX2
ANAXXX4
ANAXXX8
ANAXXX1X
ANAXXX2X
ANAXXX4X
ANAXXX8X
SH7
D21-15
C30-3
D21-5
ANALOG
ADDRESS
DATA
E20-8
SH 2
C6
7453
D1
7453
D16
7400
D11
7460
D2
7453
D7
7453
D12
7453
D11
7450
D17
7450
D17
7450
SH 9
D13-3
D18-3
D22-3
D13-2
D18-2
D23-2
D22-2
D18-1
D23-1
D22-1
ADDRESS/DATA SELECTOR DIG.1,2,&3
Signal Paths — I
Data Tap Module
Module Logic Diagram
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA.

DIGIT SEQUENCER

NUMERIC LED DISPLAY

(LED MOUNTING ASSY, BEHIND FRONT PANEL)

A4-2 IS ADJACENT TO FRONT PANEL

A4-1 IS MOUNTED BEHIND A4-2 & JUMPERS WIRED TO A4-2

ALL I/O WIRING TO A4-1 & 2 IS DONE VIA A4-1 WW PINS

Signal Prefix — J

NUMERIC LED DATA DISPLAY & DRIVE LOGIC

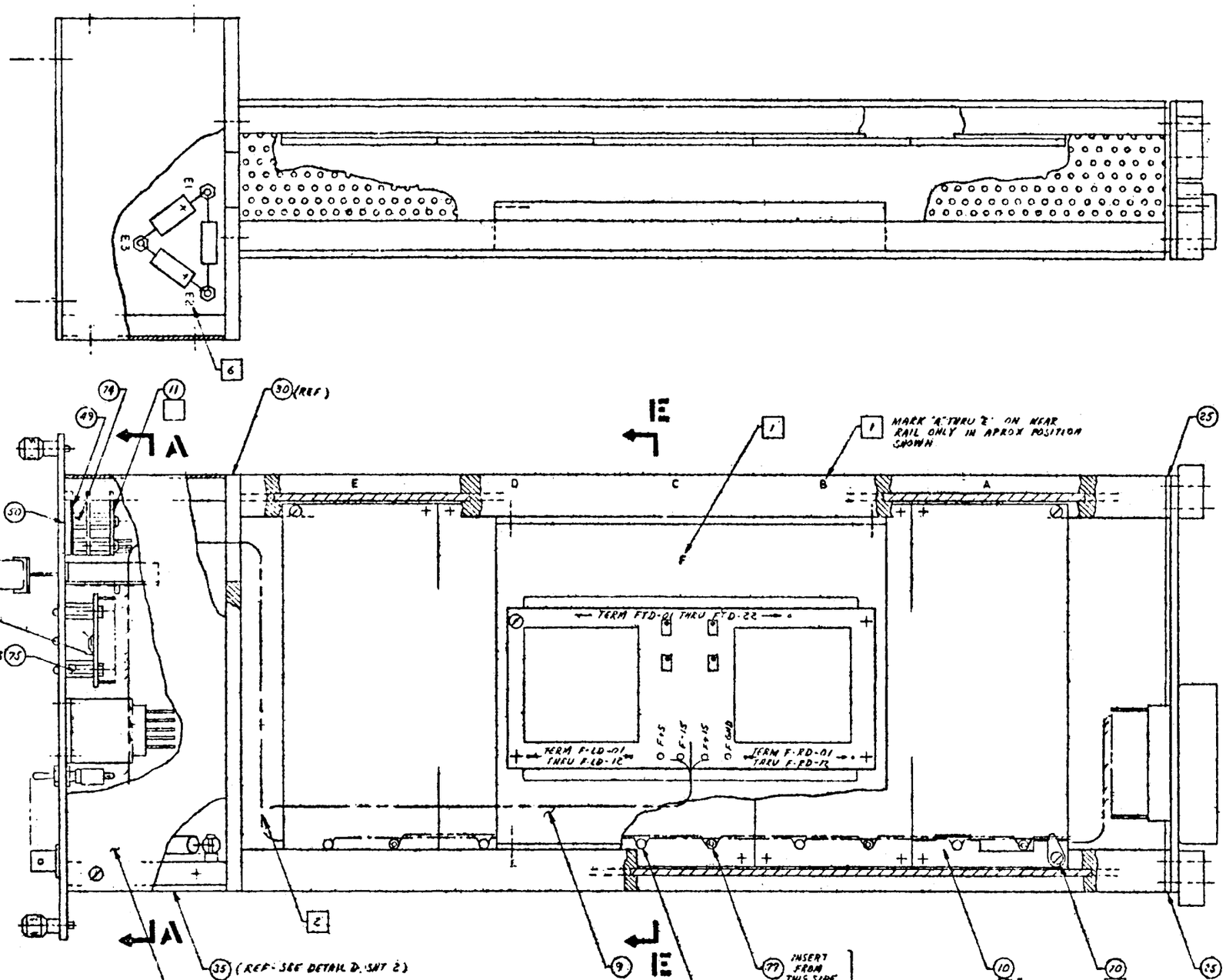
NATIONAL RADIO ASTRONOMY OBSERVATORY

DATA TAP MODULE (MOD 2)

MODULE LOGIC DIAGRAM

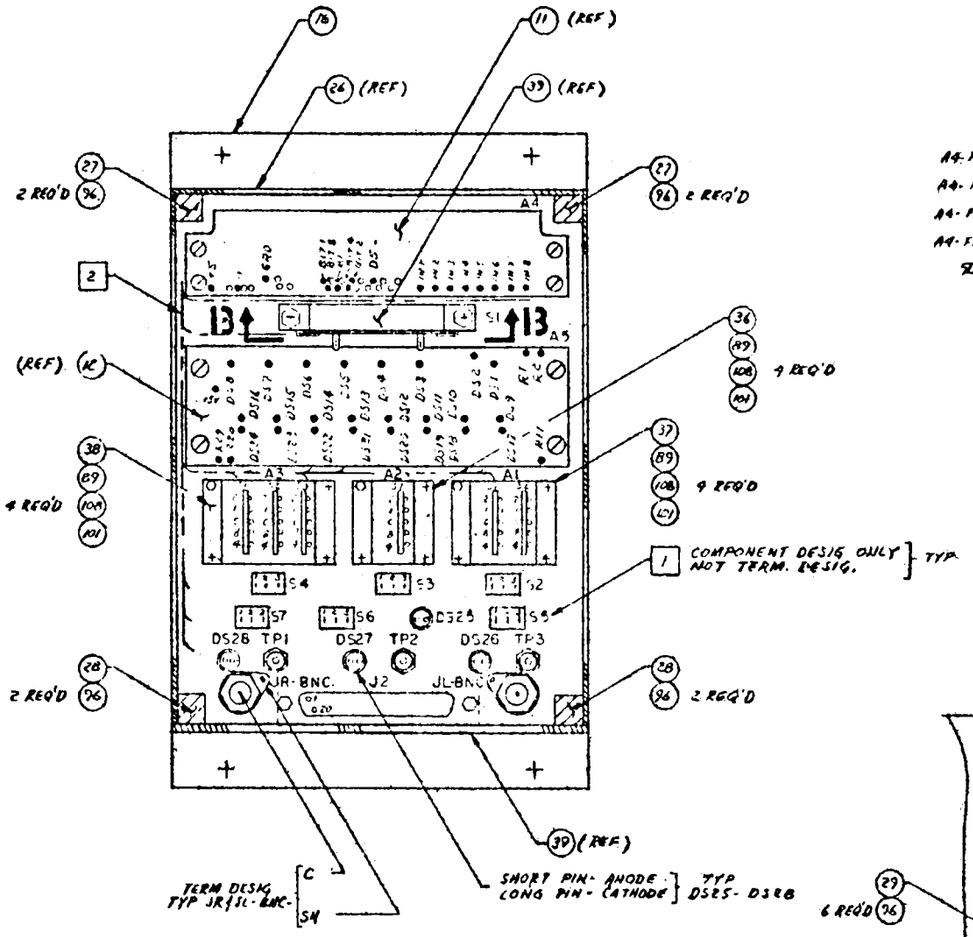
NOTES:

1. MARKING SHALL BE 1/8" HIGH, LEGIBLE AND PERMANENT. LOCATE APROX. AS SHOWN.
2. A WIRING SERVICE LOOP OF SUFFICIENT LENGTH TO ALLOW THE FRONT, REAR AND 'J' PANELS TO BE FOLDED FLAT MUST BE PROVIDED.
3. WHERE TWO WASHERS (ITEM 111) ARE REQ'D PLACE ONE UNDER THE SCREW HEAD AND THE OTHER BETWEEN THE GUIDE (ITEM 17) AND THE REAR PANEL (ITEM 34).
4. SOLDER 'SOLDER LUG' (ITEM 70) TO "GND" PLANE AND PLACE UNDER SCREW HEAD APROX. AS SHOWN.
5. LEADS TERMINATING AT POS. 10 & 34 USE ITEM NO 64
   LEADS TERMINATING AT POS. 15, 16 & 42 USE ITEM NO. 63
   LEADS TERMINATING AT POS. 5, 6, 7, 38, 39 & 40 USE ITEM NO'S 65, 66 & 67.
6. THE WIRE LIST REFERS TO TERMINALS E1, E2 & E3 AS FOLLOWS:
   E1 - TERM. 'FLTOUT'
   E2 - TERM. 'FLTIN'
   E3 - TERM. 'FLTGND'

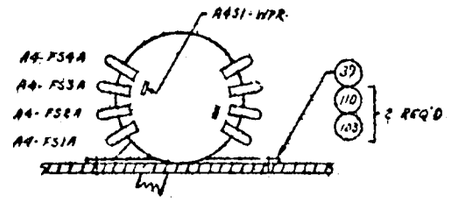


BILL OF MATERIALS A1372023

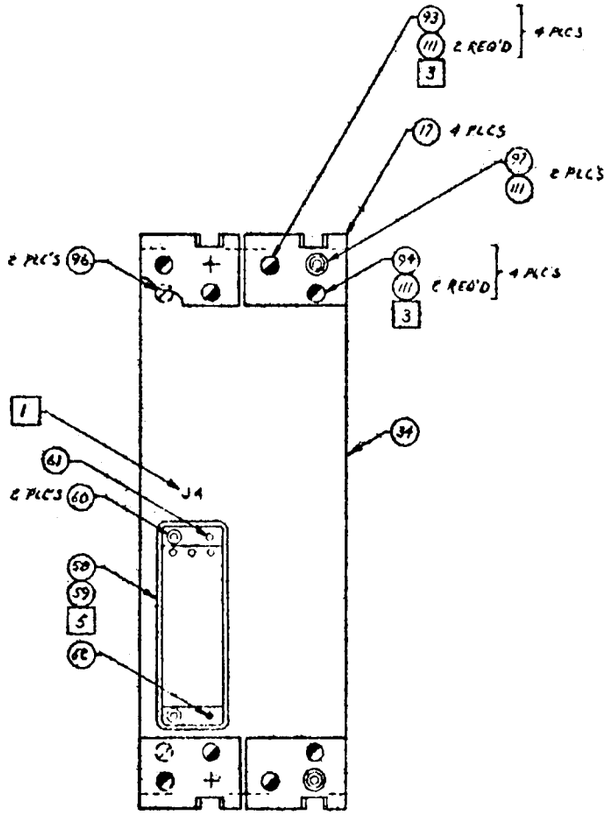
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	VLA	M2 (MODEL B)	NATIONAL RADIO ASTRONOMY OBSERVATORY
MATERIAL:		DATA TAP MODULE	
FINISH:			
NEXT ASSY / USED ON		SHEET NUMBER 1 OF 2	DRAWING NUMBER D1372029 REV A



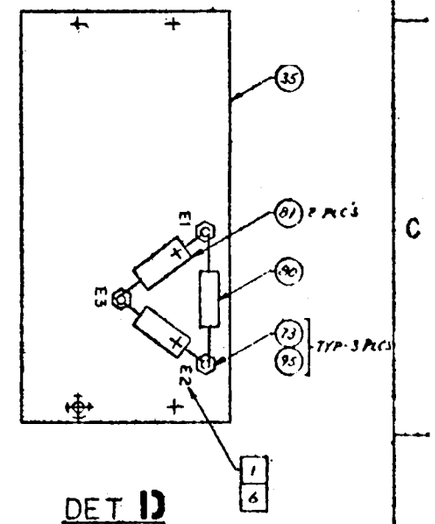
SECT A-A



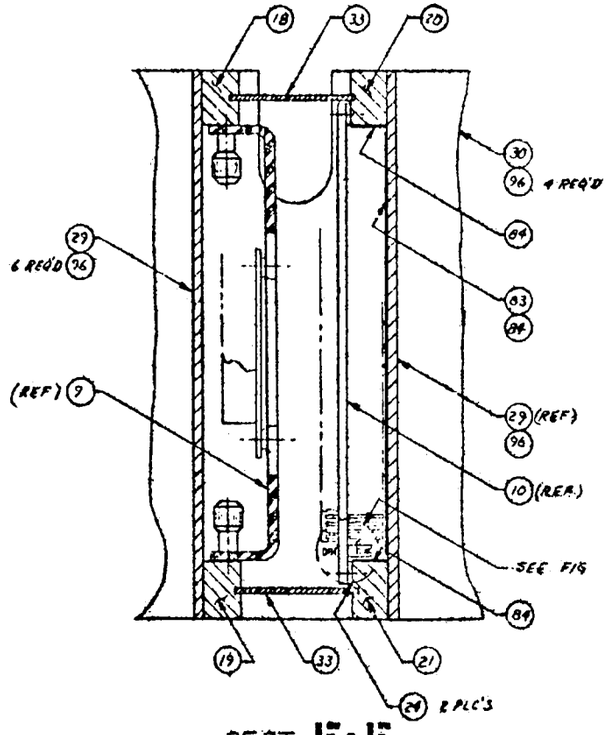
SECT B-B



VIEW C-C



DET D



SECT E-E

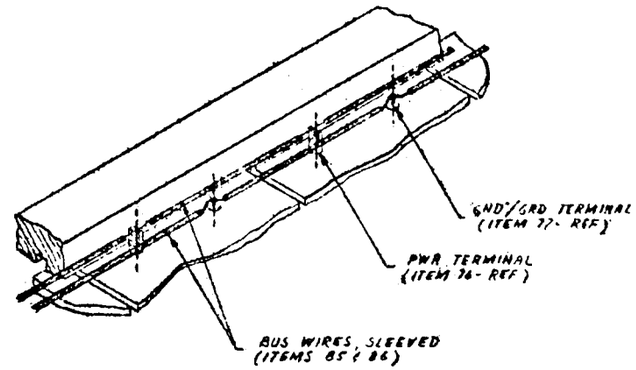
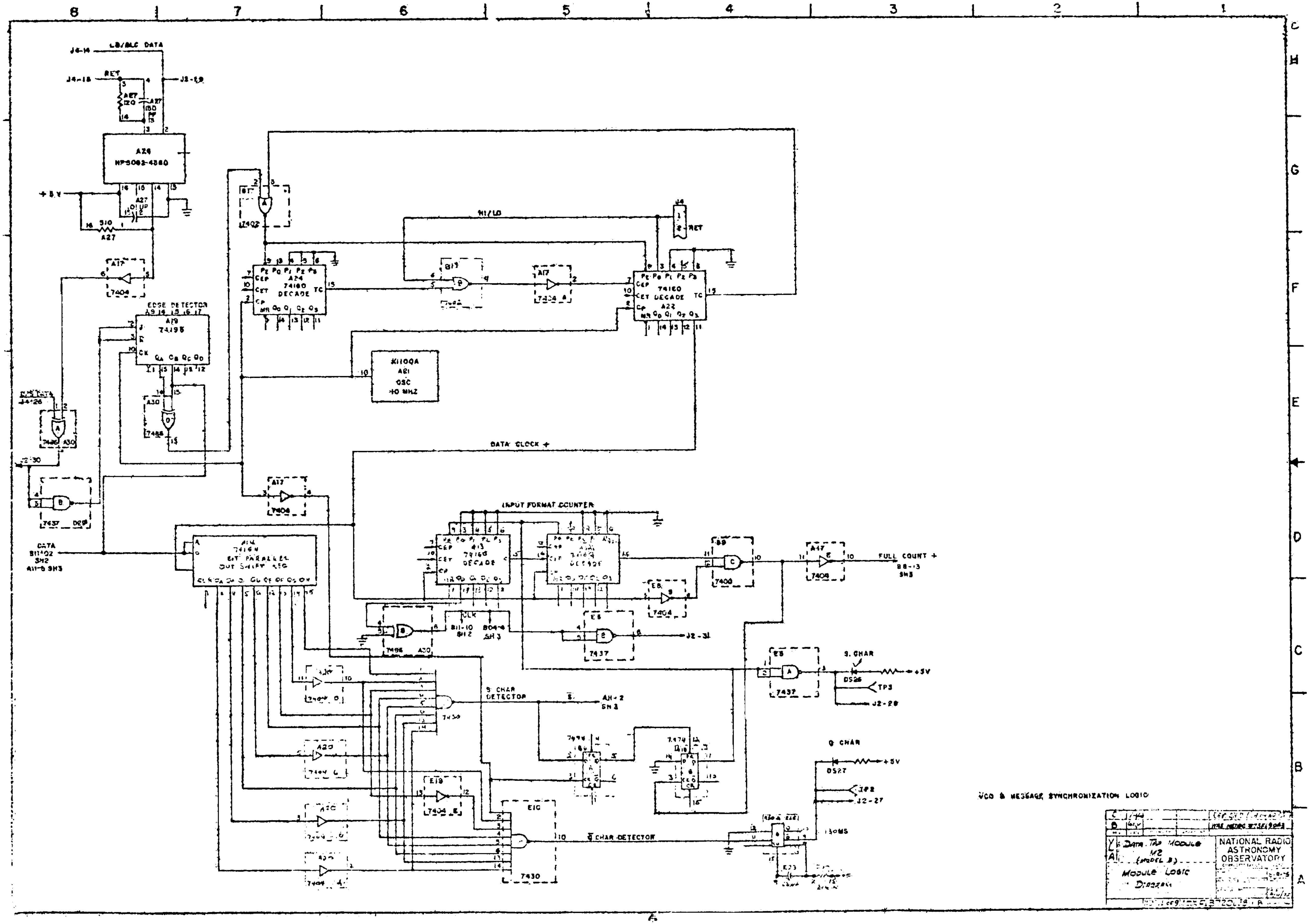


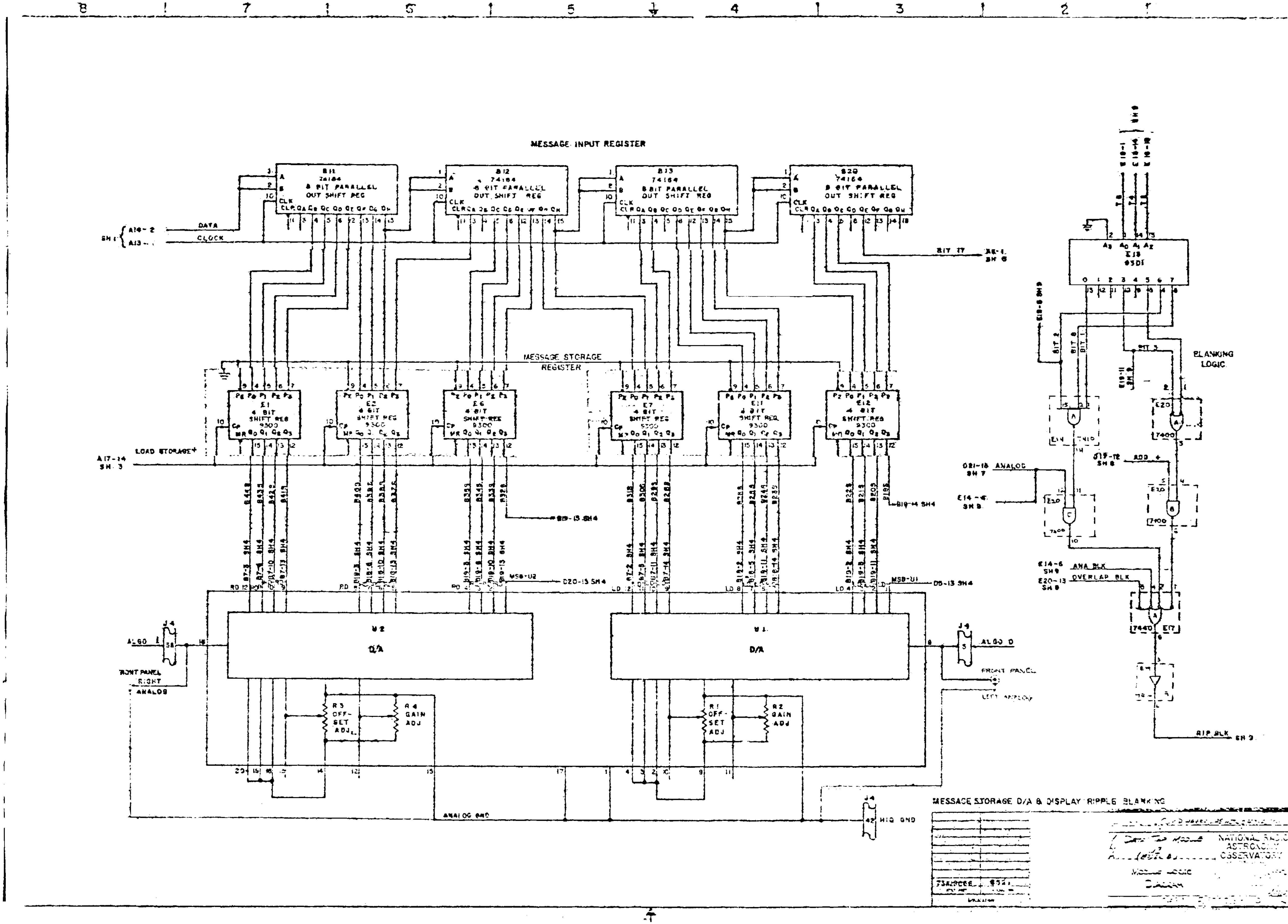
FIG F

PICTORIAL VIEW OF PWR-GND BUS. (UNDERSIDE OF I.C MODULE SUB-ASSY - ITEM 10)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		(MODEL B)	NATIONAL RADIO ASTRONOMY OBSERVATORY
MATERIAL			DRAWN BY / DATE
FINISH			CHECKED BY / DATE
			APPROVED BY / DATE
NEXT ASSY	USED ON		SIZE A — DRAWING NUMBER D137P09 — REV A

8 7 6 5 4 3 2 1 — D C B A


LB/BLC DATA
A26
HP5082-4360
EDGE DETECTOR
74195
7404
7486
7437
7402
74160
DECADE
HI/LO
DATA CLOCK +
X1100A
A21
OSC
10 MHZ
INPUT FORMAT COUNTER
FULL COUNT +
DATA
8 BIT PARALLEL OUT SHIFT REG
S CHAR DETECTOR
S CHAR
Q CHAR
Q CHAR DETECTOR
7430
7474
TP3
TP2
J2-27
J2-31
VCO & MESSAGE SYNCHRONIZATION LOGIC
Data Tap Module
M2
(Model B)
Module Logic
Diagram
NATIONAL RADIO
ASTRONOMY
OBSERVATORY


MESSAGE INPUT REGISTER
B11 74164 8 BIT PARALLEL OUT SHIFT REG
B12 74164 8 BIT PARALLEL OUT SHIFT REG
B13 74164 8 BIT PARALLEL OUT SHIFT REG
B20 74164 8 BIT PARALLEL OUT SHIFT REG
DATA
CLOCK
BIT 17
MESSAGE STORAGE REGISTER
E1 4 BIT SHIFT REG 9300
E2 4 BIT SHIFT REG 9300
E6 4 BIT SHIFT REG 9300
E7 4 BIT SHIFT REG 9300
E11 4 BIT SHIFT REG 9300
E12 4 BIT SHIFT REG 9300
LOAD STORAGE
E18 8501
BLANKING LOGIC
ANALOG
ANA BLK
OVERLAP BLK
RIP BLK
D/A
D/A
ALGO
FRONT PANEL
RIGHT ANALOG
FRONT PANEL
LEFT ANALOG
ALGO D
R3 OFF-SET ADJ
R4 GAIN ADJ
R1 OFF-SET ADJ
R2 GAIN ADJ
ANALOG GND
HIQ GND
MESSAGE STORAGE D/A & DISPLAY RIPPLE BLANKING
NATIONAL RADIO ASTRONOMY OBSERVATORY

MESSAGE SELECT LOGIC

ADDRESS COMPARISON LOGIC

MJR ADDRESS SWITCHES A3

DSA DIGIT SWITCH A2

ANTENNA SWITCHES A1

NATIONAL RADIO ASTRONOMY OBSERVATORY

BINARY LED DISPLAYS

SEL RIGHT +

SELECT & MULTIPLY ANALOG DATA X 5

B21 7483 FULL ADDER

B20 7483 FULL ADDER

B23 7483 FULL ADDER

B22 7483 FULL ADDER

B24 7483 FULL ADDER

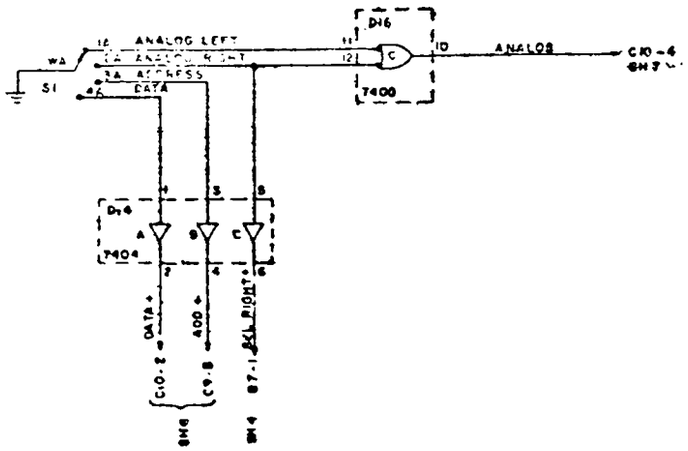
B25 7483 FULL ADDER

BINARY DATA DISPLAY & ANALOG DATA SELECT/MULTIPLY

NOTE:
1. REMOVE VCC FROM PIN 16 OF B21, B25, B26, B24, B25 B774219
2. REMOVE GND FROM PIN 8 OF B26, B27 & B23

NATIONAL RADIO ASTRONOMY OBSERVATORY

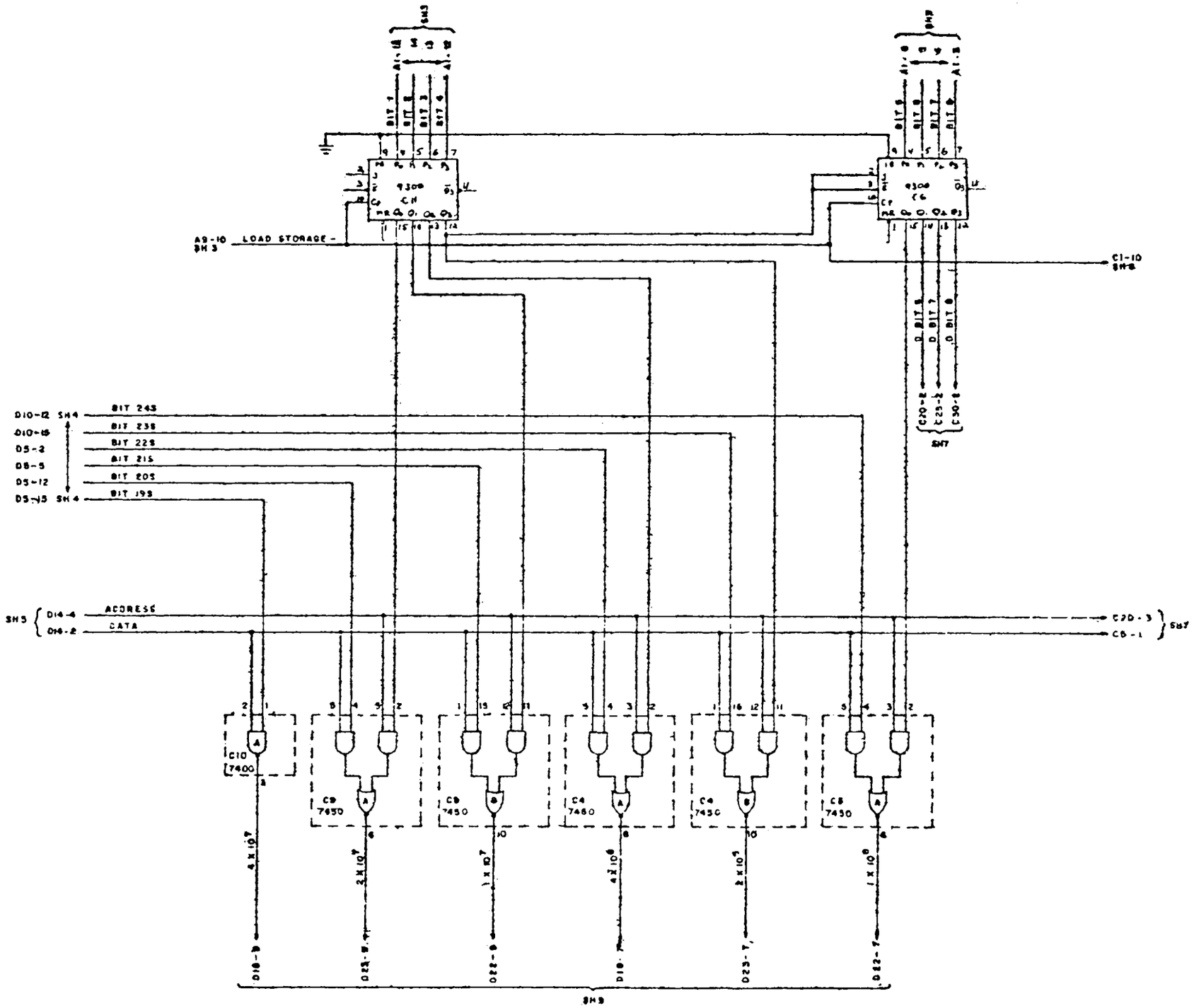
BINARY TO BCD ANALOG
DATA CONVERTER



BIN/BCD ANALOG DATA CONVERSION

NATIONAL RADIO ASTRONOMY OBSERVATORY

MODULE LOGIC DIAGRAM

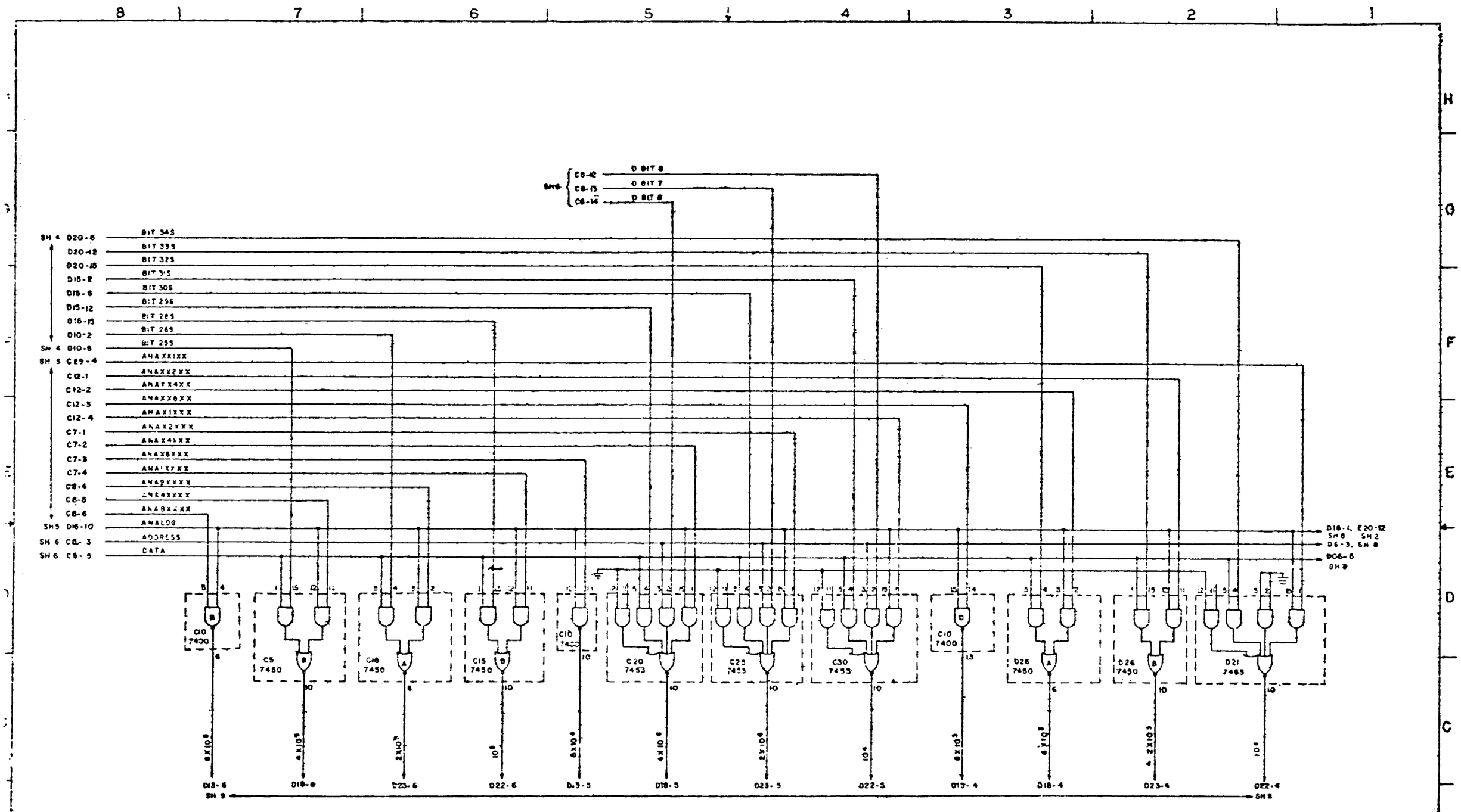


ADDRESS/DATA SELECTOR DIG 78 8

NATIONAL RADIO ASTRONOMY OBSERVATORY

MODULE LOGIC DIAGRAM

Signal Process - G

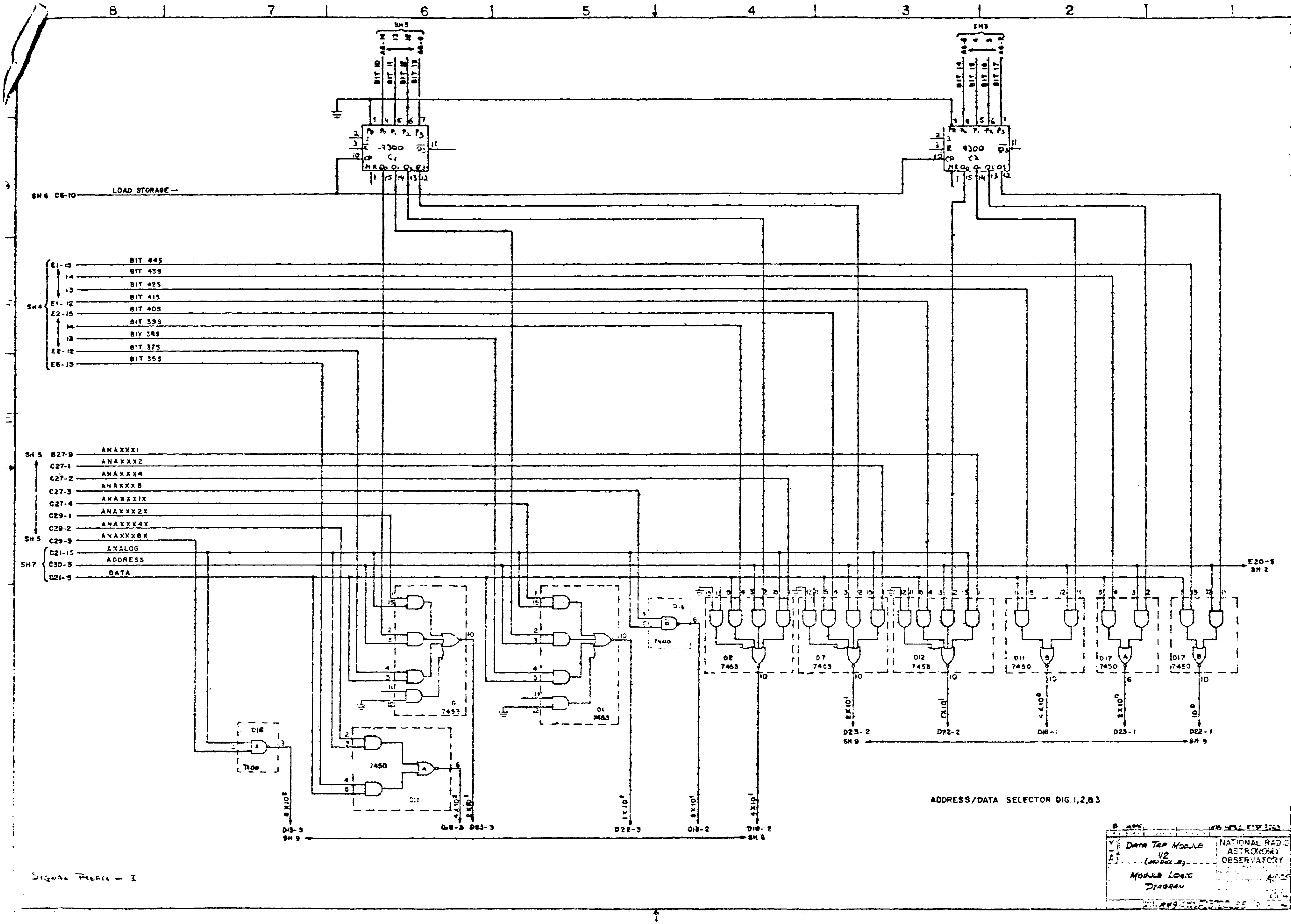


ADDRESS/DATA SELECTOR DIG 4,5,8 6

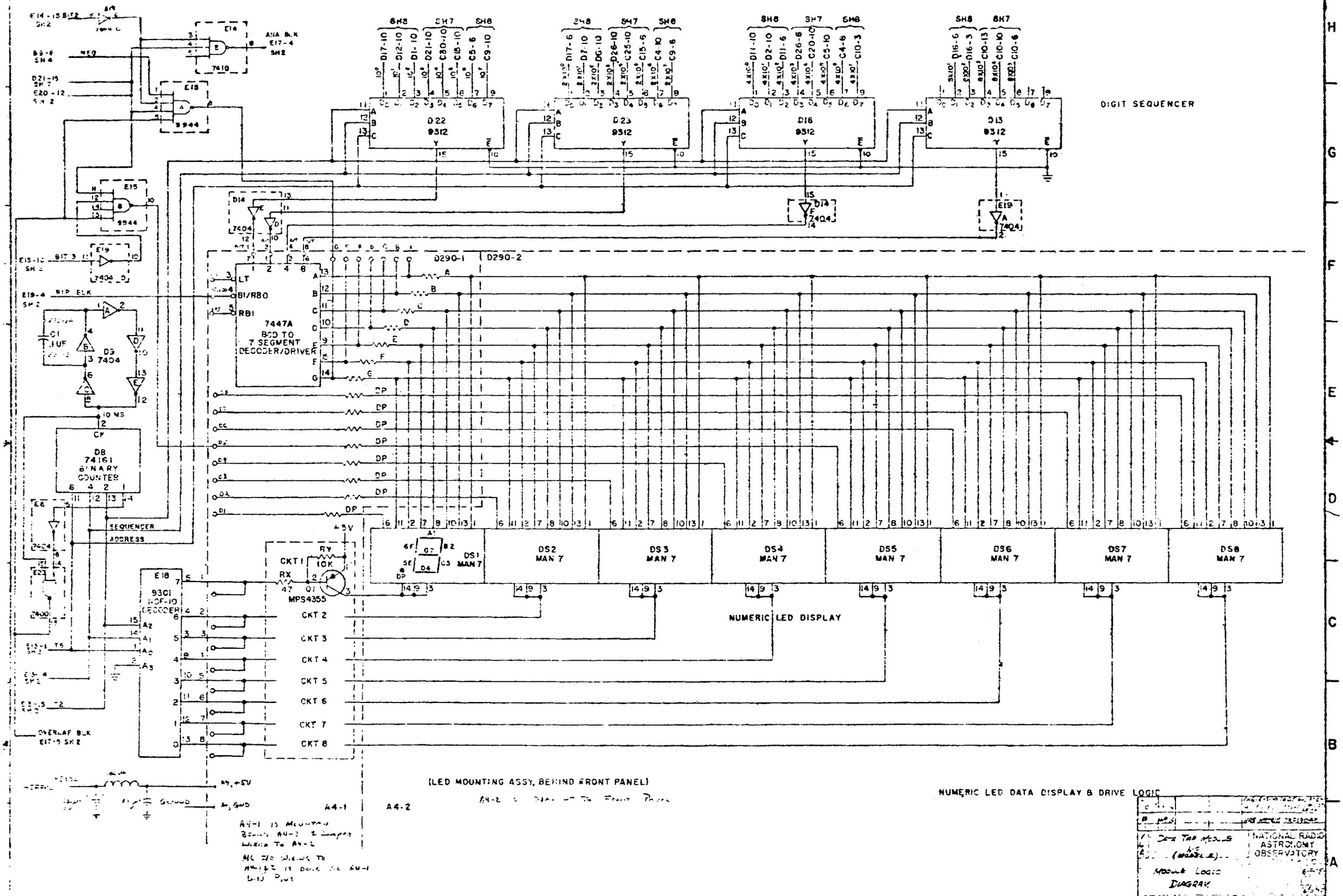
NATIONAL RADIO ASTRONOMY OBSERVATORY

MODULE LOGIC DIAGRAM

Sheet Prefix - H



LOAD STORAGE
SH 6 C6-10
BIT 44S
BIT 43S
BIT 42S
BIT 41S
BIT 40S
BIT 39S
BIT 38S
BIT 37S
BIT 36S
SH4
ANAXXX1
ANAXXX2
ANAXXX4
ANAXXX8
ANAXXX1X
ANAXXX2X
ANAXXX4X
ANAXXX8X
ANALOG
ADDRESS
DATA
SH 5
SH7
E20-5
SH 2
9300
7453
7450
7400
D2
D7
D12
D11
D17
D16
D18-2
D22-3
D23-3
D15-3
D22-2
D23-2
SH 9
ADDRESS/DATA SELECTOR DIG.1,2,&3
DATA TAP MODULE
NATIONAL RADIO ASTRONOMY OBSERVATORY
MODULE LOGIC DIAGRAM
SIGNAL PREFIX — I


DIGIT SEQUENCER
D290-1
D290-2
7447A
BCD TO
7 SEGMENT
DECODER/DRIVER
DS1 MAN 7
DS2 MAN 7
DS3 MAN 7
DS4 MAN 7
DS5 MAN 7
DS6 MAN 7
DS7 MAN 7
DS8 MAN 7
NUMERIC LED DISPLAY
CKT 1
CKT 2
CKT 3
CKT 4
CKT 5
CKT 6
CKT 7
CKT 8
MPS4355
9301
1-OF-10
DECODER
D22 9312
D23 9312
D18 9312
D13 9312
D8
74161
BINARY
COUNTER
SEQUENCER
ADDRESS
10 MS
OVERLAP BLK
(LED MOUNTING ASSY, BEHIND FRONT PANEL)
A4-1
A4-2
NUMERIC LED DATA DISPLAY & DRIVE LOGIC
NATIONAL RADIO
ASTRONOMY
OBSERVATORY
MODULE LOGIC
DIAGRAM

5.0 SPECIAL COMPONENT DATA SHEETS

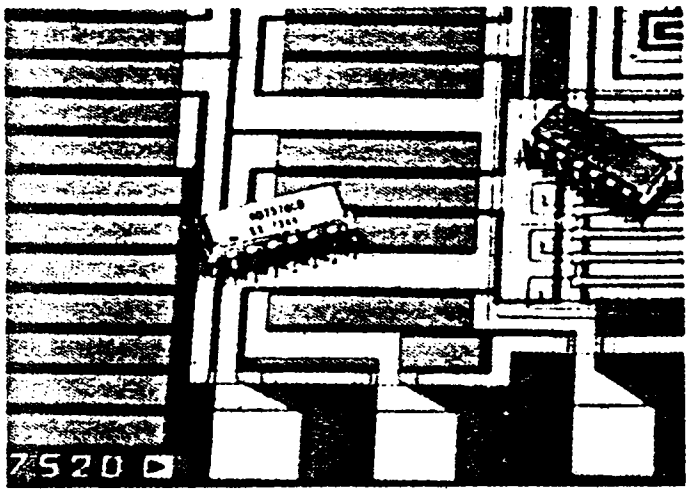
ANALOG DEVICES

CMOS 10 & 12 BIT MONOLITHIC MULTIPLYING D/A CONVERTERS

AD7520, AD7521

FEATURES

AD7520:	10 Bit Resolution
AD7521:	12 Bit Resolution
Linearity:	8, 9 and 10 Bit
Nonlinearity Tempco:	2 ppM of FSR/°C
Low Power Dissipation:	20 mW
Current Settling Time:	500 ns
Feedthrough Error:	1/2 LSB @ 100 kHz
TTL/DTL/CMOS Compatible	



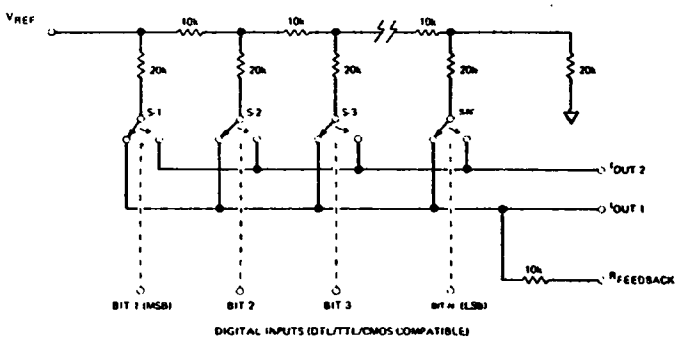
GENERAL DESCRIPTION

The AD7520 (AD7521) is a low cost, monolithic 10-bit (12-bit) multiplying digital-to-analog converter packaged in a 16-pin (18-pin) DIP. The devices use advanced CMOS and thin film technologies providing up to 10-bit accuracy with TTL/DTL/CMOS compatibility.

The AD7520 (AD7521) operates from +5V to +15V supply and dissipates only 20 mW, including the ladder network.

Typical AD7520 (AD7521) applications include: digital/analog multiplication, CRT character generation, programmable power supplies, digitally controlled gain circuits, etc.

FUNCTIONAL DIAGRAM



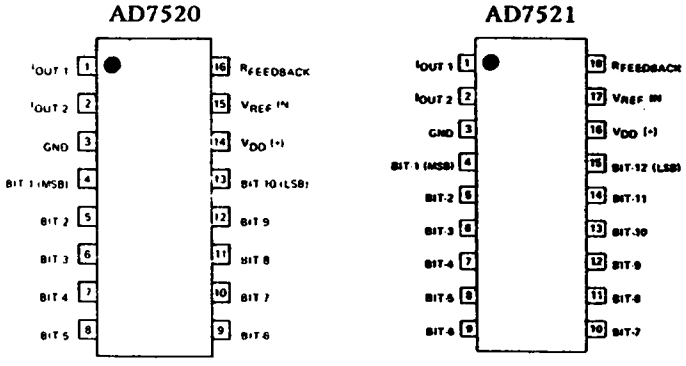
AD7520: N=10
AD7521: N=12
Logic: A switch is closed to $I_{OUT\ 1}$ for its digital input in a "HIGH" state.

ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0 C to +70 C	−25°C to +85°C	−55°C to +125°C
0.2% (8-Bit)	AD7520JN AD7521JN	AD7520JD AD7521JD	AD7520SD AD7521SD
0.1% (9-Bit)	AD7520KN AD7521KN	AD7520KD AD7521KD	AD7520TD AD7521TD
0.05% (10-Bit)	AD7520LN AD7521LN	AD7520LD AD7521LD	AD7520UD AD7521UD

PIN CONFIGURATION

TOP VIEW



PACKAGE IDENTIFICATION

Suffix D: Ceramic DIP package
Suffix N: Plastic DIP package

Route 1 Industrial Park; P.O.Box 280; Norwood,Mass.02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 213/595-1783 Mid-West 312/894-3300 Texas 214/231-5094

SPECIFICATIONS (V_{DD} = +15, V_{REF} = +10 V, T_A = 25°C unless otherwise noted)

PARAMETER		AD7520	AD7521	UNITS	LIMIT	TEST CONDITIONS		FIG.
DC ACCURACY (Note 1)								
Resolution		10	12	Bits				
Nonlinearity	J S	0.2 (8 Bit)		% of FSR	Max	S, T, U: over −55°C to +125°C −10V ≤ V_{REF} ≤ +10V		5
	K T	0.1 (9 Bit)		% of FSR	Max			5
	L U	0.05 (10 Bit)		% of FSR	Max			5
Nonlinearity Tempco		2		PPM of FSR/°C	Max	−10V ≤ V_{REF} ≤ +10V		
Gain Error (Note 2)		0.3		% of FSR	Typ			
Gain Error Tempco (Note 2)		10		PPM of FSR/°C	Max			
Output Leakage Current (either output)		200		nA	Max	Over specified temperature range		
Power Supply Rejection		50		PPM of FSR/%C	Typ			6
AC ACCURACY Output Current Settling Time		500		ns	Typ	To 0.05% of FSR All digital inputs low to high and high to low		10
Feedthrough Error		10		mV pp	Max	V_{REF} = 20 V pp, 100 kHz All digital inputs low		9
REFERENCE INPUT Input Resistance (Note 4)		5 k		Ω	Min			
		10 k			Typ			
		20 k			Max			
ANALOG OUTPUT Output Capacitance	$I_{OUT\ 1}$	120		pF	Typ	All digital inputs high		8
	$I_{OUT\ 2}$	37		pF	Typ			
	$I_{OUT\ 1}$	37		pF	Typ	All digital inputs low		8
	$I_{OUT\ 2}$	120		pF	Typ			
Output Noise (both outputs)		Equivalent to 10 kΩ Johnson noise			Typ			7
DIGITAL INPUTS (Note 3)								
Low State Threshold		0.8		V	Max	Over specified temperature range		
High State Threshold		2.4		V	Min			
Input Current (low to high state)		1		μA	Typ			
Input Coding		Binary				See Tables 1 & 2 on page 6		
POWER REQUIREMENTS Power Supply Voltage Range		+5 to +15		V				
I_{DD}		5		nA	Typ	All digital inputs at GND		
		2		mA	Max	All digital inputs high or low		
Total Dissipation (Including ladder)		20		mW	Typ			
PRICE (100-499)	8 BIT	AD7520JN AD7520JD AD7520SD		$12.00 17.00 33.00		AD7521JN AD7521JD AD7521SD	$15.00 20.00 37.00	
	9 BIT	AD7520KN AD7520KD AD7520TD		$16.25 25.00 49.00		AD7521KN AD7521KD AD7521TD	$19.25 28.00 53.00	
	10 BIT	AD7520LN AD7520LD AD7520UD		$22.00 33.00 69.00		AD7521LN AD7521LD AD7521UD	$25.00 36.00 73.00	

NOTES:
1. Full scale range (FSR) is 10V for unipolar mode and ±10V for bipolar mode.
2. Using the internal $R_{FEEDBACK}$
3. Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4. Ladder and feedback resistor tempco is approximately −150ppM/°C.

Specifications subject to change without notice.

SPECIFICATIONS (CONTINUED)

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

V_{DD} (to Gnd)	+17 V
V_{REF} (to Gnd)	±25 V
Digital Input Voltage Range	V_{DD} to Gnd
Output Voltage (Pin 1, Pin 2)	−100mV to V_{DD}
Power Dissipation (package)	
up to +75°C	450 mW
derates above +75°C by	6 mW/°C
Operating Temperature	
JN, KN, LN Versions	0°C to +70°C
JD, KD, LD Versions	−25°C to +85°C
SD, TD, UD Versions	−55°C to +125°C
Storage Temperature	−65°C to +150°C

CAUTION

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

TYPICAL PERFORMANCE CURVES (T_A = +25°C, V_{DD} = +15 V unless otherwise noted)

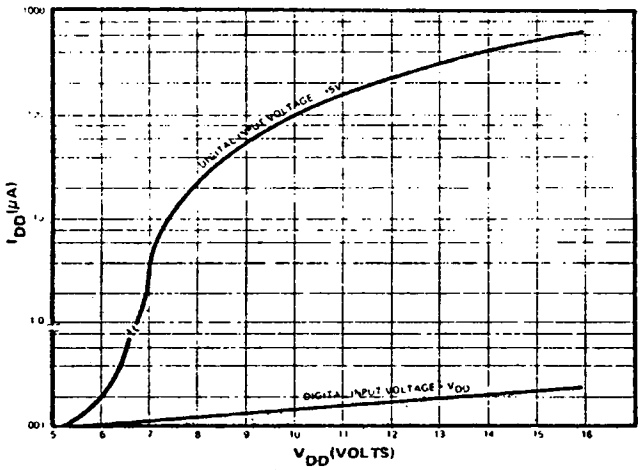


FIG. 1. SUPPLY CURRENT VS. SUPPLY VOLTAGE

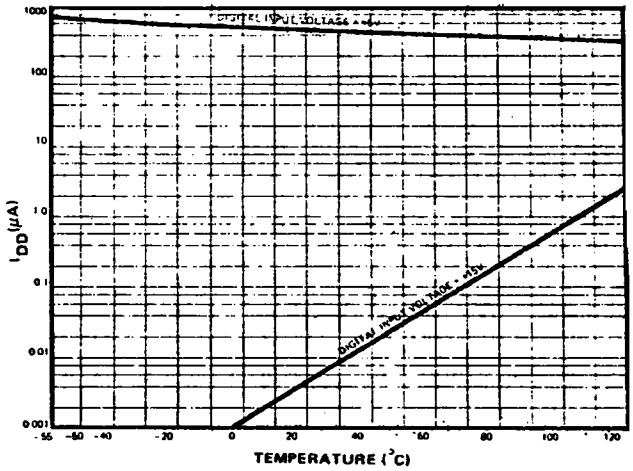


FIG. 2. SUPPLY CURRENT VS. TEMPERATURE

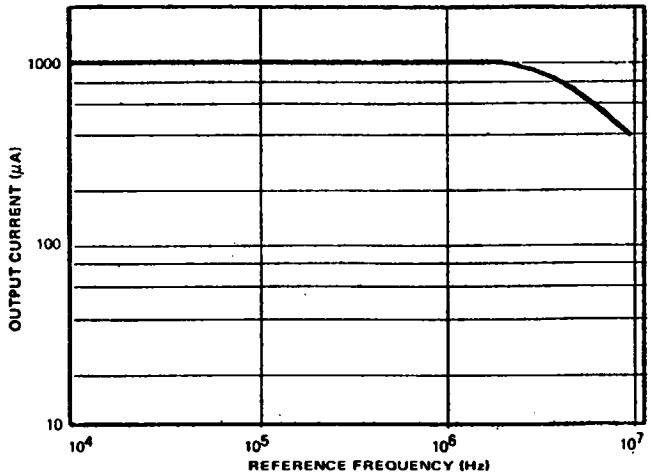


FIG. 3. OUTPUT CURRENT BANDWIDTH

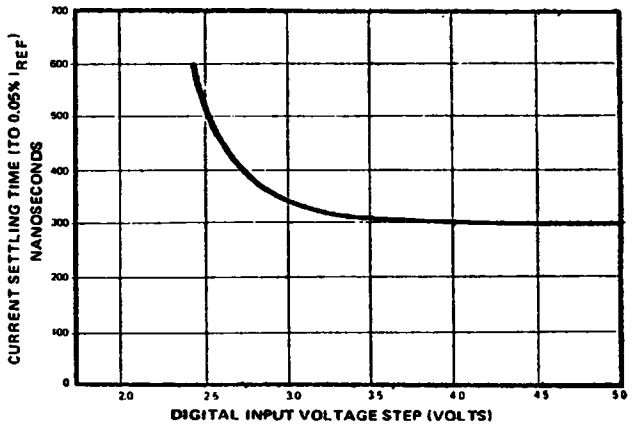


FIG. 4. OUTPUT CURRENT SETTLING TIME VS DIGITAL INPUT VOLTAGE

TEST CIRCUITS

Note: The following test circuits apply for the AD7520. Similar circuits can be used for the AD7521.

DC PARAMETERS

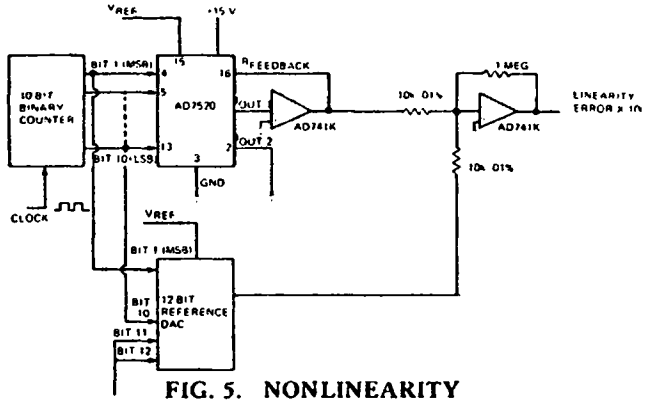


FIG. 5. NONLINEARITY

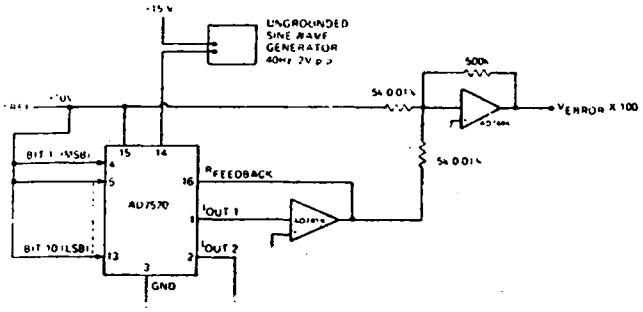


FIG. 6. POWER SUPPLY REJECTION

AC PARAMETERS

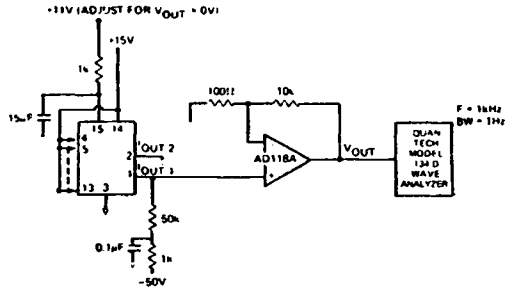


FIG. 7. NOISE

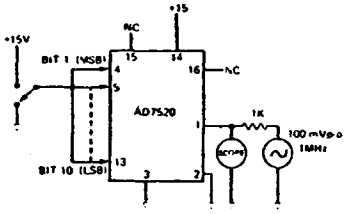


FIG. 8. OUTPUT CAPACITANCE

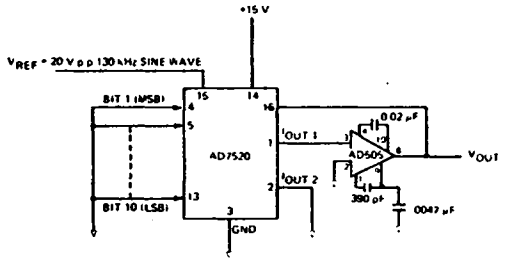


FIG. 9. FEEDTHROUGH ERROR

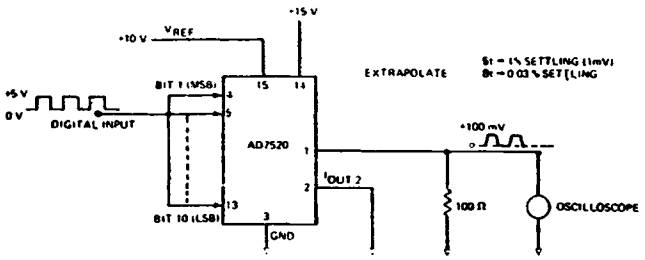


FIG. 10. OUTPUT CURRENT SETTLING TIME

TERMINOLOGY

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from $I_{OUT\ 1}$ and $I_{OUT\ 2}$ terminals to ground.

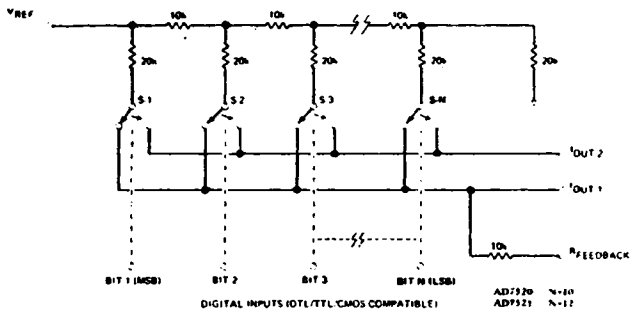
OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7520 (AD7521), a 10-bit (12-bit) multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten (twelve) CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in figure 11. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the $I_{OUT\ 1}$ and $I_{OUT\ 2}$ bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.



(Switches shown for Inputs "High")

FIG. 11. AD7520 (AD7521) FUNCTIONAL DIAGRAM

One of the CMOS current switches is shown in figure 12. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the first six switches are binarily scaled so the voltage drop across each switch is the same. For example, switch-1 of figure 12 was designed for an "ON" resistance of 20 ohms, switch-2 of 40 ohms and so on. For a 10 V reference input, the current through switch 1 is 0.5 mA, the current through switch 2 is 0.25 mA, and so on, thus maintaining a constant 10 mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

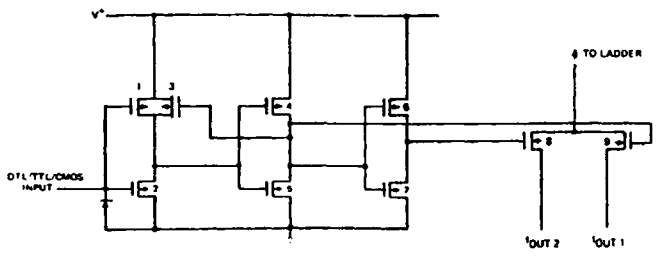


FIG. 12. CMOS SWITCH

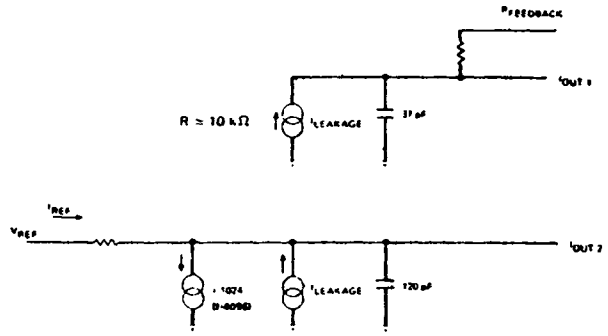


FIG. 13. AD7520 (AD7521) EQUIVALENT CIRCUIT– ALL DIGITAL INPUTS LOW

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in figures 13 and 14. In figure 13 with all digital inputs low, the reference current is switched to $I_{OUT\ 2}$. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{1}{1024}\left(\frac{1}{4096}\right)$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 120pF, as shown on the $I_{OUT\ 2}$ terminal. The "OFF" switch capacitance is 37 pF, as shown on the $I_{OUT\ 1}$ terminal. Analysis of the circuit for all digital inputs high, as shown in figure14, is similar to figure 13; however, the "ON" switches are now on terminal $I_{OUT\ 1}$, hence the 120 pF at that terminal.

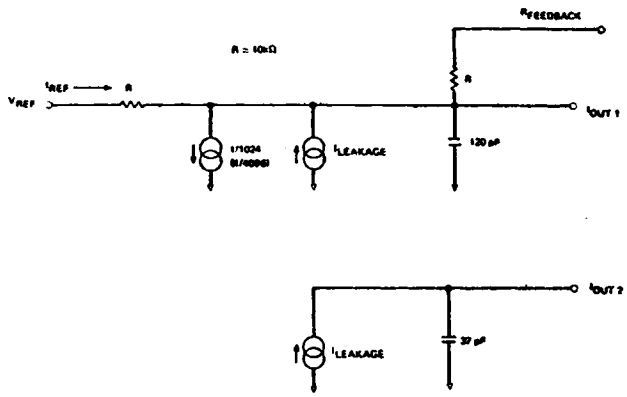


FIG. 14. AD7520 (AD7521) EQUIVALENT CIRCUIT– ALL DIGITAL INPUTS HIGH

UNIPOLAR BINARY OPERATION

Figure 15 shows the circuit connections required for unipolar operation using the AD7520. Since V_{REF} can assume either positive or negative values, the circuit is also capable of 2-quadrant multiplication. The input code/output range table for unipolar binary operation is shown in Table 1.

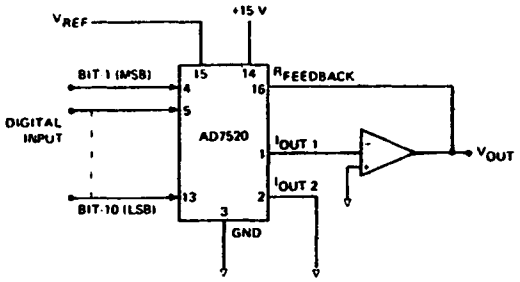


FIG. 15. UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Zero Offset Adjustment

1. Tie all digital inputs to the AD7520 (AD7521) to GND potential.
2. Adjust the offset trimpot on the output operational amplifier for 0 V ± 1 mV at V_{OUT}.

Gain Adjustment

1. Tie all digital inputs to the AD7520 (AD7521) to the +15V supply.
2. To increase V_{OUT}, place a resistor R in series with the amplifier output terminal and $R_{FEEDBACK}$ of the AD7520 (AD7521). (R=0 to 500Ω)
3. To decrease V_{OUT}, place a resistor R in series with V_{REF}. (R=0 to 500Ω)

TABLE 1
CODE TABLE – UNIPOLAR BINARY OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1-2^{-10})$
1000000001	$-V_{REF}(1/2+2^{-10})$
1000000000	$\frac{-V_{REF}}{2}$
0111111111	$-V_{REF}(1/2-2^{-10})$
0000000001	$-V_{REF}(2^{-10})$
0000000000	0

NOTE: 1 LSB = 2^{-10} V_{REF}

BIPOLAR (OFFSET BINARY) OPERATION

Figure 16 illustrates the AD7520 connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. Input coding is offset binary (modified 2's complement) as shown in Table 2.

TABLE 2
CODE TABLE – BIPOLAR (OFFSET BINARY) OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1-2^{-9})$
1000000001	$-V_{REF}(2^{-9})$
1000000000	0
0111111111	$V_{REF}(2^{-9})$
0000000001	$V_{REF}(1-2^{-9})$
0000000000	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

When a switch's control input is a logical "1", that switch's current is steered to $I_{OUT\ 1}$, forcing the output of amplifier #1 to

$$V_{OUT} = -(I_{OUT\ 1})(10k)$$

where 10k is the value of the feedback resistor.

A logical "0" on the control input steers the switch's current to $I_{OUT\ 2}$, which is terminated into the summing junction of amplifier #2. Resistors R1 and R2 need not track the internal R-2R circuitry; however, they should closely match each other to insure that the voltage at amplifer #2's output will force a current into R2 which is equal in magnitude but opposite in polarity to the current at $I_{OUT\ 2}$. This creates a push-pull effect which halves the resolution but doubles the output range for changes in the digital input.

With the MSB a logic "1" and all other bits a logic "0", a 1/2 LSB difference current exists between $I_{OUT\ 1}$ and $I_{OUT\ 2}$, creating an offset of 1/2 LSB. To shift the transfer curve to zero, resistor R-9 is used to sum 1/2 LSB of current into the $I_{OUT\ 2}$ terminal.

Offset Adjustment

1. Make V_{REF} approximately +10 V.
2. Tie all digital inputs to +15 V (logic "1").
3. Adjust amplifier #2 offset trimpot for 0 V ±1 mV at amplifier #2 output.
4. Tie MSB (Bit-1) to +15 V, all other bits to ground
5. Adjust amplifier #1 offset trimpot for 0 V ± 1 mV at V_{OUT}.

Gain Adjustment

Gain adjustment is the same as for unipolar operation.

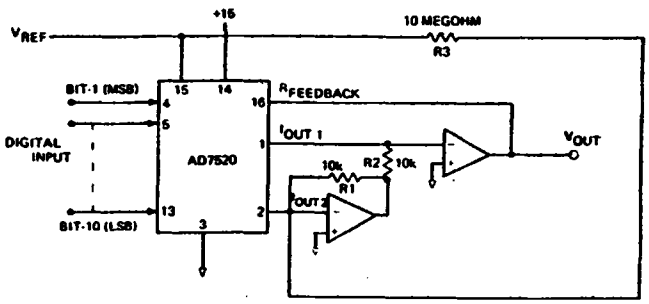


FIG. 16. BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

DYNAMIC PERFORMANCE CHARACTERISTICS

The following circuits and associated waveforms illustrate the dynamic performance which can be expected using some commonly available IC amplifiers. All settling times are to 0.05% of 10 V.

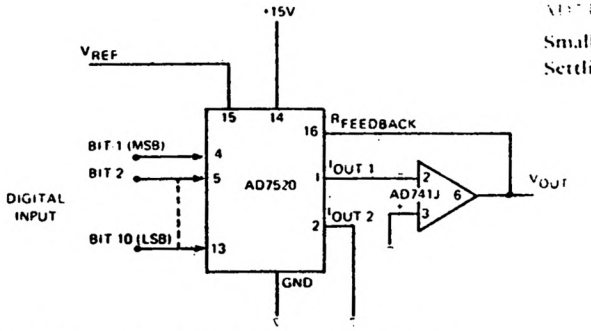


FIG. 17. DAC CIRCUIT USING AD741J

AD741J

Small Signal Bandwidth: 180kHz
Settling Time: 20μs

20μs/DIV

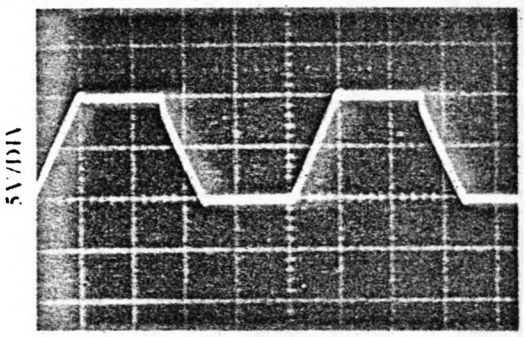


FIG. 18. OUTPUT WAVEFORM

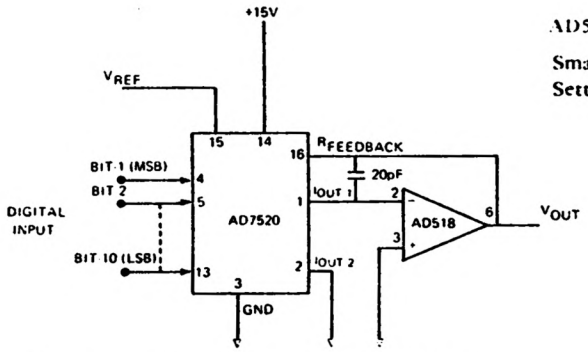


FIG. 19. DAC CIRCUIT USING AD518K

AD518K

Small Signal Bandwidth: 1.0 MHz
Settling Time: 6.0μs

1μs/DIV

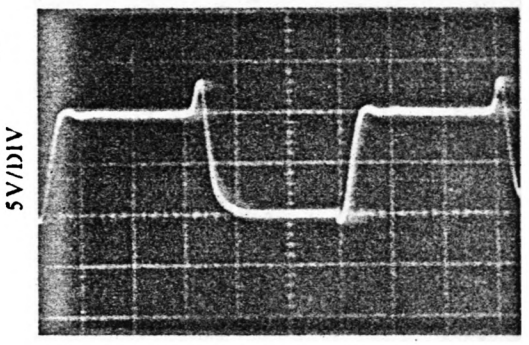


FIG. 20. OUTPUT WAVEFORM

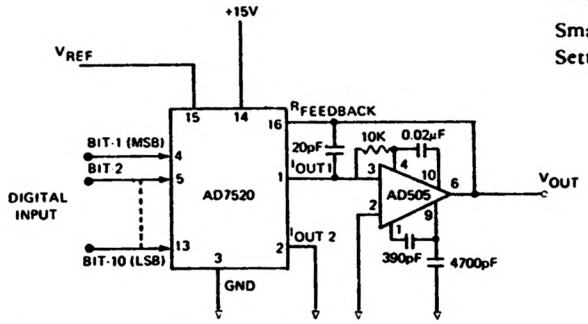


FIG. 21. DAC CIRCUIT USING AD505J

AD505J

Small Signal Bandwidth: 1.0MHz
Settling Time: 2.5μs

1μs/DIV

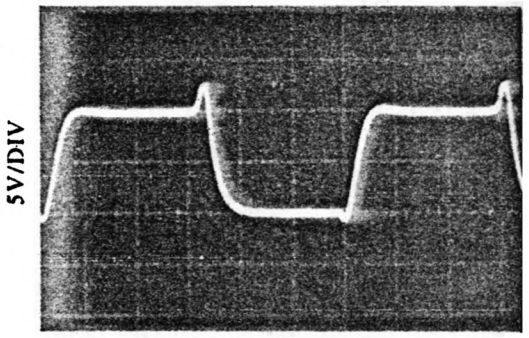


FIG. 22. OUTPUT WAVEFORM

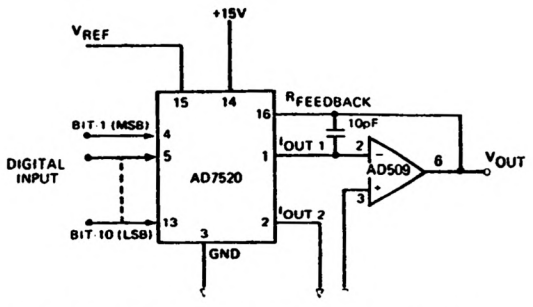


FIG. 23. DAC CIRCUIT USING AD509K

AD509K

Small Signal Bandwidth: 1.6MHz
Settling Time: 2.0μs

1μs/DIV

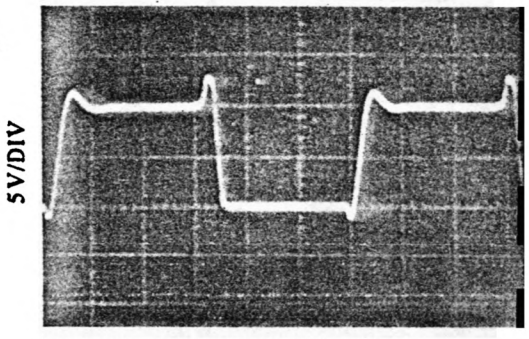


FIG. 24. OUTPUT WAVEFORM

APPLICATIONS (CONTINUED)

ANALOG/DIGITAL DIVISION

With the AD7520 connected in its normal multiplying configuration as shown in figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_x assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in figure 25, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit-10) ON, the gain is 1024. With all bits ON, the gain is 1 (±1 LSB).

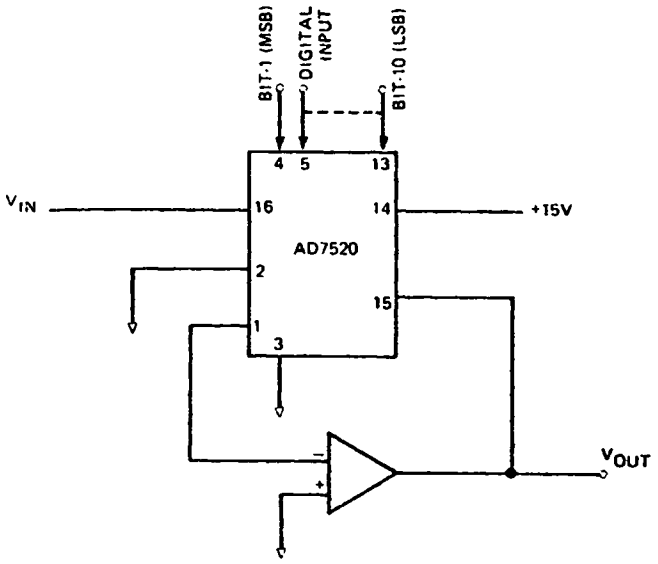


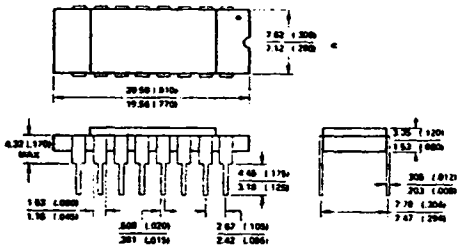
FIG. 25. ANALOG/DIGITAL DIVIDER

MECHANICAL INFORMATION

OUTLINE DIMENSIONS

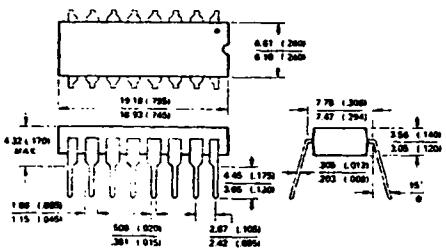
AD7520

16 PIN CERAMIC DIP



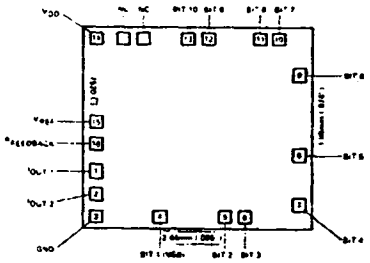
1. Lead no. 1 identified by dot or notch.
2. Dimensions in millimeters (inches).

16 PIN PLASTIC DIP



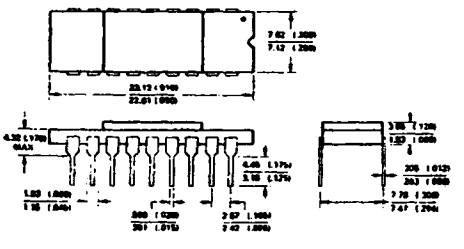
1. Lead no. 1 identified by dot or notch.
2. Dimensions in millimeters (inches).

BONDING DIAGRAM



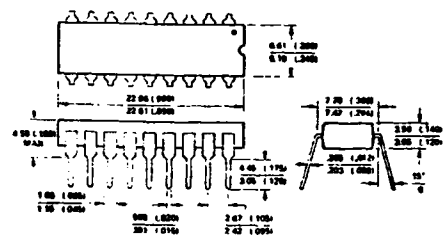
AD7521

18 PIN CERAMIC DIP



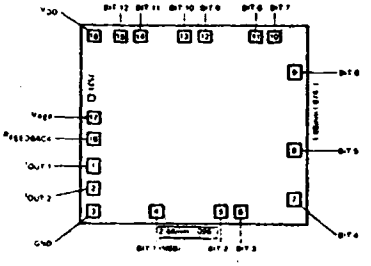
1. Lead no. 1 identified by dot or notch.
2. Dimensions in millimeters (inches).

18 PIN PLASTIC DIP



1. Lead no. 1 identified by dot or notch.
2. Dimensions in millimeters (inches).

BONDING DIAGRAM



BINARY DIGITAL TO ANALOG CONVERTER
MODELS CY2035, CY2135, CY2235

TECHNICAL DATA - JANUARY, 1972

DESCRIPTION

The CY2035 (8 Bit), CY2135 (10 Bit), and CY2235 (12 Bit), Digital to analog Converter Series features a combination of linearity, temperature stability, and settling time compatible with moderate environment operational requirements, at the LOWEST POSSIBLE COST.

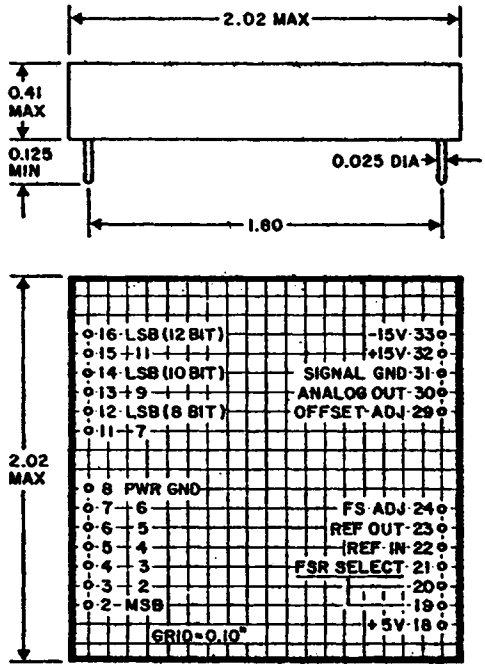
Use of stable thin film resistor networks, high quality reference devices and low drift operational amplifiers in CYCON proprietary circuitry offers the user the most economical solution where reliability and long term stability are important requirements.

This economical series of D/A converters is exceptionally suited for high quantity DAC applications. Typical examples include: precise generation of non-linear functions, digitally programmed power supplies, and replacing analog sample/hold circuits in multiple channel closed loop process control systems.

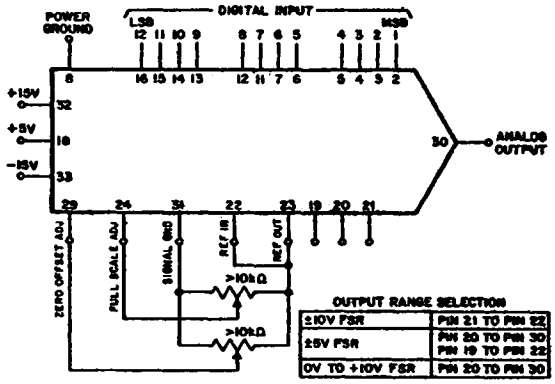
The Series is size and pin compatible with the CYCON CY2X36 and CY2X37 Series of DAC's, and features the same high quality modular construction techniques.

FEATURES

- INEXPENSIVE - a significant breakthrough in price/performance ratio.
- LOW LINEARITY DRIFT - 0.0005% per °C over full operational temperature range.
- LOW ZERO OFFSET DRIFT - improved design provides greatly reduced offset drift over full operational temperature range.
- INTERNAL/EXTERNAL REFERENCE - User selectable by jumper wire. Internal reference available for external use.
- 3 OUTPUT RANGES - ±10V, 0-10V, or ±5V are standard options by simply jumpering pins.
- FULL SCALE AND ZERO OFFSET ADJUSTABLE - externally fine trimable for improved accuracy.
- PARALLEL INPUT - DTL/TTL compatible, one line per bit, one TTL load per line. Straight binary or offset binary options.
- RUGGED CONSTRUCTION - Encapsulated module designed for DIP IC compatibility. High quality brass, gold plated pins on .1" centers.



BOTTOM VIEW
ALL DIMENSIONS IN INCHES



CYCON Inc
1080E DUANE AVE. SUNNYVALE, CALIF. 94086
TEL. 408-732-8311 TWX. 910-339-9216

OPERATIONAL CHARACTERISTICS

FULL SCALE OUTPUT VOLTAGE RANGES (user selectable by jumper)	0V to +10V, Straight Binary Code -5V to +5V, Offset Binary Code -10V to +10V, Offset Binary Code
OUTPUT LOAD, rated specifications (short Circuit proof)	$R_L \geq 2K\Omega$, $C_L \leq 1000pf$
OUTPUT IMPEDANCE (DC)	≤ 0.1 ohm
REFERENCE OUTPUT	+10.08V nominal at 5mA
INPUT LOGIC LEVELS	TTL/DTL compatible, 8, 10 or 12 parallel bits V_H = Logical "1", +2.1V to +5.5V V_L = Logical "0", 0V to +0.7V
DATA LOADING	1 TTL Load/Line
TEMPERATURE RANGE	
Rated Specifications	0°C to +70°C
Operational	-25°C to +85°C
Storage	-55°C to +100°C
POWER REQUIREMENTS	+15V ±5% at 30mA -15V ±5% at 20mA + 5V ±5% at 80mA

SPECIFICATIONS (T_A =25°C unless otherwise noted)

MODEL NUMBER	CY2035	CY2135	CY2235
RESOLUTION (Binary Bits)	8	10	12
SETTLING TIME in μs (to ±0.05% of full scale, 0 to +10V)	20	20	20
LINEARITY in percent of full scale: (at 25°C)	0.2	0.05	0.0125
(at 0°C to +70°C)	0.25	0.075	0.0375
ZERO OFFSET in percent of full scale[1]	0.2	0.05	0.05
SCALE FACTOR (GAIN) ERROR in percent of reading[1]	0.2	0.1	0.1
ZERO DRIFT in percent of full scale per °C from 0°C to +70°C	0.005	0.002	0.002
SCALE FACTOR (GAIN) DRIFT in percent of reading per °C from 0°C to +70°C			
with Internal Reference	0.005	0.005	0.004
with External Reference	0.003	0.003	0.002
LONG TERM STABILITY in percent of full scale: Per 1000 hours	0.1	0.05	0.05
Per Year	0.3	0.1	0.1
PRICE 1 - 24 →	19.00	29.00	49.00
25-99			

FOB Sunnyvale, California - Prices subject to change without notice

[1] Zero Offset and Scale Factor Error are initially adjusted to the indicated tolerances on the 0V to +10V Output Range, with the Internal Reference connected, at 25°C ±5°C. Adjustment terminals are provided for optional external fine trimming of zero and scale factor.

CYCON Inc
1080E DUANE AVE. SUNNYVALE, CALIF. 94086
TEL. 408-732-8311 TWX. 910-339-9216

ANALOG DEVICES

Lowest Cost High Accuracy IC Op Amps

AD741J,K,L,S

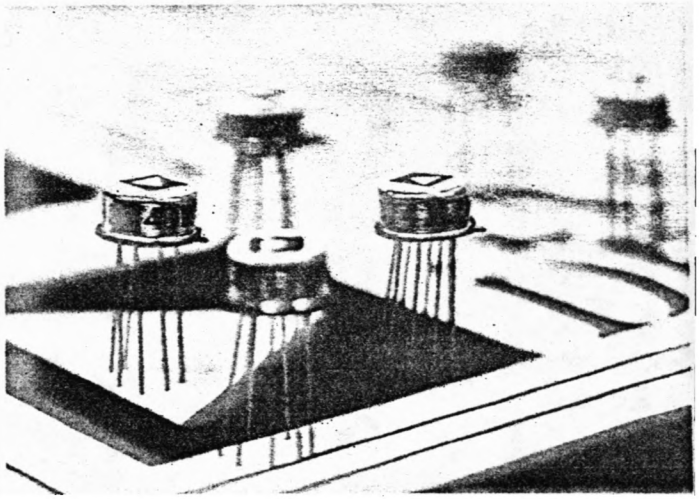
FEATURES

Precision Input Characteristics
- Low V_{OS}: 0.5mV max (L)
- Low V_{OS} Drift: 5μV/°C max (L)
- Low I_b: 50nA max (L)
- Low I_{OS}: 5nA max (L)
- High CMRR: 90dB min (K, L)

High Output Capability
- A_{OL} = 25,000 min, 1kΩ load (J, S)
  T_{min} to T_{max}
- V_O = ±10V min, 1kΩ load (J, S)

Low Cost (100 pieces)

AD741J	$1.25
AD741K	$2.25
AD741L	$6.00
AD741S	$3.30



GENERAL DESCRIPTION

The Analog Devices AD741J, AD741K, AD741L and AD741S are specially tested and selected versions of the popular AD741 operational amplifier. Improved processing and additional electrical testing guarantee the user precision performance at a very low cost. The AD741J, K and L substantially increase overall accuracy over the standard AD741C by providing maximum limits on offset voltage drift, and significantly reducing the errors due to offset voltage, bias current, offset current, voltage gain, power supply rejection, and common mode rejection (see Error Analysis). For example, the AD741L features maximum offset voltage drift of 5μV/°C, offset voltage of 0.5mV max, offset current of 5nA max, bias current of 50nA max, and a CMRR of 90dB min. The AD741S offers guaranteed performance over the extended temperature range of −55°C to +125°C, with max offset voltage drift of 15μV/°C, max offset voltage of 4mV, max offset current of 25nA, and a minimum CMRR of 80dB.

HIGH OUTPUT CAPABILITY

Both the AD741J and AD741S offer the user the additional advantages of high guaranteed output current and gain at low values of load impedance. The AD741J guarantees a minimum gain of 25,000, swinging ±10V into a 1kΩ load from 0°C to +70°C. The AD741S guarantees a minimum gain of 25,000, swinging ±10V into a 1kΩ load from −55°C to +125°C.

All devices feature full short circuit protection, high gain, high common mode range, and internal compensation. The AD741J, K and L are specified for operation from 0°C to +70°C, and are available in both the TO-99 and mini-DIP packages. The AD741S is specified for operation from −55°C to +125°C, and is available in the TO-99 package.

GUARANTEED ACCURACY

The vastly improved performance of the AD741J, AD741K, AD741L and AD741S provides the user with an ideal choice when precision is needed and economy is a necessity. An error budget is calculated for all versions of the AD741 (see page 3); it is obvious that these selected versions offer substantial improvements over the industry-standard AD741C and AD741. A typical circuit configuration (see Figure 1) is assumed, and the various errors are computed using maximum values over the full operating temperature range of the devices. *The results indicate a factor of 8 improvement in accuracy of the AD741L over the AD741C, a factor of 5 improvement using the AD741K, and a factor of 2.5 improvement using the AD741J. The AD741S, similarly, achieves a factor of 3.5 improvement over the standard AD741.* Note that the total error has been determined as a sum of component errors, while in actuality, the total error will be much less. Also, while the circuit used for the error analysis is only one of a multitude of possible applications, it effectively demonstrates the great improvement in overall 741 accuracy achievable at relatively low cost with the AD741J, K, L or S.

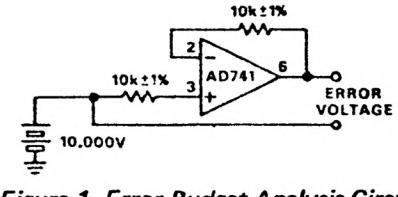


Figure 1. Error Budget Analysis Circuit

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577

SPECIFICATIONS (typical @ +25°C and ±15VDC, unless otherwise specified)

MODEL	AD741J	AD741K	AD741L	AD741S
OPEN LOOP GAIN				
R_L = 1kΩ, V_O = ±10V	50,000 min (200,000 typ)			•
R_L = 2kΩ, V_O = ±10V		50,000 min (200,000 typ)	50,000 min (200,000 typ)	
Over Temp Range, T_{min} to T_{max}, same loads as above	25,000 min	•	•	•
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 1kΩ, T_{min} to T_{max}	±10V min (±13V typ)			•
Voltage @ R_L = 2kΩ, T_{min} to T_{max}		±10V min (±13V typ)	±10V min (±13V typ)	
Short Circuit Current	25mA	•	•	•
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1MHz	•	•	•
Full Power Response	10kHz	•	•	•
Slew Rate, Unity Gain	0.5V/μsec	•	•	•
INPUT OFFSET VOLTAGE				
Initial, $R_S \leq$ 10kΩ (adjustable to zero)	3mV max (1mV typ)	2mV max (0.5mV typ)	0.5mV max (0.2mV typ)	2mV max (1mV typ)
T_{min} to T_{max}	4mV max	3mV max	1mV max	•
Avg vs Temperature (untrimmed)	20μV/°C max	15μV/°C max (6μV/°C typ)	5μV/°C max (2μV/°C typ)	15μV/°C max (6μV/°C typ)
vs Supply, T_{min} to T_{max}	100μV/V max (30μV/V typ)	15μV/V max (5μV/V typ)	15μV/V max (5μV/V typ)	•
INPUT OFFSET CURRENT				
Initial	50nA max (5nA typ)	10nA max (2nA typ)	5nA max (2nA typ)	10nA max (2nA typ)
T_{min} to T_{max}	100nA max	15nA max	10nA max	25nA max
Avg vs Temperature	0.1nA/°C	0.2nA/°C max (0.02nA/°C typ)	0.1nA/°C max (0.02nA/°C typ)	0.25nA/°C max (0.1nA/°C typ)
INPUT BIAS CURRENT				
Initial	200nA max (40nA typ)	75nA max (30nA typ)	50nA max (30nA typ)	75nA max (30nA typ)
T_{min} to T_{max}	400nA max	120nA max	100nA max	250nA max
Avg vs Temperature	0.6nA/°C	1.5nA/°C max (0.6nA/°C typ)	1nA/°C max (0.6nA/°C typ)	2nA/°C max (0.6nA/°C typ)
INPUT IMPEDANCE				
Differential	1MΩ	2MΩ	2MΩ	2MΩ
INPUT VOLTAGE RANGE (Note 1)				
Differential, max safe	±30V	•	•	•
Common Mode, max safe	±15V	•	•	•
Common Mode Rejection, $R_S \leq$ 10kΩ, T_{min} to T_{max}, V_{in} = ±12V	80dB min (90dB typ)	90dB min (100dB typ)	90dB min (100dB typ)	•
POWER SUPPLY				
Rated Performance	±15V	•	•	•
Operating	±(5 to 18)V	±(5 to 22)V	±(5 to 22)V	±(5 to 22)V
Current, Quiescent	3.3mA max (2.0mA typ)	2.8mA max (1.7mA typ)	2.8mA max (1.7mA typ)	2.8mA max (2.0mA typ)
TEMPERATURE RANGE				
Operating, Rated Performance	0°C to +70°C	•	•	−55°C to +125°C
Storage	−65°C to +150°C	•	•	•

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

*Specifications same as AD741J.

Specifications subject to change without notice.

ERROR BUDGET ANALYSIS

PARAMETER	AD741C SPEC (0°C to +70°C)	AD741C ERROR	AD741J SPEC (0°C to +70°C)	AD741J ERROR	AD741K SPEC (0°C to +70°C)	AD741K ERROR	AD741L SPEC (0°C to +70°C)	AD741L ERROR	AD741 SPEC (−55°C to +125°C)	AD741 ERROR	AD741S SPEC (−55°C to +125°C)	AD741S ERROR
Gain (*Error = $10V_{in}/G$*)	15,000	660μV	25,000[1]	400μV	25,000	400μV	25,000	400μV	25,000	400μV	25,000[1]	400μV
I_b (*Error = I_b x resistor mismatch*)	800nA	160μV	400nA	80μV	120nA	24μV	100nA	20μV	1500nA	300μV	250nA	50μV
I_{os} (*Error = I_{os} x 10kΩ*)	300nA	3000μV	100nA	1000μV	15nA	150μV	10nA	100μV	500nA	5000μV	25nA	250μV
$\Delta V_{os}/\Delta T$ (*Error = $\Delta V_{os}/\Delta T \times \Delta T$*)	25μV/°C[2]	1125μV	20μV/°C	900μV	15μV/°C	675μV	5μV/°C	225μV	25μV/°C[2]	2500μV	15μV/°C	1500μV
CMRR (*Error = 10V/CMRR*)	70dB	3300μV	80dB	1000μV	90dB	330μV	90dB	330μV	70dB	3300μV	80dB	1000μV
PSRR (*assume a ±5% power supply variation*)	150μV/V	450μV	100μV/V	300μV	15μV/V	45μV	15μV/V	45μV	150μV/V	450μV	100μV/V	300μV
TOTAL		8.7mV		3.7mV		1.6mV		1.1mV		12.0mV		3.5mV
PRICE (*100 pieces*)	$1.00		$1.25		$2.25		$6.00		$2.00		$3.30	

[1] AD741J and AD741S...Open Loop Gain is guaranteed with a 1kΩ load.
[2] AD741C and AD741...$\Delta V_{os}/\Delta T$ is not guaranteed (for complete specifications, contact the factory for data sheet).

INPUT CHARACTERISTICS

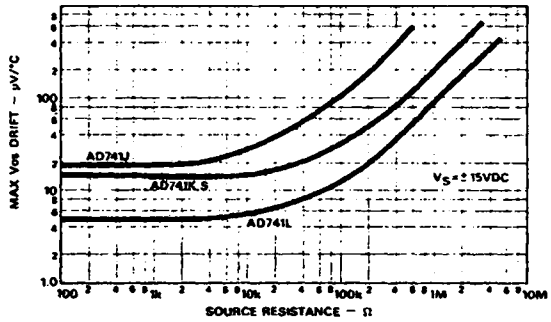


Figure 2. Max Equivalent Input Offset Drift vs. Source Resistance

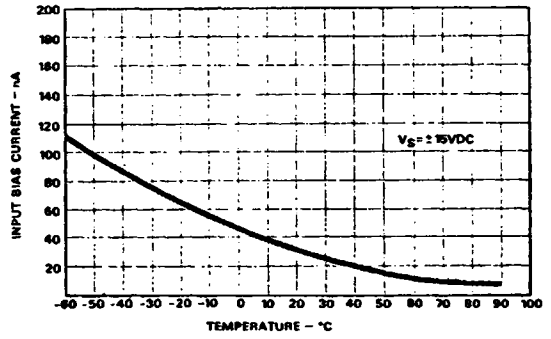


Figure 3. Input Bias Current vs. Temperature

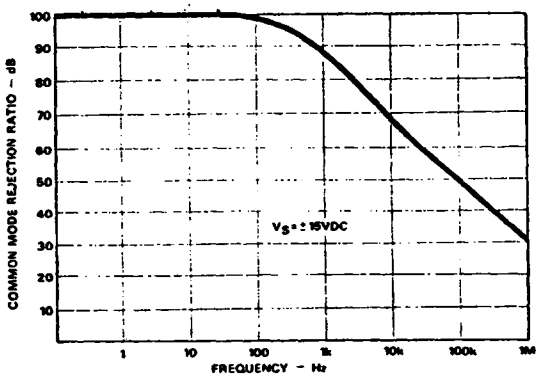


Figure 4. Common Mode Rejection vs. Frequency

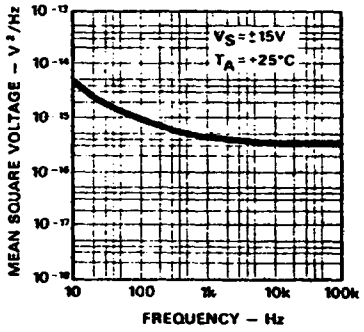


Figure 5. Input Noise Voltage vs. Frequency

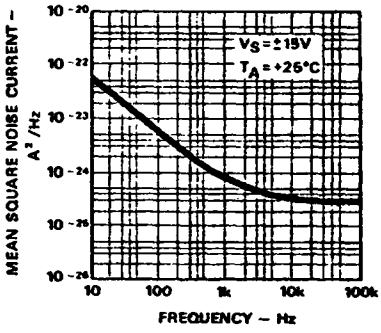


Figure 6. Input Noise Current vs. Frequency

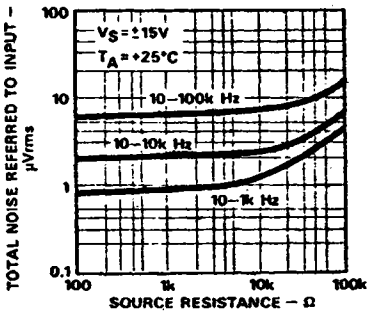


Figure 7. Broadband Noise vs. Source Resistance

OUTPUT CHARACTERISTICS

The AD741J and AD741S are specially selected for high output current capability. High efficiency output transistors, thermally balanced chip design and precise short circuit current control insure against gain degradation at high current levels and temperature extremes. The AD741J guarantees a minimum gain of 25,000, swinging ±10V into a 1kΩ load from 0°C to +70°C. The AD741S guarantees minimum gain of 25,000, swinging ±10V into a 1kΩ load from −55°C to +125°C. The AD741K and AD741L are guaranteed with the standard 2kΩ load.

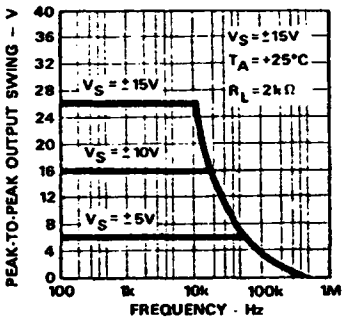


Figure 8. Output Voltage Swing vs. Frequency

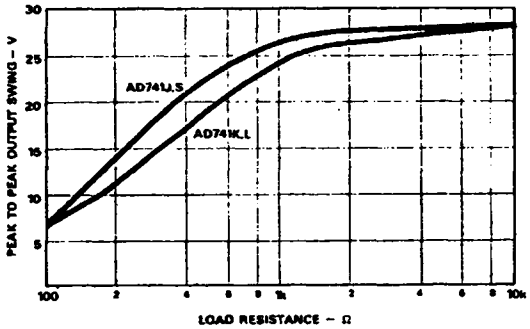


Figure 9. Output Voltage Swing vs. Load Resistance

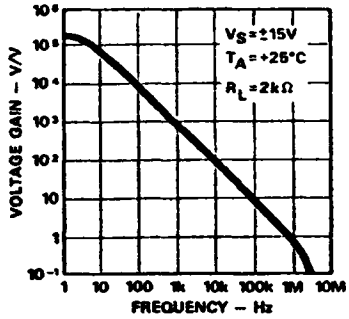
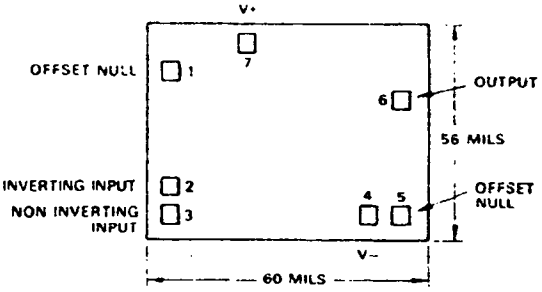


Figure 10. Open Loop Gain vs. Frequency

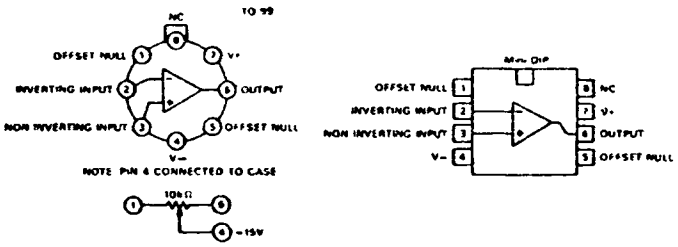
BONDING DIAGRAM

All versions of the AD741 are available in chip or wafer form, fully tested at +25°C. Because of the critical nature of using unpackaged devices, it is suggested that the factory be contacted for specific information regarding price, delivery and testing.



CONNECTION DIAGRAMS

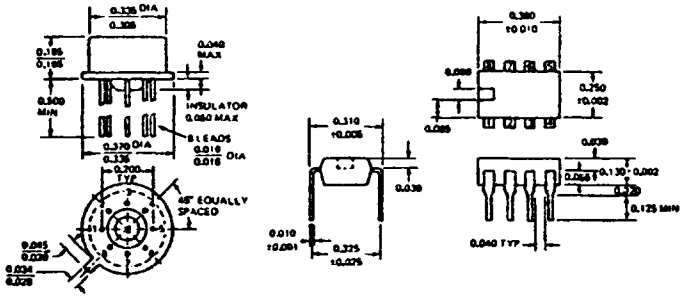
(Top View)



(H package) (N package)

PHYSICAL DIMENSIONS

(In Inches)



MIL-STANDARD-883

The AD741S is available with 100% screening to MIL-STD-883, Method 5004, Class A, B, or C. Consult the factory for pricing and delivery.

ORDERING GUIDE

MODEL	TEMP. RANGE	ORDER NUMBER	PRICE (1–24)	PRICE (25–99)	PRICE (100–999)
AD741J	0°C to +70°C	AD741J*	$1.85	$1.50	$1.25
AD741K	0°C to +70°C	AD741K*	$3.40	$2.70	$2.25
AD741L	0°C to +70°C	AD741L*	$9.00	$7.20	$6.00
AD741S	−55°C to +125°C	AD741SH	$4.95	$4.00	$3.30

*Add Package Type Letter; H = TO-99, N = Mini-DIP.

Motorola K1100A Crystal Clock Oscillators

30 MHz 250 kHz to 20 MHz

.815" x .515" AREA

.200" SEATED HEIGHT

DUAL IN-LINE SPACING

WIDE FREQUENCY RANGE

+5V dc INPUT

TTL COMPATIBLE OUTPUT

±.01% STABILITY

Features

■ **HIGH DENSITY PACKAGING** — takes up only .815" x .515" on a circuit board, and its seated height of .200" lets you use standard logic boards with no loss of spacing. Can be soldered directly to the PCB or mounted in a DIP socket, according to your production needs.

■ **TTL COMPATIBLE**—uses standard +5V dc input, drives standard TTL logic, fan out of 10.

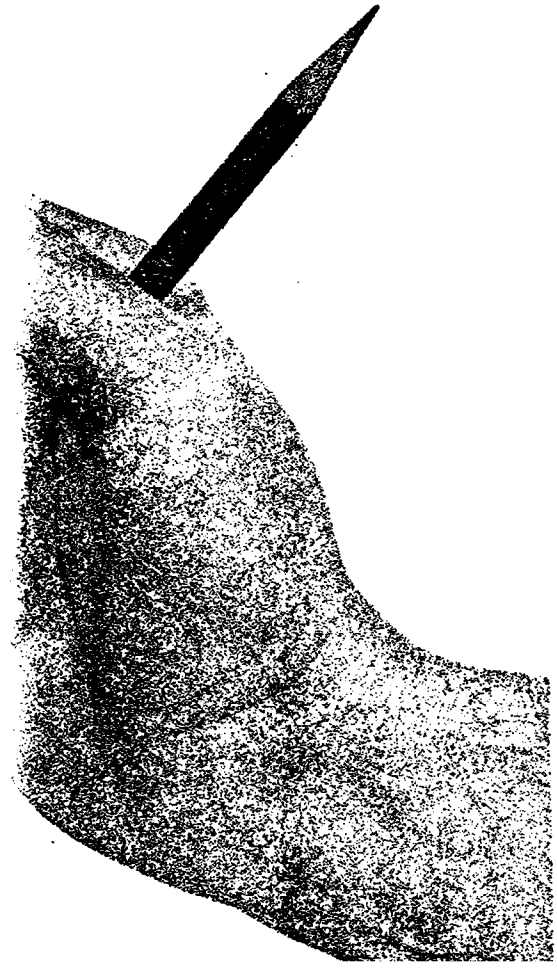
■ **±0.01% FREQUENCY STABILITY** —over the range of 0°C to 70°C, suitable for most applications in data communication logic timing. This specification is inclusive of calibration tolerance, stability vs. input voltage change, stability vs. load change, aging, and stability vs. shock and vibration.

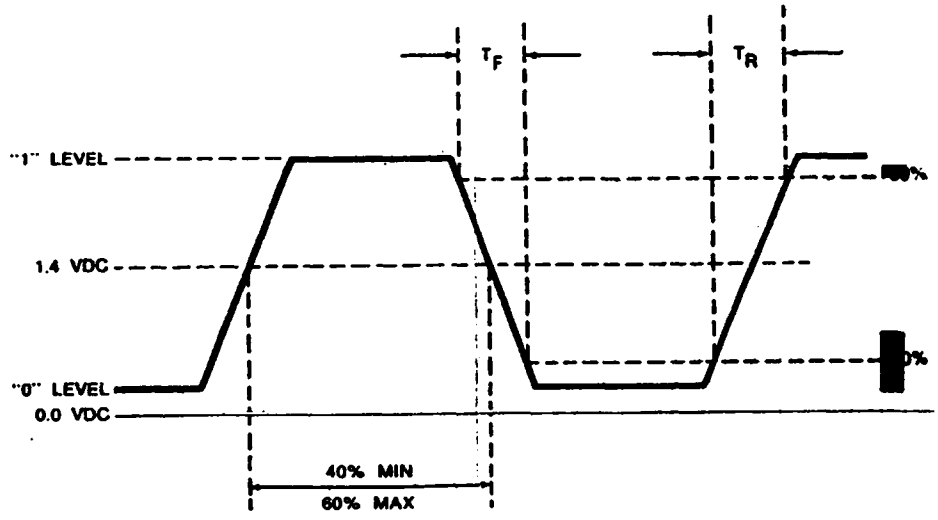
■ **RUGGED, RELIABLE** — maximum reliability at minimum cost is the result of combining two of Motorola's fields of experience: quartz crystal technology and thick film hybrid integrated circuit processing. Mass automated production techniques assure volume production. Gold plating of all crystals and Class 100 clean room processing testify that no short cuts are taken that might diminish reliability. Environmental testing proves the effectiveness of the rugged design for those applications in which shock and vibration are common hazards.

■ **YOUR TIMING NEEDS IN ON[E] PACKAGE** — The K1100A oscillator uses essentially the same components to generate any discrete frequency from 250 kHz to 20 MHz; only the frequency-determining elements and laser-trim settings change. The manufacturing savings inherent in this design are passed on to you, simplifying your make vs. buy decision. You can divert engineering manhours from oscillator design to equipment or system design, saving chronological time as well. And with a packaged oscillator, you eliminate source-hunting and source-qualifying for its components, cut down on direct labor for parts insertion, cut down on overhead costs for Receiving, Incoming Inspection, Purchasing and Accounts Payable.

■ **COMPLETE PROCESS CONTROL** —Motorola is the only totally integrated manufacturer of quartz frequency control devices. Full control of all the processes from growing, sawing, lapping, and finishing quartz to combining it with other components into an electronic product—CRYSTAL CLOCK OSCILLATORS.

■ **VOLUME PRODUCTION**—production facilities oriented to mass automated production techniques. And, if required, capital for expansion is available to meet even greater requirements.





K1100A CRYSTAL CLOCK OSCILLATOR WAVE SHAPE

specifications

- **FREQUENCY RANGE:** 250 kHz-~~20 MHz~~ 30 MHz
- **FREQUENCY STABILITY:** ± .01%
  (Inclusive of calibration tolerance at 25°C, operating temperature range, input voltage change, load change, aging, shock, and vibration).
- **TEMPERATURE RANGE:**
  OPERATING: 0°C to 70°C
  STORAGE: −55°C to +125°C
- **INPUT VOLTAGE:** +5V dc ±0.5V
- **INPUT CURRENT:**

	MAX. @ 25°C	MAX. OVER TEMP.
250-999.999 kHz	105 mA	115 mA
1.0-3.999 MHz	90 mA	100 mA
4.0-8.999 MHz	30 mA	40 mA
9.0-20.0 MHz	60 mA	70 mA
CURRENT OUTPUT SHORTED:	18 mA min. 100 mA max.	

- **TTL OUTPUT (0° C to 70° C):**
  SYMMETRY: 60/40% @ 1.4V dc level
  RISE AND FALL TIMES: (10%/90% p-p output voltage) 15 ns max. 250.0 kHz-8.999 MHz; 10 ns max. 9.0 MHz-20.0 MHz
  "0" LEVEL: +0.4V max.
  "1" LEVEL: +2.4V min.
  "0" SINK CURRENT: 16 mA min. (1.6 mA /gate)
  "1" SOURCE CURRENT: −400 uA min.
  OUTPUT LOAD: 1 to 10 TTL gates

ENVIRONMENTAL:

TEMPERATURE CYCLE: ± 5 ppm max, 0 to 120°C, 3 cycles, 2 hrs. max. each, 25 ± 2°C ref.

SHOCK: 1000G's 0.35 millisec, ½ sine wave 3 shocks each plane

VIBRATION: 10-55 Hz, .060" D.A., 55 Hz-2000 Hz 35 G's. Duration time—12 hours

HUMIDITY: 85% Relative humidity, @ +85°C, 250 hours

MECHANICAL:

GROSS LEAK TEST: All units 100% leak tested in de-ionized H_2O.

HERMETICALLY SEALED PACKAGE: Mass spectrometer leak rate less than 2 x 10^{-8} atmos. cc/sec. of helium

SEAL STRENGTH: 20 lbs. max. force perpendicular to top and bottom

PIN MATERIAL: Phosphor bronze, ¼ hard, Grade A .00003" thick gold flash finish

BEND TEST: Will withstand maximum bend of 90° reference to base for 1 bend

MARKING INK: Epoxy, heat cured

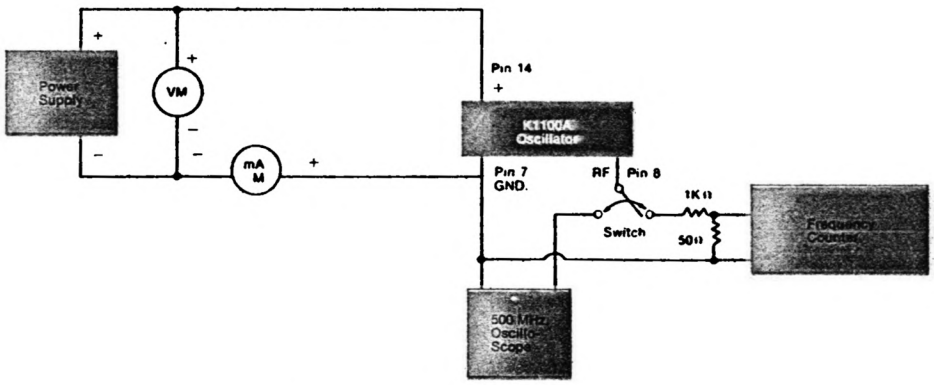
SOLVENT RESISTANCE: Isopropyl alcohol
Tricholoroethane
Freon TMC

No marking or seal destruction

Dipped 1 minute @ +25°C ± 5°C in solvent

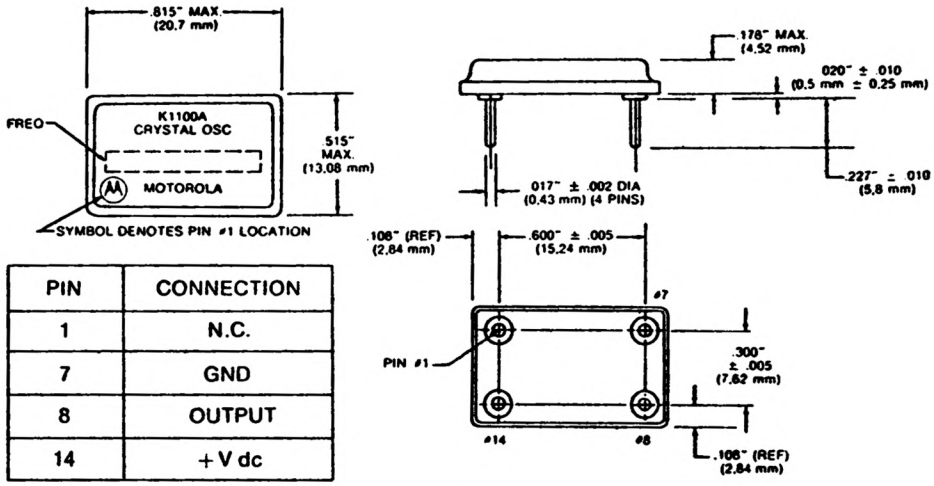
Note: (1) Unit can be cleaned by only one type solvent listed.

Note: (2) Ultrasonic degreaser not to be used unless frequency and vibration of cleaner specified.



K1100A Clock Oscillator Test Circuit

NOTE:
Oscilloscope Test Probe Capacitance must be 2 pf. Max.



PIN	CONNECTION
1	N.C.
7	GND
8	OUTPUT
14	+V dc

solderability specifications

- **MATERIALS:**
  1.1 SOLDER: 60% tin and 40% lead
  1.2 FLUX: The flux shall be 25 percent by weight of Grade WW rosin and 75 percent by weight of 99 percent isopropyl alcohol.
- **PROCEDURE:**
  2.1 SOLDER BATH: The solder bath shall be maintained at 232 ± 6°C.
  2.2. SOLDERABILITY: Dip the terminals into the flux to the depth that is to be soldered or to a maximum depth of .025" from the body of the oscillator. Keep them in the flux for at least 5 seconds. Withdraw them from the flux. Dip them immediately into the molten solder to the same depth. Keep them in the molten solder for 2 to 5 seconds.
  Withdraw them and allow the solder to cool in air.
- **REQUIREMENTS:**
  3.1 The terminals are considered solderable and acceptable for electrical connection purposes if 90 percent of the cold solder surface is uniform and free from breaks and pinholes. The other 10 percent of the cooled solder surface may show only pinholes, voids, or rough spots that are not concentrated in one area.

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COMPONENT PRODUCTS DEPT.
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Specifications subject to change without notice.