VLA Technical Report No. 39

CORRELATOR SYSTEM OBSERVER'S MANUAL

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DEFINITIONS:

QUADRANT: The correlator system consists of four identical subassemblies called quadrants. Each quadrant consists of 4 arrays where an array consists of a 27 x 27 matrix of correlator circuits. In spectral line operation one quadrant provides the auto and cross correlation products necessary in computing 4 frequency channels for all baselines at one time and in continuum operation two quadrants provide all products required of one polarization pair of outputs of the array.

MODE: The word mode is used in this manual to refer to an observational configuration of the correlator equipment. The correlator system was specified and designed to support a wide range of observational programs, the principal division of observations being continuum and spectral line. Mode designations for the multiplier subsystem specify class of observation, i.e. continuum, spectral line, polarization spectral line, etc. Mode designations for the integrator convey such information as number of lead/lag channels to be produced.

CHANNEL: Each antenna has four outputs, channels A, B, C and D with A and C being opposite polarizations of the same bandwidth and B and D being opposite polarizations of an independant bandwidth. These outputs, as they drive the sampler, are called baseband A, B, C and D as it is the baseband system that actually drives this system.

BAND: The word band was used in the early spectral

line correlator memos, and in this manual, with a somewhat different meaning from that in general VLA literature, where it usually designates observing frequency, i.e. L, C, U or K band. Table I specifies, for instance, observing in a 2 band spectral line mode. The term band indicates that the observation is being performed simultaneously at two frequencies (or bandwidths), processing, say, antenna A outputs in one half of the correlators and antenna D outputs in the other half.

SECTOR: The term sector, used in describing the integrator system, refers to partitions in the integrator whereby a given hardware correlator's output may be integrated in several hardware integrators supporting the time multiplexing usage of the correlators in spectral line mode. The integrator system is always programmed for two sector mode in continuum observations (for reasons beyond the scope of this manual) and is programmed to up to 32 sector mode for spectral line. The exact sector selection in spectral line observations depends on the number of frequency channels to be obtained.

DATA VALID: Data valid refers to the approximately 50 ms period within the waveguide cycle when valid astronomical data is present for correlation. Data invalid is the approximately 1.5 ms period within the waveguide cycle when valid data is not present.

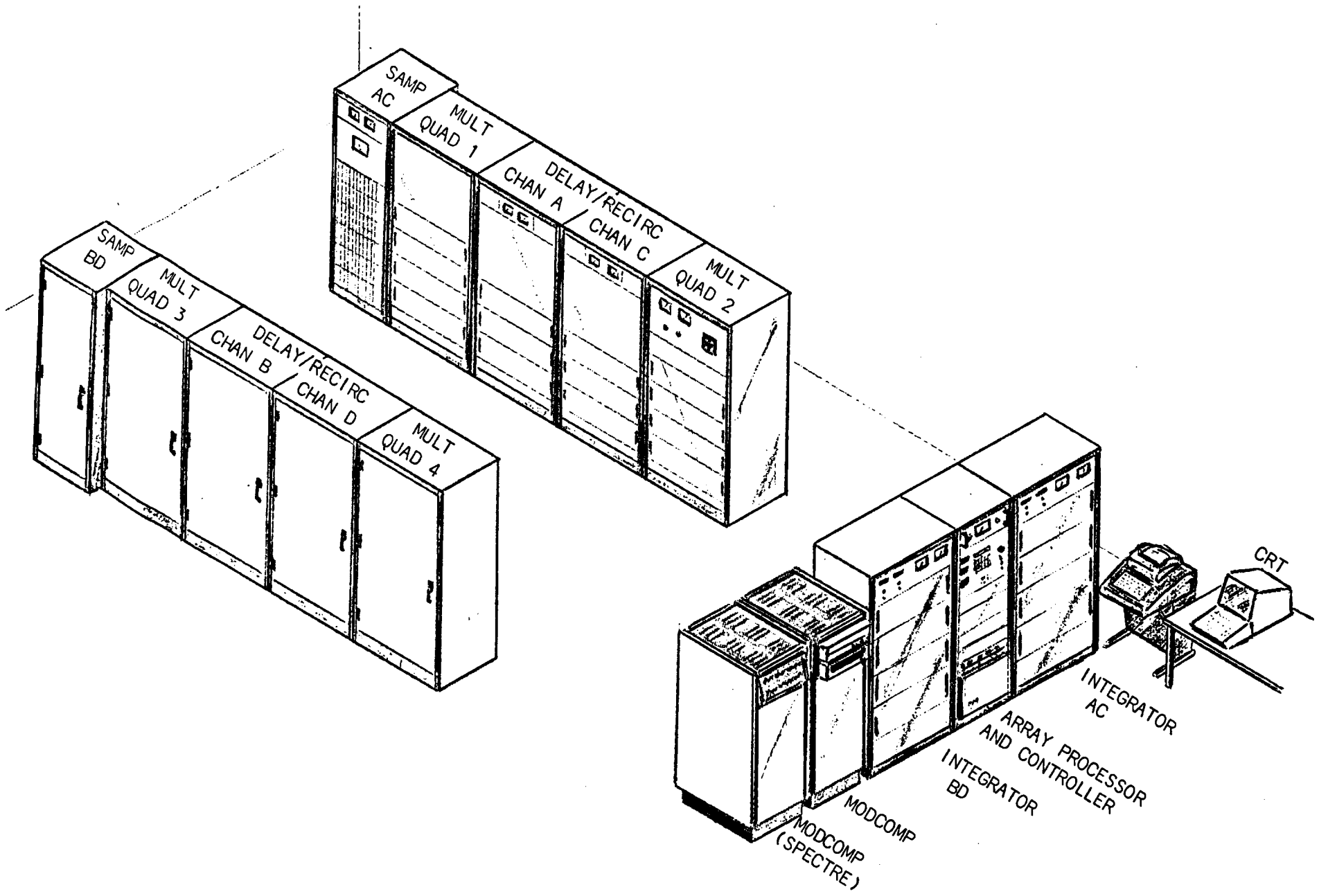
BLANKING TIME: Blanking time refers to .64 μs periods occurring each 92.8 μs within the correlator system when correlation is inhibited. This cycle is locally

derived in the correlator system and the blanking interval is used in transferring 92.16 μs correlator results into storage for transfer into the integrator.

V_s: An integration result is the product of integrating the output of a correlator over V_s samples.

1.0 INTRODUCTION

This report is intended to give observers and other persons a brief description of the VLA Correlator System. Stress will be put on the system specifications and operational modes of the correlator but basic hardware operation will be covered to give persons not interested in the detailed electronic implementation more insight into this large subsystem of the VLA. A brief description of the system controller software is also included in this report.



SCREEN ROOM RACK LAYOUT

2.0 BASIC BLOCK DIAGRAM

Figure 1 illustrates the VLA Correlator System in block diagram form with emphasis on astronomical signal flow and the four-wise modular breakdown of the hardware. The signal conditioning subsystems; samplers, delay lines and recirculator logically break down by antenna channel outputs A, B, C, and D while the driver, multiplier and integrator subsystems are given the more arbitrary quadrant breakdown reflecting rack configuration.

The function of each of the subsystems is as follows.

2.1 Samplers

The sampler system is the analog to digital converter in the VLA astronomical signal path. Inputs to the 108 sampler modules are wideband analog signals from the baseband system which are converted via a two bit, three level quantizer to a 100 MHz ECL digital format.

2.2 Delay Lines

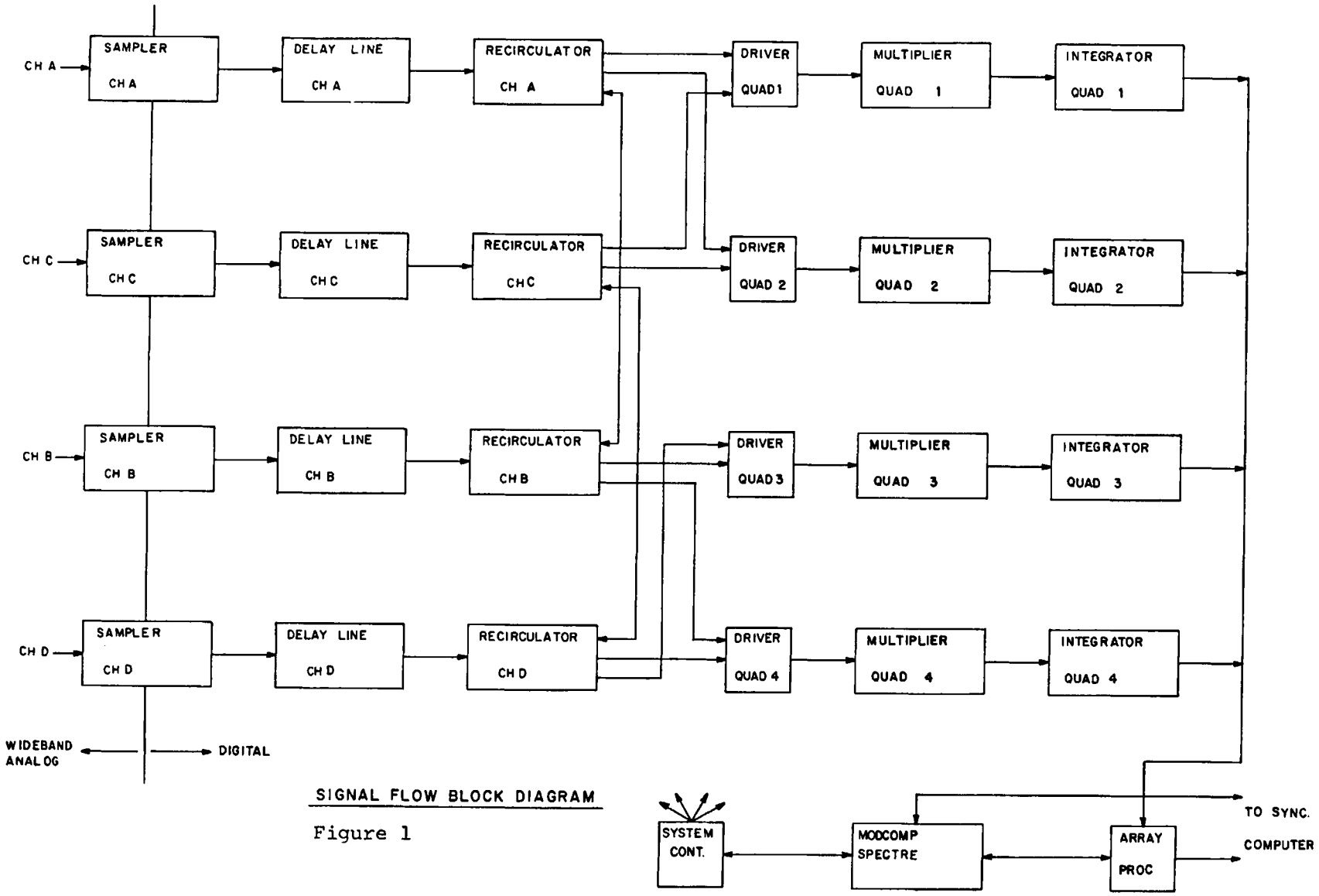
The delay system allows array phasing by providing programmable path delays for the astronomical signals. Delay lines (together with phase shifting in the sampler) provide 163.84 μs delay ranges with 625 ps resolution. The 18-bit delay program words are provided by the synchronous computers at a 19.2 Hz rate.

2.3 Recirculators

The recirculator system allows processing of astronomical data by the correlators multiple times (with differing lead/lags each time) effectively multiplying the frequency channel capacity of the spectral line instrument.

2.4 Drivers

The driver system provides fan-out from the simple recirculator interface to the more complex multiplier interface. Also programming



SIGNAL FLOW BLOCK DIAGRAM

Figure 1

the system for a given observational mode is accomplished mostly in the drivers.

2.5 Multipliers

The multiplier system provides the 11,772 auto and cross products of the various antenna signal pairs needed to support continuum or spectral line observations.

2.6 Integrator

The integrator system can integrate the up to 373248 products of the recirculator and multiplier systems for periods of up to 10 seconds.

2.7 Array Processor

The Floating Point Systems 120B array processor provides such things as V_s subtraction, normalizations and FFT functions on the integrated multiplier products.

2.8 SPECTRE

The Modcomp II/45, SPECTRE, is part of the synchronous computer system.

2.9 System Controller

The system controller is a bit-slice microprocessor that, on instruction from SPECTRE, provides programming and control signals to the system.

3.0 SYSTEM SPECIFICATIONS

3.1 General

Number of antennas:	27
Outputs per antenna:	up to 4
Bandwidth per output:	up to 50 MHz

3.2 Samplers

Input level:	1.5 V rms (ALC provided)
Quantization rate:	100×10^6 per second
Quantization:	2 bit, 3 level
Bandwidth:	200 kHz to 50 MHz
Delay range:	10 ns
Delay resolution:	625 ps
Delay and phase switching update rate:	19.2 times per second
Digital outputs per analog input:	4, 2 quadrature outputs of 2 bits each

3.3 Delay Lines

Input/output data rate:	100×10^6 bits per second
Delay range:	163.83 μs
Delay resolution:	10 ns
Update rate:	19.2 times per second
Phased array analog summation:	~.025 V/antenna rms

3.4 Recirculator

Data input rate:	$\frac{100 \times 10^6}{N}$ bits per second, N = 1, 2, 4, 8, 16, 32, 64, 128, 256
Storage:	10240 bits/input
Lag generation range:	1 to 1024 bits
Bits per recirculation:	9216
Data output rate:	100×10^6 bits per second
Recirculations:	1, 2, 4, 8, 16, 32

3.5 Multiplier

Multiplication rate:	100×10^6 times per second

Continuum products per baseline*:

As * As	Cs * Cs	Bs * Bs	Ds * Ds
As * Ac	Cs * Cc	Bs * Bc	Ds * Dc
As * Cs	Cs * Ac	Bs * Ds	Ds * Bc
As * Cc	Cc * Ac	Bs * Dc	Dc * Bc
Ac * Ac	Cc * Cc	Bc * Bc	Dc * Dc
Ac * As	Cc * Cs	Bc * Bs	Dc * Ds
Cs * As	Ac * Cs	Ds * Bs	Bc * Ds
Cc * As	Ac * Cc	Dc * Bs	Bc * Dc

Spectral line products per baseline:	4 lead and 4 lag channels per quadrant per recirculation
Integration period before dump to integrator:	92.16 μs
Output:	12 bit results

3.6 Integrator

Memory structure:	4 quadrants, 27 lines (cards) per quad, 108 products per line, 32 sectors (lag ch) per product
Integration period:	52.083 ms to 10 seconds in 52.083 ms steps
Integration output:	24 bit results plus parity/overflow bit
Storage capacity:	373248 24 bit results

3.7 Miscellaneous

Sensitivity relative to a continuous correlator:	0.81
Racks:	15
Power requirements:	50 kW
Number of IC's:	85,000
Estimated MTBF:	5 to 10 days
Automatic self test capacity:	Tests 95%† of system
Automatic self heal capacity:	Covers 65%† of system

*A, B, C, D, = antenna baseband outputs
s, c = SIN, COS (the quadrature sampler outputs)

†by IC count

4.0 OPERATIONAL MODES

Table I gives the modes possible using the VLA Correlator System.

In continuum mode all multiplier quadrants are used to produce the various baseline products to support an observation with all antenna outputs (channels : A, B, C, and D) in continuum.

In single band spectral line mode only one antenna output (channel A, B, C, or D) is active, driving all four multiplier quadrants to obtain a maximum number of frequency channels. Multiband line modes process more channels per antenna through less multiplier quadrants each to observe over more than one band at a time producing proportionally fewer frequency channels per band.

Combined modes allow simultaneous continuum and spectral line observations from a given array (subarray). For instance, in mode 15 of Table I all Channel A outputs are processed in quadrants 1 and 2 in spectral line mode while Channels B and D of the same antennas are processed in quadrants 3 and 4 in continuum mode.

Figures 2 through 6 help to illustrate the hardware configuration of each mode and provide tables of the various bandwidth possibilities.

Mode assignments are made on an antenna basis and subarrays, assigning different subarrays different modes, are possible by observing the following rules:

1) Any number of continuum subarrays can be accommodated (continuum subarrays are transparent to this system).
2) Only four sets of sample frequency, maximum lag and lag step parameters (one each for recirculators A, B, C, and D) can be accommodated.
3) Only one mode per integrator quadrant can be accommodated. However, this is not a serious restriction since data from many sectors of the integrator can be summed in the array processor to simulate a low sector integrator mode assignment for some subarray.

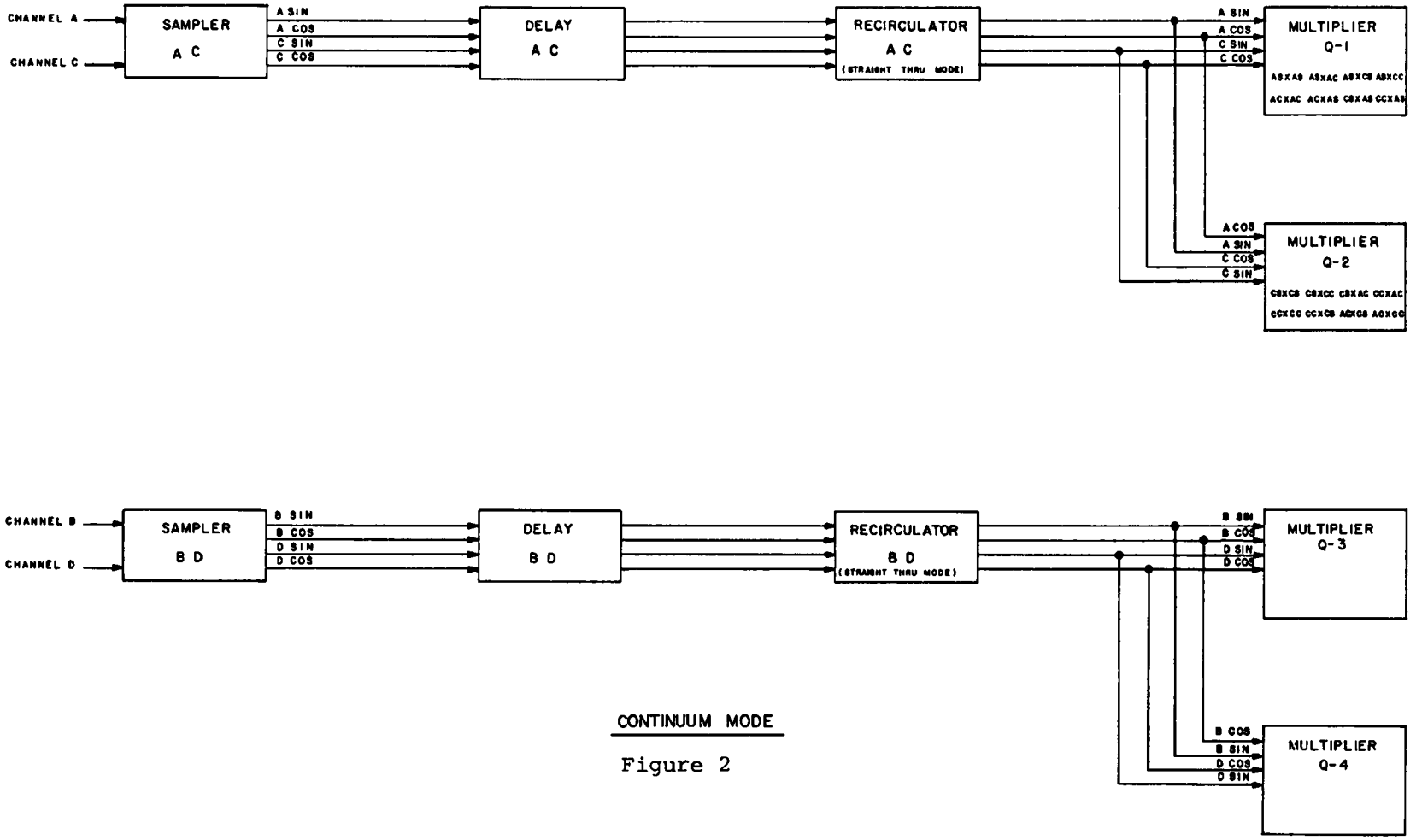
Provisions have been made for summing the phased array outputs of the delay line together thru a digital to analog converter yielding an analog output which is the IF signal received from the observed radio

TABLE I

Multiplier Mode	Observation	Baseband	Recirculator Used	Quadrant Assignment 1	2	3	4
0	None	-	-	-	-	-	-
1	Continuum (See Figure 2.)	(A) (B) (C) (D)*	None	(A) (C)	(A) (C)	(B) (D)	(B) (D)
2	1 Band Spectral Line (See Figure 3.)	A	A	A	A	A	A
3	1 Band Spectral Line (See Figure 3.)	B	B	B	B	B	B
4	1 Band Spectral Line (See Figure 3.)	C	C	C	C	C	C
5	1 Band Spectral Line (See Figure 3.)	D	D	D	D	D	D
6	2 Band Spectral Line (See Figure 4.)	A B	A B	A	A	B	B
7	2 Band Spectral Line (See Figure 4.)	A C	A C	A	A	C	C
8	2 Band Spectral Line (See Figure 4.)	A D	A D	A	A	D	D
9	2 Band Spectral Line (See Figure 4.)	B C	B C	C	C	B	B
10	2 Band Spectral Line (See Figure 4.)	B D	B D	D	D	B	B
11	2 Band Spectral Line (See Figure 4.)	C D	C D	C	C	D	D
12	4 Band Spectral Line (See Figure 5.)	A B C D	A B C D	A	C	B	D
13	Polarization Spectral Line (See Fig. 6.)	A C	A C	A*A	A*C	C*C	C*A
14	Polarization Spectral Line (See Fig. 6.)	B D	B D	D*D	D*B	B*B	B*D
15	Combined (Continuum and 1 Band Line)	A (B) (D)	A	A	A	(B) (D)	(B) (D)
16	Combined (Continuum and 1 Band Line)	B (A) (C)	B	(A) (C)	(A) (C)	B	B
17	Combined (Continuum and 1 Band Line)	C (B) (D)	C	C	C	(B) (D)	(B) (D)
18	Combined (Continuum and 1 Band Line)	D (A) (C)	D	(A) (C)	(A) (C)	D	D
19	Combined (Continuum and 2 Band Line)	A C (B) (D)	A C	A	C	(B) (D)	(B) (D)
20	Combined (Continuum and 2 Band Line)	B D (A) (C)	B D	(A) (C)	(A) (C)	B	D

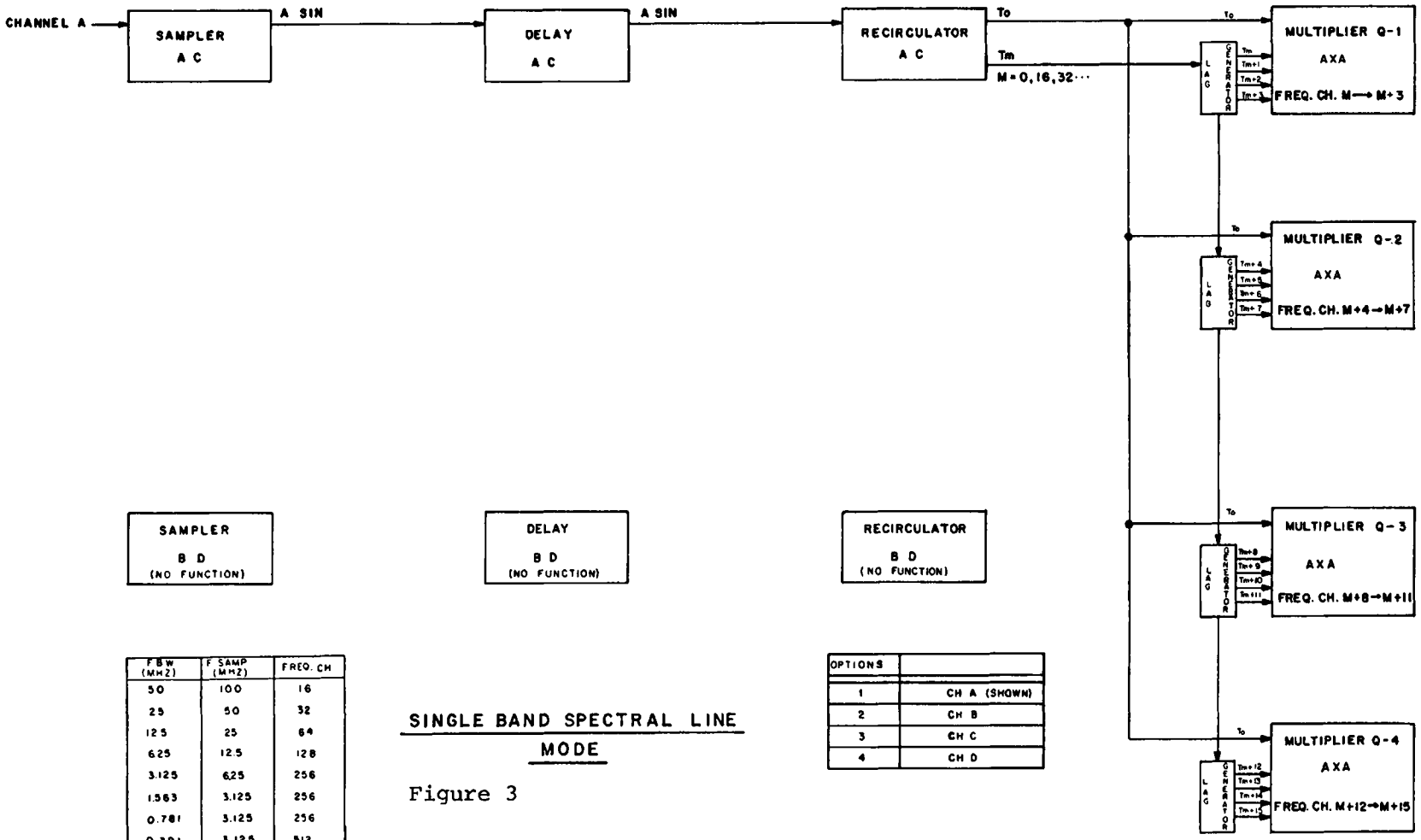
Integrator Mode	Sectors of Integration
1	2
2	4
3	8
4	16
5	32

* ( ) Denotes continuum



CONTINUUM MODE

Figure 2

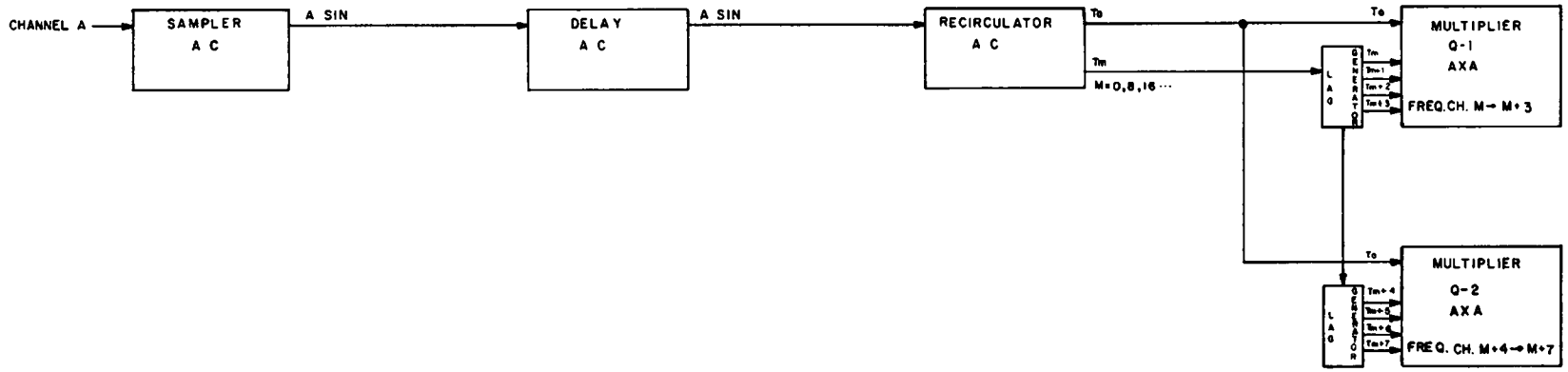


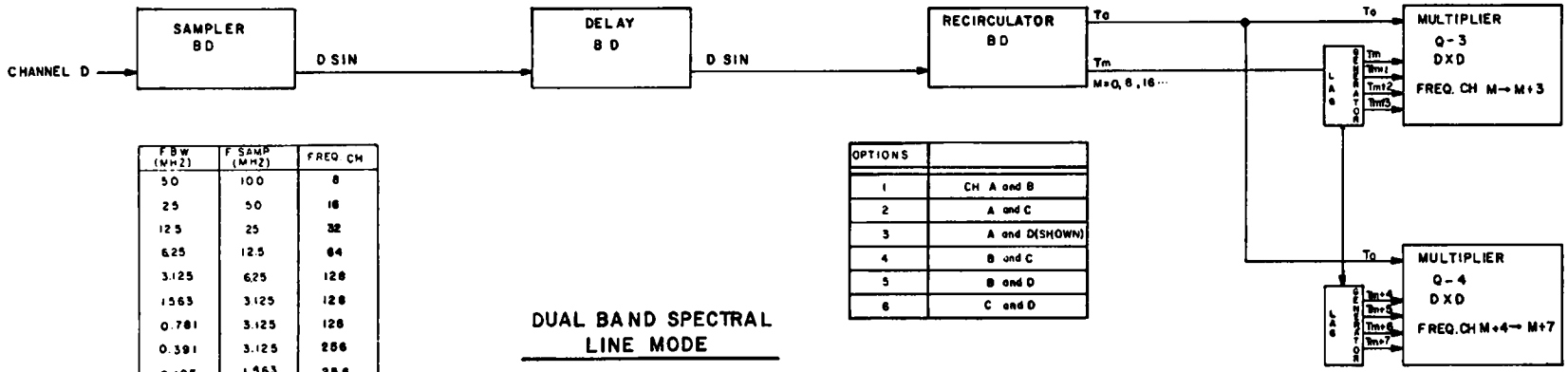
F BW (MHZ)	F SAMP (MHZ)	FREQ. CH
50	100	16
25	50	32
12.5	25	64
6.25	12.5	128
3.125	6.25	256
1.563	3.125	256
0.781	3.125	256
0.391	3.125	512
0.195	1.563	512
.097	0.781	512

OPTIONS	
1	CH A (SHOWN)
2	CH B
3	CH C
4	CH D

SINGLE BAND SPECTRAL LINE MODE

Figure 3



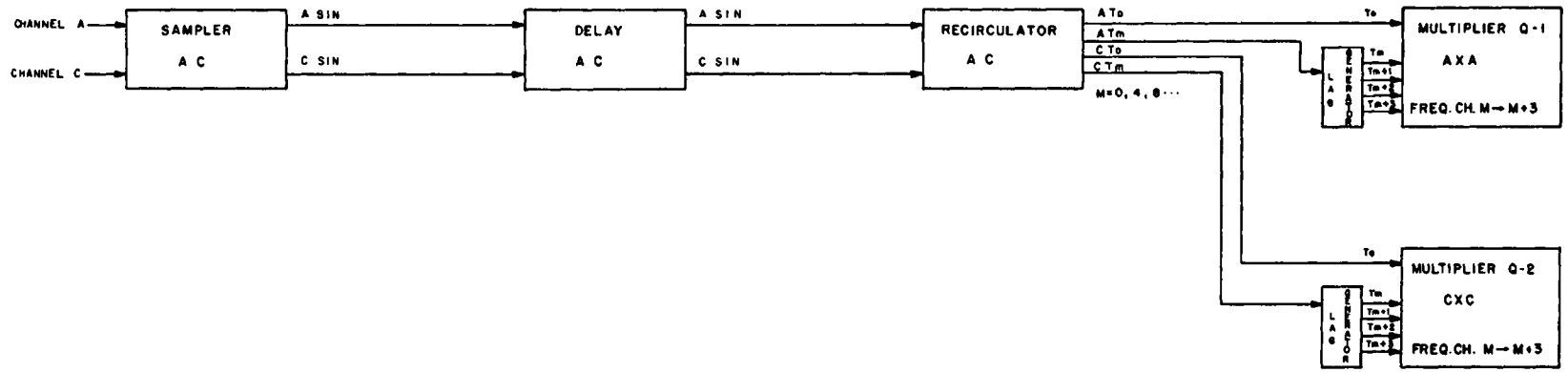


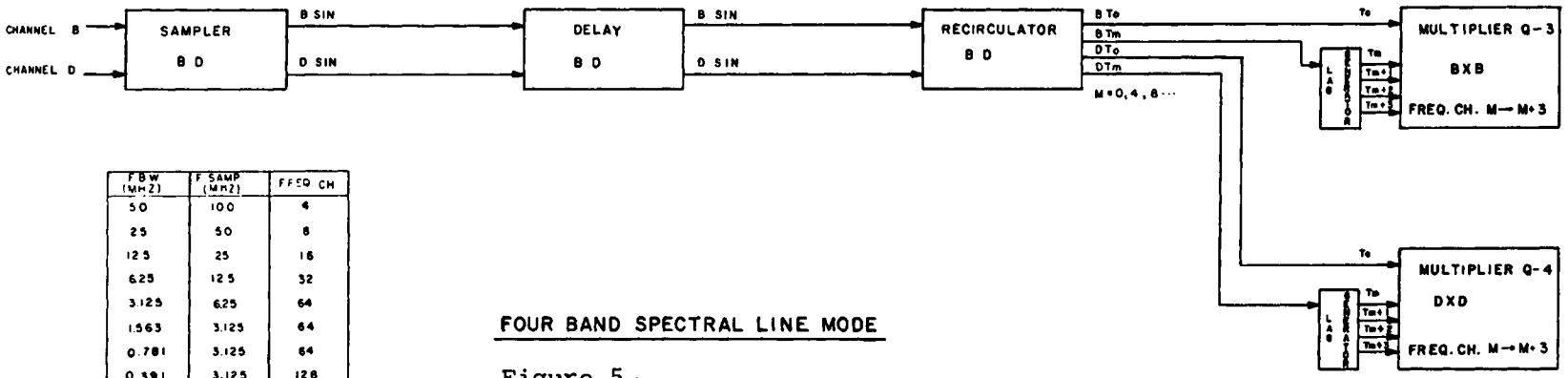
F BW (MHZ)	F SAMP (MHZ)	FREQ CH
50	100	8
25	50	16
12.5	25	32
6.25	12.5	64
3.125	6.25	128
1.563	3.125	128
0.781	3.125	128
0.391	3.125	256
0.195	1.563	256
.097	0.781	256

OPTIONS	
1	CH A and B
2	A and C
3	A and D(SHOWN)
4	B and C
5	B and D
6	C and D

DUAL BAND SPECTRAL LINE MODE

Figure 4

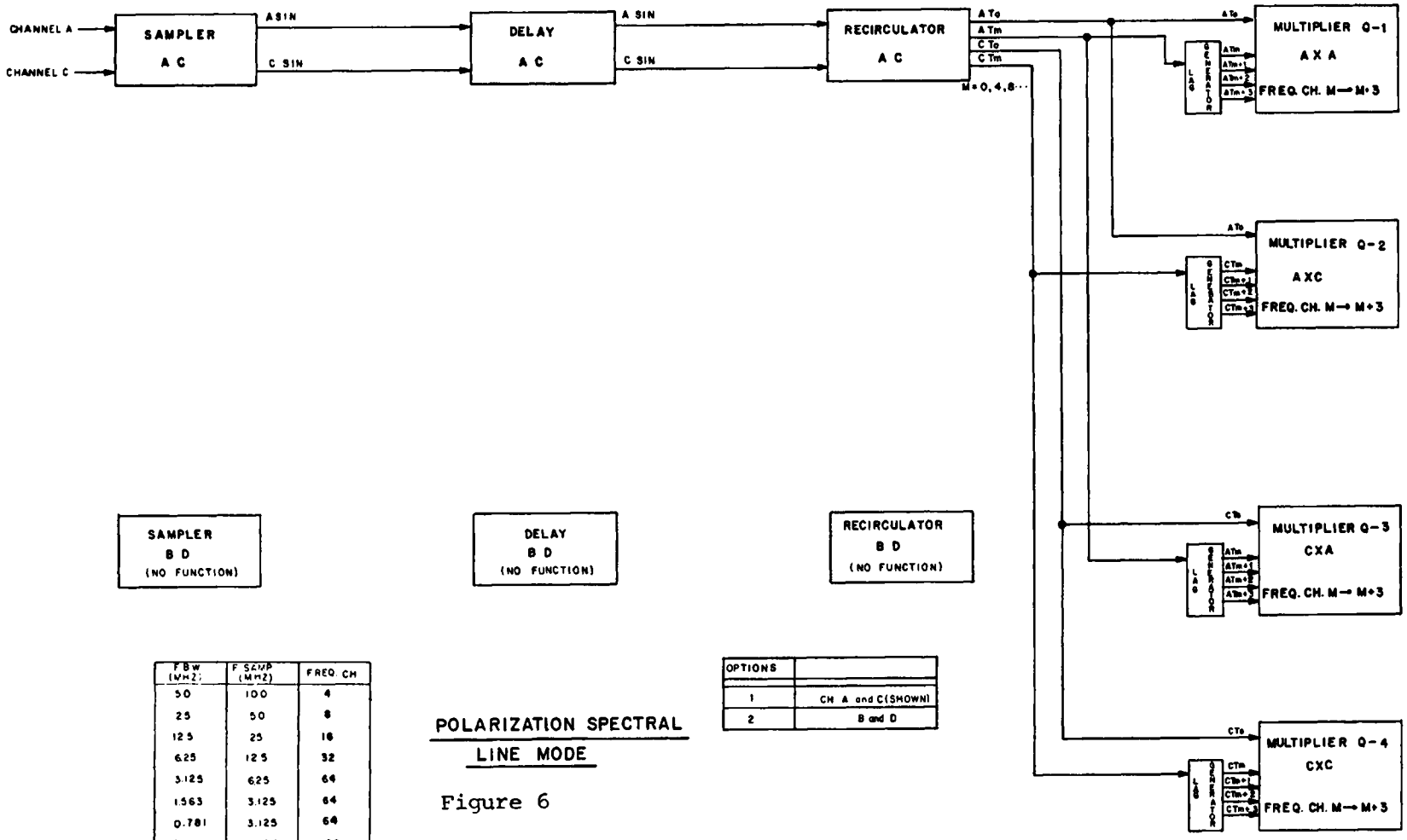




F BW (MHZ)	F SAMP (MHZ)	FREQ CH
50	100	4
25	50	8
12.5	25	16
6.25	12.5	32
3.125	6.25	64
1.563	3.125	64
0.781	3.125	64
0.391	3.125	128
0.195	1.563	128
.097	0.781	128

FOUR BAND SPECTRAL LINE MODE

Figure 5



F BW (MHZ)	F SAMP (MHZ)	FREQ. CH
50	100	4
25	50	8
12.5	25	16
6.25	12.5	32
3.125	6.25	64
1.563	3.125	64
0.781	3.125	64
0.391	3.125	128
0.195	1.563	128
.097	0.781	128

OPTIONS	
1	CH A and C (SHOWN)
2	B and D

POLARIZATION SPECTRAL
LINE MODE

Figure 6

source by the instantaneous beam of the array. Four such outputs exist, corresponding to the four channels A, B, C and D, with exclusion/inclusion options with the four sums having independent exclusion/inclusion parameters.

An external gate may be supplied to the correlator system that inhibits correlation for desired periods of time, such as pulsar off states. This signal, requiring TTL logic levels, combines with the data valid and blanking time signals to control correlation times. Each quadrant has independent gate inputs that may be either completely asynchronous to the correlator system or synchronized (internally) to the 92.8 μs internal correlation cycle; i.e. always permitting an intregal number of 92.16 μs integrations per dump. Internal counters keep track of the number of samples (V_S) contributing to each integration.

Table II gives, for single band spectral line mode, the various bandwidth/frequency channel options.

This discussion of operational mode capability of the VLA correlator system was given from a hardware standpoint and is not meant to imply that all features described have, or ever will have, computer system software to support them.

TABLE II: CORRELATOR NUMBERS FOR SINGLE-BAND LINE MODE

W_{req} MHz	f_u MHz	f_l MHz	f_s[5] MHz	$\Delta\tau * f_s$	No. Lead/Lag Pairs	FFT Length	Total Channels	Usable[4] Channels	Channel BW, kHz	Observational[6] Efficency
50	50	(1)	100	1	16	16	16	14	3125	96.2%(7)
25	25	(1)	50	1	32	32	32	29	781	95.9%
12.5	12.5	(1)	25	1	64	64	64	57	195	95.5%
6.25	6.25	(1)	12.5	1	128	128	128	111	48.8	94.8%
3.125	3.125	(1)	6.25	1	256	256	256	214	12.2	93.4%
1.563	1.563	(1)	3.125	1	512	256(2)	256	198	6.1	90.6%
0.781	0.781	(1)	3.125	2	512	256(2)	256	166	3.05	90.6%
0.391	0.781	(1)	3.125 [1.563]	2 [1]	512	512	256(3)	256	1.53	90.6% [90.6%]
0.195	0.391	0.195	1.563 [0.781]	2 [1]	512	512	256(3)	205	.763	90.6% [90.6%]
.097	0.391	0.195	0.781 [0.391]	2 [1]	512	512	256(3)	256	.381	90.6% [90.5%]

NOTES:
(1) Lower limit determined by amplifier rolloffs; approximately 0.19 MHz.
(2) Only alternate lags are processed by the FFT in these cases.
(3) All lags are processed, but half of the FFT output points are discarded.
(4) "Usable" channels assumes lower cutoff of 195 kHz and loss of 10% at filter band edges.
(5) Bracketed entries are alternative implementations.
(6) Observational efficency is defined as 100 x (duration of observation - time loss)/ duration of observation. Time losses are due to the waveguide cycle data invalid and inefficiencies in the correlator such as time required to fill the recirculator rams and blanking time.
(7) Same as continuum observational efficiency.

W_{req}: requested bandwidth
f_u : filter upper cutoff frequency
f_l : filter lower cutoff frequency
f_s: sampling frequency
$\Delta\tau$: lag step
FFT length: number of complex output points

5.0 FUNCTIONAL DESCRIPTION

Figure 7 gives a slightly more detailed block diagram of the VLA Correlator System. The discussion that follows attempts to describe each major subsystem within the correlator.

5.1 Samplers (D1 Module)

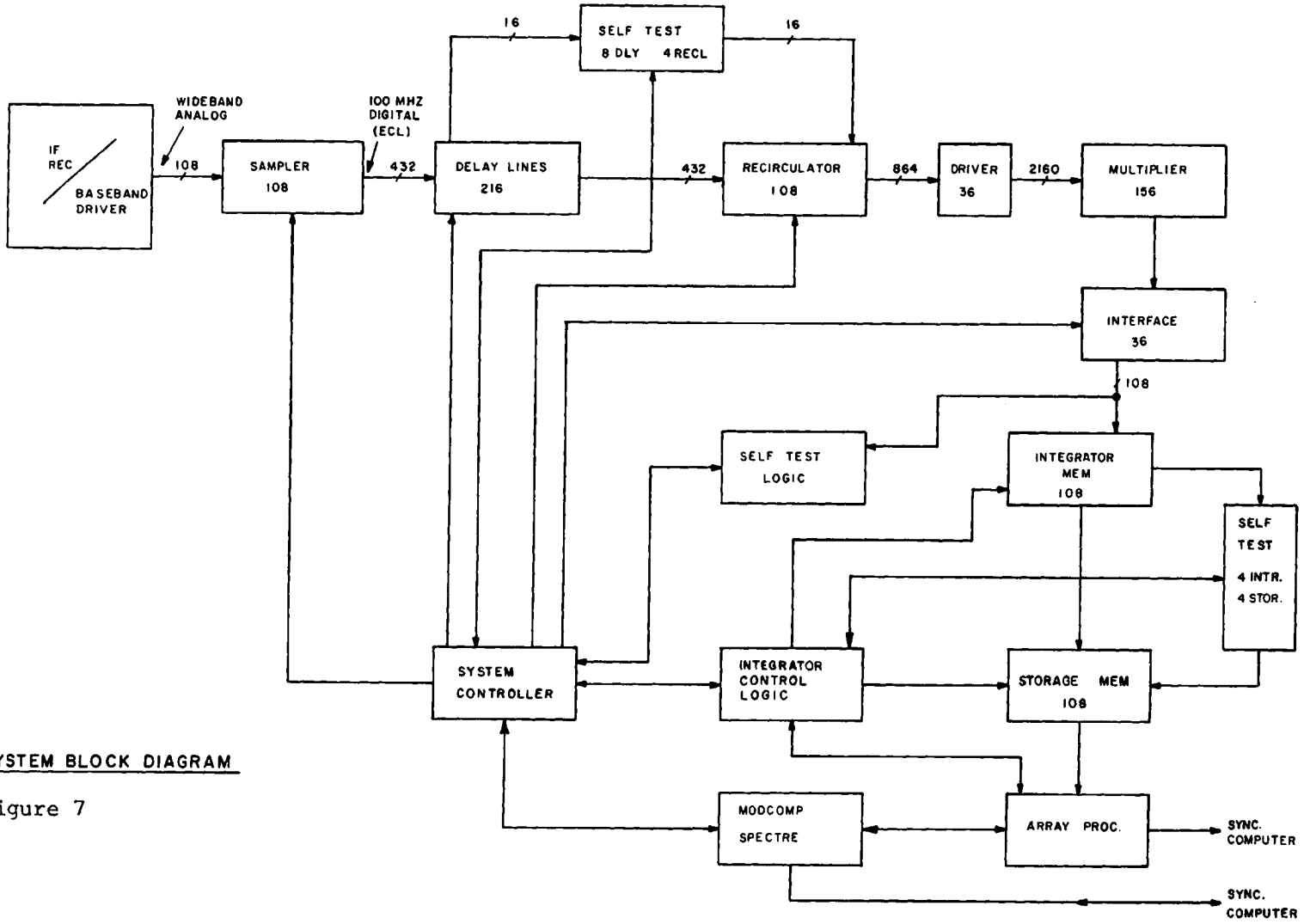
The sampler system is driven by the 108 wideband analog outputs of the baseband system. Automatic level control feedback signals are provided to the baseband system for output leveling. The 108 samplers, in the two 19" racks, are divided into four groups of 27 each, the division corresponding to the four baseband outputs of the 27 antennas, A, B, C, and D.

Each sampler is contained in a one-wide module, a block diagram of a sampler is given in Figure 8.

The quadrature network develops, from the wideband input signal, two wideband outputs in a quadrature phase relationship to each other, the sine and cosine outputs. The diode bridges and capacitor form a sample and hold circuit as a narrow sample pulse from the pulse generator allows the bridge to momentarily conduct inpressing the wideband signal onto the capacitor which stays charged during the bridge off state.

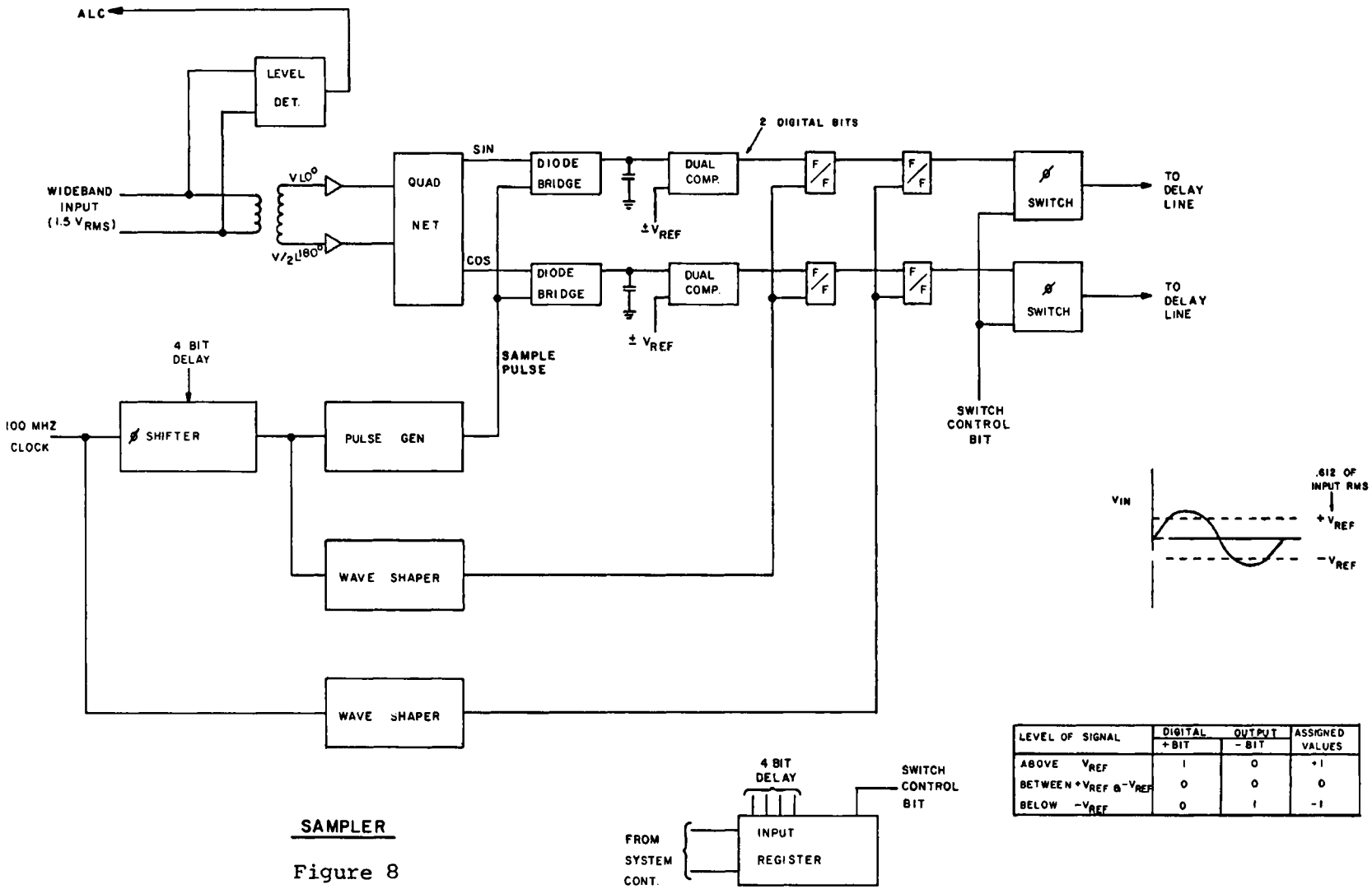
The sample pulse is derived from a 100 MHz sine wave input that can be phase shifted over a 10 ns range by 16 steps of 625 ps each. This shifting can position the sample pulse in time and accomplish the same thing as small delays provided in the signal path and is used for array phasing, augmenting the delay line phasing function.

The digital portion of the sampler rephases the digitally captured comparator output and can, on command, interpose the plus and minus bits effecting an equivalent 180^{o} inversion of the analog input. This phase shifting is used in implementing the array Walsh Function phase switches.



SYSTEM BLOCK DIAGRAM

Figure 7



LEVEL OF SIGNAL	DIGITAL OUTPUT + BIT	DIGITAL OUTPUT - BIT	ASSIGNED VALUES
ABOVE V_{REF}	1	0	+1
BETWEEN $+V_{REF}$ & $-V_{REF}$	0	0	0
BELOW $-V_{REF}$	0	1	-1

SAMPLER

Figure 8

5.2 Delay Lines

The digital delay system provides variable delays for each of the 432 digital outputs of the sampler system, each of the sampler digital outputs being a 100 MHz data rate ECL logic signal. The logic to provide 0 to 163.83 μs of delay in 10 ns increments for two 100 MHz logic signals is contained on a single multilayer delay line card. Eighteen delay line cards and nine associated recirculator cards are interconnected on a single multilayer mother board.

Each sampler output consists of a group of four signals that correspond to two bits each for two quadrature signals. Since these four digital outputs have a common analog path equal delays are provided thru the two corresponding delay line cards. These two cards accept a common 20-bit delay program word that contains 14 bits of delay information and several bits of program data. The 14-bit delay word is a binary progression to program the 0 to 163,830 ns delay with the LSB being weighted at 10 ns. Each delay line has a minimum thru-put time of approximately 80 μs, thus a delay line thru-put varies from 80 to 243.83 μs in 10 ns steps.

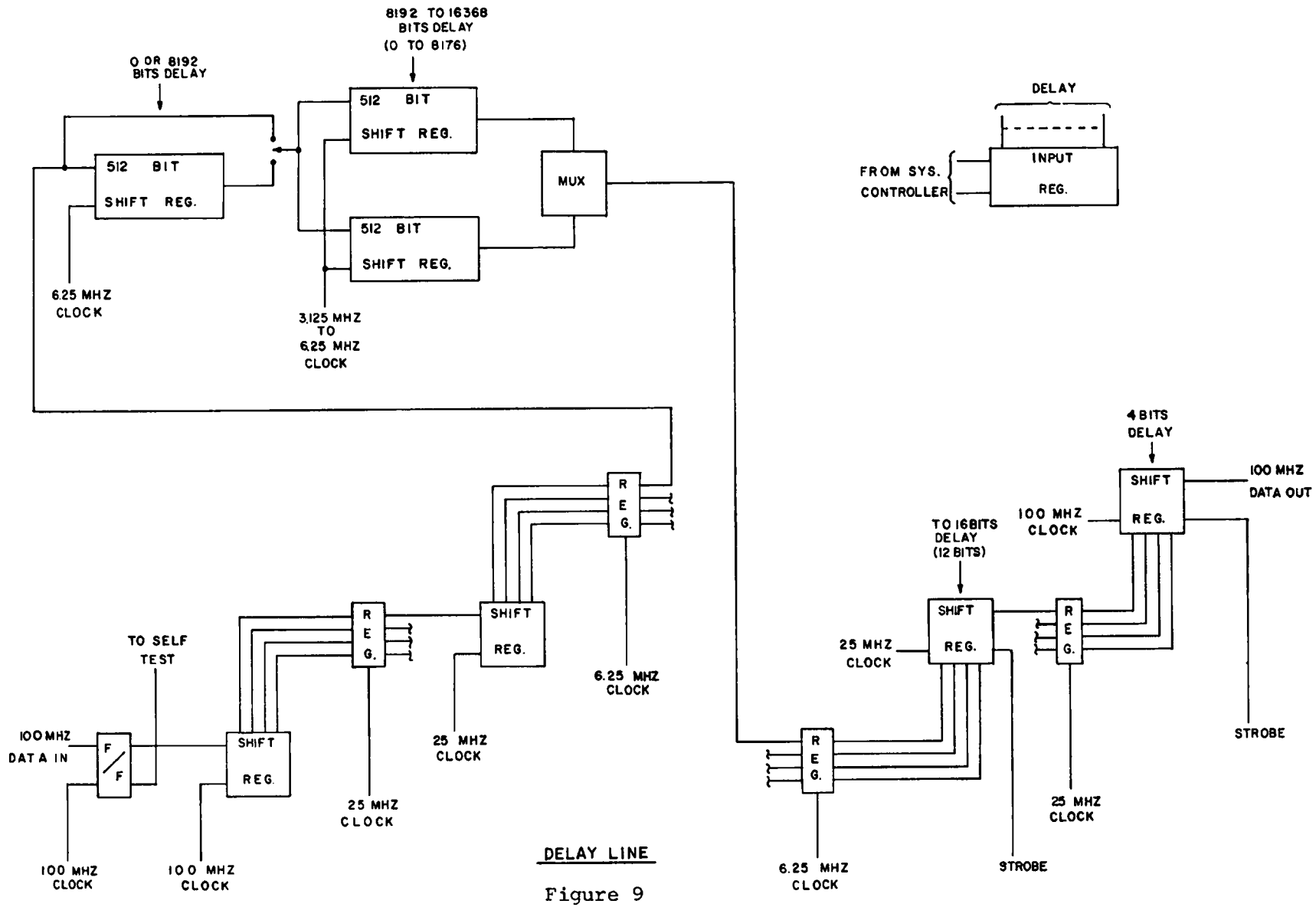
Each delay line contains ECL, TTL and MOS logic to optimize cost and performance, bulk delay being provided in low speed parallel path MOS logic, intermediate resolution at higher speed TTL circuits and the fine 10 ns timing accomplished in ECL logic.

A second input into each delay line is connected to a pseudo-random data generator that is used in system testing.

A block diagram of a delay line is shown in Figure 9. Of four 25 MHz parallel paths thru a delay line one is shown in this figure and of 16 6.25 MHz parallel paths only one is shown.

5.3 Recirculators

The main function of the recirculator system is to, for spectral line operations, store astronomical data received at a low data rate and process it thru the multipliers several times at a higher data



DELAY LINE

Figure 9

rate. For example, in the time it takes to store k bits of data received at a 6.25 MHz rate (the result of sampling a 3.125 MHz bandwidth antenna signal) k bits of previously stored data can be used to drive the multiplier system 16 times at a 100 MHz data rate. Thus hardware for 16 lead and 16 lag channels can be made to provide 256 frequency channels of spectral line information. In continuum mode this storage function is bypassed.

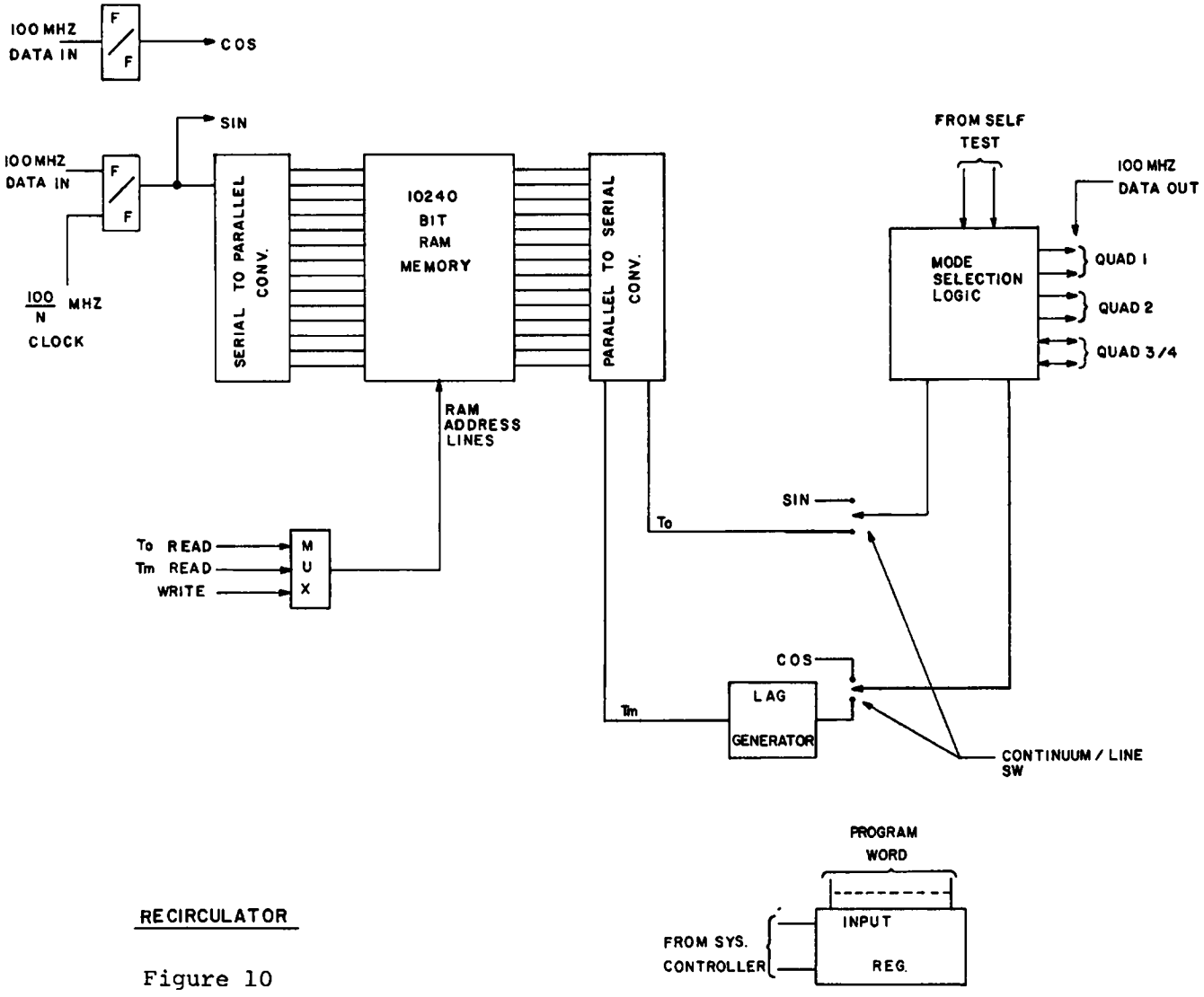
In addition some mode selecting capacity is provided in the recirculator as the signal distribution to the various driver-multiplier quadrants occurs on the recirculator card.

One multilayer pc card contains the logic to process the data outputs of two delay lines (one sampler). For continuum the two bits of a sine and the two bits of a cosine signal pass directly thru into the drivers. In spectral line mode the cosine data is discarded and each N^{th} sample of the sine input, N = 2, 4, 8, 16, 32, 64, or 128, is stored in a 10240 bit ram. In a totally separate operation two data streams of previously stored information are taken out of these same rams at a 100 MHz data rate. These two data streams, labeled T_o and T_m, are identical except that one lags the other in time by m bits. By stepping the value of m in consecutive reads, or recirculations, of the ram data the same hardware multipliers can be used to produce multiple frequency channels from the input astronomical data.

Figure 10 is a basic breakdown of the logic within a recirculator.

5.4 Multipliers

The multiplier system consists of four quadrants with each quadrant broken down into four arrays. Each array is a 27 by 27 matrix of multiplier circuits. In continuum for all antenna pairs X and Y, X > Y, (baselines) the following products are to be produced by the multipliers:



RECIRCULATOR

Figure 10

XAs * YAs	XCs * YCs	XBs * YBs	XDs * YDs
XAs * YAc	XCs * YCc	XBs * YBc	XDs * YDc
XAs * YCs	XCs * YAc	XBs * YDs	XDs * YBc
XAs * YCc	XCc * YAc	XBs * YDc	XDc * YBc
XAc * YAc	XCc * YCc	XBc * YBc	XDc * YDc
XAc * YAs	XCc * YCs	XBc * YBs	XDc * YDs
XCs * YAs	XAc * YCs	XDs * YBs	XBc * YDs
XCc * YAs	XAc * YCc	XDc * YBs	XBc * YDc

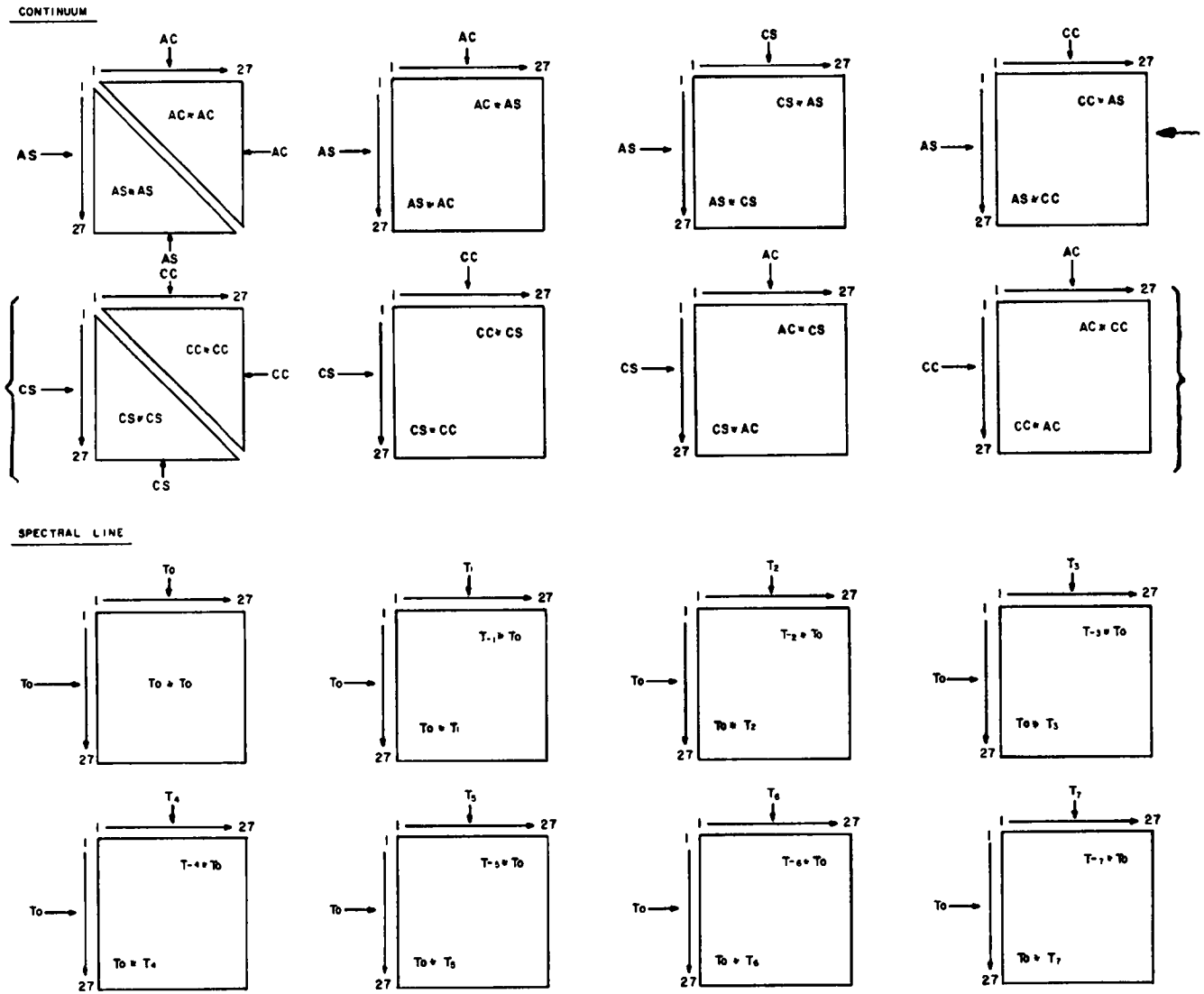
where A, B, C, and D are the four output channels of an antenna and s and c are the sin and cos outputs of a sampler.

In spectral line for all antenna pairs X and Y, X > Y, the following products are to be produced by the multipliers:

$$
\begin{array}{l}
X\ T_o \ * \ Y\ T_m \\
\quad \vdots \\
X\ T_o \ * \ Y\ T_1 \\
X\ T_o \ * \ Y\ T_o \\
X\ T_o \ * \ Y\ T_{-1} \\
\quad \vdots \\
X\ T_o \ * \ Y\ T_{-m}
\end{array}
$$

where T_o represents time reference data and T_m data displaced by m bits in time from the reference.

Figure 11 gives a geometric representation of two quadrants of the multiplier system with each array shown as a square matrix of 27 times 27 multipliers. The configuration for both continuum



THE MULTIPLIER SYSTEM (TWO QUADRANTS)

Figure 11

and one-band spectral line is shown. Thus it can be seen that two quadrants are needed to produce all the products of two baseband channels, AC or BD, in continuum and that four frequency channels per quadrant are produced in spectral line.

A two bit, three level digital signal is produced by the samplers. For details on this type of signal, reference should be made to:

Australian Journal of Physics, Correlators With Two-Bit Quantization, B. F. C. Cooper, 1970, 23, p. 521-7.

The output code of the samplers indicate that the signal is in one of three levels as follows:

LEVEL OF SIGNAL(S)	ASSIGNED VALUE	OUTPUT CODE OF SAMPLER	
		+ bit	-bit
S > +0.612 rms of signal	+1	1	0
-0.612 rms < S < 0.612 rms	0	0	0
-0.612 rms > S	-1	0	1

The value 0.612 was obtained from the above reference along with the assigned values of +1, 0 and -1 to provide the best combination of digital simplicity and high receiver sensitivity.

The output code is chosen arbitrarily to simplify the logic. A normal multiplication table for the above would be:

ANT. A → / ANT. B ↓	-1	0	+1
-1	+1	0	-1
0	0	0	0
+1	-1	0	+1

To perform this multiplication and integrate the results would require reversible counters. To simplify the system, an altered

multiplication table is used in which +1 is added to each multiplication result:

ANT. A → / ANT. B ↓	-1	0	+1
-1	2	1	0
0	1	1	1
+1	0	1	2

The array processor can correct for this change simply:

$$V'_n - V_s = V_n$$

where V'_n = results of integration of multiplier N after a period T,

V_s = number of multiplications performed (also number of samples taken) during T, and

V_n = results desired; that is, the results that would have been obtained with the unmodified multiplication table.

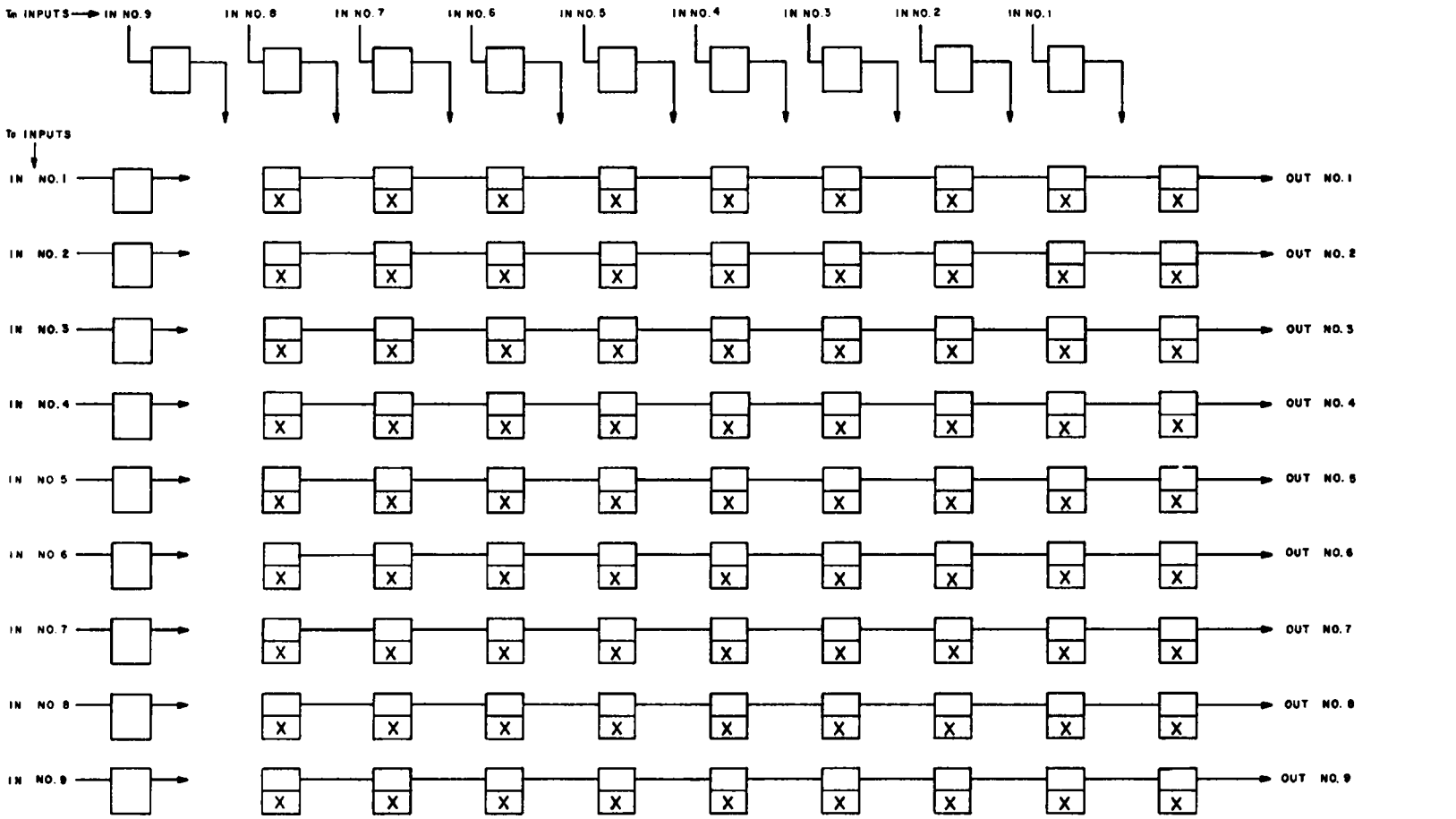
A block diagram of the multiplier card is shown in Figure 12. Each multiplier card contains 81 multipliers in a 9 by 9 matrix. Also shown in Figure 12 is the configuration of a single multiplier. The VLA-1 and VLA-2 custom IC's that make up a multiplier comprise logic to implement the table above plus a 14-bit counter to integrate results for 92.16 μs. Each 92.16 μs the first two bits (LSB's) of this 14-bit result (in the VLA-1) are discarded while the most significant 12 bits (in the VLA-2) are dumped into a register in the VLA-2 IC for shift out during the next 92.16 μs integration.

With an integration period of 92.16 μs:

$$\text{rms noise} = \sqrt{fs \cdot I} = \sqrt{V_s} = \sqrt{9216} = 96 \doteq 2^{6.6}$$

where fs = sampling frequency, I = integration period.

Therefore, the six least significant bits of the 14-bit 92.16 μs result contain mostly noise. By throwing away only two



MULTIPLIER

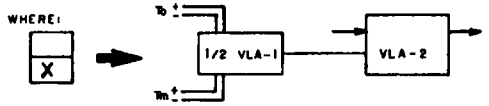


Figure 12

of the least significant bits, very little error is introduced in the final results.

5.5 Integrator

The integrator system accepts the 12-bit 92.16 μs results from the multiplier system and integrates them for up to 10 seconds. The four quadrants (16 arrays) of multipliers produce 11,664 results each 92.16 μs while the recirculator can produce unique sets of results for 32 consecutive 92.16 μs periods. Thus the integrator must process up to 373,248 different products at any one time. Results of up to 24 bits in length can be accumulated plus an overflow/parity error bit in each of the 373,248 data slots.

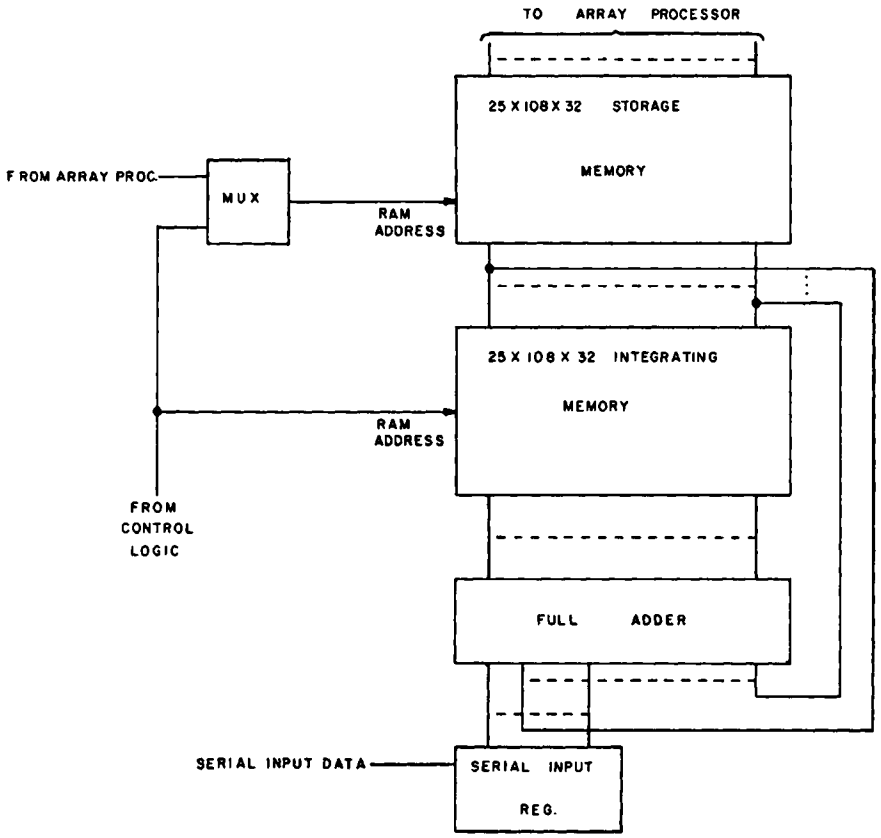
Figure 13 is a block diagram of the integrator which has both integrating and storage sections. Results accumulated in the integration section over an integration period are dumped into the storage section in from 92 to 2950 μs. These results in storage are then available for access by the array processor for the remainder of the integration cycle.

5.6 System Controller

The system controller is a 16-bit microprogrammable bit slice micro based on a 74S482 controller and a 74S381 ALU. The clock rate is 7.14 MHz and it can perform an add in 560 ns. A 64 x 256 micro code memory has been programmed for 75 instructions including arithmetic, logical, shift/rotate, branch, data move, and I/O functions. There are eight general purpose registers, eight interrupts, three I/O ports and 8 k of 16-bit macro memory.

Control of most functions in the samplers, delay lines, recirculators, drivers, integrator and the front panel is via a serial I/O card which can shift out control and program words into the system at up to a 7.14 MHz rate.

Program loading, modes, delays, etc., are provided by the



INTEGRATOR SYSTEM

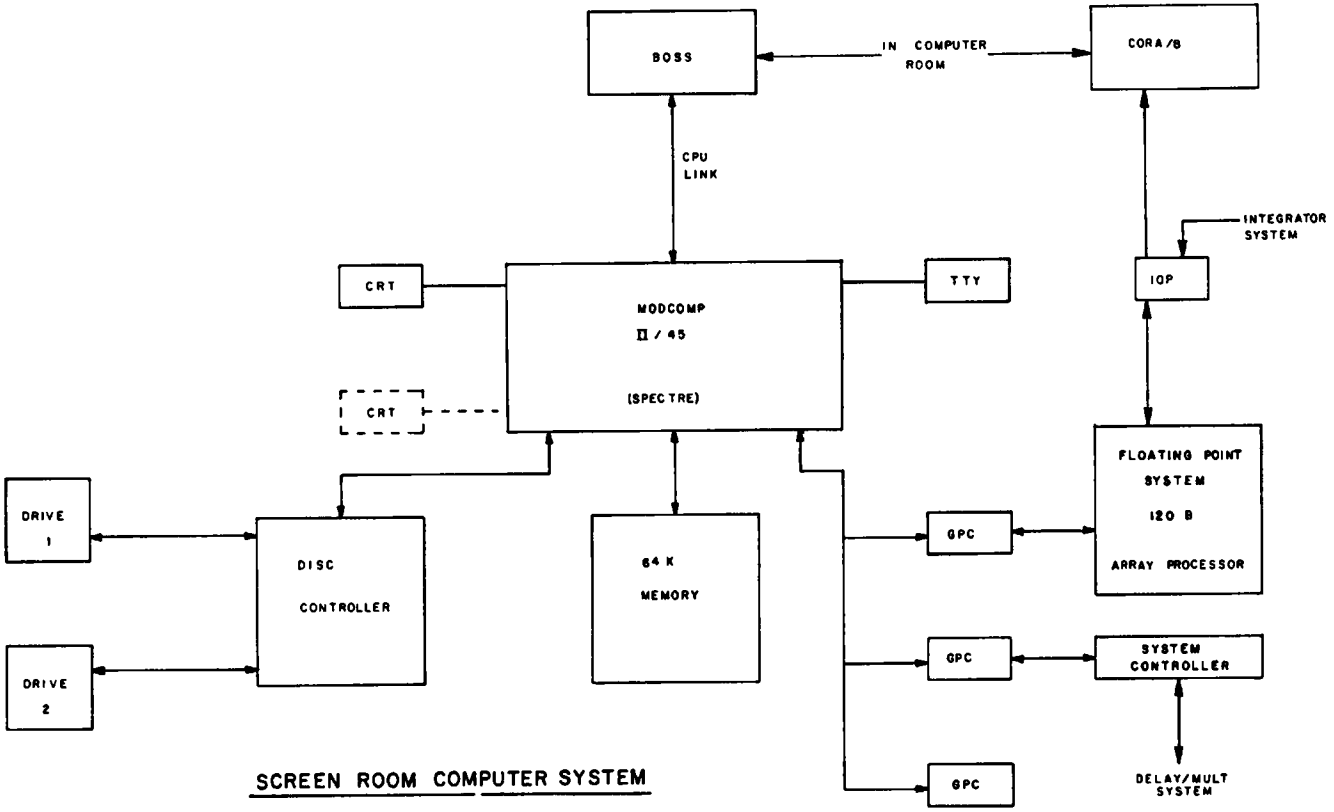
Figure 13

Modcomp, SPECTRE, via a Modcomp general purpose controller and some custom logic.

The system controller can also communicate via a CRT with an operator. However, since this function is more on the engineering level, no discussion of CRT capacity is presented here.

5.7 Computer System

Figure 14 is a diagram of the computer system associated with the Correlator System.



SCREEN ROOM COMPUTER SYSTEM

Figure 14

6.0 SYSTEM CONTROLLER SOFTWARE

The operation of the system controller is based on two cyclical functions and one asynchronous function. First there is the 19.2 Hz waveguide, next the 92.8 μs multiplier integration cycle, and last instructions, via interrupt, from SPECTRE.

A digital divider provides interrupts every 92.8 μs to allow the system controller to perform its various 92.8 μs task assignments. These 92.8 μs (blanking time) interrupts are counted with the counts reset at a 19.2 Hz rate. Individual tasks are assigned for execution in specific counts. The 19.2 Hz counter resets provide waveguide cycle visibility.

Below is an outline with brief descriptions of various system controller operations. The "main loop" refers to tasks performed with interrupts enabled and consists of several subroutines repeated each 19.2 Hz waveguide cycle. All subroutines performed under "interrupts" are time specific tasks or asynchronous servicing of I/O demands and are performed with interrupts disabled.

6.1 Main Loop

6.1.1 Check self test results

1) Shift in results of test that was run during previous data invalid period.
2) Check results against predicted results, put errors into file for displaying on front panel.
3) Check results for self heal opportunity.

6.1.2 Service front panel

1) Check array files and display errors in 4 x 5 front panel array.
2) Check front panel clear switch, clear error files if pressed.
3) Check front panel step switch, step 4 x 5 array pointer if pressed.

6.2 Interrupt

6.2.1 Blanking time (92.8 μs event indicator)

1) Service spectral line multiplier to integrator interfaces.
2) Service front panel
   a) Drive main 27 x 27 array.
   b) Drive 4 x 5 pointer/error array.
3) Initiate, on SPECTRE command, integrator to storage information dump.
4) Service spectral line lag generation logic.
5) Data invalid.
   a) Disable multiplier to integrator interfaces.
   b) Service integrator self test.
   c) Service V_s counters, sin x cos, and duty cycle hardware.
   d) Set up interface and lag routines for next waveguide cycle.
   e) Service hardware healing requirements (if any).
   f) Calculate test delay line delay values.
   g) Run self test:
      i) send test delays,
      ii) send test spectral line parameters,
      iii) enable test interfaces,
      iv) run test.
   h) Load delays.
   i) Enable continuum interfaces.
   j) Return to top of main loop.

6.2.2 Modcomp

1) Receive modes.
   a) Delay/multiplier.
   b) Spectral line parameters.
   c) Integrators.
   d) Observation.

2) Receive delays.

3) Receive dump commands.

4) Provide V_s.

5) Miscellaneous other functions.

6.2.3 CRT miscellaneous functions

7.0 SELF TEST

A copy of Electronics Memorandum No. 182 follows which describes self test within the VLA Correlator System.

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO
VERY LARGE ARRAY PROGRAM

VLA ELECTRONICS MEMORANDUM NO. 182

CORRELATOR SYSTEM SELF TEST/SELF HEAL

R. P. Escoffier

April 1979

1.0 SCOPE

This memorandum will describe the self test/self heal capability of the continuum/spectral line correlator system.

2.0 DELAY/MULTIPLIER TEST

Figure 1 shows the configuration of test hardware used in self testing and self healing of the correlator system. Figure 1 represents one antenna IF (A, B, C, or D) and hence is one-fourth of the total test logic in the system. Operation is as follows:

1. During data invalid of each 19.2 Hz waveguide cycle the system controller steers all delay line inputs to a pseudo-random data generator.
2. The system controller loads one of four delays into all delay lines and one of four lags to all recirculators. This insures all delay lines and recirculators are identically programmed while the other three delay/lag values test the system in subsequent test cycles over a small but comprehensive subset of delays and lags possible in actual operation.
3. The results of one 92.16 μsec integration for one-fourth of one quadrant (one array) are stored in RAM's at the 14 MHz interface rate for later analysis.
4. All delay lines and recirculators are returned to operational status for use in the next data valid cycle with real antenna delays.
5. During the next data valid period the one array's worth

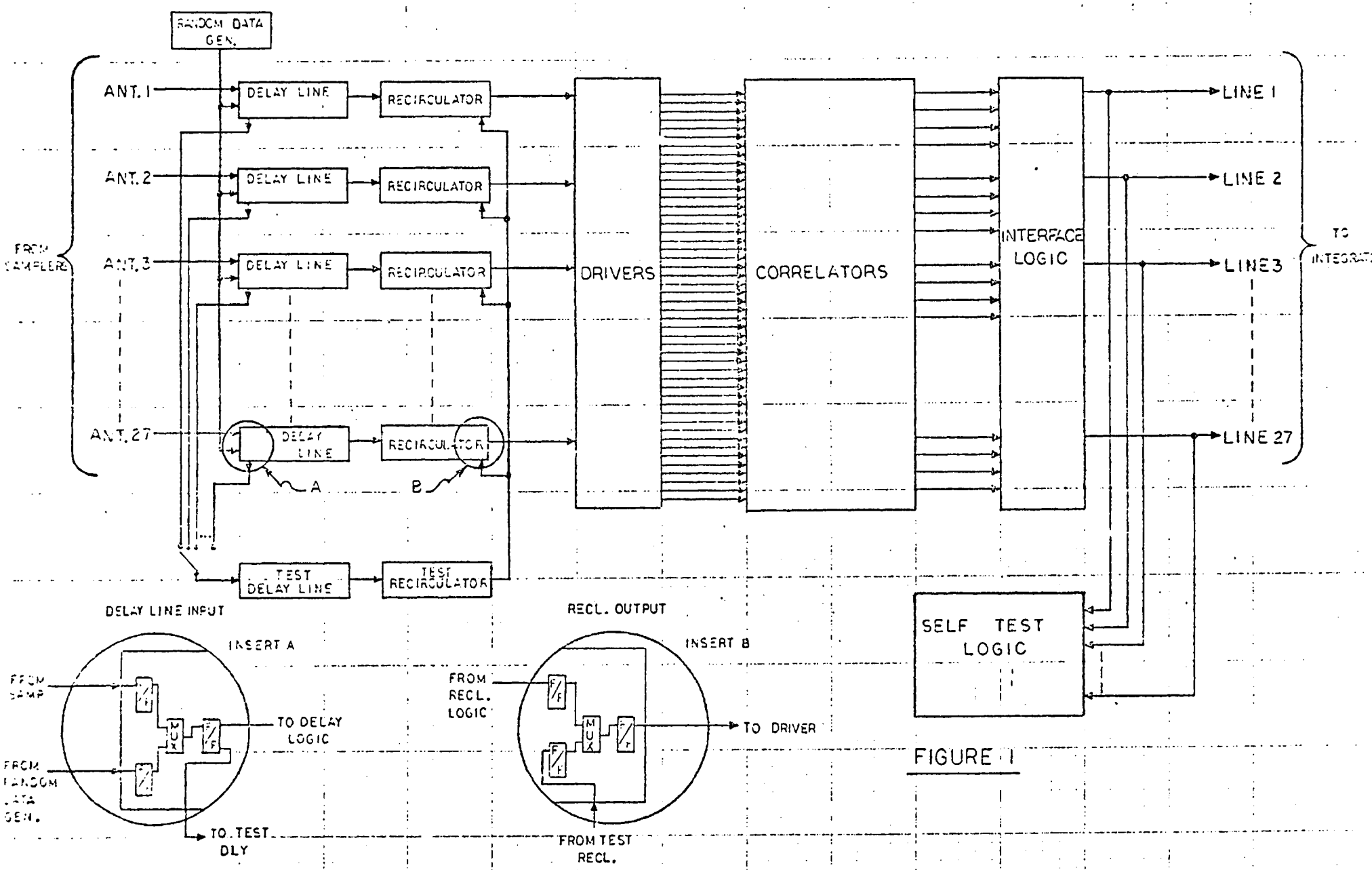

RANDOM DATA GEN.
ANT. 1
ANT. 2
ANT. 3
ANT. 27
DELAY LINE
RECIRCULATOR
TEST DELAY LINE
TEST RECIRCULATOR
A
B
DRIVERS
CORRELATORS
INTERFACE LOGIC
LINE 1
LINE 2
LINE 3
LINE 27
SELF TEST LOGIC
DELAY LINE INPUT
INSERT A
TO DELAY LOGIC
TO TEST DLY
RECL. OUTPUT
INSERT B
FROM RECL. LOGIC
TO DRIVER
FROM TEST RECL.
MUX
F/F

FIGURE 1

of 92.16 μsec correlator results (27 x 27 results) are transferred into the system controller.

6. Since the self test is run with whatever system configuration is being used in the observation in progress (continuum, one band line, 2 band line, 4 band line, legal mixed configurations, etc.) predicted values of each antenna pair are prepared reflecting: a) modes of two antennas for each result, b) array and quadrant being checked, c) which of 4 delay/lags used.
7. Predicted values are checked against actual results and no-go results flagged. Errors are displayed on the front panel and the Modcomp (SPECTRE) is notified.
8. After all 8 arrays of a quadrant pair (quad 1 and 2 or quad 3 and 4) have been tested (with the same delay/lag) these results are checked to see if a pattern of errors exist that would indicate a bad delay line or recirculator. Briefly this pattern would be recognized if all correlator results a given delay line or recirculator (which is bad cannot be determined) contributed to are bad.
9. If such a pattern is recognized one of several things may happen:
   a) A flag is set that will result in an exchange of the test delay/recl path for the suspected busted delay/recl path during the next data invalid period in an attempt to heal the system for the next and subsequent data valid cycles.
   b) Recognition that the test delay/recl path is not available (either since it is already used on another path or has been flagged to not exchange) will take place and no further action will be attempted (except as below).
   c) Recognition that that particular delay/recl path is

already bypassed will lead the system to assume that an early attempt to fix the same problem was unsuccessful and hence the test logic is itself bad. In this case the test path will be removed and flagged so as to attempt no future healing action.

d) The busted path may belong to an antenna that is not in use (no mode has been assigned it) in which case no action is taken so as to not waste the test path on an unused antenna.

A summary of test/heal features would be as follows:

1. The delay/recirculator/driver/correlator/interface portion of the system can, during inactive periods, test itself on a noninterfere basis requiring 16 waveguide cycles (times 4 for all four delay/lag words) for a complete test in the final four IF system.
2. Error filtering is obtained since a problem must be present for 4, 6, or 8 (depending on mode) consecutive waveguide cycles for the pattern of errors inducing a healing attempt to be recognized.
3. A busted path within the delay/recl subsystem can be healed using alternate test paths.
4. The effectiveness of such an attempt at healing can be observed in subsequent operation and abandoned if ineffective.
5. All errors encountered and subsequent actions taken are reported to SPECTRE. Appendix 1 gives the form of error reporting.
6. SPECTRE can modify at will any action taken by the system controller on its own. Appendix II gives the command format for such control.
7. If a delay line or recirculator card is changed (either while substituted for by the test path or otherwise) the test logic will quickly see this busted path and disqualify

itself from further healing attempts. Pressing the front panel reset switch will clear errors and again allow exchange of test logic for suspected busted cards. If the recirculator card is changed, the program word stored on that card will be lost and the observation must be restarted.

8. Substitution, and disabling substitution, occur on an IF basis, each of the four IF circuits acting independently.

Since a path through the test delay/recirculator must be via cables not needed in normal paths, extra delay to signals in this path must be compensated for by the test delay line. In continuum an extra 10 bits of delay are encountered and the system controller will load delays to this delay line that are 10 bits less than that to which BOSS specifies for the normal delay line it is paralleling. Thus a requirement for using the test path is that BOSS supply no delays less than 10 to any delay line in continuum. For spectral line a more complicated requirement exists where the minimum delay is (5N + 5) where the sample rate is 100/N MHz.

3.0 INTEGRATOR TEST

Figure 2 shows the configuration of test hardware used in self testing and self healing of the integrator system. This figure represents one quadrant and hence is one-fourth of the total test logic in the system. Operation is as follows:

1. The test memory path parallels one normal memory path each dump period (0.3 to 10 seconds). When the array processor reads information from the paralleled memory its contents are compared with that of the test memory and an error is flagged if noncomparison occurs.
2. Normally the test memory circulates around a loop of all used lines requiring KD seconds for a complete loop where K represents the number of antennas being observed with and D the dump period.

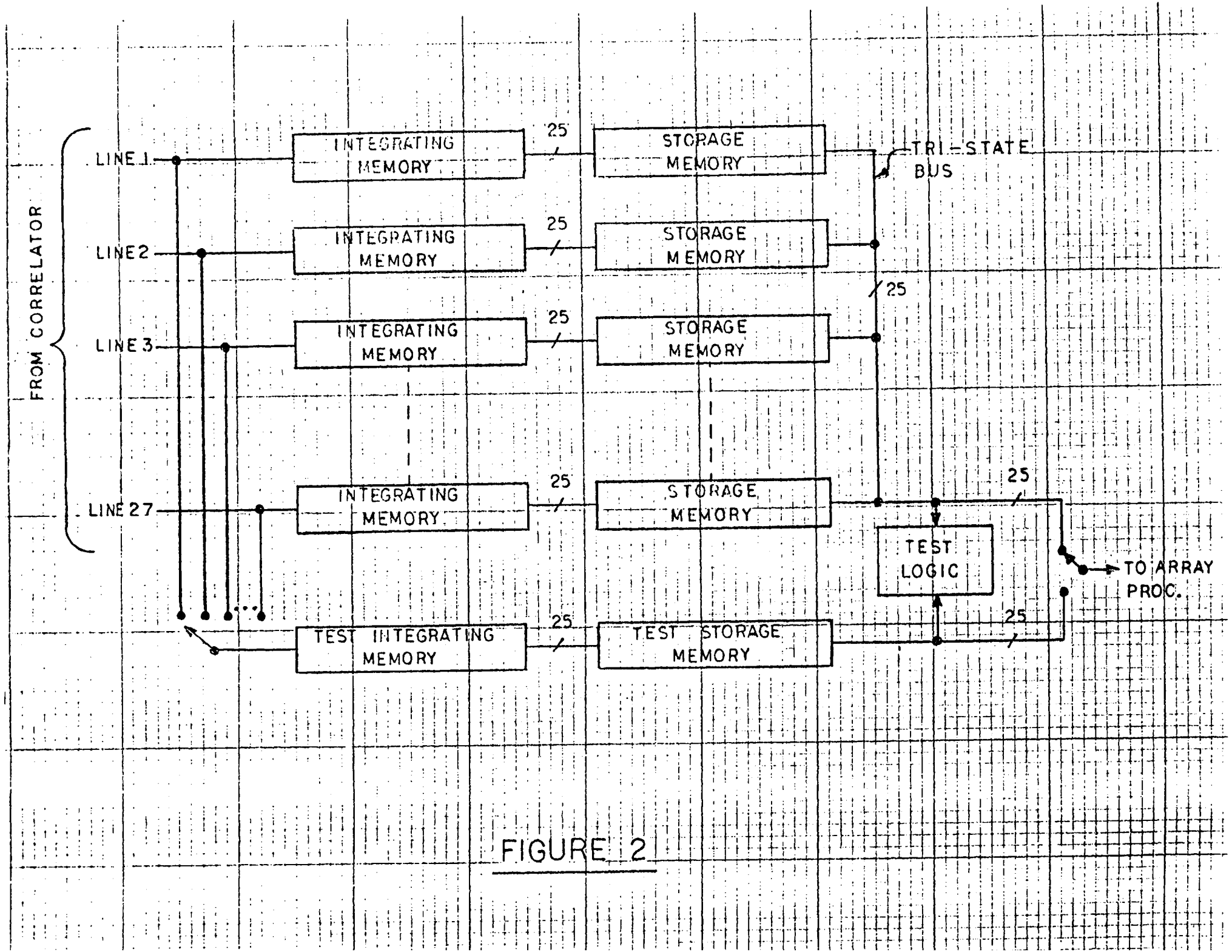

FROM CORRELATOR
LINE 1
LINE 2
LINE 3
LINE 27
INTEGRATING MEMORY
INTEGRATING MEMORY
INTEGRATING MEMORY
INTEGRATING MEMORY
TEST INTEGRATING MEMORY
25
STORAGE MEMORY
STORAGE MEMORY
STORAGE MEMORY
STORAGE MEMORY
TEST STORAGE MEMORY
TRI-STATE BUS
TEST LOGIC
TO ARRAY PROC.

FIGURE 2

3. If an error is detected the test memory advances once more and awaits the result of this test. A second consecutive error causes the logic to assume the test memory is itself bad and a flag is set to prevent any future substitution with the test memory. If no error is found the test memory backs up one place and substitutes for the suspected busted path.
4. No logic exists allowing evaluation of the effectiveness of the healing attempt by looking at data sent to CORA, however, the test memory can still check the suspected busted memory and it continues to do so even after it has substituted for that memory. If 16 consecutive dump times (at any period while substitution exists) are observed with no errors unsubstitution occurs and the test memory resumes its normal circuit in test mode.

Again in summary the test/heal features are:

1. Using observational data and conditions, not artificial data and conditions as in the correlator self test, the integrator system can test and heal itself on a noninterfere basis requiring KD seconds (see above) for a complete test.
2. Error filtering is obtained in that even after an exchange of test logic for suspected busted normal logic has taken place unexchange occurs unless continued malfunctioning is observed.
3. Some testing of the test logic occurs in that 2 consecutive errors in different lines causes the test system to disqualify itself for future healing attempts.
4. All error indications and healing actions are displayed on the front panel and reported to SPECTRE (see Appendix 1).
5. SPECTRE can modify at will any action taken by the system controller on its own (see Appendix 2).
6. Operation is on a quadrant basis with the four sets of test hardware acting independently of each other.

APPENDIX 1 AND 2
of
VLA Electronics Memorandum No. 182
Not Included in This Manual