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AN OVERVIEW OF THE MONITOR AND CONTROL SYSTEM

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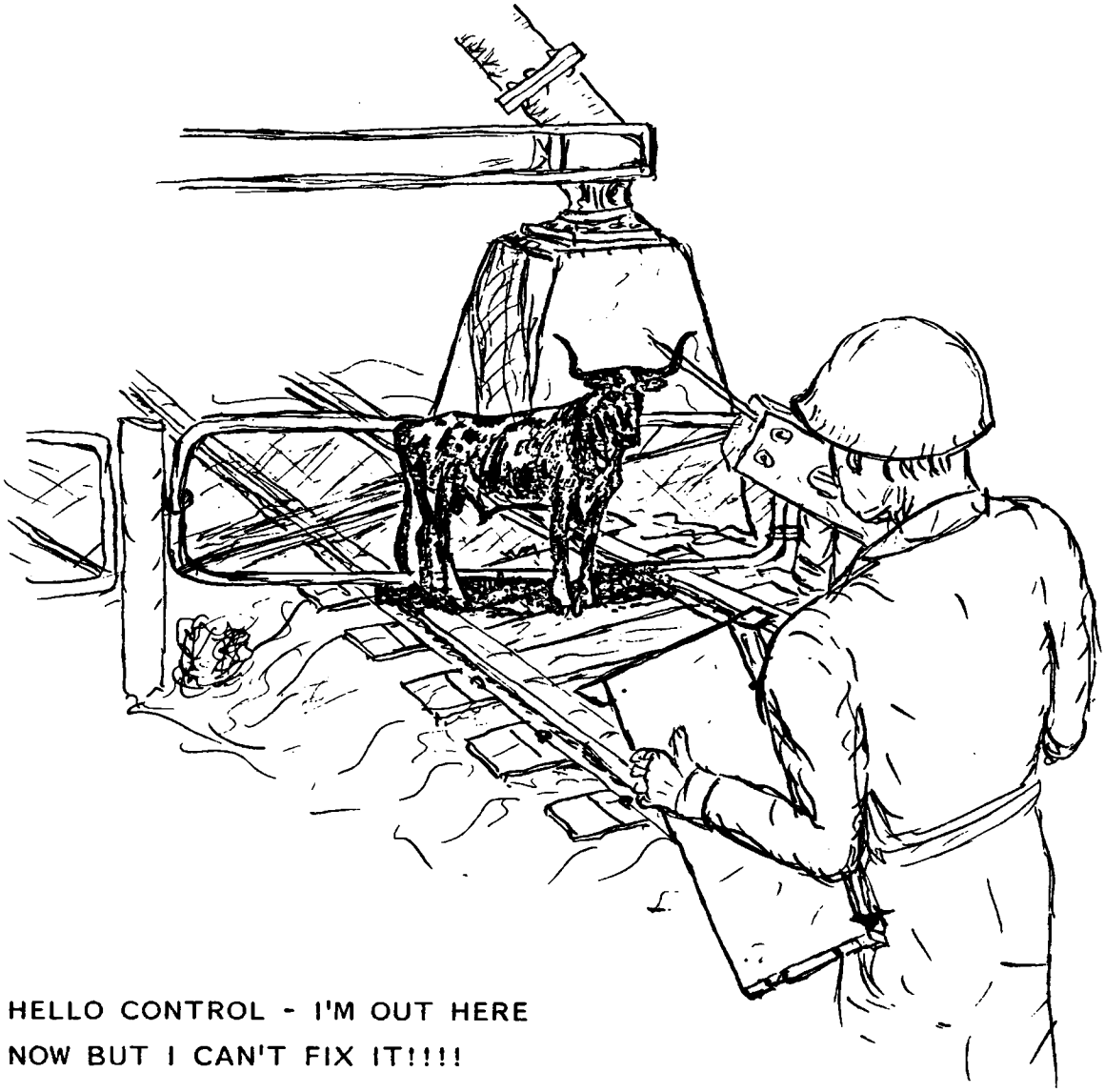

HELLO CONTROL - I'M OUT HERE
NOW BUT I CAN'T FIX IT!!!!

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1.0 INTRODUCTION AND SYSTEM ROLE

This manual describes the system properties of the Monitor and Control System and covers the system functions, the interactions with the VLA electronics and a brief functional description of the system components.

Since the emphasis of this manual is on the important operational characteristics of the system, details of the hardware and logic implementation have been omitted. The interested reader is referred to the system components maintenance manuals for this information.

The first portion of this manual (Sections 1.0 and 2.0) states the important system specifications and describes the message structure, design features, command and monitor data message flow, timing, error rates, and is oriented toward the reader who is primarily interested in the salient system characteristics. The latter portion of the manual (Section 3.0) is a brief functional description of the system components at a block diagram level and describes the system to a finer detail level than the first part for readers who may have an interest in the component operation. Appendix I is a list of related manuals and drawings which may be of interest to the reader and Appendix II is a glossary of terms used in this manual.

The Monitor and Control System conceptual design and specification was performed by Sander Weinreb. The detailed logic design and fabrication of the first lot of units was done on contract by Metrics System, Inc. of Ft. Walton Beach, Florida. The contract specifications were NRAO Specification A13710N1.

The characteristics of the Monitor and Control System as described in this manual differ in minor detail from those in the specification as a result of design changes and improvements caused either by changes in other portions of the VLA system or problems that arose in usage of the system. These changes and problems were so extensive that the system components have been completely redesigned and the original Metrics modules have been retrofitted to the new designs.

The Monitor and Control System is sometimes referred to by the title "Digital Communication System" which was used in Metrics contract and drawings. The title, Monitor and Control System, is more comprehensive in that it also encompasses the computer interfaces, software aspects and control/data interfaces which are part of the system.

The VLA electronics are closely integrated in that few subsystems can be considered to be fully independent of the other subsystems. This is the case with the Monitor and Control System which is closely linked with the LO, IF and Modem subsystems and is wholly dependent upon them for proper operation. Since this manual is narrowly focused on the Monitor and Control System, the operations performed by these subsystems are given a simplistic treatment and are discussed only where they are important to the system description or appear as interfaces.

The Monitor and Control System performs the functions of distribution of control and monitoring information in the VLA system. The control information is generated by the control computers (MONTY, BACCUS and BOSS), accessed by the Monitor and Control System, formatted into discrete digital time sequence command messages and distributed to the various devices which must be controlled. VLA system performance data is gathered from the VLA system components, converted and formatted into discrete digital time sequence monitor data messages and routed to the control computers. This data is analyzed by the computers to evaluate system and component performance and to provide diagnostic information for maintenance purposes.

The Monitor and Control System components are: Serial Line Controller (SLC), Central Buffer, Antenna Buffer, Data Tap, Data Set, Recording Tap, Command Simulator, Device Controllers, and Modcomp Interface.

The important system specifications and influences of the system environment are as follows:

1.1 The VLA control philosophy is that of central control in which all control commands are centrally formulated and then routed to the controlled devices and monitor data is gathered for performance and diagnostic analysis in the central control computers.

1.2 The system error control strategy shall be to detect errors at the message destination and report their occurrence along with parameters which describe address and occurrence rate. Error-tainted commands are not to be executed.

1.3 The system architecture should be similar to the rest of the antenna-associated electronics in that it should be structured with independent parallel information flow paths. Common elements should be held to a minimum. This structure permits antennas and electronics to be added to the system without perturbing the portions of the systems which are already in operation and improves overall reliability in that a failure in one portion of the system is less likely to affect information flow to other antennas.

1.4 The system must be capable of delivering a set of six commands to each antenna and associated electronics in each machine cycle. Both antenna and central commands should be delivered to the target devices at approximately the same time.

1.5 The command and monitor message flow must be synchronized to and be compatible with the LO/waveguide communication system which operates half-duplex with a 1 millisecond transmit-to-the-antenna period and 51.083 millisecond transmit-from-the-antenna period.

1.6 Command information shall be accessible from either of two computers in accordance with the settings of SLC panel toggle switches. Monitor data shall be input to both computers.

1.7 The message signal frequency components must be restricted to a frequency band of 500 kHz to 1.5 MHz and not contain a dc component as the LO Receiver output is ac coupled. The LO Transmitters and Receivers serve as the links between the Monitor and Control System and the waveguide/modem. The monitor and control messages are amplitude modulated on an 1800-MHz carrier by the LO Transmitter. This carrier is also used to generate 600 MHz at the receiving end which imposes bandwidth constraints on the message signal components. For this reason, high- and low-pass filters in the LO Transmitters and Receivers limit the band-pass to a 30-kHz to 1.5-MHz band. The low-frequency constraint is required to keep the region near the 1800-MHz carrier free of low-frequency modulation products as the 600-MHz signal is derived by mixing the 1800-MHz and 1200-MHz carriers.

The high-frequency constraint is required to suppress higher-frequency modulation products so that adjacent IF signals are not perturbed.

1.8 Message transmission down the LO/waveguide system must be time-serial as parallel transmission would require an excessive amount of bandwidth and hardware. The modest message flow rates do not justify the cost and complexity of parallel transmission when serial techniques are adequate.

1.9 The system must be able to gather and distribute monitor data without the participation of the control computers.

1.10 The command and monitor information are to be formatted into discrete digital messages with error detection coding features. The system must be capable of detecting and reporting message errors.

1.11 System bit error rate shall not exceed 1 bit error per 3.24×10^6 bits or 1 error every 6.25 seconds for the whole system.

1.12 The system must operate at data rates ranging from computer parallel DMA I/O rates to modest clock rates which permit digital signals to be easily routed over the lines between control terminals and commanded/monitored devices.

1.13 Serial transmission techniques should be used between units so that cable runs and rack wiring are minimized.

1.14 The system should have a minimum number of types of units and be packaged in the standard VLA module hardware.

1.15 Control terminals (Data Sets) must be able to error test and output digital commands and gather both digital and analog data. The analog data to be gathered is in the range of ±10 volts and should be converted to 12-bit binary values with modestly priced A/D converters.

1.16 The Data Sets must be capable of servicing a large number of command and data channels or devices.

1.17 Data Sets should be located near the devices to be serviced to minimize the length and bulk of wire runs.

1.18 The composition of monitor data from any Data Set should be programmable by a custom programmed PROM (programmable read only memory) to select the data at sampling rates most appropriate for the particular devices being serviced.

1.19 Data Sets data channel sampling should be synchronized so that all Data Set PROM's have identical address states at any given time. For example this permits all DS 1 data input to the

computers to be the same data parameter from all antennas at any given moment.

1.20 The Data Set must be capable of sampling a designated data channel each machine cycle for intensive analysis. The selected channel address shall be controllable by a command directed to the Data Sets.

1.21 Data Set A/D circuitry shall use differential amplifiers with common mode noise rejection properties. CMRR should be at least 60 dB with 1000-ohm signal source impedances and common mode voltages up to ±10 volts.

1.22 The system shall have provisions to sense, select, store, convert and display command and monitor data messages in the antennas, central electronics room and control room. The message components shall be displayable in binary, decimal and octal formats and the selection and storage operation shall be independent of the operation of the control computers. The unit which performs this function is the Data Tap and shall have D/A converters to permit D/A conversion of the stored messages.

2.0 SYSTEM FUNCTIONAL DESCRIPTION

2.1 Message Structure

Figure 1 depicts the message structure used throughout the Monitor and Control System (hereinafter abbreviated to MCS). The format is common to both commands and monitor messages and represents a message associated with a specific channel or device. The device association is conveyed by the address components (i.e., DCS address, Data Set address and Multiplex address). In the case of commands, the composite address refers to a device which is the message destination. In contrast, the composite address in monitor data messages refers to a device which is the data source.

Since the portion of the VLA electronics which communicates with the antennas uses independent parallel paths, a portion of the address is associated with an antenna and is called "DCS address" (formerly "antenna address" which was a functional misnomer). These five bits in the message format provide 32 DCS addresses to designate the 27 antennas and enable some reserve capacity for distributed non-antenna associated functions. DCS addresses are associated with "D"-Rack physical locations and sequence from 1 through 33_8 (1 through 27_{10}) starting with "D"-Rack 1 on the southwest arm row of "D"-Racks. The buffer's associated DCS address are displayed on front panel LED's.

The Data Set address (0 through 7) refers to the control terminal which serves as the command executor and data gatherer. The Data Set is placed in the midst of a group of devices which must be commanded and monitored. Up to six Data Sets may be serviced in an antenna. The Data Sets associated Data Set address is displayed on a front panel LED.

Finally, the Multiplex address designates the specific device or channel serviced by a given Data Set in a given antenna. Up to 256 devices can be serviced by a Data Set, and these are partitioned into functional groups as follows:

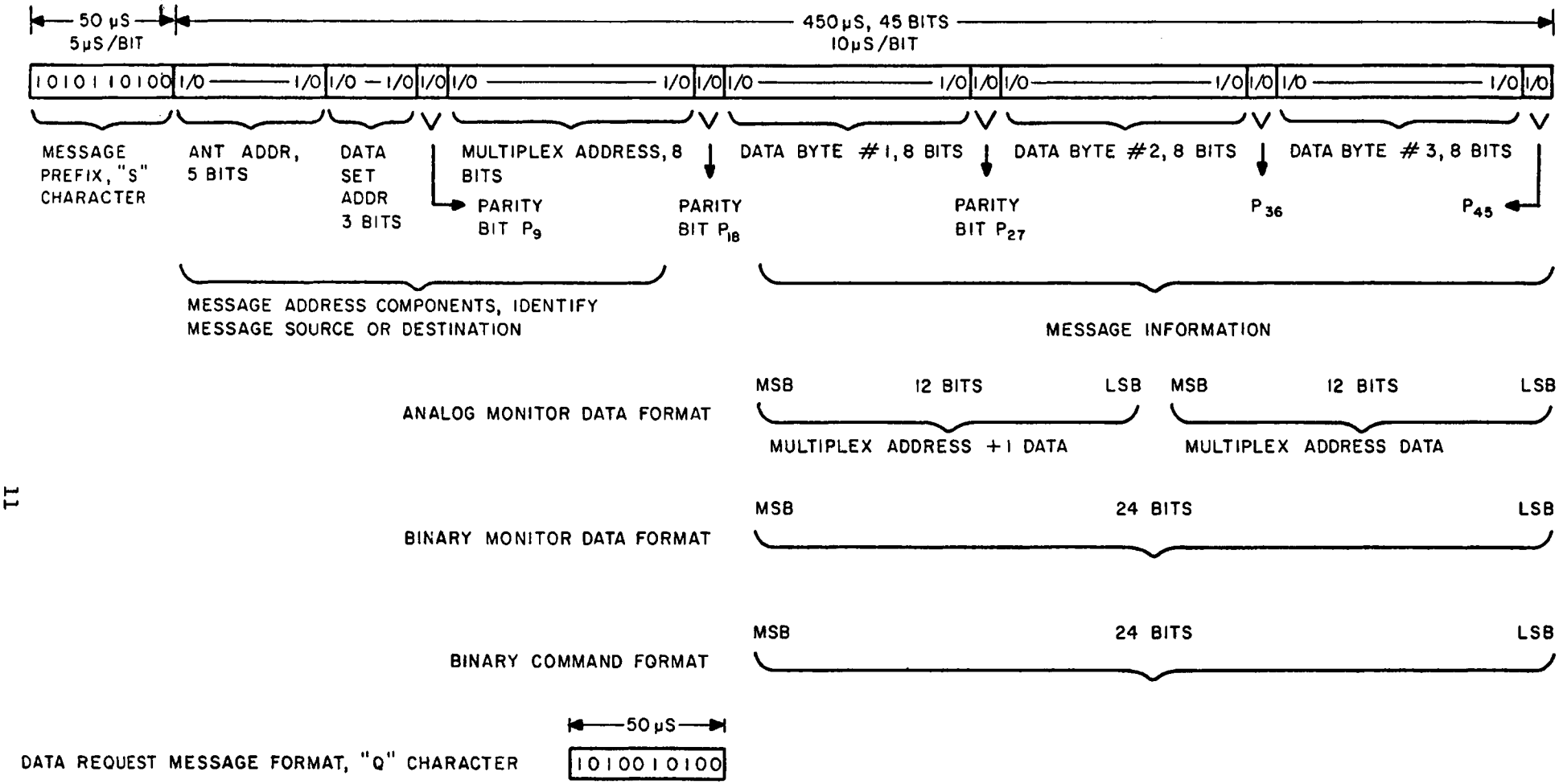


FIGURE 1: DATA SET COMMAND AND MONITOR DATA AND DATA REQUEST MESSAGE FORMATS

TABLE I: MULTIPLEX ADDRESS USAGE

Decimal	Octal	Usage	Channel Capacity
0 - 127	0 - 177	Analog Monitor Data	128
128 - 191	200 - 277	Binary Monitor Data	64
192 - 207	300 - 317	Data Set Mode Commands	16
208 - 255	320 - 377	Binary Commands	48

All address components are encoded in binary format and are usually referenced as octal numbers in this and other MCS manuals.

The information conveyed in the message is carried in the 24 bits which have the binary and analog formats shown in Figure 1.

Parity bits occur at every ninth bit and establish odd parity over the preceding eight bits. A message is prefixed by a preamble or "start" character which is used as a signal to message detection logic that a message is arriving and must be acted upon. This preamble (often abbreviated to an "S" on the logic diagrams) is discarded at the final message destination. The bit rate of the "start" character is twice that of the message components so that it may be uniquely detectable.

The messages are formatted at the message source and traverse the system unaltered (with one minor exception discussed later). Message bit rates range from 50 kHz to 1 MHz and are determined by the requirements of the particular path in the system. Messages to and from the SLC use the 1-MHz bit rate as the SLC is the convergence/divergence point for all messages and must handle a large volume of message traffic between the computers and the MCS.

The data request message of Figure 1 is a ten-bit burst that resembles the "S" portion of the command and monitor data messages and has the same bit rate as the "S". The data request message is often referred to as the "Q" (for query) character in the logic drawings and module manuals.

2.2 System Design Features

Figure 2 depicts the Monitor and Control System block structure. Many features are common in MCS units; these are outlined below:

2.2.1 System operations are based upon time -- as triggered events or time-qualified operations. In each unit which has system control (i.e., SLC, Central and Antenna Buffers), there is a time base which is triggered on by synchronization signals from the LO system. Timing terms derived from this time base are causative in initiating system operations or enabling inputs or outputs.

2.2.2 Communications between units are time-serial and are effected by two lines per controlled unit: a "command" line and "monitor data" line. This pair forms a port on units such as the SLC and Antenna Buffer which communicate with a number of units.

2.2.3 Command and monitor data messages are temporarily stored in memories in the buffers and are then "pushed" through the LO/waveguide system, buffer-to-buffer. This storage and push-thru tactic is required for command messages because the 1-ms waveguide transmission period is too short to permit six commands for 32 antennas (128 total) to be accessed from the control computers, formatted and serially output. The same tactic is used in monitor data messages as the data is gathered at a different rate than that used in transmission down the waveguide. In effect then, messages progress through the system, stage-by-stage, in a time-ordered manner.

2.2.4 At the receiving ports the messages are treated as an asynchronous, discontinuous burst. Receiving logic circuits sense edge transitions for synchronization, sample

and analyze the incoming stream bit pattern to detect the "S" character. When the "S" is detected, a loading sequence is initiated to store the entire message for subsequent readout to a downstream unit. In short, the message reception tactics are "detect and tuck away".

2.2.5 The three units vested with MCS control (i.e., SLC, Central and Antenna Buffers) all gather monitor data from their subordinate sources by polling with the data request message. A data request message is transmitted to a specific unit on the command lines and, when detected, evokes a response in the form of a monitor data message. If the polled unit does not respond within a given time period, the polling unit will press on and poll the next unit in the sequence. The exception to this polling operation is the "pushing" of monitor data down the waveguide from the Antenna Buffer to the Central Buffer in which polling is not possible because of the half-duplex properties of the LO/ waveguide system.

2.2.6 As polled monitor data messages are evoked by the SLC and Antenna Buffers, they are immediately rebroadcast on the command lines so that the antenna Data Sets and Central Buffers "hear" their own outputs. The effect of this rebroadcasting is to locally distribute <u>all</u> commands and monitor data messages to all units. The reason for this recursive property is that a Data Tap may be connected to any Central Buffer, antenna Data Sets or SLC port so that it can trap and display any command or monitor data message locally available.

2.2.7 The monitor data message sources are Data Sets which emit two monitor data messages per cycle in response to two data request messages from the buffers. The first

message contains data sampled under PROM address control and the second message contains data sampled in accordance with either the designated address or a sequential scanning mode. The system as presently implemented has monitor data memory capacity and ports to service up to 6 Data Sets/antenna. Two additional Data Sets/antenna could be added to the system by modest logic changes. The present system monitor data capacity is 384 monitor data messages per cycle or 2 messages/Data Set × 6 Data Sets/antenna × 32 antennas.

2.2.8 Command messages from the SLC are broadcast to all Central Buffers where they are detected and analyzed for address relevance. That is, the DCS (antenna) address and Data Set address components of the message are decoded to determine if the command is directed to the buffer's associated antenna and electronics. If so, then the commands are temporarily stored in two command memories: one for antenna commands and the other for central commands. The commands are then emitted by being "pushed" out of the memories by different time discretes so that they are delivered to their target Data Sets at approximately the same time.

2.2.9 The Data Sets test the Data Set address component of the incoming message stream (consisting of command, monitor data and data request messages) to determine if the message is a command and is addressed to it for execution. If so, the command message is immediately loaded into the address-designated device.

2.2.10 All inter-unit communication ports use optical isolators on command inputs to eliminate ground loop and common mode noise effects.

2.2.11 The antenna hardware serial number is read out of each antenna on a binary data channel 202_8 in the Antenna Buffer. This serial number is completely unrelated to the DCS (antenna) address component of the command or monitor data messages.

2.2.12 The number of commands detected at an antenna in each cycle is read back to the computer by a psuedo Data Set, DS 4. This readback provides a cycle-by-cycle check of the integrity of the command path to the antenna.

2.2.13 Messages are error tested at the terminus and flagged bad if there is a parity error. The SLC tests the monitor data messages and sets a flag bit if there is a parity error. The Data Set tests messages (both command and monitor) and flags faulty messages by storing address components and error counts which are read out as binary monitor data.

2.2.14 To minimize rack wiring, command and binary data lines are routed as daisy chain buses between the Data Set and Device Controllers. Serial information is routed on these buses as information, clock and strobe lines. A daisy chain address bus from the Data Set to the Device Controllers enables the controllers to be selected by the Data Set.

2.2.15 Analog data is selected for conversion by a dual level multiplexing scheme; the first level is a multiplexer in a Device Controller which selects among analog signals in the device serviced by the controller. The second level is a multiplexer in the Data Set which selects among Device Controller multiplexers. The Device Controller multiplexer address is driven by the daisy chain address bus.

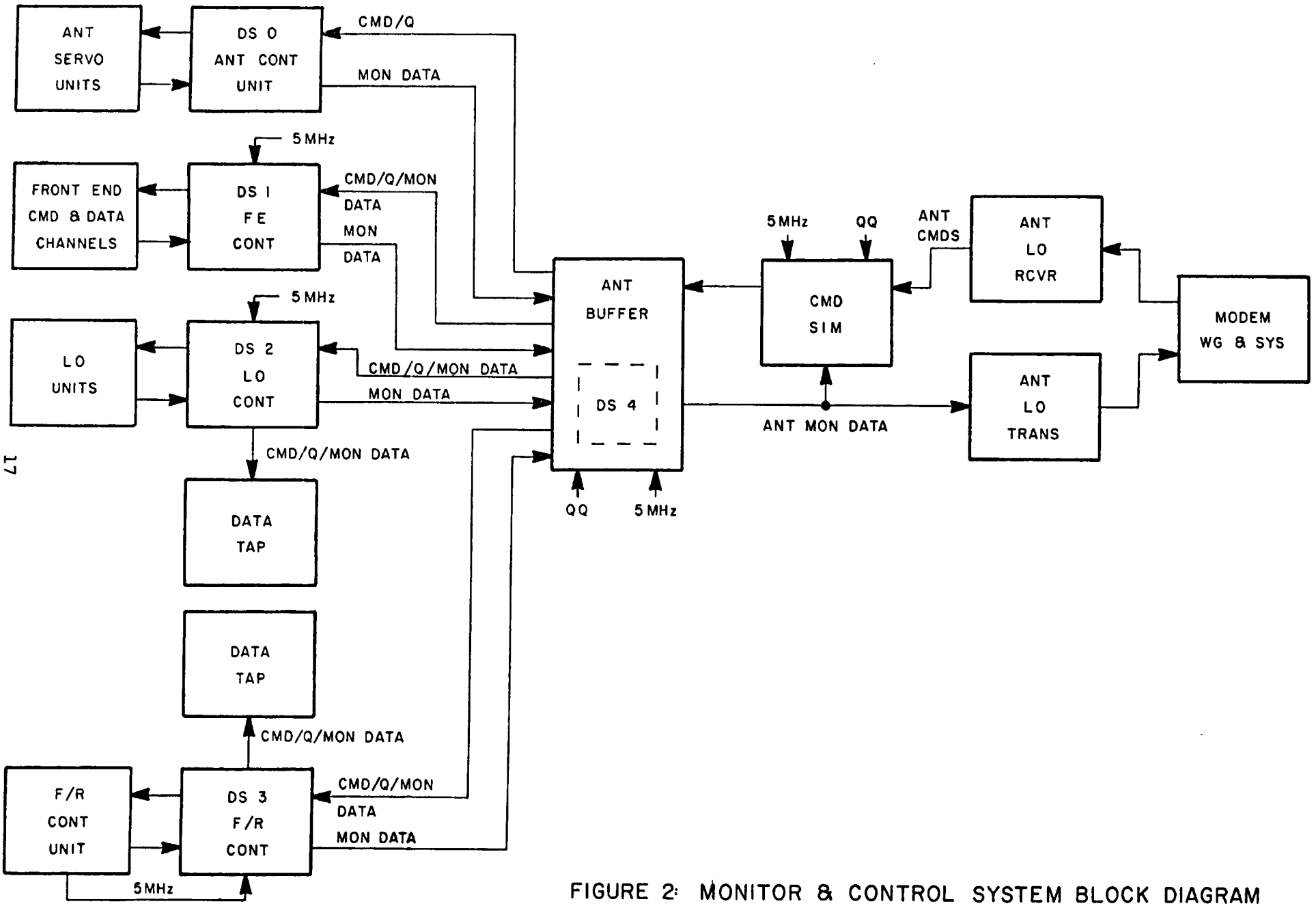


FIGURE 2: MONITOR & CONTROL SYSTEM BLOCK DIAGRAM

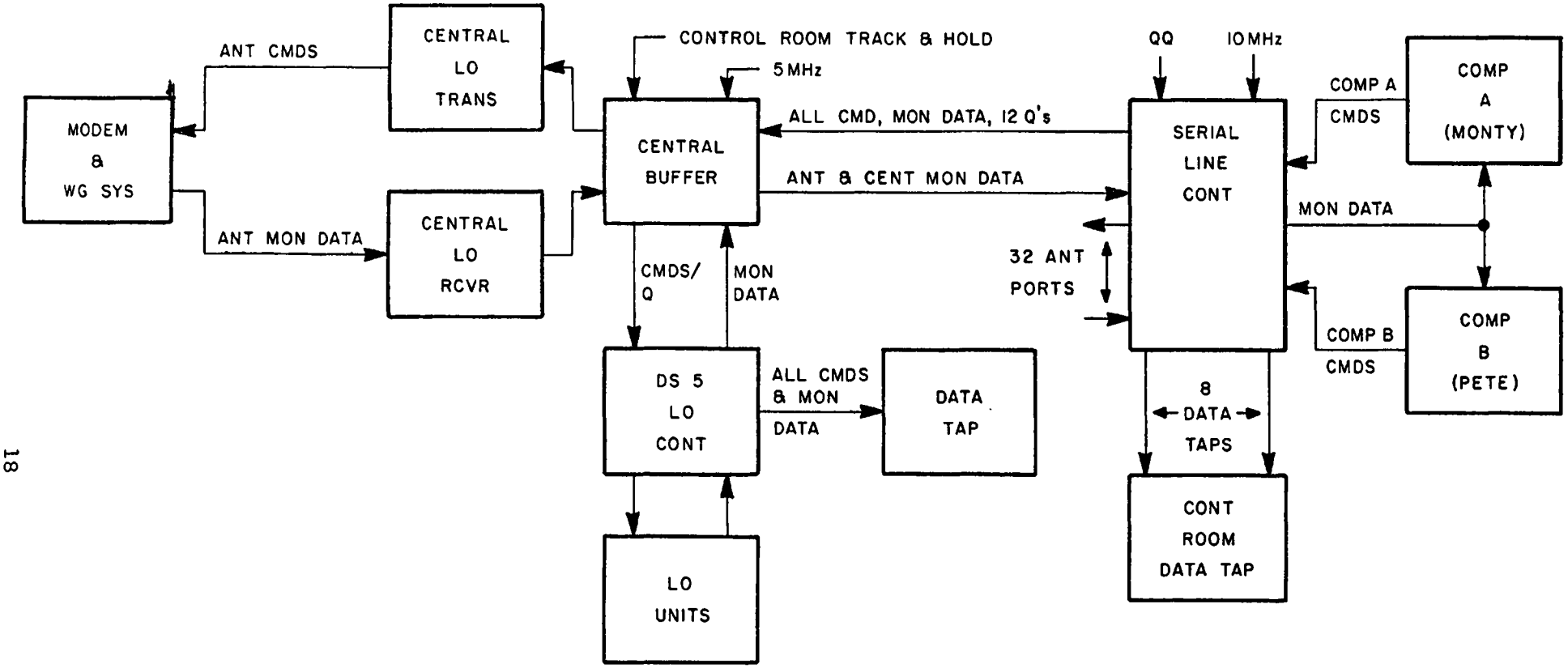


FIGURE 2: CONTINUED

2.3 Command Operations

Timing diagrams 1 and 2 depict the central and antenna timing operations. In this section we consider the flow of command messages through the system, from computer to Device Controllers.

Command operations are initiated by the Serial Line Controller (SLC) at t = 29,000 μsec. The SLC begins to alternately access command message components from either of the control computers. The three message components are depicted in Figure 3. The SLC combines the components, formulates message parity, prefixes an "S" character and serially outputs the message on a broadcast basis to all Central Buffers at a 1-μsec/bit rate. Specially designed interfaces in MONTY and BACCUS provide the command message components via the computer's DMA channels. The actual number of command messages output by the SLC depends upon the number of command message components placed in the computer's command buffer area in core and the settings of the SLC front panel switches. The switches determine the assignment of DCS addresses to the control computers and may be set to A Master (MONTY) or B Master (BACCUS) in which all command messages are to be output only from the selected computer or to the Select mode in which individual switches determine the accepted source computer. At the termination of the command output period, the SLC provides an interrupt to MONTY and BACCUS via the custom interface.

The Central Buffers all hear the broadcast command messages. The Central Buffer loads these messages and tests the DCS (antenna) and Data Set address components. If the DCS address components match those assigned the buffer (via hardwiring on the bin connector), the buffer will store the message in either of the two command memories in accordance with the Data Set address components. The command messages directed to the central Data Set (DSA 5) are stored in a 6-message memory which is unloaded at a 10-μsec bit rate beginning at t =

8 μs. Antenna command messages are stored in a 4-word buffer which is unloaded at t = 0 at a 4-μs/bit rate. An 80-μsec preamble is prefaced to the antenna command message transmission to damp out a switching transient in the LO Receiver at the antenna. The duration of the antenna command message transmission is 896 μsec (80-μsec preamble + 4 each 100-bit messages × 2-μsec bit + 8 dummy bits/message × 2-μsec/bit). Approximately 1016 μsec is available for antenna command message transmission through the LO/waveguide system. A biphase modulator in the Central Buffer modulates the antenna command messages in biphase L format with a 500-kHz clock.

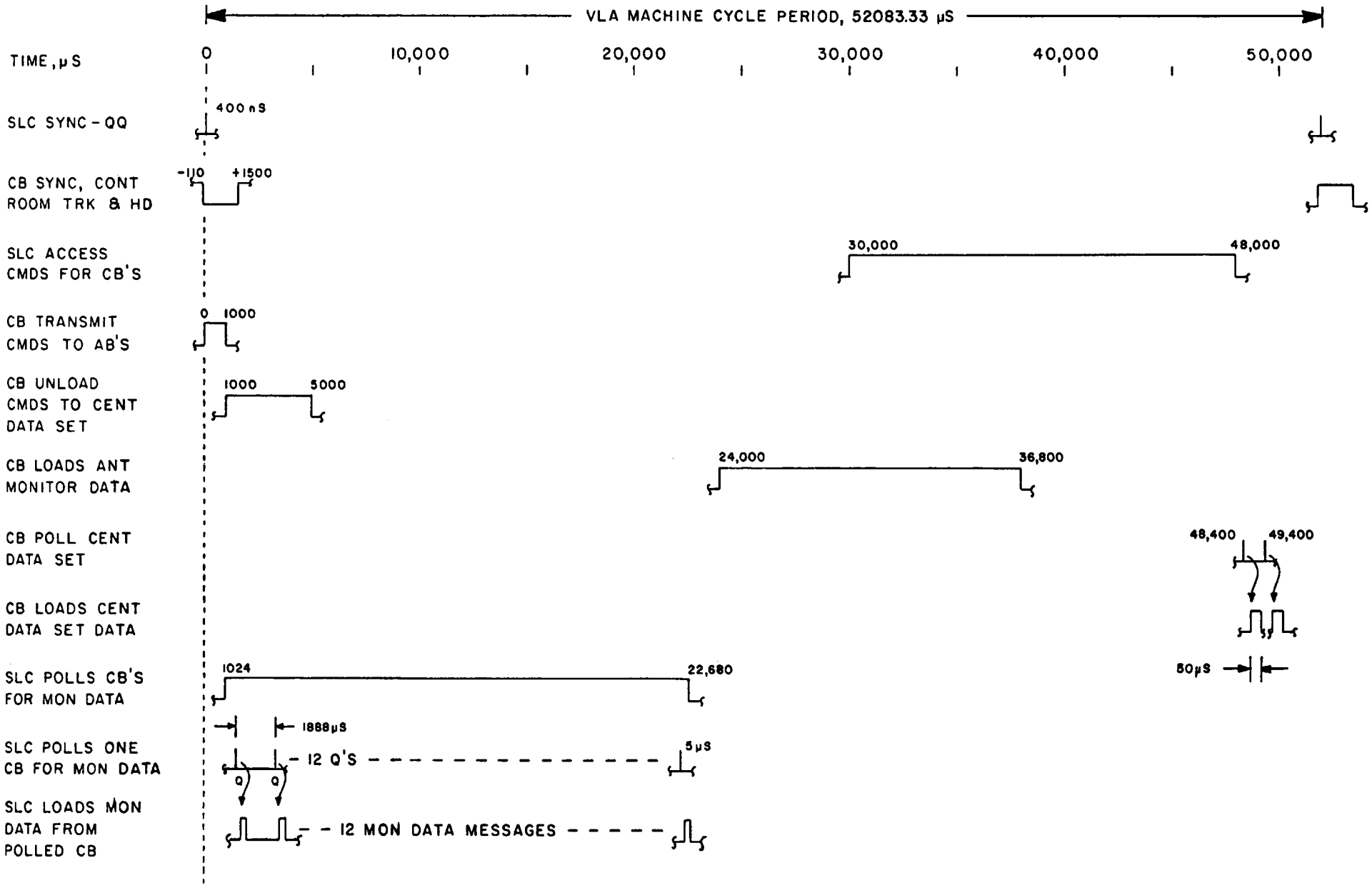
The Antenna Buffer receives the antenna command messages via the LO Receiver. A 0 to 1000-μsec enable on the buffer input permits it to respond to command messages only during this period. This enable truncates large signal perturbations associated with the transitions of the LO/waveguide system to the receive mode at t = 0 and return to the transmit mode at t = 1016 μsec.

As the antenna command messages are input by the Antenna Buffer, the DCS-DSA components (1 byte) are parity tested and if found acceptable the DCS address is stored in a memory for subsequent use by the buffer. The antenna command messages are stored in a buffer memory which is subsequently unloaded at t = 1000 μsec at a 10-μsec/bit rate. The command messages (up to four) are broadcast to all antenna Data Sets by the Antenna Buffer in the unload process.

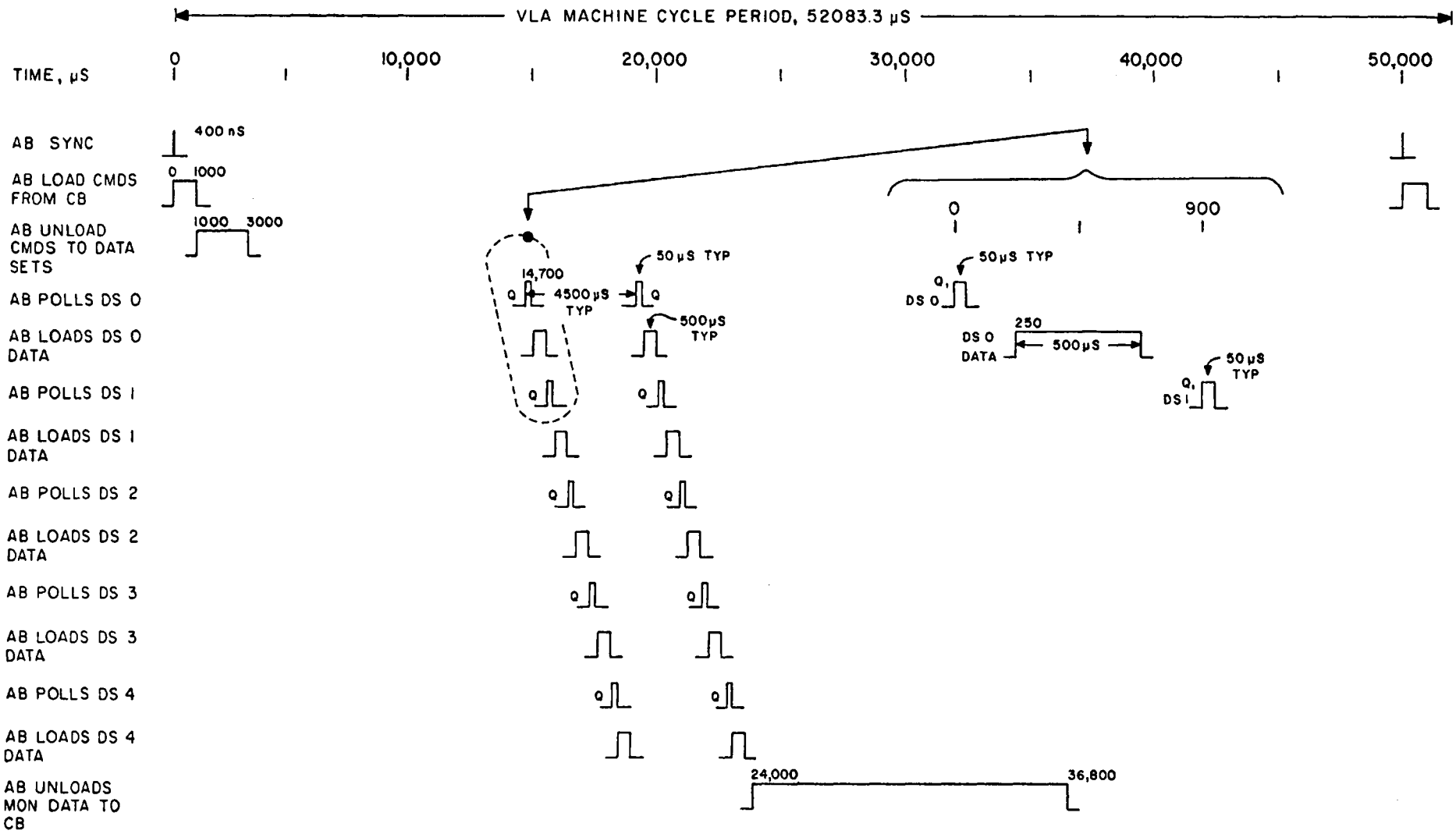
The Data Sets detect and load the command messages and test the Data Set and multiplex address components (the DCS address is ignored) to determine if the command message is directed to the Data Set and is a command. If the command message is not tainted by parity errors the Multiplex address components are decoded to activate output data, clock and strobe lines to cause the command information to be loaded into the target Device Controller.

The Antenna Control Unit receives, detects and executes the commands addressed to it as if it were one of the NRAO Data Sets but does not hear the rebroadcast monitor data messages from Data Sets 1, 2, 3, and 4. This data has been disconnected from the Antenna Buffer's ACU command line.

There is a time lag between the access of the command information in MONTY or BACCUS core memory and the arrival of this information at the designated Device Controller. This effect may be inferred from timing diagram 1. In terms of nominal machine cycles, if a command is output by the computers in cycle N it will be executed in cycle N+1.



TIMING DIAGRAM 1: CENTRAL TIMING OPERATIONS



TIMING DIAGRAM 2: ANTENNA TIMING OPERATIONS

2.4 Monitor Data Operations

In this section we consider the flow of monitor data messages through the system, from Data Sets to the computers.

When stimulated by either buffer the Data Set gathers digital and analog data from Device Controllers and converts and formats the data into monitor data messages which are then output to the buffers.

At t = 14,700 μsec the Antenna Buffer begins polling the five antenna Data Sets by means of the data request message to evoke two monitor data messages from each Data Set. If a Data Set responds with a monitor data message, the Antenna Buffer rebroadcasts the message to all Data Sets via the command lines and injects the DCS address into the monitor data message as it is stored. The DCS address is obtained from the register in which it was stored in the command operations of 2.3 above. By connecting a Data Tap to any Data Set in the antenna, it is possible to monitor and display any command or data message in the antenna environment.

In the event that a Data Set does not respond to the data request message within 300 μs, Data Set 4 is triggered into operation and substitutes a message for the nonresponsive Data Set. The Data Set address in the substitute message is that of the nonresponsive Data Set and the MUX address is 205_8.

The antenna monitor data messages stored in the buffer memory are unloaded into the LO/waveguide system at t = 24,000 μsec at a 20-μsec/bit rate. The ~~ten monitor data messages~~ require 12,800 microseconds to effect the transfer from Antenna to Central Buffer. A preamble of 800 microseconds is used to damp out the LO Receiver switching transient. As the antenna monitor data is unloaded into the LO/waveguide system it is biphase modulated by a 500-kHz clock to eliminate dc and low-frequency signal components.

As the antenna monitor data messages arrive at the Central Buffer they are demodulated to NRZ format and stored in a

buffer memory for subsequent output to the SLC and computers. At t = 48,400 μsec and 49,400 μsec the central Data Set (DS 5) is queried by the data request message to evoke two monitor data messages which are added to the contents of the Central Buffer data memory.

At t = 1024 μsec the SLC begins to poll the Central Buffers by means of the data request message to unload monitor data messages which are then loaded into the SLC, error tested and then transferred to the two control computers in three-word components as depicted in Figure 3.

The polling sequence begins at the Central Buffer assigned DCS address 0, sequences to address 37_8 and repeats the 0 through 37_8 sequence eleven times to transfer 384 monitor data messages to the SLC and computers. The SLC error tests the monitor data messages and if an error is detected a Parity Error flag bit is set in the first word transferred to the computer. If a Central Buffer does not respond to the data request message a No Response flag bit is set in the first computer word.

The DCS address component of the monitor data message is compared with the SLC port address (an internal SLC function) and if they are different the No Response flag bit is set. This comparison tests for the occurrence of misidentified data which can happen if an antenna is not receiving commands and the DCS address stored in the Antenna Buffer has been perturbed.

Substitute data messages generated by DS 4 on a default basis are also flagged as No Response messages.

As the monitor data messages are input to the SLC, they are rebroadcast on the SLC command lines so that the Central Buffers "hear" their own output data messages. A Data Tap connected to the Central Buffer is thus able to hear all command and monitor data messages.

When the SLC has completed the Central Buffer polling operation it generates an interrupt to the computers to signal that the data is now available for analysis.

The response time for computer verification of the execution of a command is 2 machine cycles. If MONTY or BACCUS outputs a command message to the SLC in cycle N, it will arrive at the designated device in cycle N+1. The response to the command may be sampled (if the Data Set is selected to monitor the appropriate channel) in cycle N+1 and then will be input to the computers in cycle N+2.

2.5 System Time Synchronization

As indicated in the descriptions above the Monitor and Control System operates in a time-ordered manner in which message polling and transfers are initiated and enabled only during appointed time periods. To affect these time-ordered operations time bases in the Antenna and Central Buffers and Serial Line Controller generate triggers and enabling terms which initiate message transfers and enable their reception and storage.

The time bases in the buffers are driven by a 5-MHz clock and the SLC by a 10-MHz clock from the LO system. The buffer time bases are synchronized (i.e., zero referenced) by discrete signals from the LO system which stimulate the buffers time base into operation. If these discrete signals are absent or not detected the buffers will remain in a quiescent state.

At the antenna, time synchronization is implemented by sensing the arrival of the leading edge of the 1200-MHz carrier. The LO Receiver routes this edge to the slave (i.e., antenna) L8 which performs all the timing operations in the antenna. L8 causes the Modem to shift to the receive mode for 1 millisecond to enable antenna commands (and also LO frequency information) to be received. L8 has flywheeling logic to enable continued operation in the event that the 1200-MHz carrier on signal is not detected. If synchronization is totally lost, L8 will continue to issue time discretes and synchronizing signals but will periodically shift the Modem to the sustained receive mode to assist the Modem in searching for the signals from the central Modem.

When synchronization is lost, the Antenna Buffer will continue to gather data for transmission to the Central Buffer; however, when the Modem is switched to the sustained receive mode, the antenna data flow is interrupted for a period of several seconds. If the Modem is unable to reacquire lock, the data flow will continue to be periodically interrupted.

The Antenna Buffer and SLC are synchronized by the "QQ" signal and the Central Buffer is synchronized by the "Control Room Track and Hold" signal. These signals are provided by L8 or the L8 signal distribution system.

If the "QQ" synchronizing signal to the SLC is absent or undetectable the SLC time base will recycle at t = 53,000 μsec so that the next machine cycle operations may continue. Consecutive nondetection of the "QQ" signal will cause the SLC to quickly lose synchronization with the Central Buffers.

The Data Sets require a 5-MHz clock from the LO system but do not have a time base as they are wholly subordinate to the buffers and respond to the buffers stimulus whenever it is detected.

The Data Tap uses an internal 10-MHz crystal clock in lieu of a clock provided by the LO system. The Data Tap does not have a time base so it can respond to any message it hears.

The time synchronizing signals from L8 (i.e., QQ and C/R Track and Hold) have a 3-state period sequence of 0, 200 ns and 10 μsec so that when synchronized to one of these terms (say with a scope at an Antenna Buffer) signals which are synchronized to the other term will appear to jitter by 10 μsec. Thus commands will arrive at an Antenna Buffer with an apparent 10-μsec time jitter. This jitter is not a malfunction but does require more care in interpreting logic operation.

2.6 Message Density and Capacity

As stated earlier the monitor data capacity is 384 messages/machine cycle and the SLC inputs this quantity to the computers. Unimplemented DCS channels are input as dummy messages with all bits set to zero and the No Response flag set. The monitor data capacity of the system (either more Data Sets or more data/cycle from Data Sets) could be increased by adding more memory to the Antenna and Central Buffers and increasing the polling rate or by adding more Data Set ports up to a total quantity of 8. There is little likelihood that such changes will ever be necessary as the present data channel usage is ~50% of capacity for analog data and ~5% of capacity for digital data. Adding additional antenna-associated electronics racks might make it desirable to add more Data Sets.

The command message capacity as presently implemented in the SLC is 225 messages/cycle from either of two computers (112 maximum from a single computer). The capacity of the Central Buffers is 10 messages/cycle (4 antenna + 6 central) which suggests that the SLC message capacity should be 640 messages/cycle, (10 × 32 = 320/comp × 2 computers). Specification A13710N1 specified a capacity of 6 × 32 = 192 command messages accessed from either of two computers. In practice the existing capacity is more than adequate as the average message density/antenna is 0.319. The command assembly programs generate four command messages/antenna/cycle (the command messages may not necessarily be antenna-associated) and these are designated words A, B, C, and D and imply their time ordering in the Central Buffer memories. The usage and rate of message emission are tabulated on the following page (10 sec or 192 machine cycles is the averaging base).

Peak message density/antenna can be 4 if the operator types commands very rapidly and is properly synchronized (usually not the case). A special test program permits 4 commands/cycle to be continuously output to a DCS channel but few people know how to invoke it.

TABLE II: USAGE AND RATE OF COMMAND MESSAGES

WORD:	A	B	C	D
USAGE:	ACU only	Observing	Initialization	Operator Manual
RATE:	1/cycle	6 cmds/every 24 cycles	4 cmds every 192 cycles	Slow
TYPE:	Alternate Az and El pos cmds	2 ea L7 rate 2 ea L7 phase 1 ea L7 phase switch 1 ea T5 noise signal switch sync	4 ea Data Set PROM sync	Operator Initiated
CMD DENSITY:	1/1 (192/192)	6/24 (48/192)	4/192	~0
	Start/stop observing: Mode change	Source change time: 4 front end frequency and mode 2 F/R pos 2 L6 frequencies 8 Fluke synth frequencies		

AVERAGE DENSITY: 10 Sec (192 cycles) average: D = 245/768 = .319 excluding source change cmds
D = 261/768 = .339 including source change cmds

2.7 System Error Rates

Specification A13710N1 specified a maximum error rate of 1-bit error per 3.24×10^6 bits or 1 error per 6.25 seconds for the whole system. This corresponds to 1 error/120 machine cycles with message flow at the specified full capacity [i.e., (6 command messages/cycle-ant + 12 monitor messages/cycle-ant) × 32 antennas or 576 messages per cycle]. 120 machine cycles at this message density would contain 69,120 messages.

Extrapolating this error rate to the actual message densities cited above for 27 antennas and the master LO system (DCS 0) the system error rate would be (69,120)(6.25) ÷ [(12 + .319×4) (28)(120)] = 1 message error every 9.7 seconds. The error rate on a things-are-looking-good observing day is much better than this. Although there are no detailed recorded error statistics the system will on the average accumulate a few errors/antenna over a 2-day period when in this well-behaved state. The error rate on occasionally less felicitous days may be as high as 1 every few seconds and is localized to one antenna path. Interchanging buffers between a high and low error rate paths seldom alters the situation. When errors occur they are preponderantly monitor data errors - command errors are rare. There is reason to believe that these monitor data errors are the result of some spurious RF interference effects upon the 1800-MHz carrier. It has been observed for example that when the system is set to observe at certain L-band frequencies the monitor error rate may be high in certain antennas. Changing the observing frequency will virtually eliminate the errors. In other cases a high error rate can be eliminated by turning off front end paramps. There is also the possibility that some intermodulation exists between the IF's and the 1200- and 1800-MHz carriers. These anomalies have been investigated from time to time without any success in identifying and isolating the problem.

The command and monitor signal sidebands on the 1800-MHz carriers are typically about 26 dB to 30 dB above the noise floor. The realized bit error rate is consistent with this signal-to-noise ratio.

3.0 SYSTEM COMPONENTS DESCRIPTION

The components descriptions are brief and emphasize the salient features of the units; more detailed descriptions will be found in the various module manuals.

3.1 Serial Line Controller

Figure 4 depicts the Serial Line Controller logic block structure. The prime function of the SLC is to serve as a parallel-to-serial and serial-to-parallel interface between the control computers and the Central Buffers. Time is the control parameter in the SLC operations and terms derived from the time base initiate and permit transfers between the computers and buffers. The time base is synchronized by the QQ signal from the master L8. The SLC time base is clocked at 10 MHz from the master LO system.

At t = 29,000 μsec the SLC begins to alternately query the two computers (MONTY and BACCUS) for command message components. The queries are DMP requests, and the SLC tests for the first word synchronization pattern of a message set (see Figure 3). If the computer outputs a 16-bit word with this pattern the SLC appends the next two words, develops parity over the five bytes, prefixes the start character to the message and serially unloads it to the output buffer gates.

During the message formulation the computer A/B command select logic compares the DCS address components output by the computer with the settings of the front panel select switches. If the address/switch comparisons agree the message is permitted to pass through the output buffer gates to the Central Buffers and SLC-driven Data Tap. Commands may thus be output from either computer on a switch selectable basis or exclusively by either computer. This feature permits two computers to operate independent control/monitoring operations such as concurrent astronomical and test observations.

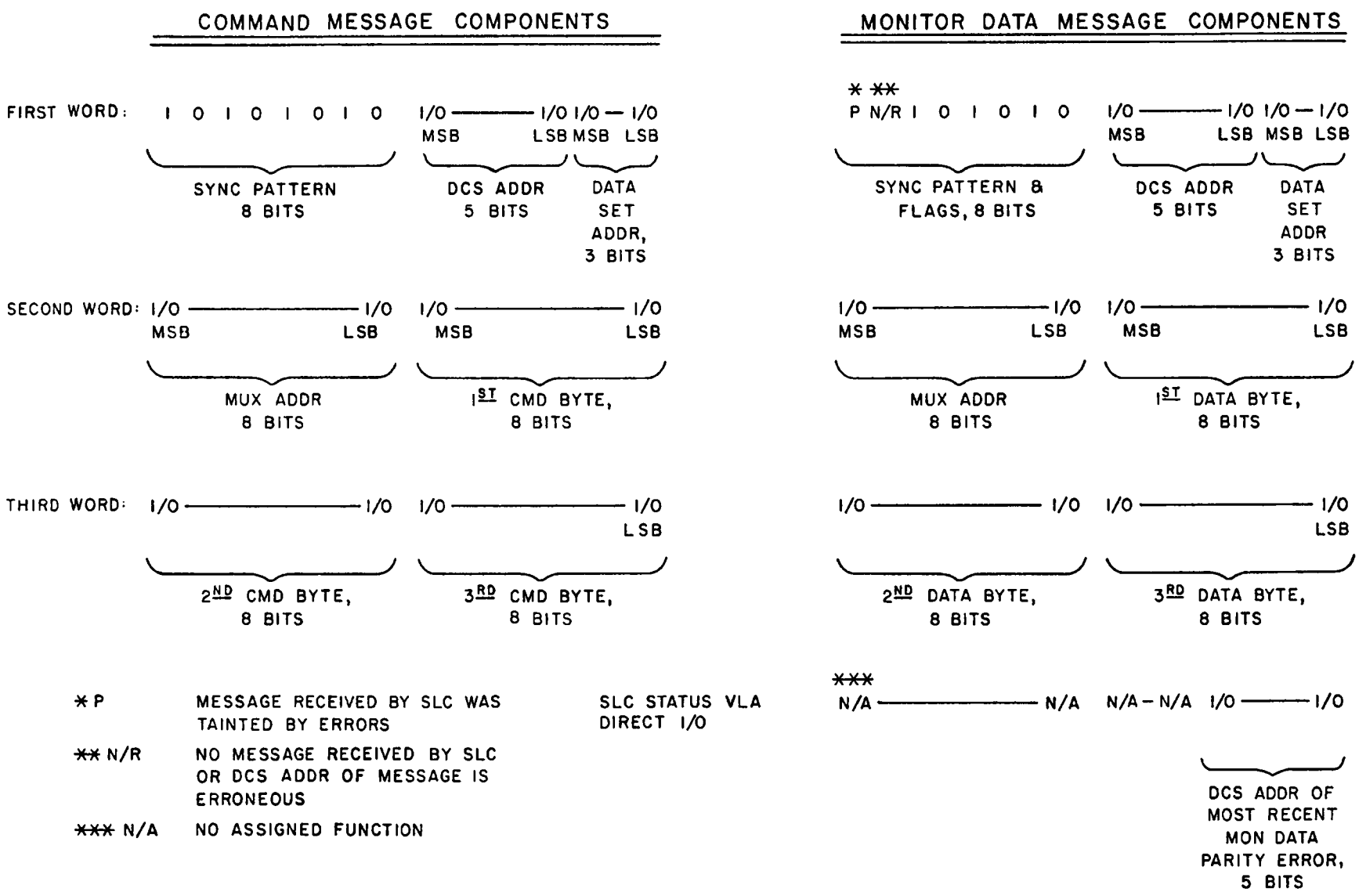


FIGURE 3: MODCOMP/SLC CMD/MON WORD TRANSFER FORMATS

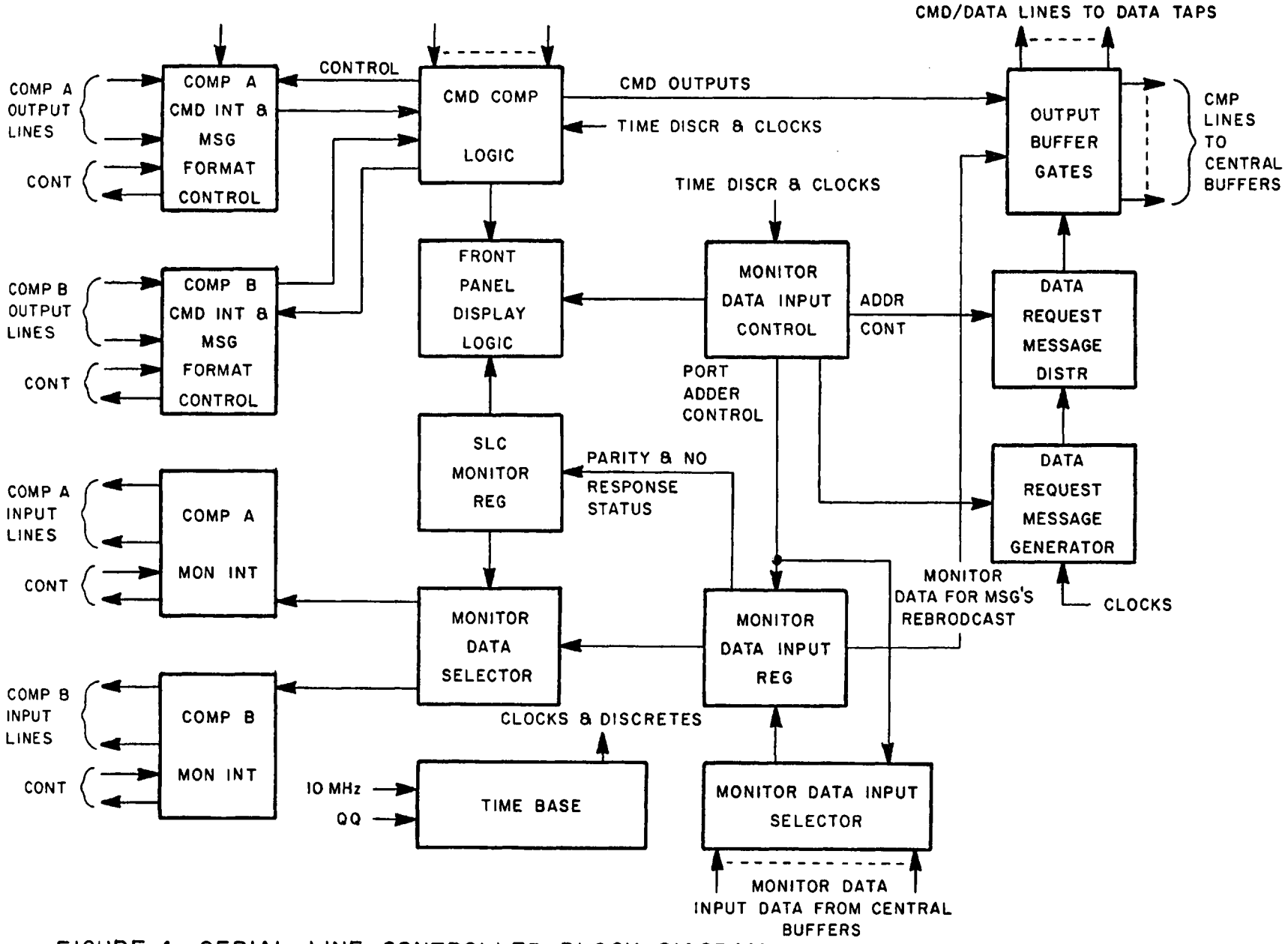


FIGURE 4: SERIAL LINE CONTROLLER BLOCK DIAGRAM

The SLC will attempt to output up to 225 command messages and then terminate the command operations with an interrupt to the computer. Note that the SLC imposes no constraints on the composition or address content of the command messages. The order, content and quantity of the command messages are solely under software control by the DCS program in MONTY and BACCUS. The program first clears and then loads the command buffer with 3-word sets of command message components which are to be output to the SLC.

The command message bit rate transmitted to the Central Buffers is 2 MHz for the start character and 1 MHz for the balance of the message.

At t = 1024 μsec the SLC begins to poll the Central Buffers for monitor data messages by means of the data request message which is directed first to the CB with DCS address "0". The polling is controlled by the data request message distributor and monitor data input sequencer logic. If Central Buffer DCS address "0" responds with a monitor data message it is error tested and output to the computers in three 16-bit word transfers. A synchronizing pattern is appended to the message information and appears in the first byte of the first word (see Figure 3 for details). Two flag bits are included in this sync pattern: Parity Error flag and No Response flag which respectively indicate a distorted or tainted message or that either the Central Buffer did not respond to the data request or that the DCS address component of the buffers monitor data message did not agree with the SLC port address. The SLC port address (a 5-bit code) is generated by the monitor data input sequencer logic and is identical to the DCS address. The purpose of this comparison is to verify that the DCS address assigned to the commands is correctly injected into the monitor data messages by the Antenna Buffer. This apparent malfunction can occur if the command flow to an antenna is terminated and the buffer is glitched by power perturbations which alter the content of the DCS address memory.

As the monitor data message from Central Buffer, DCS "0", is received by the SLC it is immediately rebroadcast via the output buffer gates to all Central Buffers so that it is available to the "D"-Rack Data Taps via the Central Buffers input circuitry. The Central Buffers command input logic does not respond to this message flow during the polling period.

As the monitor data message from Central Buffer DCS "0" is being input to the computer, the monitor data input sequence logic increments the SLC port address to 1 and outputs a data request message to Central Buffer, DCS "1". The buffer-polling/computer-input operations are thus overlapped in time. The buffer polling operation has very tight timing; 56 μsec are required to emit a data request message (10 bits at 2-MHz bit rate), evoke a response and completely load the monitor data message into the SLC. Fifty-eight μsec is available for these operations. The SLC message transfers to both computers are in step and sequence at a rate of 16 μsec/transfer. The computers DMA request line (DATARS) is raised and the computer is expected to sample the input lines within 16 μsec.

The SLC will poll Central Buffers DCS "0" through DCS "37_8", then repeat the sequence 11 times for a total of 384 monitor data message transfers.

All communications between the computer and SLC are terminated on optical isolators for common mode noise rejection and ground isolation purposes. The cable run between the SLC and computers is about 150' of shielded, twisted pair cable. The DMA transfer rate realized over this SLC/Modcomp interface is typically 6 μsec/transfer.

3.2 Central Buffer

Figure 5 depicts the Central Buffer (M3) block structure. The primary functions of the Central Buffer are message acquisition/storage/emission and system control. The Central Buffer is assigned a DCS address via hardwiring on the buffer bin I/O

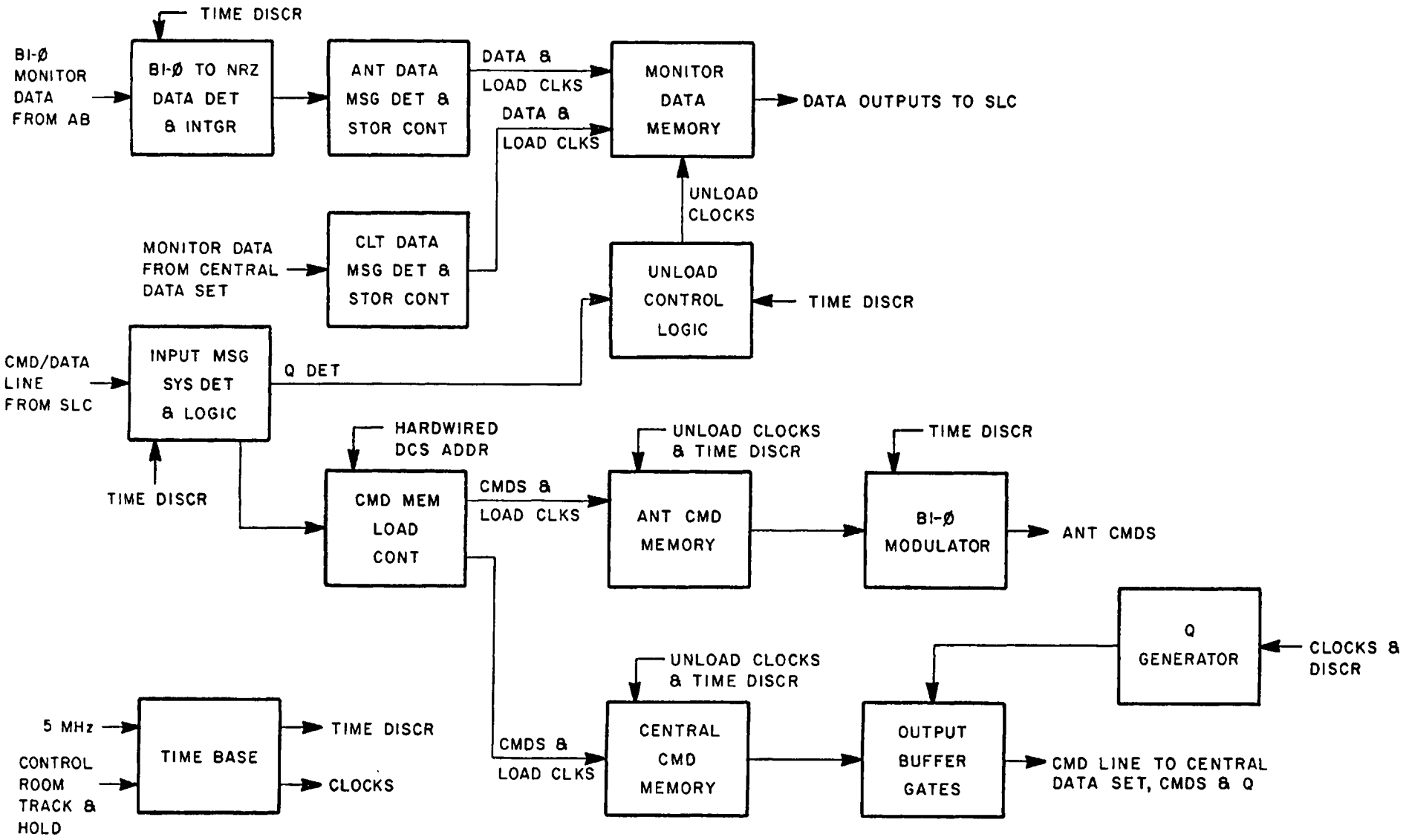


FIGURE 5: CENTRAL BUFFER BLOCK DIAGRAM

connector. The Central Buffer is permitted to listen to the command messages broadcast by the SLC during the period t = 30,000 to 48,000 μsec. The input message synchronization and detection logic detects the "S" character and compares the DCS address of the command message with the hardwired address, and if they agree, the message is stored in either an antenna command memory or central command memory in accordance with the Data Set address component of the message (i.e., commands for DS 0 through DS 4 are antenna commands and commands for DSA 5 are central commands). The antenna command memory has a 4-message capacity and the central command memory has a 6-message capacity. At t = 0 the antenna command messages are pushed out of the antenna command memory at a 2-μsec/bit rate for the "S" bits and 4 μsec/bit for the message components. These commands are modulated by a biphase modulator and sent to the central LO Transmitter for transmission through the LO/waveguide system. At t = 3000 the central commands are pushed out of the central command memory at a 5-μsec/bit rate for the "S" character and 10-μsec/bit rate for the message components. These messages are directed to the central Data Set (DSA 5) which services each "D"-Rack.

For the period t = 24,000 to 48,000 μsec the Central Buffer is permitted to listen for antenna monitor data messages from the central LO Receiver. These messages are biphase modulated at a 500-kHz rate and have a data rate of 10 μsec/bit for the "S" bits and 20 μsec/bit for the message bits. A preamble of biphase zeros precede the message to damp out the LO Receiver switching transient. The messages are demodulated to NRZ format, integrated over the bit period (there are 10 biphase cycles per data bit) and loaded into a monitor data buffer memory. At t = 48,400 μsec and 49,400 μsec the Central Buffer polls the Central Data Set (DSA 5) for two monitor data messages. This data is added to the monitor data buffer memory. At t = 0 the data in this memory is positioned so that it is immediately available at

the buffers output port so that when the SLC polls the buffer for monitor data it can be immediately output. As successive polling requests unload monitor data messages the next message in memory is positioned at the memory output. Up to 12 monitor data messages may be gathered and stored in the Central Buffer. If required, additional capacity could be added by modest logic changes.

The time-base logic is synchronized by the Control Room Track and Hold term from the L8 signal distribution system. This term is true from t = -110 μsec through t = 1550 μsec. The Central Buffer times out the 110 μsec and turns on the time-base counters at t = 0. At t = 51,000 μsec the time base is turned off and awaits the arrival of the next Control Room Track and Hold signal. If it is not detected the buffer remains quiescent. The time-base logic is clocked by a 5-MHz clock from the LO 5-MHz distribution system. Front panel LED's indicate message flow activity.

3.3 Antenna Buffer

Figure 6 depicts the Antenna Buffer (M4) block structure. The prime functions of the Antenna Buffer are command message storage/emission and monitor data polling, storage and emission.

The Antenna Buffer is permitted to listen for antenna command messages during the period t = 0 to 1000 μsec. This time aperture is vital because of the presence of large switching transients from the LO system when it switches from transmit-to-receive and receive-to-transmit. The command messages are demodulated from biphase to NRZ code, detected and stored in a command memory. As the messages are being loaded by the command message storage logic the DCS/DSA address byte is parity error tested and, if found error free, the DCS address is stored in a memory for use in formatting monitor data messages. At t = 1000 μsec the stored command messages are pushed out of the command memory at a rate of 5 μsec/bit for the "S" char-

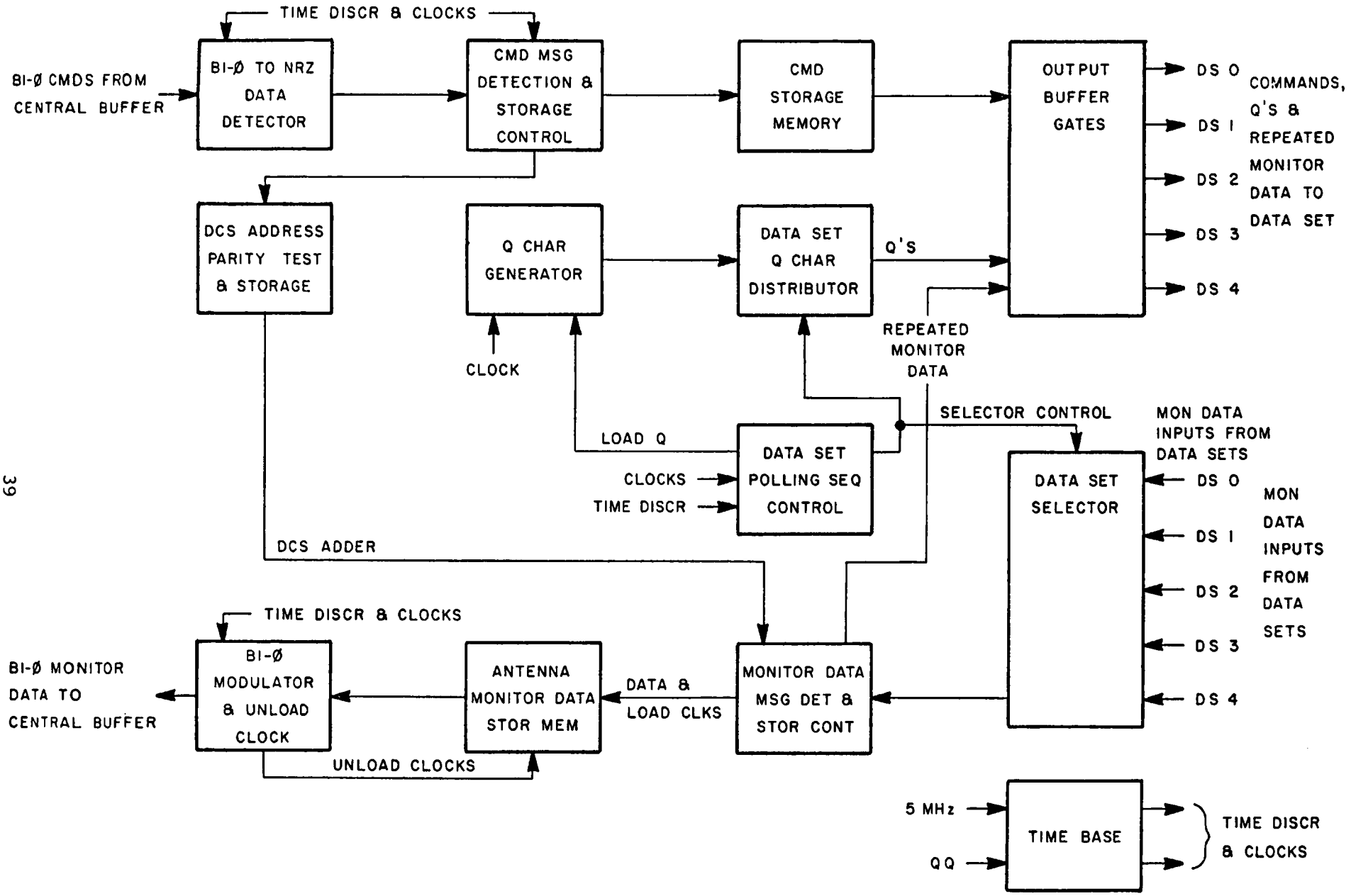


FIGURE 6: ANTENNA BUFFER BLOCK DIAGRAM

acter and 10 μsec/bit for the message components. Up to 4 command messages may be stored in the command memory. The command messages are broadcast to all antenna Data Sets by the output buffer gates.

At t = 14,700 μsec the Antenna Buffer begins polling the antenna Data Sets with the data request message to gather and store monitor data messages. The polling sequence is 0, 1--4, 0, 1--4 and is controlled by the Data Set polling sequence control logic which also controls the Data Set selector logic. The data request message is output to a selected Data Set at a 5-μsec/bit rate and the polling period is 900 μsec/Data Set. The time required for a Data Set to detect the request, gather and output a monitor data message is 750 μsec so there is a 150-μsec time margin. As the Data Sets emit their monitor data messages the monitor data message detection and storage control logic dubs the stored DCS address into the message and reformulates the DCS/DSA address byte parity. As the monitor data messages are received by the Antenna Buffer they are immediately rebroadcast to all the Data Sets via the output buffer gates. This rebroadcasting occurs upstream of the DCS address dubbing point so that the DCS address component of the rebroadcast data is always zero. The rebroadcasting of the antenna monitor data messages enables a Data Tap connected to any Data Set (except for the Antenna Control Unit, DSA 0) in the antenna to hear all command and monitor data messages locally available.

In the event that a Data Set does not respond to the data request message DS 4 is triggered to generate a substitute data message which is stored and rebroadcast. This substitution preserves the data ordering in the buffer's memory.

At t = 24,000 μsec the antenna monitor data is pushed out of the data memory, through a 500-kHz biphase modulator to the LO Transmitter for transmission to the Central Buffer. The transmission bit rate is 10 μsec/bit for the "S" character and 20 μsec/bit for the message components. The message has an 800-

μsec preamble of biphase zeros which precede the first message to damp out LO Receiver switching transients. Ten dummy biphase zero bits are placed between messages to simplify the data integration process in the Central Buffer. The Antenna Buffer time-base logic is synchronized by a "QQ" pulse from the slave L8 in the antenna. The time-base logic shuts itself off at t = 50,000 and awaits the next "QQ" pulse to stimulate the time base into operation at t = 0. If the "QQ" pulse is absent, the buffer will remain quiescent. A 5-MHz clock provided by L8 clocks the time-base logic.

Front panel numeric LED's indicate the stored DCS address and a command and monitor LED flash to indicate message flow activity.

3.4 Data Set

Figure 7 depicts the Data Set (M1) block structure.

The Data Set has two functions: to detect, error test and execute commands addressed to it and to select, convert, format, and output monitor data. In both these operations the Data Set is passive until stimulated into operation by the buffers.

When a command or monitor data message is detected by the message detection logic the message is error tested and, if found error free, the DSA and Multiplex address components are tested to see if the message is a command addressed to the Data Set. If so, the command information and Multiplex address are loaded into output registers.

The Multiplex address enables command output lines and activates the sub-MUX lines to Device Controllers. The sub-MUX lines are the least significant four bits of the Multiplex address and enable the Device Controllers to perform a 1 of 16 decode. The channel enables which are the higher-order portion of the Multiplex address activate one of the three sets of command output lines which drive Device Controllers. The combination of sub-MUX decode and channel enables provide a unique

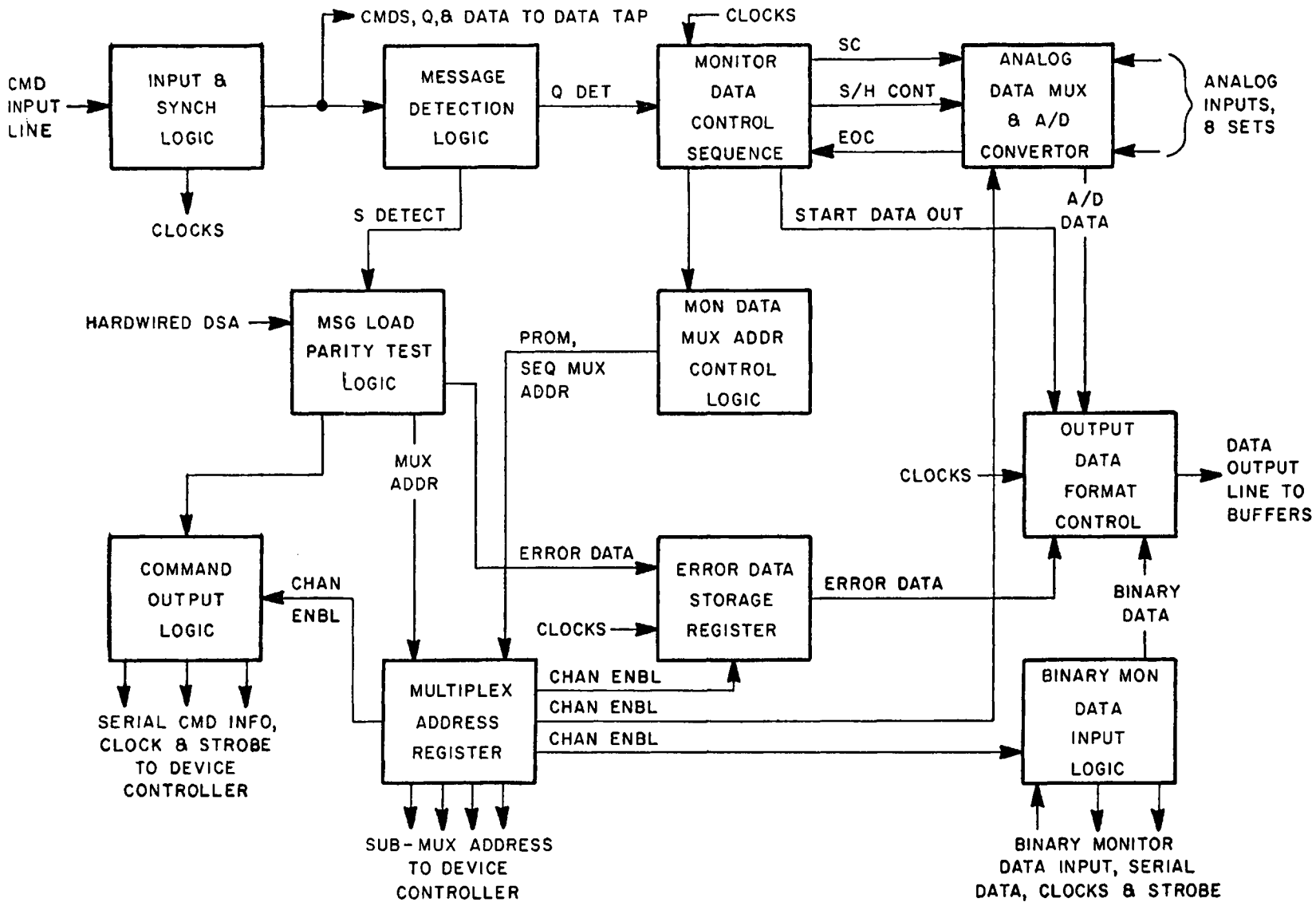


FIGURE 7: DATA SET BLOCK DIAGRAM

decode of the Multiplex address. The commands are loaded into Device Controllers by three lines: an information, clock and a strobe line. The timing relationship of these signals is shown on timing diagram 3.

If the command or monitor data messages are tainted by errors, address components are stored in a register which is read out as a binary monitor channel, address 200_8. If more than one message error is detected between 200_8 readouts, each occurrence is counted and the count is included in the 200_8 readout.

When the Data Set detects a data request message a data gathering sequence is initiated. The buffers evoke two monitor data messages per cycle. The first message samples data sources (Multiplex addresses) in accordance with the contents of a PROM which is custom-programmed to sample data in a manner most appropriate for the Data Set application. The second monitor word can be either sequential mode in which all analog addresses are sequentially sampled twice and all digitals once in ten seconds or in a selected mode in which the Multiplex address is fixed at a computer-commanded address.

Detection of a data request message causes the monitor data control sequencer logic to be activated which generates terms to formulate and load the Multiplex address (from the PROM, sequential or select registers), trigger the sample and hold and A/D converter and initiate the data output sequence. The output data format control logic then begins shifting out the data, and formulates and injects parity data bits into the output format. If binary data is being read out the binary monitor data logic issues a binary load strobe, load clocks and reads binary data shifted out of a selected Device Controller in response to the strobe and clocks. If analog data is being read out, the data from the A/D converter storage registers are injected into the output data stream. If error data is being read out (address 200_8) the contents of these registers are injected into the

output data stream. The Multiplex address determines which of the eight analog channels or four digital groups are selected for the output data stream. If analog data is being sampled and converted, two analog data sources are converted to 12-bit 2's complement format and packed into the 24-bit message format. The Multiplex address included in the message is that of the first channel converted. Table I shows the Data Set address usage.

A front panel numeric LED displays the Data Set address and a green and red LED flash to indicate monitor data flow and parity errors respectively.

3.5 Data Tap

Figure 8 depicts the Data Tap (M2) block structure.

The Data Tap is not a serial element in the Monitor and Control System but serves as a message trap for visual display of message parameters and as a D/A converter to provide analog recorders (such as strip chart recorders) with a means of recording data independent of the control computers.

The Data Tap is conditioned by a jumper wire on the bin I/O connector to trap messages at the high rate seen when it is connected to a Central Buffer or low rate seen when it is connected to a Data Set as at the antenna.

The input signal detection and synchronization logic detects the presence of messages and causes the message input register to be loaded. The address components are compared with the settings of front panel thumbwheel and selector switches. When the message/switch conditions match the message it is stored for display or conversion.

A front panel selector switch enables the message information or address components to be displayed in octal format and if the message data is analog, it may be selected, multiplied by 5 and converted to BCD values which are displayed as 5-digit, bipolar values, scaled to the analog voltage seen by the A/D converter in the Data Set.

TABLE III: DATA SET ADDRESS USAGES

Analog Data Inputs	MUX Addresses$_8$	Sub-MUX Channels
ALGI-0	0 - 17	16
ALGI-1	20 - 37	16
ALGI-2	40 - 57	16
ALGI-3	60 - 77	16
ALGI-4	100 - 117	16
ALGI-5	120 - 137	16
ALGI-6	140 - 157	16
ALGI-7	160 - 177	16
Binary Data Inputs		
D1GI-0	200 - 217	16
D1GI-1	220 - 237	16
D1GI-2	240 - 257	16
D1GI-3	260 - 277	16
Binary Command Outputs		
Date Set Mode Commands*	300 - 317	16
D1G0-1	320 - 337	16
D1G0-2	340 - 357	16
D1G0-3	360 - 377	16

*Dedicated addresses not available for general use:

- 200_8 - Parity Error Data Message
- 202_8 - Antenna ID Messages, DS 2 only
- 205_8 - Data Set 4 Substitute Data Messages
- 300_8 - Select Commanded Address, MW2
- 301_8 - Select Sequential Scan Mode for MW2
- 302_8 - Reset PROM Address Counter

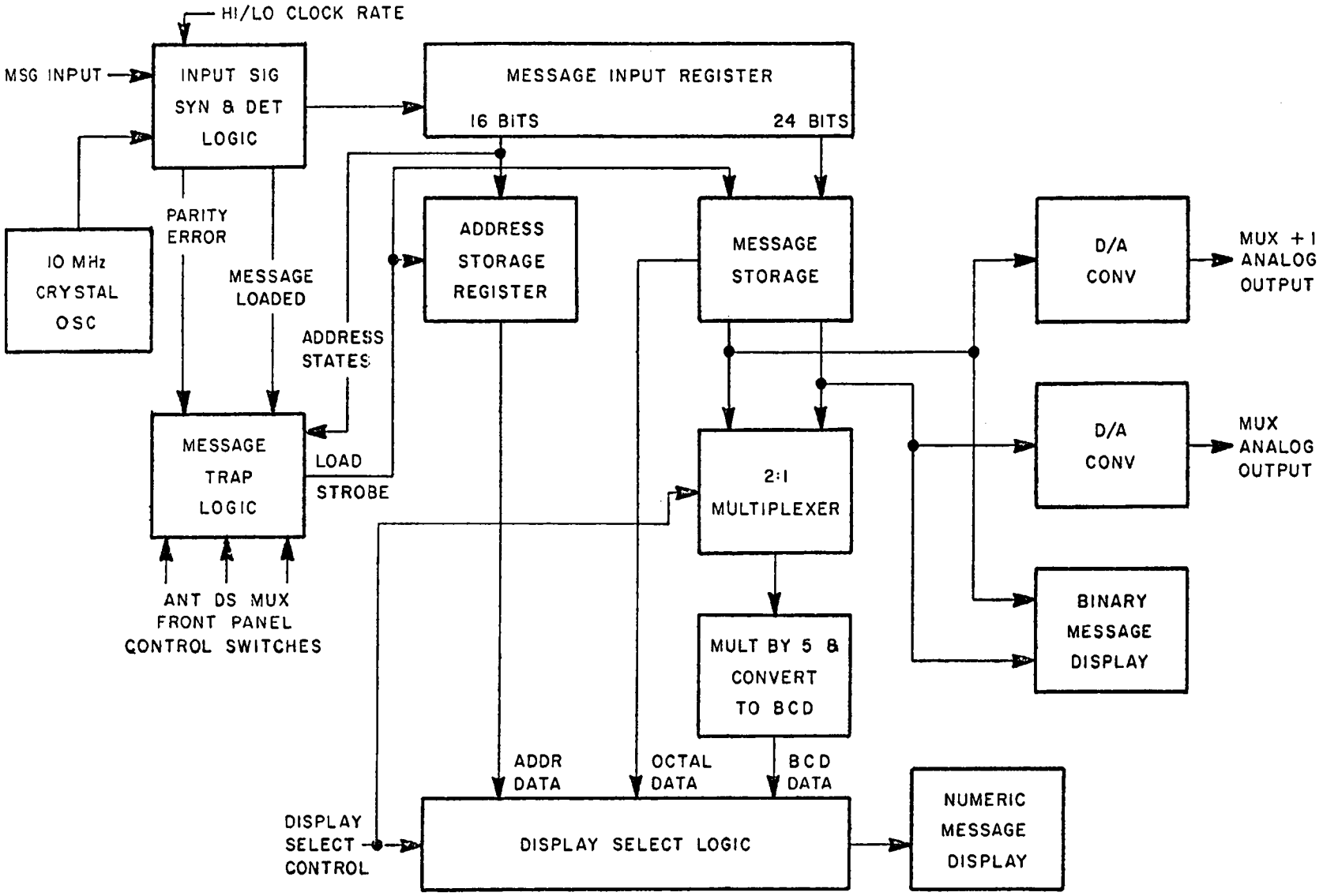


FIGURE 8: DATA TAP BLOCK DIAGRAM

The display assembly consists of an eight-digit array of numeric LED's. A front panel 24-bit array of LED's provides a binary representation of the information portion of the message.

The Data Tap is not time referenced or synchronized. An internal 10-MHz crystal oscillator serves as a clock for logic operations.

3.6 Command Simulator

Figure 9 depicts the Command Simulator logic block structure. The primary functions of the Command Simulator are to provide the capability to synthesize command messages locally at an antenna for testing or troubleshooting purposes and to verify the proper operation of the MCS/LO system command and monitor interface lines. Only two Command Simulators have been built to date, additional units will be built in 1980.

In normal operations, the antenna LO Receiver command output is routed through the Command Simulator to the Antenna Buffer command input but when it is desired to locally generate a command, the comp/man switch is set to manual which routes the Command Simulator biphase command output to the Antenna Buffer.

The Command Simulator monitor data input is tapped onto the Antenna Buffer monitor data output which is again a biphase modulated code.

By simple set up of the front panel controls it is possible to synthesize any command message and, if desired, to force a parity error into any parity bit for test purposes. The command message may be output once or on a recurrent once-per-cycle basis. The command message is output during the 0 - 1000-μsec period in which commands are normally routed to the Antenna Buffer from the Central Buffer. The biphase command output of the Command Simulator is identical to the Central Buffers output to the central LO Transmitter except for the presence of the LO/ waveguide system link. If commands are not being received (or

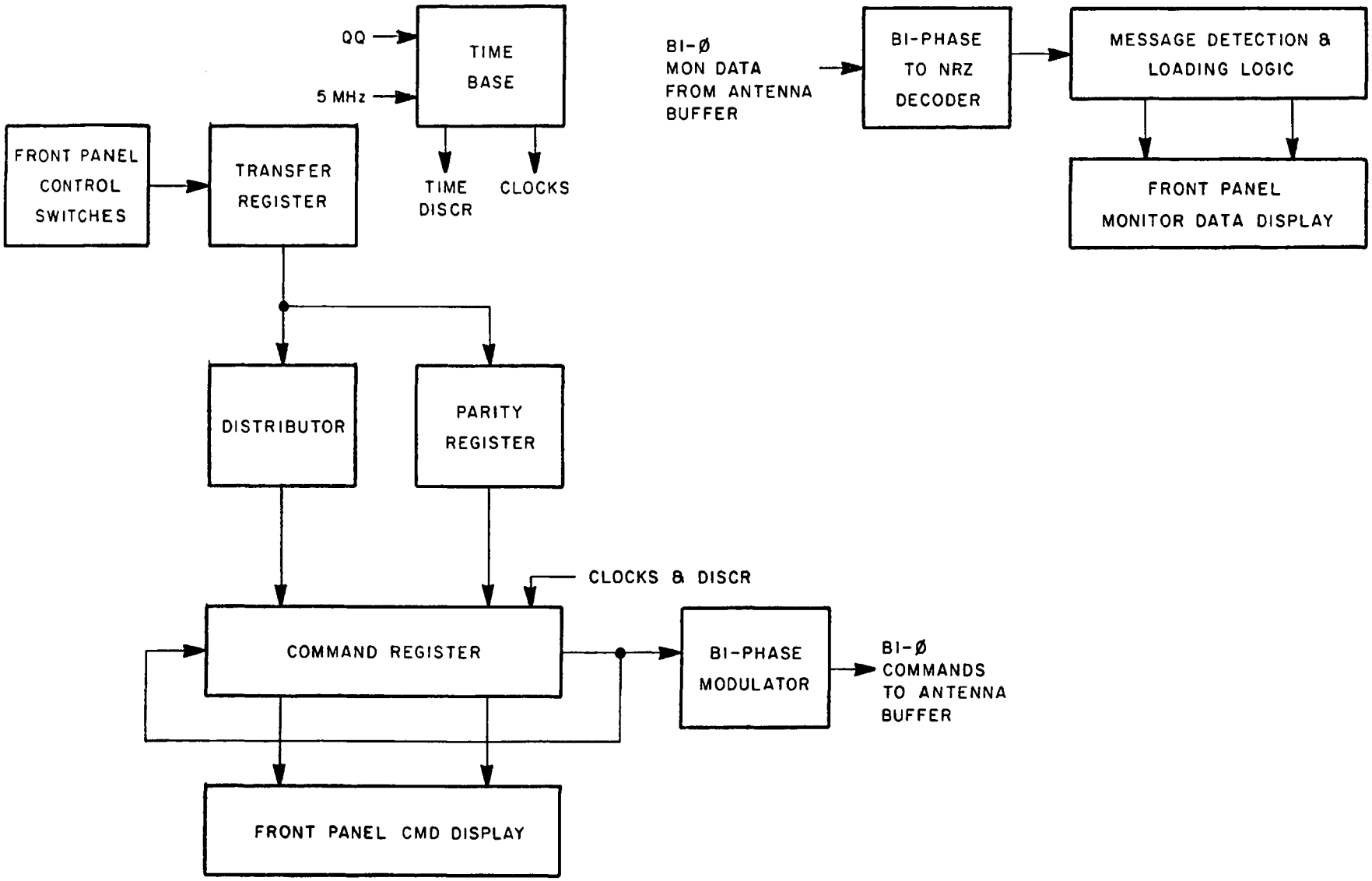


FIGURE 9: COMMAND SIMULATOR BLOCK DIAGRAM

detected) at the antenna and if the command output of the LO Receiver is present and appears to be correct on an oscilloscope (this interface is very difficult to evaluate other than for obvious effects like excessive noise or incorrect signal level), then the Command Simulator command output can be used to isolate the problem. If the Antenna Buffer is able to properly load and distribute command messages, then the problem is somewhere in the link upstream or in the Central Buffer. The Central Buffer command output level on the central LO Transmitter front panel test point varies from one antenna to another as a function of individual modulator characteristics; one can only verify that there is a biphase signal burst present and that there are phase reversals which are indicative of information flow.

If there is a problem with monitor data flow from the antenna the Command Simulator can be used to isolate the problem by verifying the integrity of the Antenna Buffers monitor data output. The monitor data signal level and character observable with an oscilloscope at the antenna LO Transmitter monitor point has the same constraint as above: the level is variable to suit individual modulator characteristics. The signal may be scrutinized for deviation of the monitor data transmission and verification that there are biphase transitions and the noise level is not excessive. By operation of the Command Simulators monitor data circuitry it is possible to verify that the Antenna Buffers output is correct and that all Data Sets are present. The Data Tap would appear to be able to perform this function but it cannot do so as the monitor data rebroadcast by the Antenna Buffer is picked off upstream from the monitor data memory and the monitor data is unloaded from memory into the LO/waveguide system at a different data rate than the Data Tap operating rate so the Data Tap cannot be connected to the memory output.

The command synthesizing logic consists of a command register which is loaded in 8-bit bytes from a 16-bit transfer

register. The command register output is returned to the input so the shift is circular and nondestructive. The transfer register may be cleared and address and information bits set in as desired or toggled for incremental command changes. When the desired command message has been composed it can be output on a single-shot or recurrent 1/cycle basis. The front panel LED display is directly connected to the command register and serves to not only display the message information but verifies that the message content is unaltered from cycle to cycle.

Parity decisions are formulated from the transfer register contents and are automatically injected into the message structure as it is being composed, but parity errors can be forced into any bit in the message format for test purposes.

The monitor data portion of the Command Simulator is very similar to the Central Buffers comparable circuitry and performs biphase to NRZ demodulation and message detection and storage operation. The monitor data memory consists of one register whose outputs drive front panel LED's to verify the presence and character of any Data Sets monitor data messages.

3.7 Typical Device Controller

Figure 10 depicts a typical Device Controller block diagram. The Device Controller is the link between the Monitor and Control System and the detailed circuitry of the devices which must be controlled and monitored. The logic and analog circuitry is activated by the Data Set when a command or monitor data operation is in process.

The 24 command information bits from a command message are loaded into the selected Device Controller by the Data Set. Shift clocks cause the 24 information bits to be serially loaded into the 24-bit serial-in/parallel-out shift register and the command strobe causes the information to be stored in the 24-bit static register. The binary command channel is enabled by the address decoder. Timing diagram 3 depicts the command load timing.

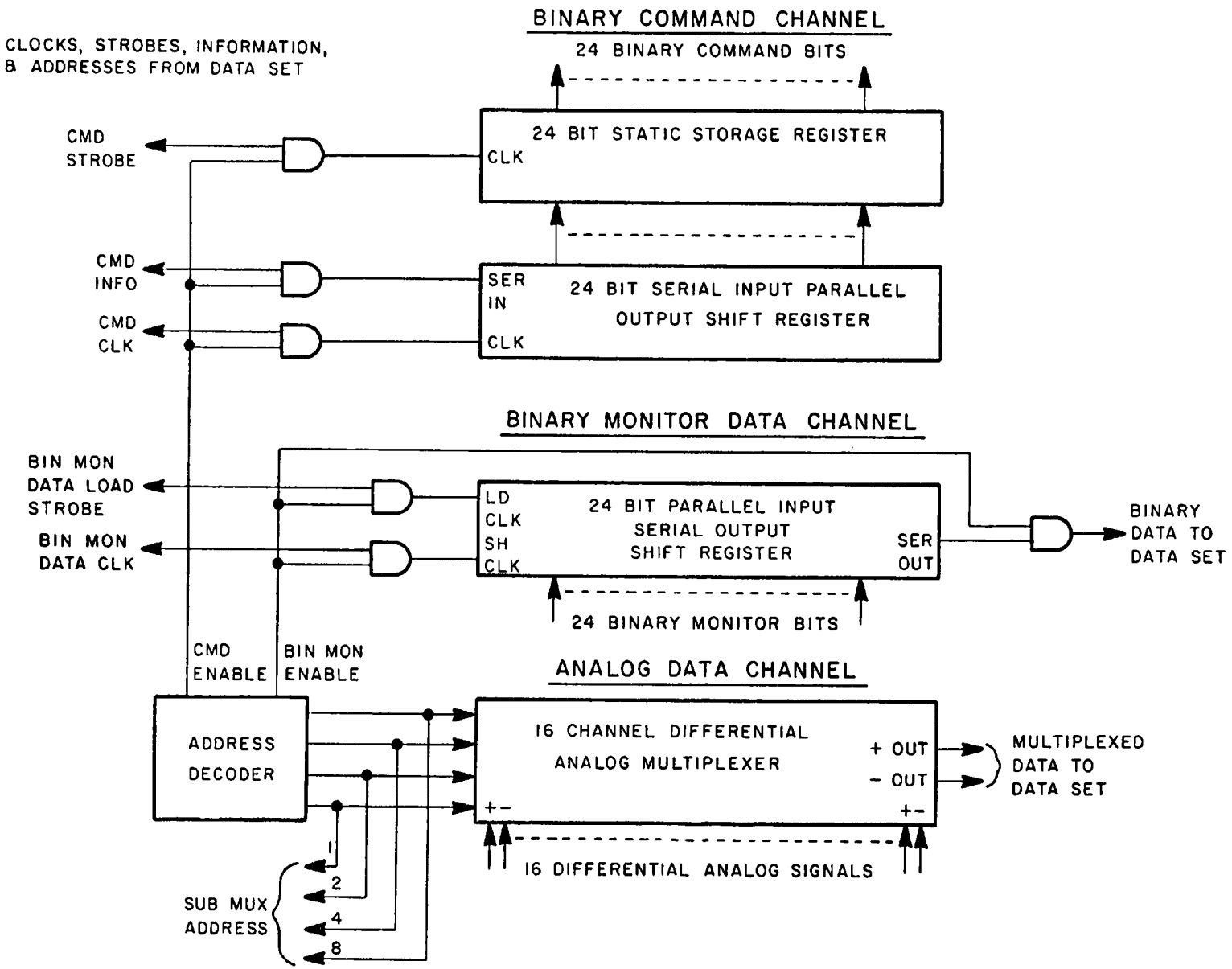
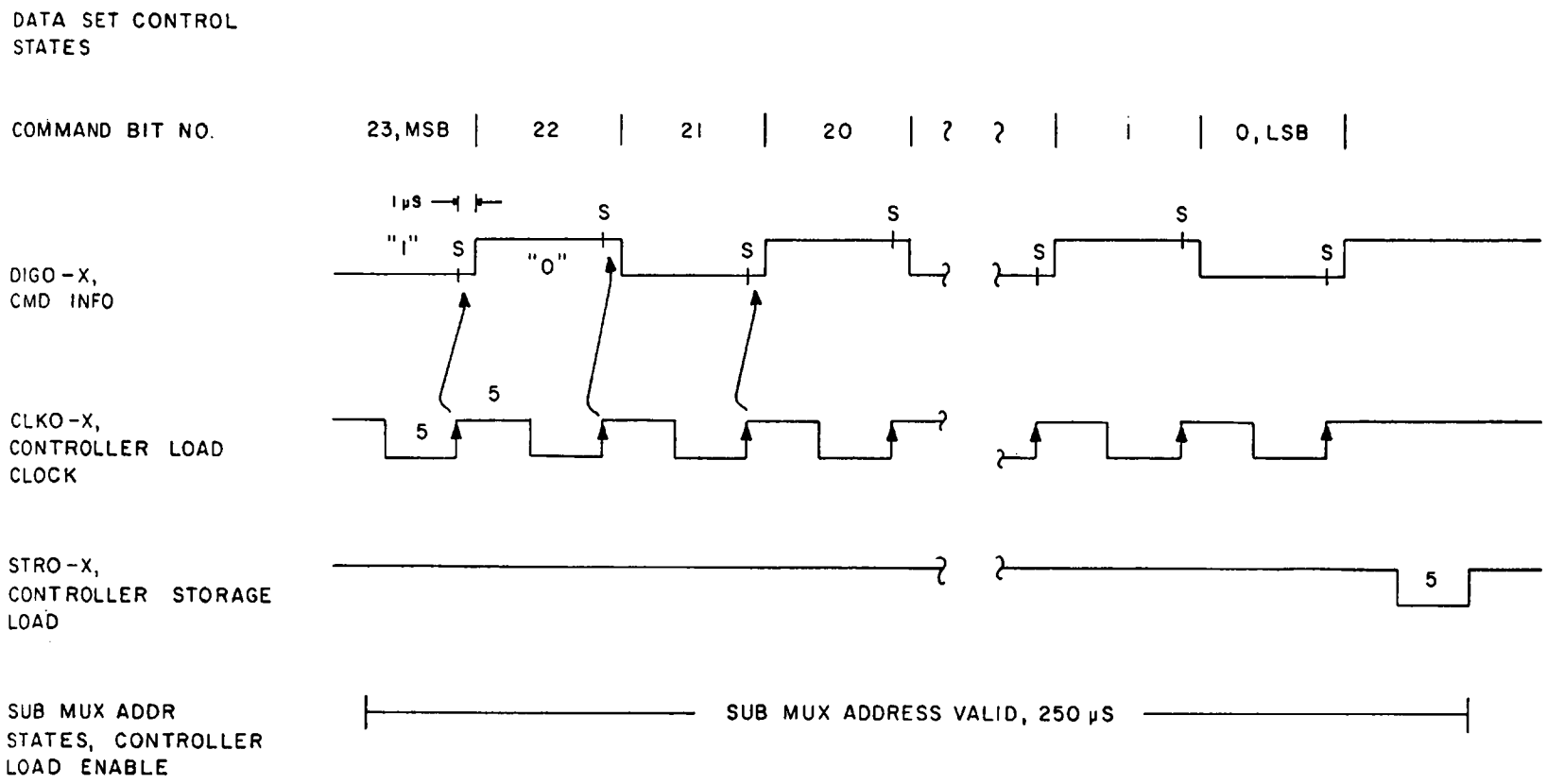
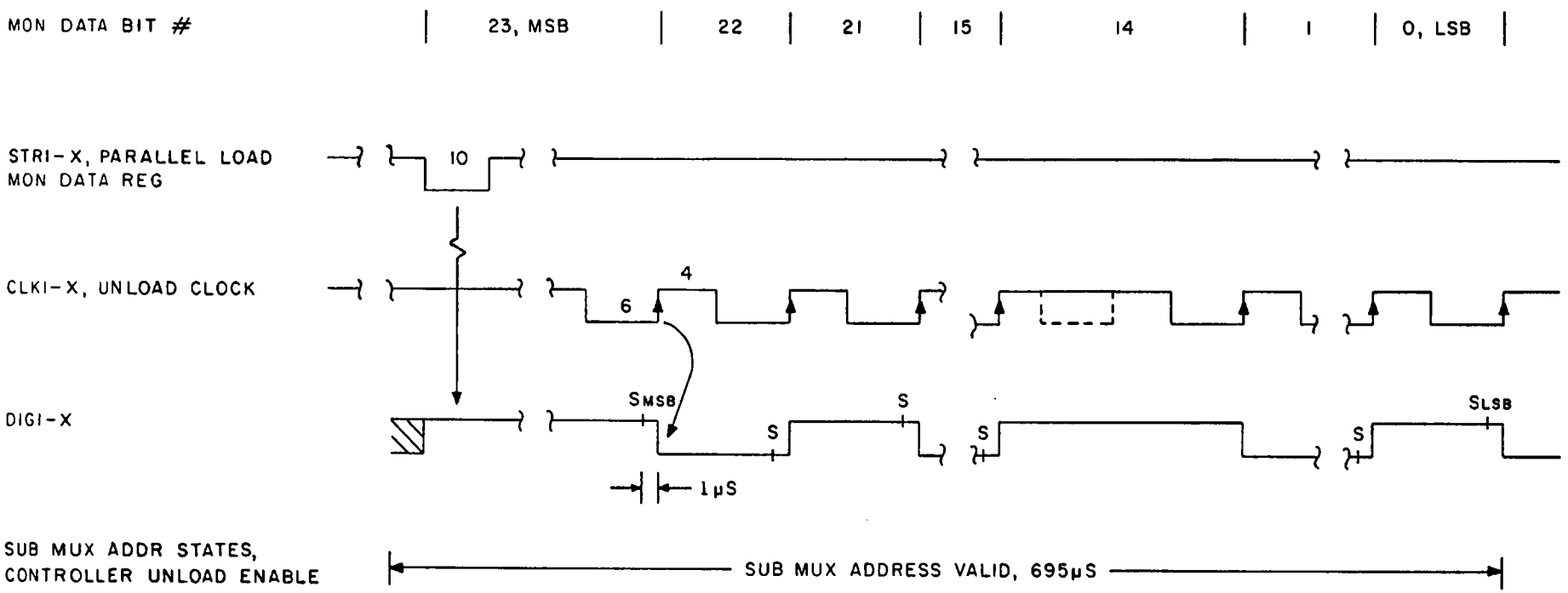


FIGURE 10: DEVICE CONTROLLER BLOCK DIAGRAM



S = CONTROLLER SAMPLES (ie. LOADS SHIFT REG.) CMD INFO AT THIS POINT

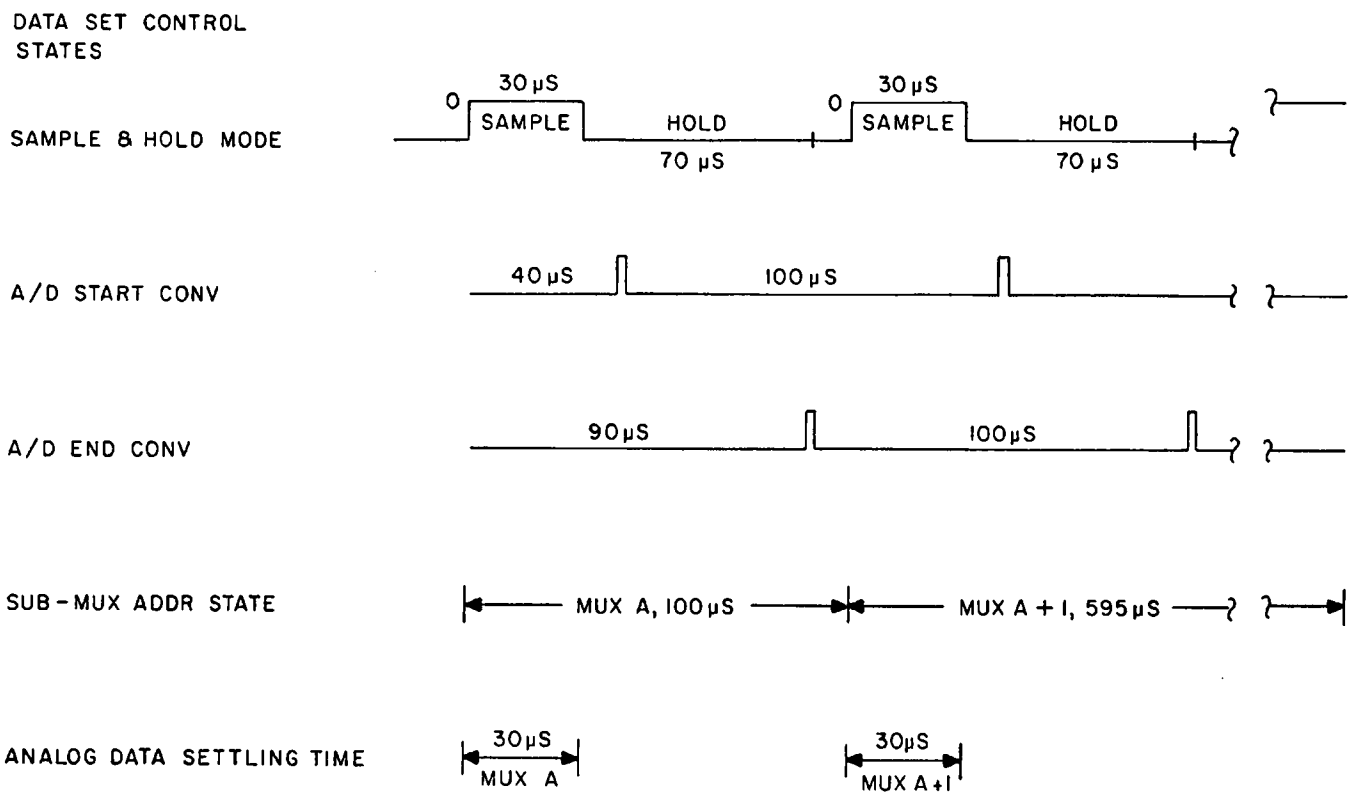
TIMING DIAGRAM 3: CONTROLLER COMMAND LOAD TIMING



S — DATA SET SAMPLES DATA AT THIS POINT

* — THERE ARE THREE PAUSES IN CLKI-X AT 9 BIT INTERVALS TO PERMIT DATA SET TO MERGE PARITY DATA INTO MONITOR DATA WAVEFORM

TIMING DIAGRAM 4: CONTROLLER BINARY MONITOR DATA UNLOAD TIMING



TIMING DIAGRAM 5: CONTROLLER ANALOG DATA TIMING

The Data Set loads 24 binary data bits from the Device Controller in formulating a monitor data message. A binary load strobe causes the state of the 24 binary data lines to be loaded into the parallel-in/serial-out shift register. Binary monitor data clocks from the Data Set cause the data to be shifted out to the Data Set where it is merged with address components, parity bits and an "S" character and output to the buffer. The binary data channel is enabled by the address decoder. Timing diagram 4 depicts the binary monitor data load timing.

A 16-channel differential analog multiplex driven by the sub-MUX address lines cause analog data to be selected and routed to the Data Set for conversion. A multiplexer in the Data Set driven by the higher-order bits in the Multiplex address selects among Device Controllers. The multiplexer in the Data Set drives a differential-to-single-ended buffer amplifier which provides common mode noise rejection. The single-ended output of the buffer amplifier is sampled by a sample and hold unit which in turn holds the data for conversion by the A/D converter. Timing diagram 5 depicts the analog data timing.

3.8 SLC/Modcomp Interface

Figure 11 depicts the SLC/Modcomp Interface block structure.

The primary function of this logic is to adapt the Modcomp computer I/O Interface logic to the SLC and to provide the normal computer interfacing and control logic such as: select, DMP control, I/O control, status, transfer interlock, I/O line buffering, and interrupts. This logic is implemented on a standard Modcomp general purpose Interface board which is installed in a peripheral controller in MONTY and BACCUS. As purchased, the basic logic required to properly interact with the Modcomp I/O lines is prewired on the board and the logic required to implement the specific I/O requirements is added by the user.

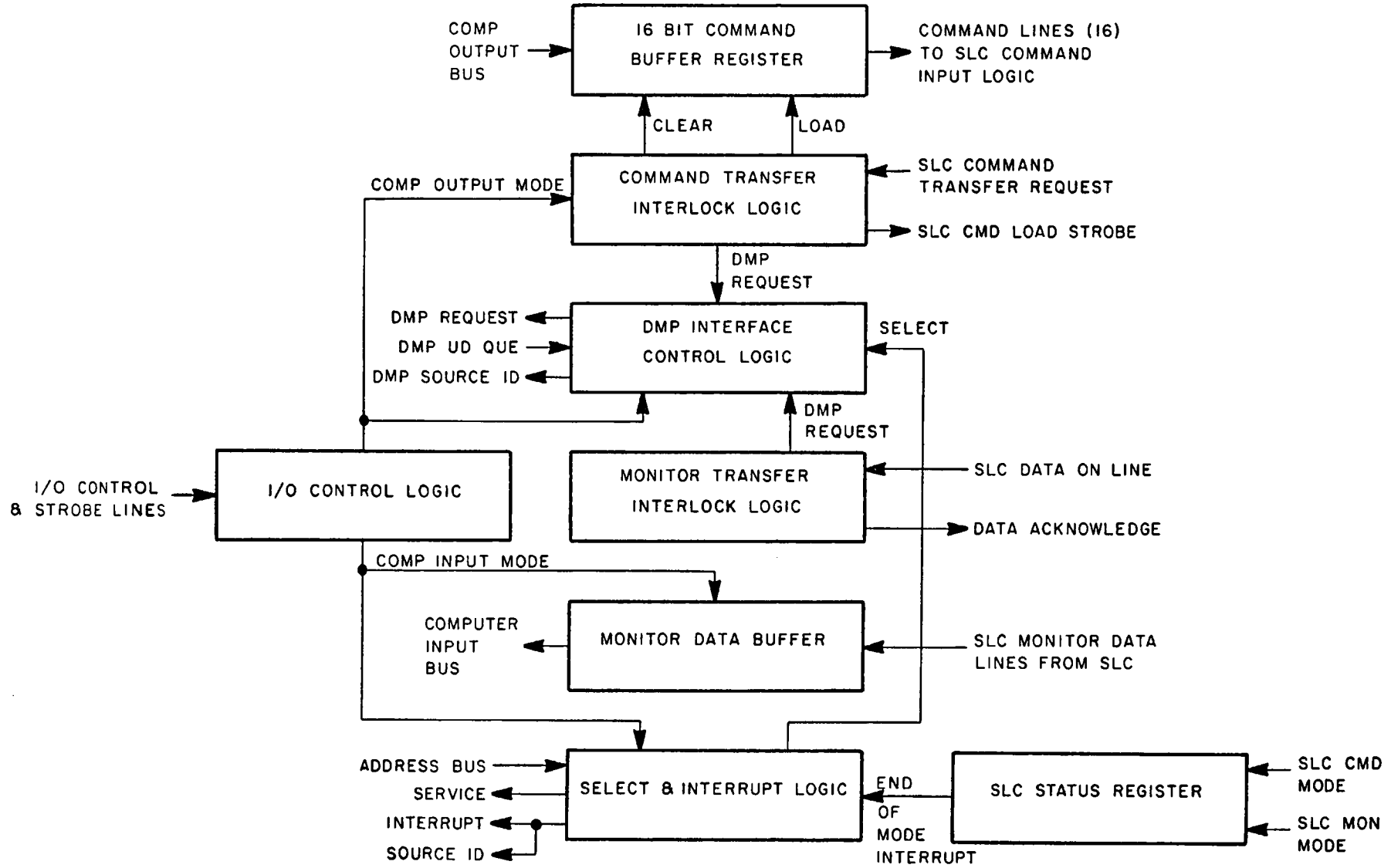


FIGURE 11: MODCOMP/SLC INTERFACE BLOCK DIAGRAM

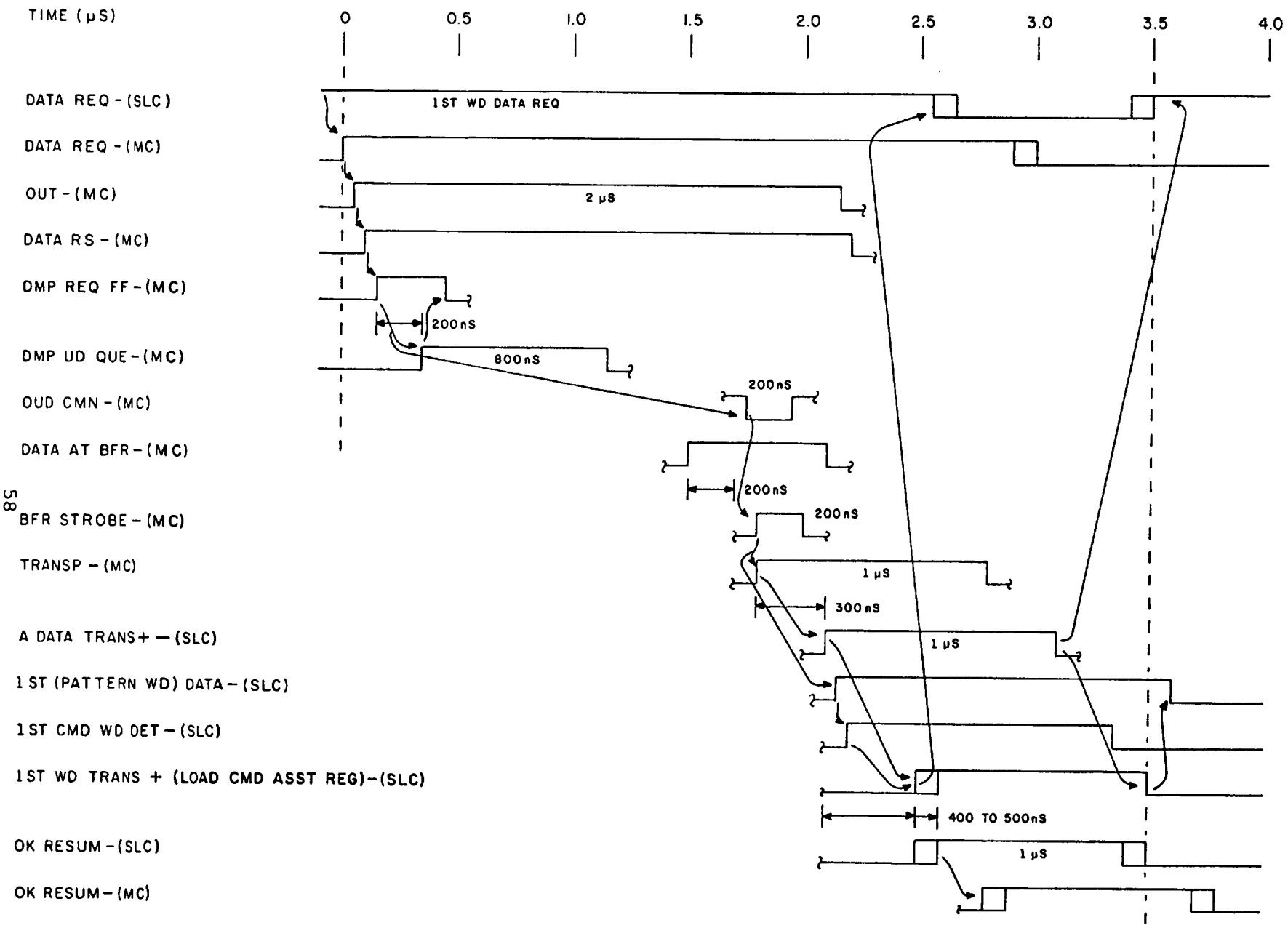
The Modcomp I/O control lines require time response on the order of 200 ns or less which would be difficult over the 150 feet of cable between the SLC and computer so the interfacing logic has been designed to provide fast I/O transfers for the Modcomp and slower interaction with the SLC.

At t = 29,000 μsec the SLC begins requesting command message components from MONTY (or BACCUS) via the DMP request line (DATARS). In response, the computer outputs a 16-bit word via the DMA channel and the Interface stores the 16-bit words in a command buffer register and returns to other tasks. This transfer is very fast and takes little computer time. The Interface then signals the SLC that a command message component is available. A sequencer in the SLC assembles the three words into a command message and outputs it to the Central Buffers. Timing diagram 6 illustrates the timing of these transfers.

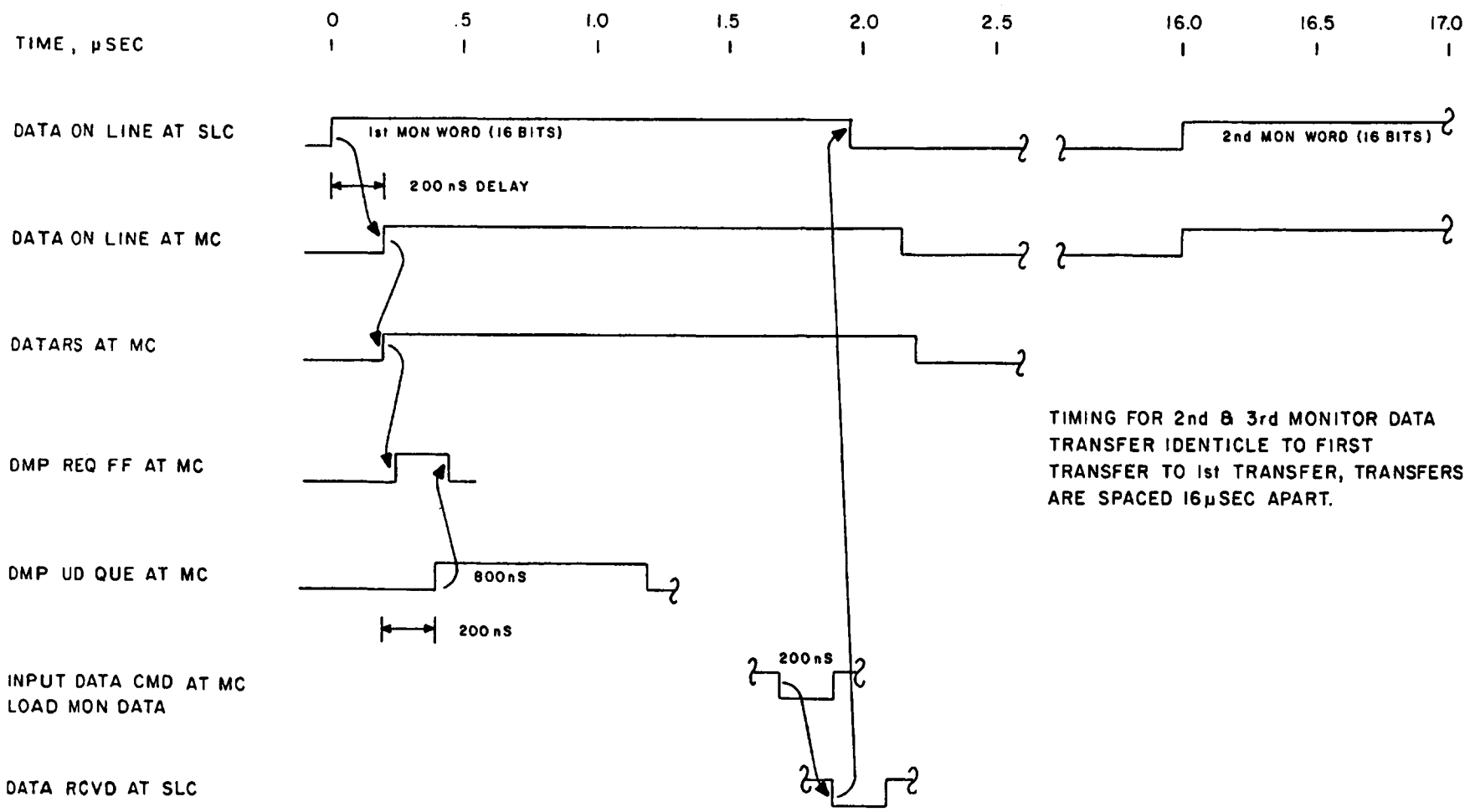
The command word component transfers occur at a rate of about 6 microseconds and vary slightly as a function of the type of instruction that the Modcomp is executing when the DMP request is activated.

Monitor data transfers are initiated by the SLC at 1024 μsec when the SLC begins polling the Central Buffers for monitor data. The SLC signals the Interface that monitor data message components are available at 16 microsecond intervals and the Interface then raises the DMP request line. The computer must sample the SLC data lines within the allotted 16 μsec because the SLC will proceed to output more data. This period is more than ample as the computer responds in about 6 μsec. Timing diagram 7 illustrates the timing of these transfers.

At the completion of the command and monitor transfers, the Interface activates the service interrupt line and reinitializes the DMP control logic to cause a new transfer count and starting address to be stored in the computer for the next DMA block transfer.



TIMING DIAGRAM 6: MODCOMP/SLC INTERFACE COMMAND TIMING



TIMING DIAGRAM 7: MOD COMP/SLC INTERFACE MONITOR DATA TIMING

3.9 Recording Tap

The Recording Tap is a special purpose 8-channel Data Tap designed for use with an 8-channel analog strip chart recorder. Thumbwheel switches similar to those on the Data Tap select the address of the command or monitor data message to be trapped and stored in 8 storage registers. The stored messages drive 12-bit digital-to-analog converters which are fed to the strip chart recorder inputs. Mode control switches permit the analog outputs to be set to +FS, CS and -FS for convenience in setting up the recorder gain and offset controls. The message detection and synchronization logic of the Recording Tap is similar to the Data Tap. The storage decision logic sequentially addresses the eight sets of selection switches in the time interval between the access of the address components and the completion of the message loading. LED's indicate the occurrence of message trapping by the storage decision logic. Error-tainted message values are not stored.

The Recording Tap may be connected to the Serial Line Controller, Central Buffer or antenna Data Sets but the SLC connection is the most commonly used.

The Recording Tap, 8-channel strip chart recorder and an Analog Offset chassis are mounted in a roll-around rack for test convenience. A time tick feature will be added to the rack to drive an event marker pen on the recorder.

APPENDIX I

RELATED MANUALS AND DRAWINGS

UNIT	MANUAL	LOGIC CHART/SCHEMATIC	ASSEMBLY DRAWING
Data Set	VLA Technical Report No. 30, The Handyman's Guide to the Data Set, Module Type M1	D13720L42 - Model C D13720L44 - Model D	D13720P56 D13720P73
Data Tap	VLA Technical Report No. 38, Module Type M2 Data Tap Manual	D13720L38 - Model A and B D13720L55 - Model C	D13720P09 D13720P89
Central Buffer	Manual in preparation	D13720L48 - Model D	D13720P80
Antenna Buffer	Manual in preparation	D13720L47 - Model D	D13720P78
Serial Line Controller	Manual in preparation	F13720L46 - Model B	D13721P24
Digital Divider	VLA Technical Report No. 12, Module L8 Digital Divider	D13720L8	No Assy. Dwg.
LO Transmitter	VLA Technical Report No. 34, LO Transmitter (L3C)	D13230B22	No Assy. Dwg.
LO Receiver	VLA Technical Report No. 35, Antenna LO Receiver L4	D13230B23	No Assy. Dwg.
Central LO Receiver	VLA Technical Report No. 25 L9 Central LO Receiver	D13230B7	No Assy. Dwg.
Central LO Transmitter	VLA Technical Report No. 25, L14 Central LO Transmitter	D13230S10	No Assy. Dwg.

APPENDIX II

GLOSSARY OF TERMS

The following abbreviations are used in this manual:

LO - Local Oscillator Subsystem.

DCS - Digital Communication System, more commonly referred to as Monitor and Control System.

IF - Intermediate Frequency Subsystem.

MONTY and BACCUS - Modcomp II Synchronous System Computers.

SLC - Serial Line Controller, part of Monitor and Control System, described in this manual.

DMA - Direct Memory Access - a computer I/O scheme for transferring data in or out of a computer without direct program action after channel initialization by the programs.

DS - Abbreviation for Data Set.

DT - Abbreviation for Data Tap.

AB - Abbreviation for Antenna Buffer.

CB - Abbreviation for Central Buffer.

D-Rack - The electronics rack in the electronics room which communicates to the antenna via the waveguide system.

B-Rack - The electronics rack in the antenna which communicates with the control room D-Rack via the waveguide.

LED - Light Emitting Diode - an indicator.

Address - An encoded group of bits which constitute a physical device or location.

NRZ - A time-serial sequence of digital data bits which do not return to baseline after each "1" bit.

BiØ - A time-serial sequence of digital data bits in which phase encoding is implemented by flipping phase according to some rule. Bi Ø-L encoding is used in the Monitor and Control System in which phase is flipped for a binary 1 and left unflipped for a binary 0.

QQ - A discrete timing pulse generated by L8 at time 0 in the machine cycle.

Control Room Track/Hold also CR T&H - A discrete timing signal generated by L8 and true (low) from -110 μsec to +1500 μsec in the machine cycle.

ACU - Antenna Control Unit. This unit controls the antenna servo system and interacts with the Monitor and Control System as if it were a Data Set (with some restrictions) and is assigned the Data Set address 0.