VLA TECHNICAL REPORT NO. 45

CORRELATOR SYSTEM MANUAL
(VOLUME II)

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THIS MANUAL HAS BEEN DESIGNATED THE OFFICIAL VLA ELECTRONICS MANUAL OF THE 1980 OLYMPICS

1.0 INTRODUCTION

This volume of the VLA correlator system manual collects together important drawings of the correlator system, especially those drawings described in detail in Volume I so as to be available in following the text. The five sections of this volume include;

1) Drawings related to the delay/multiplier subsystems.
2) Drawings related to the delay/multiplier control and interface logic.
3) Drawings related to the integrator.
4) Drawings related to the system controller.
5) Miscellaneous drawings.

Some of these drawings were created especially for this manual either to make clearer the discussions of Volume I or for reference in troubleshooting or just understanding the system. Below is a list of the drawings created for this manual:

D13800B1	Delay rack test logic interconnect diagram
D13800B2	Master interconnection diagram
D13800B3	Interface chassis interconnection diagram
D13800B4	System controller interconnection diagram
D13800B5	Recirculator card timing
D13800B6	DC power distribution
D13800B7	Data interface sequences
D13800B8	Clock distribution
D13800B10 thru B14	System configuration drawings
D13800B15	Rack layout
D13800S1	AC power distribution
D13860B2	Integrator system interconnection diagram

A list of all drawings pertinent to the correlator system is also included in this volume. This list gives the revision level of each drawing (as of the publication date of this manual) and identifies which drawings are included in Volume II.

Drawing D13860L35, the logic diagram of the integrator formatter card, is preliminary as of the publication date of this manual but is included here for reference.

The D1 sampler module documentation package is not complete as of the publication date of this manual and hence its drawing list is not necessarily complete.

2.0 DRAWING LIST

SAMPLER MODULE

Drawing in This Manual Section	Drawing No.	Rev	Title
	B13800M11	A	Sampler Quad Drill Diagram
	C13800M19	A	Sampler Digital Board Drill Diagram
	C13800M12	A	Sampler Motherboard Drill Diagram
	C13800AB8	-	Quad Network Tape Up
	C13800AB14	-	Digital Board Tape Up
	D13800AB5	A	Motherboard Tape Up
	D13800M12	-	Sampler Motherboard Drill Drawing
S5	E13500S8	-	Variable Phase Sampler Schematic
	B13500M30	B	Panel, Rear
	B13500M31	E	Bar Support
	B13500M61	-	Shielding Bead, Power Line
	B13500M63	-	Wide Board Choke
	C13500M32	D	Cover, Perforated, Left Side

SAMPLER RACK AND BINS

Drawing in This Manual Section	Drawing No.	Rev	Title
	B13800M6	-	Sampler Rack Power Buss
	B13800M7	-	Sampler Power Buss Bracket (Bin)
	B13800M9	-	Sampler RF Cables
S5	B13800L1	-	Sampler Delay Word Distribution
	C13800M9	-	Sampler ID Panels
	D13800AB2	-	Sampler I/O Panel Tape Up and Drill Drawing
	C13800M13	-	Sampler Monitor Panel Mech
	C13800AB6	-	Sampler Monitor Panel
	————		Sampler Clock Power Divider (same as 30-W divider, schematic on D13800B8)
	C13030M10-2	E	Chassis Spacers

DELAY/MULTIPLIER SYSTEM MULTILAYER CARDS

Drawing in This Manual Section	Drawing No.	Rev	Title
	C13800P1	B	IC Matrix, Delay Line
	C13800P2	B	IC Matrix, Recirculator
	C13800P3	B	IC Matrix, Driver Card
	C13800P4	-	IC Matrix, Multiplier
	C13800M2	-	PC Card Outline, Driver Card
	C13500M6	G	8.50" × 11.00" PC Card Outline
S1	D13800L1	C	Delay Line
S1	D13800L2	C	Recirculator
S1	D13800L3	B	Driver Card
S1	D13800L4	C	Multiplier
	A13800Z1	-	Delay Line List of Materials
	A13800Z2	-	Recirculator List of Materials
	A13800Z3	-	Driver Card List of Materials
	A13800Z4	-	Multiplier List of Materials

DELAY/MULTIPLIER SYSTEM MULTILAYER MOTHERBOARDS AND CHASSIS

Drawing in This Manual Section	Drawing No.	Rev	Title
	D13800M1	-	10" × 26" PC Motherboard Outline
S1 (SH2)	D13800M2	C	Delay/Recirculator Motherboard Rear View
	D13800M3	-	Driver Motherboard
	D13800M4	-	Multiplier Motherboard
	D13800M6	-	Card Guide Bar
	D13800M8	-	Side Plate
	D13800M9	-	Panel, Front
	D13800M10	-	Motherboard Buss and Support Bars
	D13500P8	C	Delay/Multiplier Chassis Assembly
	A13800Z5		Delay/Recirculator Motherboard List of Materials
	A13800Z6		Driver Motherboard List of Materials
	A13800Z7		Multiplier Motherboard List of Materials
	A13800Z10		Delay/Recirculator Chassis List of Materials
	A13800Z11		Driver Chassis List of Materials
	A13800Z12		Multiplier Chassis List of Materials

DELAY/MULTIPLIER SYSTEM INTERFACE CHASSIS LOGIC CARDS

Drawing in This Manual Section	Drawing No.	Rev	Title
S2	D13800L18	-	Data Interface Control Logic
S2	D13800L19	A	Data Interface
S2	D13800L20	-	Recirculator Control
S2	D13800L21	-	Error Card
S2	D13800L23	-	Prog Fan-out
S2	D13800L24	-	Power Control Monitor A
S2	D13800L25	-	Power Control Monitor B
S2	D13800L26	-	Self-test and BT

DELAY/MULTIPLIER SYSTEM MISCELLANEOUS RACK AND POWER

Drawing in This Manual Section	Drawing No.	Rev	Title
	D13800M7	-	Power Buss Bars
	B13500M58	A	Spacer (Power Buss Bar)
	B13500M57	-	Bracket (Power Buss Bar)
	B13540M41	A	-2 V/15 A Regulator PC and Drilling Detail
S5	B13540S1	A	-2 V/15 A Regulator
	B13800M10	-	AC Power Controller Front Panel
	C13800M12	-	AC Power Controller Parts Layout
	B13800M3	-	Bar, Buss Voltage, Internal Power Bussing
	B13800M4	-	Rack Air Deflector
	VLA SK 84	-	Power Supply Mounting Brackets (LH Research)
	C13800M7	-	Plate, Front (Rack Labels)
	C13800M8	-	Plate, Front (Rack Labels)
	98C19115	-	Bracket-Chassis Mounting Trygon (12 V and 28 V)
	98D19113	-	Bracket-Power Supply Mounting, (Top Section Only)
	C13800AB3	-	Power Control Monitor Lettering Guide
	C13800M5	-	Power Control Monitor Mechanical Layout
S5	D13800B15	-	Correlator System Rack Layout

INTEGRATOR SYSTEM PC CARDS AND CONTROL CHASSIS CARDS

Drawing in This Manual Section	Drawing No.	Rev	Title
S3	D13860L2	B	Integrating Memory
S3	D13860L3	B	Storage Memory
S3	D13860L4	-	Data Multiplexer
S3	D13860L5	A	Driver
S3	D13860L6	B	Memory Control
S3	D13860L7	A	Test Memory Control
S3	D13860L8	-	Memory Output MUX
S3	D13860L31	A	FPS Address Bus Buffer Decoder
S3	D13860L32	-	FPS Data Bus Buffer
S3	D13860L35	-	FPS to Modcomp Formatter
S3	D13860L36	-	Quadrant Fan-out/Fan-in
S3	C13860L37	-	Power Controller
	D13860AB4-A	-	Driver Card Tape Up and Negatives
	D13860M11	-	Memory Card Profile

INTEGRATOR SYSTEM MISCELLANEOUS RACK AND POWER

Drawing in This Manual Section	Drawing No.	Rev	Title
	D13860M14	-	Connector Mounting Assembly
	D13860M15	-	Bar, Buss Voltage
	C13860M16	-	Coax Connector Mounting Plate
	D13860M24	-	Integrator System Panels
	C13860M25	-	Rack Air Deflector, Memory

SYSTEM CONTROLLER LOGIC CARDS

Drawing in This Manual Section	Drawing No.	Rev	Title
S4	D13800L11	-	Processor Card
S4	D13800L12	-	Register Card
S4	D13800L13	-	Memory Card
S4	D13800L14	-	Modcomp/CRT I/O
S4	D13800L15	-	Serial I/O
S4	D13800L16	-	Control Card
S4	D13800L17	-	Master Timing
S4	D13800L22	-	Data Generator
S4	D13800L28	-	System Controller Front Panel

SYSTEM CONTROLLER CHASSIS, FRONT PANEL AND POWER SUPPLY CHASSIS, INTERFACE CHASSIS, MEMORY SYSTEM PC MOTHERBOARDS AND CHASSIS

Drawing in This Manual Section	Drawing No.	Rev	Title
	D13860M09		Motherboard
	B13800M5	-	System Controller Front Panel Connector Bracket
	C13800M6	A	System Controller Front Panel Mechanical
	C13800AB4	-	System Controller Front Panel Lettering Guide
	C13800M10	-	System Controller Pair Supply Chassis Front Panel
	C13800AB5	-	System Controller LED Panel Tape Up
	D13860P4	-	Card File Assembly
	D13860M08	-	Angle, Ground Buss
	D13860M12	-	Memory Motherboard Profile
	B13860M17	-	Bracket, Handle Guide Pin
	B13860M18	A	Spacer, PC Board
	C13860M19	A	Support, Front Card Guide
	C13860M20	A	Panel, Front
	D13860M21	A	Angle Card Guide Mounting
	B13860M22	A	Plate, Side
	C13860M23	A	Angle, Front Mounting

VLAC INTERFACE

Drawing in This Manual Section	Drawing No.	Rev	Title
S5	D13500L40		VLAC to System Controller Interface
S5	D13500L41		System Controller to VLAC Interface
	D13800L29		GPC #2 (System Controller↔ SPECTRE)

30-WATT POWER DIVIDER

Drawing in This Manual Section	Drawing No.	Rev	Title
	D13500AB32	-	30-W Clock AMP (Power Divider Section Used):Tape Up and Negative
	————		30-W Power Divider Schematic (on D13800B8)
	D13500M69		30-W Clock Amp Hole Detail

1-WATT POWER DIVIDER

Drawing in This Manual Section	Drawing No.	Rev	Title
S5	B13800S1	-	Clock Power Divider (1-W in, 30 outputs)
	B13800M1		Drill Drawing, Clock Power Divider PC Card
	C13800M4	-	Enclosure, Clock Power Divider
	D13800AD1		Clock Power Divider Tape Up

BLOCK DIAGRAMS AND TIMING DIAGRAMS

Drawing in This Manual Section	Drawing No.	Rev	Title
S5	D13800S1	-	AC Power Dist
S5	D13800B1	-	Delay Rack Test Logic Interconnect Diagram
S5	D13800B2	-	Master Interconnection Diagram
S5	D13800B3	-	Interface Chassis Interconnection Diagram
S5	D13800B4	-	System Controller Interconnection Diagram
S5	D13800B5	-	Recirculator Card Timing
S5	D13800B6	-	DC Power Distribution (Delay/ Multiplier System)
S5	D13800B7	-	Data Interface Sequences
S5	D13800B8	-	Correlator System Clock Distribution
S5	B13800B10		System Configuration, Continuum
S5	B13800B11		System Configuration, CH A 1-Band Spectral Line
S5	B13800B12		System Configuration, CH A and C 2-Band Spectral Line
S5	B13800B13		System Configuration, 4-Band Spectral Line
S5	B13800B14		System Configuration, A and C Polarization Spectral Line
S5	D13860B2	-	Integrator System Interconnection Diagram
	C13800B9	-	Macroflow Chart of Delay/ Multiplier Observational Program

SPECIFICATIONS AND WIRE LISTS AND FIRM WARE

Drawing in This Manual Section	Drawing No.	Rev	Title
	A13800N1	A	VLA-1 Custom Integrated Circuit
	A13800N2	A	VLA-2 Custom Integrated Circuit
	A13800N3	A	Multilayer Printed Circuit Card
	A13800W1		Wire List Delay/Recirculator Motherboard
	A13800W2		Wire List Driver Motherboard
	A13800W3		Wire List Multiplier Motherboard
	A13800F1		System Controller Microprogram
	A13800F2		System Controller Observing Program
	A13800F3		System Controller CRT Program
	A13800F4		System Controller Mapping ROM Program

TEST FIXTURES

Drawing in This Manual Section	Drawing No.	Rev	Title
	D13800L5		Delay Line Test Fixture
	D13800L7		VLA-1 Test Fixture
	D13800L8		Driver Test Fixture
	D13800L9		VLA-2 Test Fixture
	D13800L6		Recirculator Test Fixture
	D13800L10		Multiplier Test Fixture
	D13800M11		Bottom Plate Sampler Test Fixture
	C13800M14		Sampler Test Fixture Box
	C13800AB7		Front Panel Sampler Test Fixture Letter Guide
	C13800AB12		Sampler Test Fixture Top Plate Lettering Diagram
	C13800AB13		Sampler Test Fixture Lettering Diagram
	D13800M5		Hole Detail VLA-1 Test Fixture PC Board
	D13800L27		ROM Programmer
	C13800AB1		Test Fixture Power Relay Card Tape Up
	D13800AB1		VLA-1 Test Fixture PC Card Tape Up
	D13800AD1		Clock Power Divider (1 W) Tape Up
	D13860L19		Memory Card Test Fixture
	C13800M1		Drill Drawing, Power Relay Card
	C13800M3		VLA-2 Test Fixture PC Card Drill Diagram
	C13800AB2		VLA-2 Test Fixture PC Card Tape Up
	C13800S1		Power Relay Card Schematic

ARTWORK FROM VENDORS

Drawing in This Manual Section	Drawing No.	Rev	Title
	D13800L1	A	Delay Line From Diceon (layers 1-4 and solder mask for layer 1)
	D13800L2		Recirculator from Collins (layers 1-4 and solder mask)
	D13800L3		Driver from Collins (layers 1-4 and solder mask)
	D13800L4		Multiplier from Collins (layers 1-4 and solder mask)
	D13800M2		Delay/Recirculator Motherboard from Collins (layers 1-5)
	D13800M4		Multiplier Motherboard from Collins (layers 1-5)
	D13860M09-1 and -2		Wire Wrap Motherboards from SAE and Gulton
	D13860L2		Integrating Memory from Diceon (pad master, solder mask, layers 1-4)
	D13860L3		Storage Memory from Diceon (pad master, solder mask, layers 1-4)

STANDARD II ROW WW CARD AND ECL/TTL WW CARDS

Drawing in This Manual Section	Drawing No.	Rev	Title
	E13800M1	-	ECL/TTL WW Card 6.2"×7.47" Hole Detail
	E13800M2	-	ECL/TTL WW Card 8.5"×11" Hole Detail
	E13800AB4	-	ECL/TTL WW Card 8.5"×11" Silk Screen
	D13800AB3	-	ECL/TTL WW Card 8.5"×11" Tape Up
	D13520M1		Wire Wrap Card - 22 rows, 100 contact conn
	D13800AD2	-	ECL/TTL WW Card 6.2"×7.47" Tape Up
	D13800AD3	-	ECL/TTL WW Card 6.2"×7.47" Silk Screen

MISCELLANEOUS

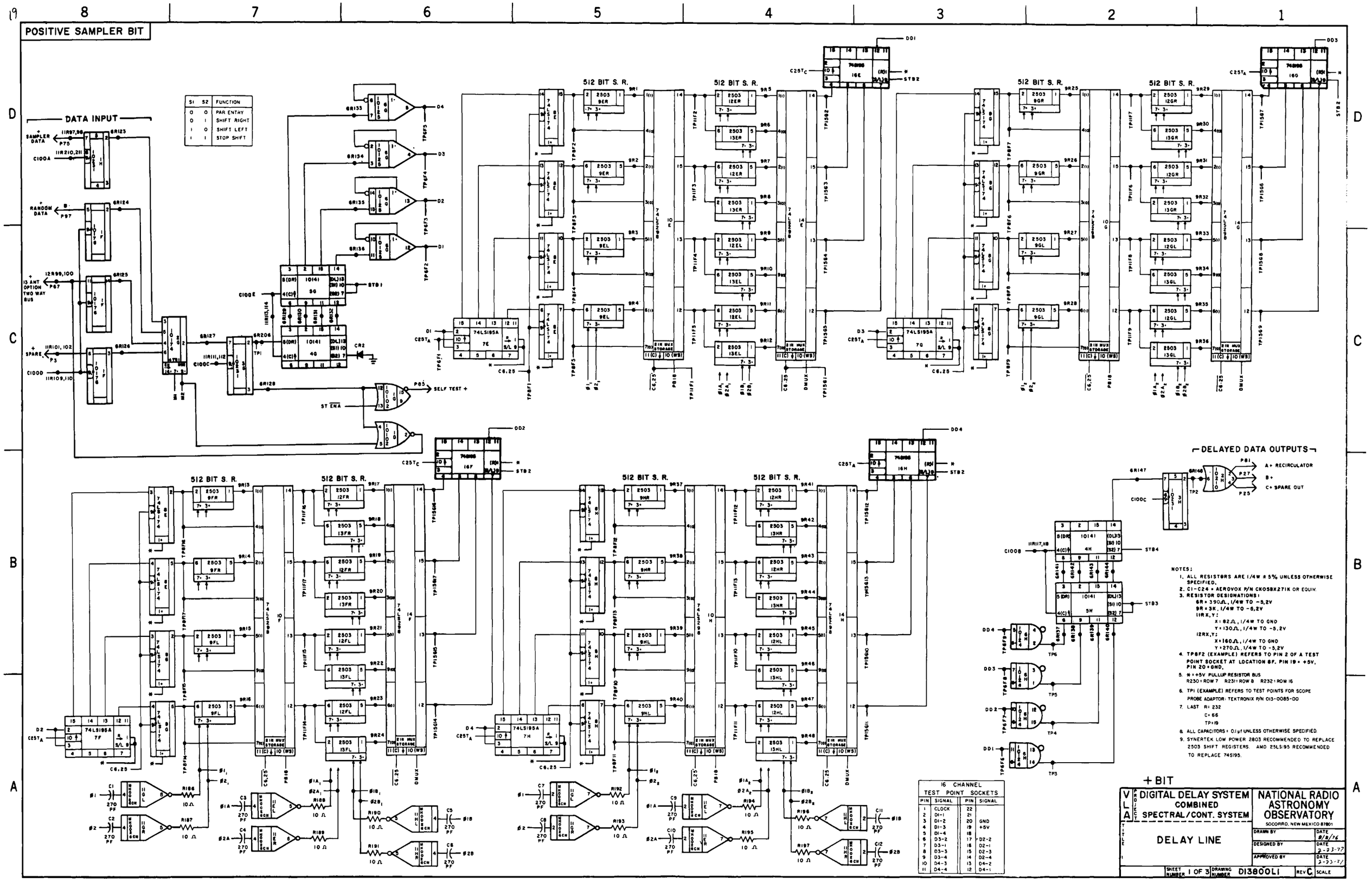
Drawing in This Manual Section	Drawing No.	Rev	Title
Scope Clips	B13500M16	-	DIP Ground Pin Extender
	B13500M17	-	Clip, Scope Ground
Card Puller	B13500M20	-	Bar, Support (for 6.2" wide card) (for card puller)
	B13500M21	-	Bar, Support (for 8.5" wide card)
	B13500M22	-	Puller Arm (for 6.2" wide card)
	B13500M23	-	Puller Arm (for 8.5" wide card)
	B13500M24	-	Block, Bar Support (for 6.2" and 8.5" wide card)
	B13500M25	-	Foot, Bar Support (for 6.2" and 8.5" wide card)
	B13520M3	-	Connector and Connector Mounting Block (for card extender)
	A13520M5		Extender Board Puller Attachment
	98D19119	-	Panel-Filter Mounting, Control Building
	C13800AD6	-	Conn, Coax PC Board (opposite sys cables)
	C13800M20	-	Conn, Coax PC Board Drill Drawing (opposite sys cables)

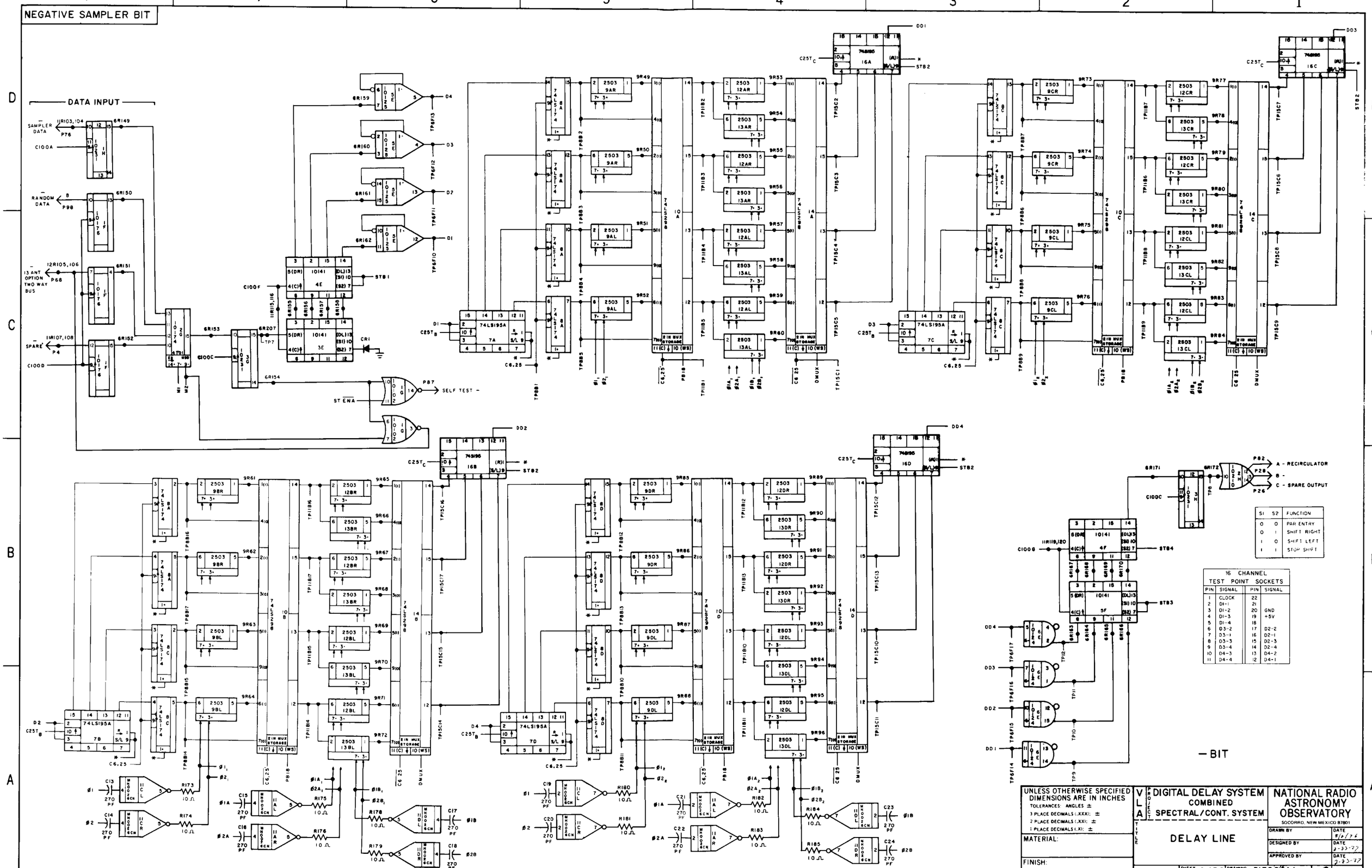
3.0 DRAWINGS

The following five sections contain the system drawings in the order of listing in the drawing list.

DRAWING SECTION 1 Drawings related to the delay/multiplier Subsystems

D13800L1
D13800L2
D13800L3
D13800L4
D13800M2 (SH2)


POSITIVE SAMPLER BIT
DATA INPUT
SAMPLER DATA
RANDOM DATA
SPARE
SELF TEST +
ST ENA
512 BIT S. R.
DELAYED DATA OUTPUTS
A+ RECIRCULATOR
B+
C+ SPARE OUT
+BIT
NOTES:
1. ALL RESISTORS ARE 1/4W ± 5% UNLESS OTHERWISE SPECIFIED.
2. C1-C24 = AEROVOX P/N CK05BX271K OR EQUIV.
3. RESISTOR DESIGNATIONS:
6R = 390Ω, 1/4W TO -5.2V
9R = 3K, 1/4W TO -5.2V
11RX,Y:
X = 82Ω, 1/4W TO GND
Y = 130Ω, 1/4W TO -5.2V
12RX,Y:
X = 160Ω, 1/4W TO GND
Y = 270Ω, 1/4W TO -5.2V
4. TP6F2 (EXAMPLE) REFERS TO PIN 2 OF A TEST POINT SOCKET AT LOCATION 6F. PIN 19 = +5V, PIN 20 = GND.
5. * = +5V PULLUP RESISTOR BUS
R230 = ROW 7 R231 = ROW 8 R232 = ROW 16
6. TP1 (EXAMPLE) REFERS TO TEST POINTS FOR SCOPE PROBE ADAPTOR: TEKTRONIX P/N 013-0085-00
7. LAST R = 232
C = 66
TP = 19
8. ALL CAPACITORS = 0.1μf UNLESS OTHERWISE SPECIFIED.
9. SYNERTEK LOW POWER 2803 RECOMMENDED TO REPLACE 2503 SHIFT REGISTERS. AMD 25LS195 RECOMMENDED TO REPLACE 74S195.
16 CHANNEL TEST POINT SOCKETS
VLA PROJECT
DIGITAL DELAY SYSTEM COMBINED SPECTRAL/CONT. SYSTEM
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
TITLE
DELAY LINE
DRAWN BY
DATE 8/8/76
DESIGNED BY
DATE 2-23-77
APPROVED BY
DATE 2-23-77
SHEET NUMBER 1 OF 3
DRAWING NUMBER D13800L1
REV C
SCALE



S1	S2	FUNCTION
0	0	PAR ENTRY
0	1	SHIFT RIGHT
1	0	SHIFT LEFT
1	1	STOP SHIFT

16 CHANNEL TEST POINT SOCKETS

PIN	SIGNAL	PIN	SIGNAL
1	CLOCK	22	
2	D1-1	21	
3	D1-2	20	GND
4	D1-3	19	+5V
5	D1-4	18	
6	D3-2	17	D2-2
7	D3-1	16	D2-1
8	D3-3	15	D2-3
9	D3-4	14	D2-4
10	D4-3	13	D4-2
11	D4-4	12	D4-1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

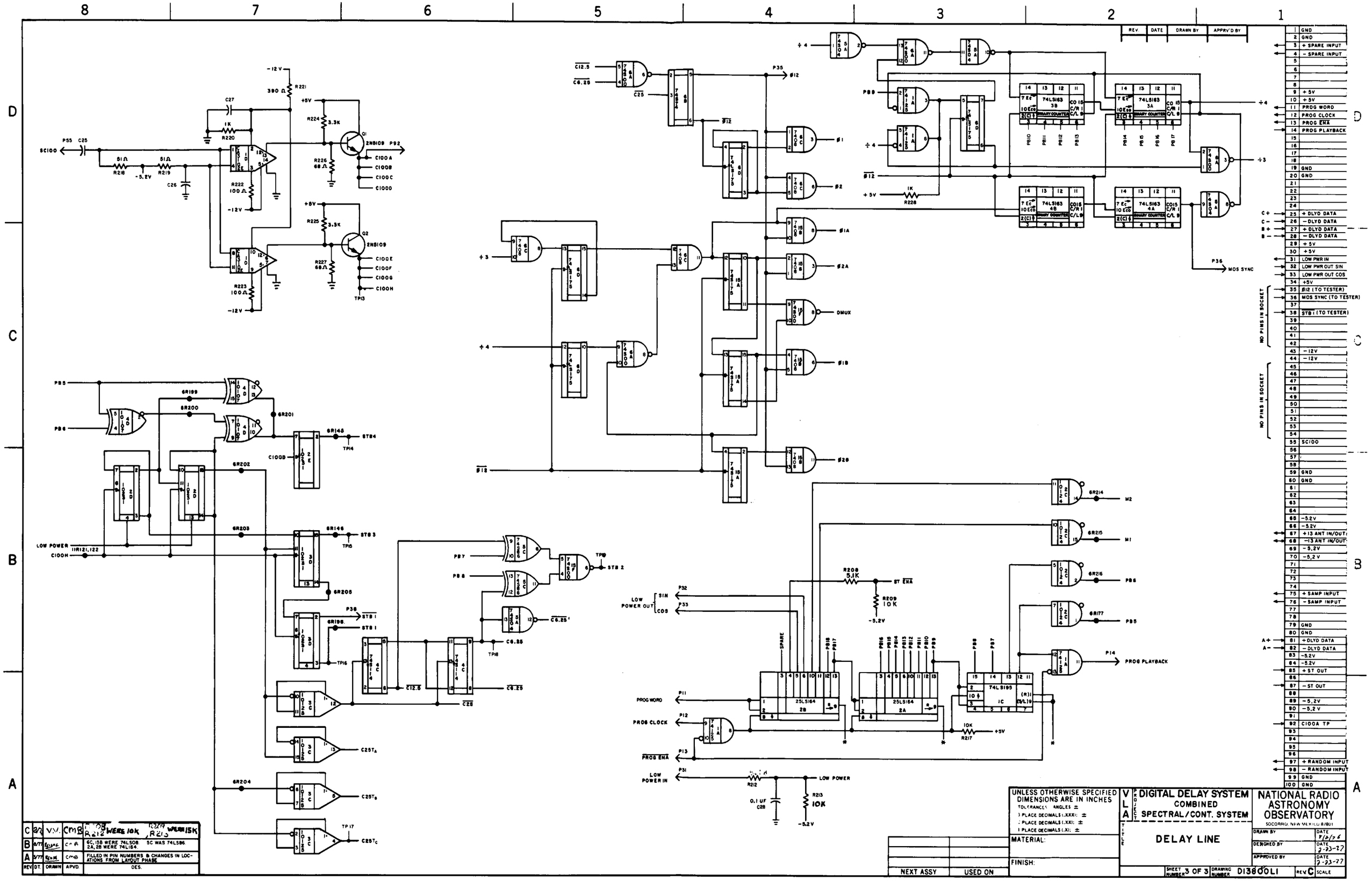
VLA PROJECT: DIGITAL DELAY SYSTEM COMBINED SPECTRAL/CONT. SYSTEM

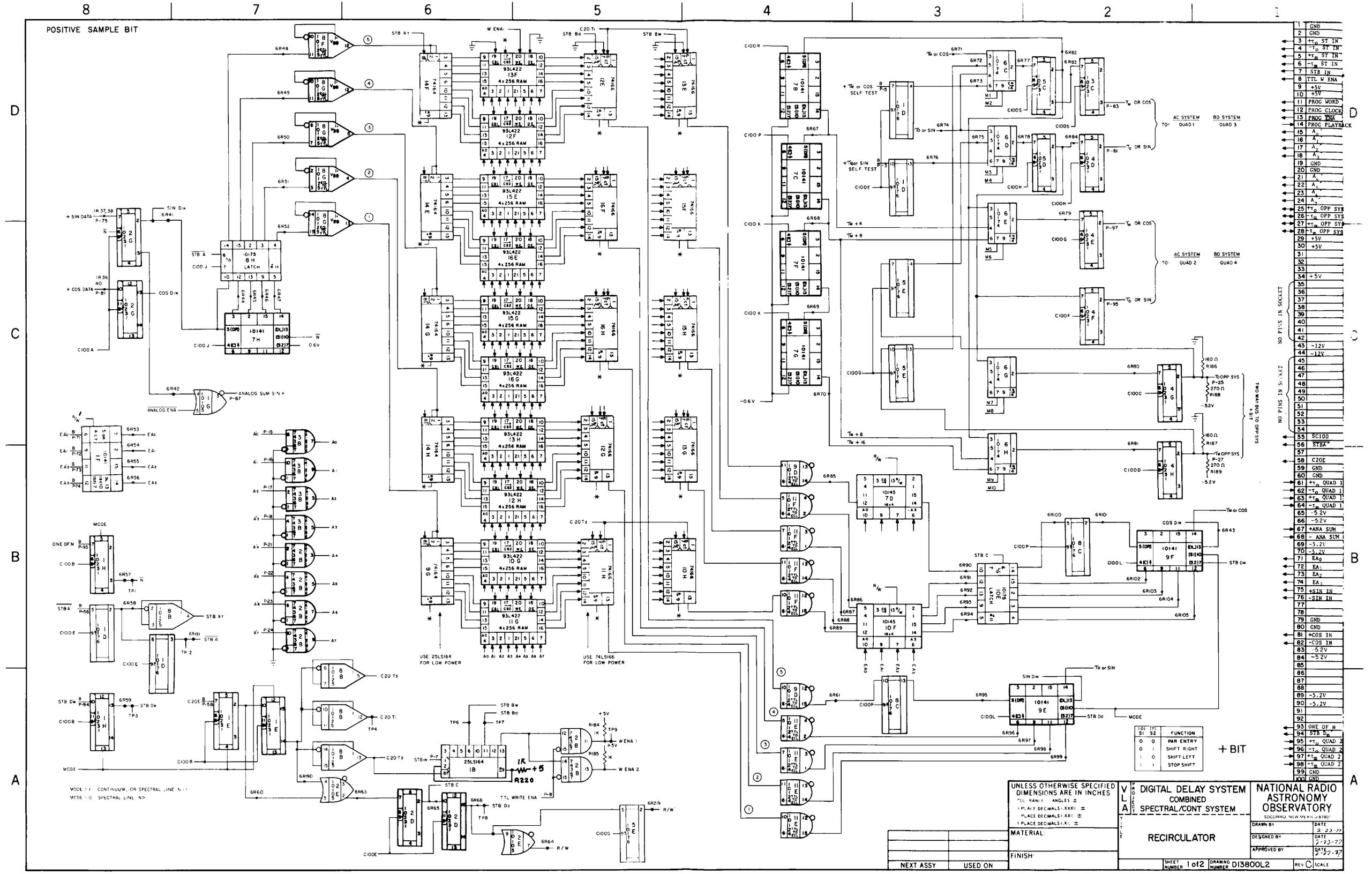
TITLE: DELAY LINE

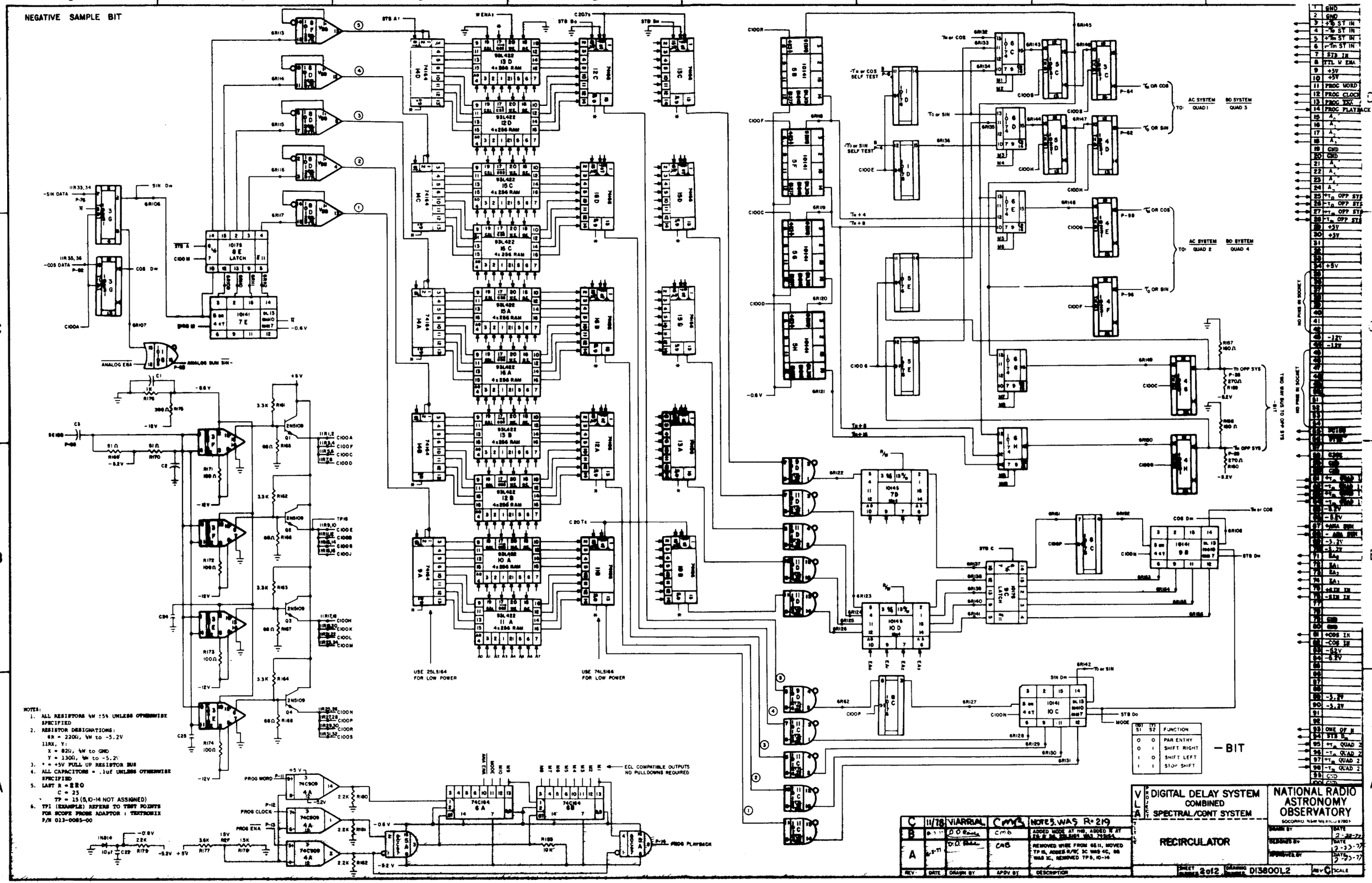
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

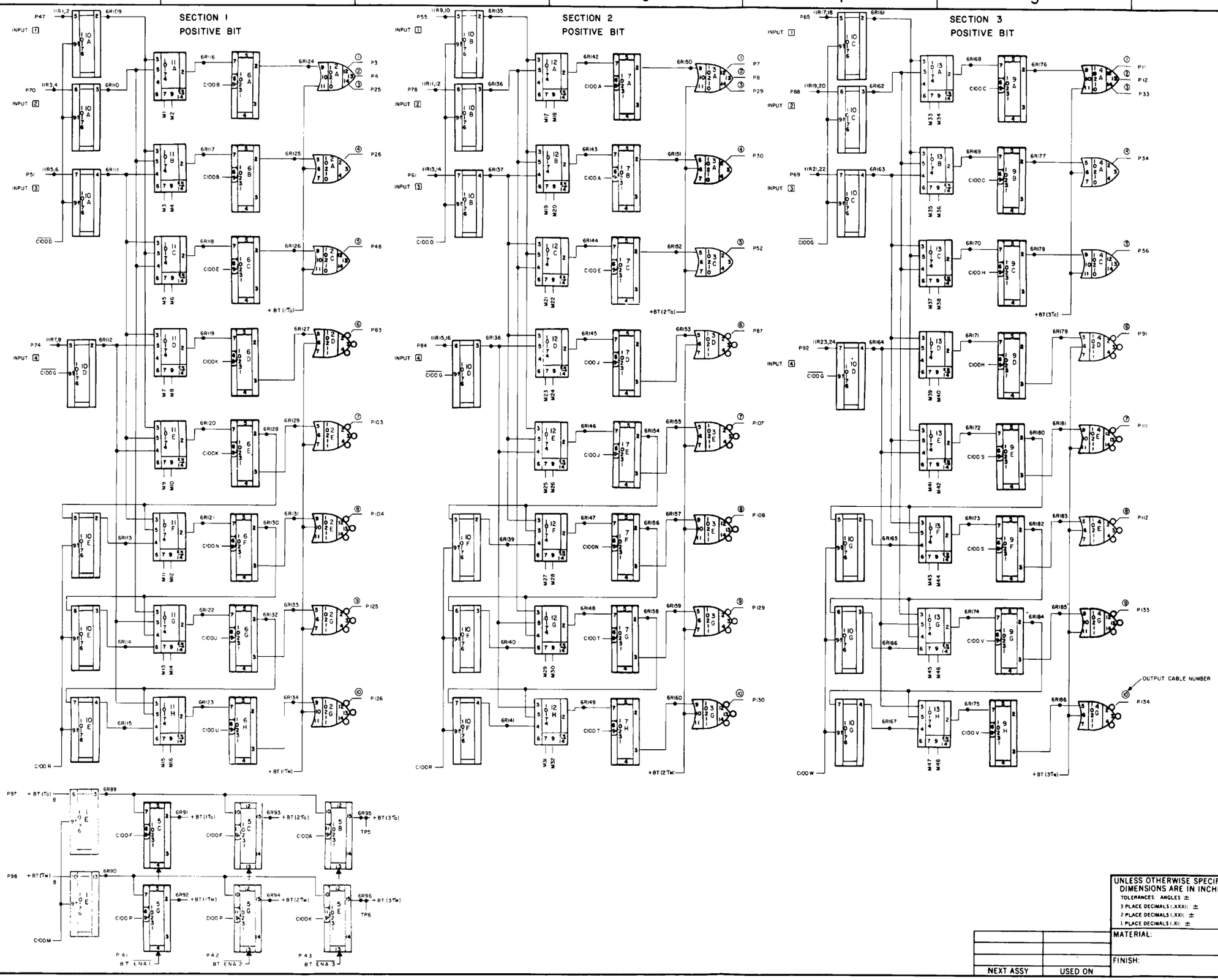
DRAWN BY		DATE 8/1/76
DESIGNED BY		DATE 2-23-77
APPROVED BY		DATE 2-23-77

SHEET NUMBER 2 OF 3 | DRAWING NUMBER D13800LI | REV C | SCALE


8 7 6 5 4 3 2 1
D C B A
REV. DATE DRAWN BY APPRV'D BY
1 GND
2 GND
3 + SPARE INPUT
4 − SPARE INPUT
9 + 5V
10 + 5V
11 PROG WORD
12 PROG CLOCK
13 PROG ENA
14 PROG PLAYBACK
19 GND
20 GND
25 + DLYD DATA
26 − DLYD DATA
27 + DLYD DATA
28 − DLYD DATA
29 + 5V
30 + 5V
31 LOW PWR IN
32 LOW PWR OUT SIN
33 LOW PWR OUT COS
34 +5V
35 Ø12 (TO TESTER)
36 MOS SYNC (TO TESTER)
38 STB I (TO TESTER)
NO PINS IN SOCKET
43 −12V
44 −12V
55 SC100
59 GND
60 GND
65 −5.2V
66 −5.2V
67 +13 ANT IN/OUT
68 −13 ANT IN/OUT
69 −5.2V
70 −5.2V
75 + SAMP INPUT
76 − SAMP INPUT
79 GND
80 GND
81 + DLYD DATA
82 − DLYD DATA
83 −5.2V
84 −5.2V
85 + ST OUT
87 − ST OUT
89 −5.2V
90 −5.2V
92 C100A TP
97 + RANDOM INPUT
98 − RANDOM INPUT
99 GND
100 GND
SC100
P55 C25
51Ω R218
51Ω R219
−5.2V C26
390Ω R221
C27
1K R220
R222 100Ω
R223 100Ω
R224 3.3K
R225 3.3K
R226 68Ω
R227 68Ω
2N5109 Q1
2N5109 Q2
P92
C100A
C100B
C100C
C100D
C100E
C100F
C100G
C100H
TP13
PB5
PB6
6R199
6R200
6R201
6R202
6R203
6R205
6R196
6R145
6R146
ST84
TP14
TP15
TP16
ST83
LOW POWER
11R121,122
C100H
P38
STB I
C25TA
C25TB
C25TC
TP17
6R204
PB7
PB8
TP19
STB 2
C6.25'
C6.25
TP18
C12.5
C6.25
C25
Ø12
P35
Ø1
Ø2
Ø1A
Ø2A
DMUX
Ø1B
Ø2B
÷4
÷3
74LS163 3B
74LS163 3A
74LS163 4B
74LS163 4A
BINARY COUNTER
CO15 C/R1 C/L9
PB10
PB11
PB12
PB13
PB14
PB15
PB16
PB17
P36
MOS SYNC
M2
M1
PB6
PB5
6R214
6R215
6R216
6R177
P14
PROG PLAYBACK
R208 5.1K
ST ENA
R209 10K
−5.2V
LOW POWER OUT
SIN
COS
P32
P33
SPARE
25LS164 2B
25LS164 2A
74LS195 1C
PROG WORD
PROG CLOCK
PROG ENA
P11
P12
P13
10K R217
+5V
P31
LOW POWER IN
R212
0.1 UF C28
R213 10K
LOW POWER
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
VLA PROJECT
DIGITAL DELAY SYSTEM
COMBINED
SPECTRAL/CONT. SYSTEM
TITLE
DELAY LINE
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DATE 7/2/76
DESIGNED BY
DATE 7-23-77
APPROVED BY
DATE 7-23-77
SHEET NUMBER 3 OF 3
DRAWING NUMBER D138001I
REV C
SCALE
C 8/8 VW CMB R212 WERE 10K, R213 WERE 15K
B 8/77 CMB 6C, 15B WERE 74LS08. 2A, 2B WERE 74LS164. 5C WAS 74LS86.
A 5/77 CMB FILLED IN PIN NUMBERS & CHANGES IN LOCATIONS FROM LAYOUT PHASE
REV DT. DRAWN APVD. DES.


POSITIVE SAMPLE BIT
93L422 4x256 RAM
74LS164
74LS166
10141
10175 8H LATCH
25LS164
USE 25LS164 FOR LOW POWER
USE 74LS166 FOR LOW POWER
MODE = 1 CONTINUUM, OR SPECTRAL LINE N=1
MODE = 0 SPECTRAL LINE N>
+ BIT
AC SYSTEM QUAD 1
BD SYSTEM QUAD 3
AC SYSTEM QUAD 2
BD SYSTEM QUAD 4
TWO WAY BUS TO OPP SYS
NO PINS IN SOCKET
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL:
FINISH:
NEXT ASSY
USED ON
DIGITAL DELAY SYSTEM
COMBINED SPECTRAL/CONT SYSTEM
RECIRCULATOR
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DESIGNED BY
APPROVED BY
SHEET NUMBER 1 of 2
DRAWING NUMBER D13800L2
REV C
SCALE


NEGATIVE SAMPLE BIT
USE 25LS164 FOR LOW POWER
USE 74LS164 FOR LOW POWER
ECL COMPATIBLE OUTPUTS NO PULLDOWNS REQUIRED
NOTES:
1. ALL RESISTORS ¼W ±5% UNLESS OTHERWISE SPECIFIED
2. RESISTOR DESIGNATIONS:
6R = 220Ω, ¼W to -5.2V
11RX, Y:
X = 82Ω, ¼W to GND
Y = 130Ω, ¼W to -5.2V
3. * = +5V PULL UP RESISTOR BUS
4. ALL CAPACITORS = .1uf UNLESS OTHERWISE SPECIFIED
5. LAST R = ZERO
C = 25
TP = 15 (5,10-14 NOT ASSIGNED)
6. TP1 (EXAMPLE) REFERS TO TEST POINTS FOR SCOPE PROBE ADAPTOR : TEKTRONIX P/N 013-0085-00
FUNCTION
PAR ENTRY
SHIFT RIGHT
SHIFT LEFT
STOP SHIFT
— BIT
DIGITAL DELAY SYSTEM
COMBINED
SPECTRAL/CONT SYSTEM
RECIRCULATOR
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO NEW MEXICO 87801
SHEET NUMBER 2 of 2
DRAWING NUMBER D138001.2
REV C
SCALE
NOTES. WAS R-219
REV DATE DRAWN BY APPV BY DESCRIPTION



REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	6-8-77			EXTENSIVE LOCATION CHANGES FROM LAYOUT PHASE
B	9/27/77			BAR CLOCKS WERE TRUE CLOCKS, R 262 WAS 10K.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON

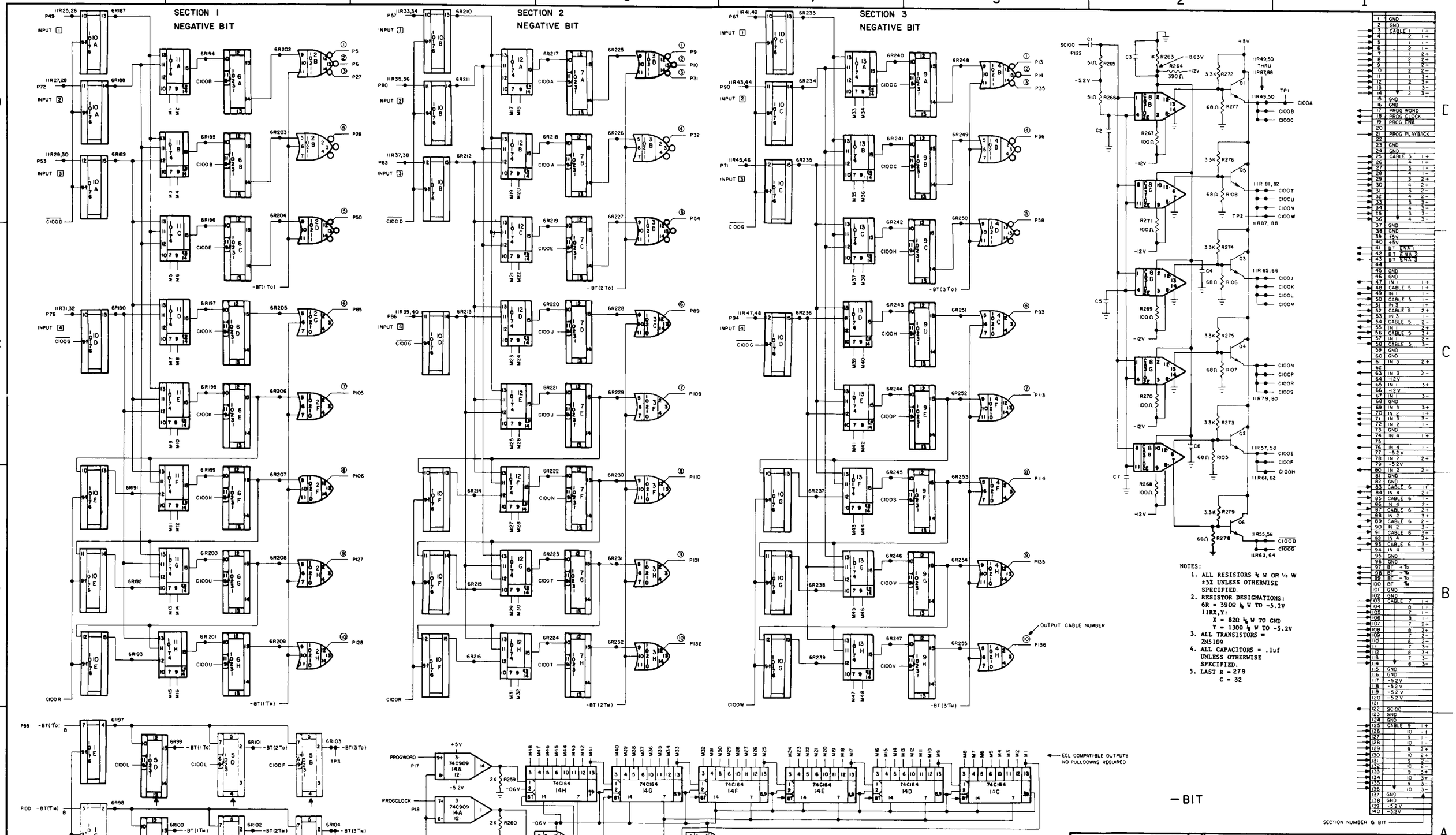
VLA PROJECT: DIGITAL DELAY SYSTEM COMBINED SPECTRAL/CONT SYSTEM

TITLE: DRIVER CARD

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 2-24-77
DESIGNED BY	DATE 2-24-77
APPROVED BY	DATE 2-24-77

SHEET NUMBER 1 of 2 DRAWING NUMBER D13800L3 REV B SCALE



NOTES:

1. ALL RESISTORS ¼ W OR ⅛ W ±5% UNLESS OTHERWISE SPECIFIED.
2. RESISTOR DESIGNATIONS:
   6R = 390Ω ⅛ W TO -5.2V
   11RX,Y:
   X = 82Ω ¼ W TO GND
   Y = 130Ω ¼ W TO -5.2V
3. ALL TRANSISTORS = 2N5109
4. ALL CAPACITORS = .1uf UNLESS OTHERWISE SPECIFIED.
5. LAST R = 279
   C = 32

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	
TOLERANCES ANGLES ±	
3 PLACE DECIMALS (.XXX): ±	
2 PLACE DECIMALS (.XX): ±	
1 PLACE DECIMALS (.X): ±	
MATERIAL:	
FINISH:	
NEXT ASSY	USED ON

VLA PROJECT

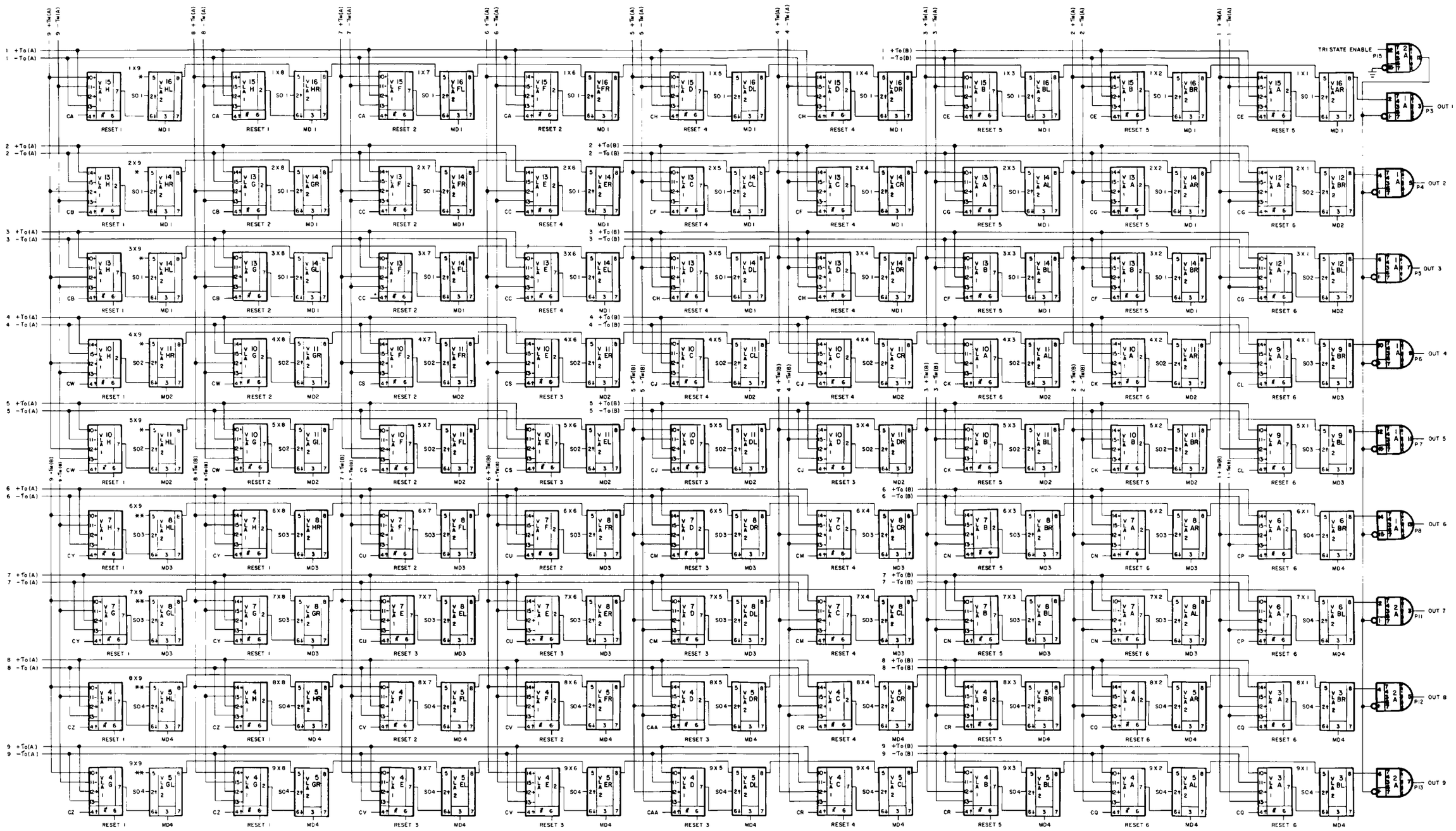
DIGITAL DELAY SYSTEM
COMBINED
SPECTRAL/CONT SYSTEM

TITLE: DRIVER CARD

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 2-21-77
DESIGNED BY	DATE 3-24-77
APPROVED BY	DATE 3-24-77

SHEET NUMBER 2 of 2 | DRAWING NUMBER D13800L3 | REV B | SCALE



** OR * = +5V PULL UP BUS

REV	DATE	DRN	APD	DES
C	4/77			ADDED R.E.D.D
B	11/78			R11 THRU R116 WERE 390Ω
A	7-27-77			SWITCHED CD & CH. FILLED IN PIN NOS. FROM LAYOUT

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY | USED ON

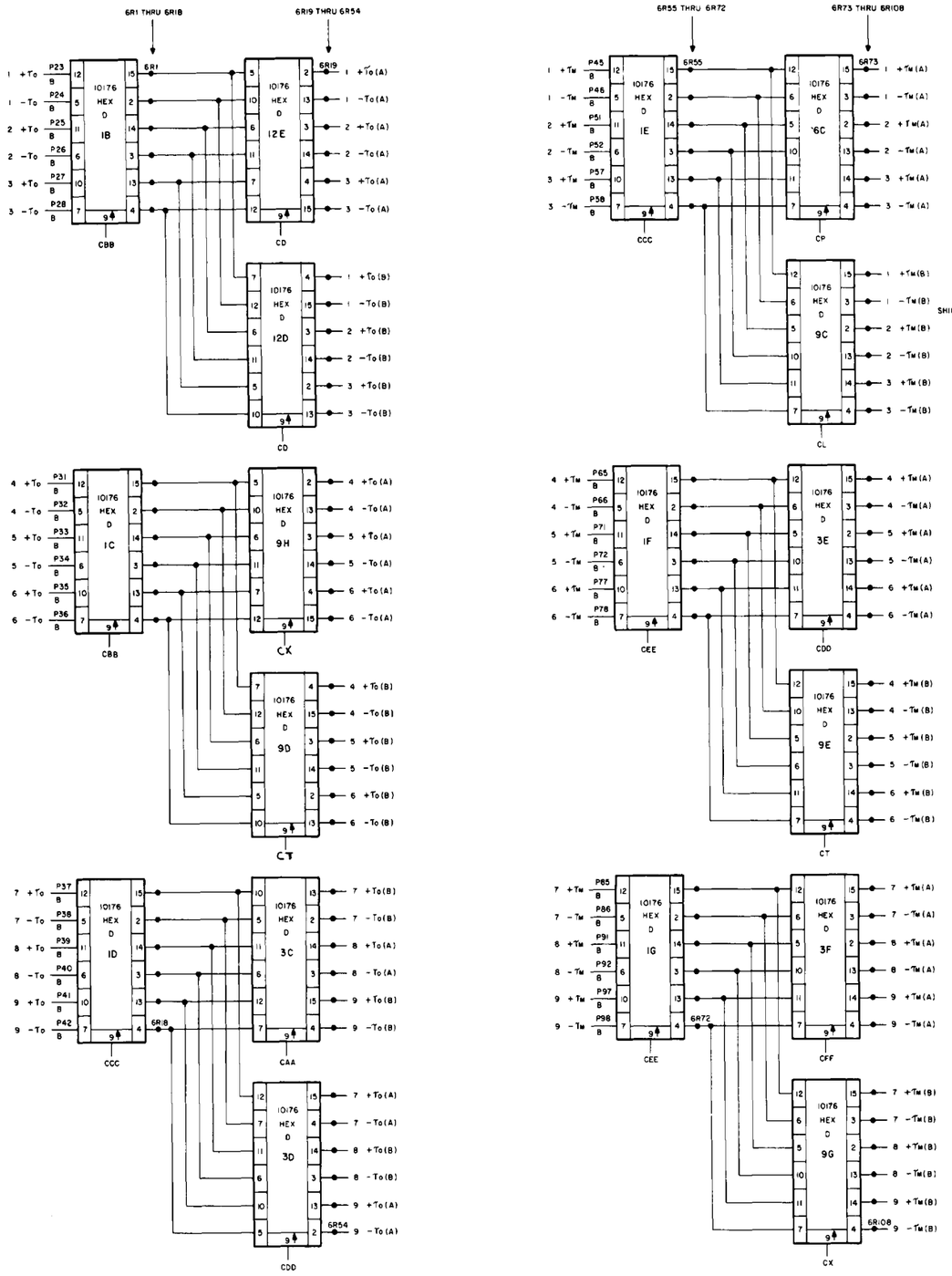
VLA PROJECT: DIGITAL DELAY SYSTEM
COMBINED SPECTRAL/CONT SYSTEM

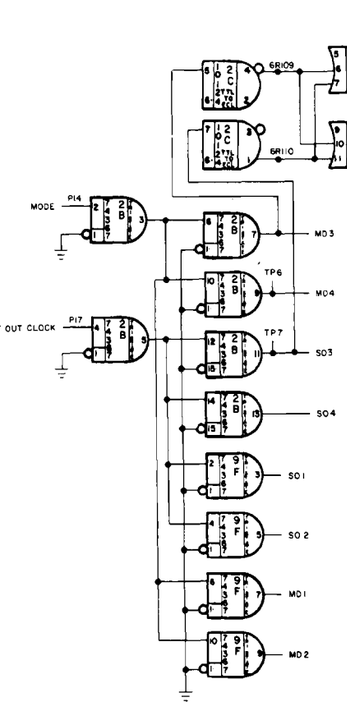
TITLE: MULTIPLIER

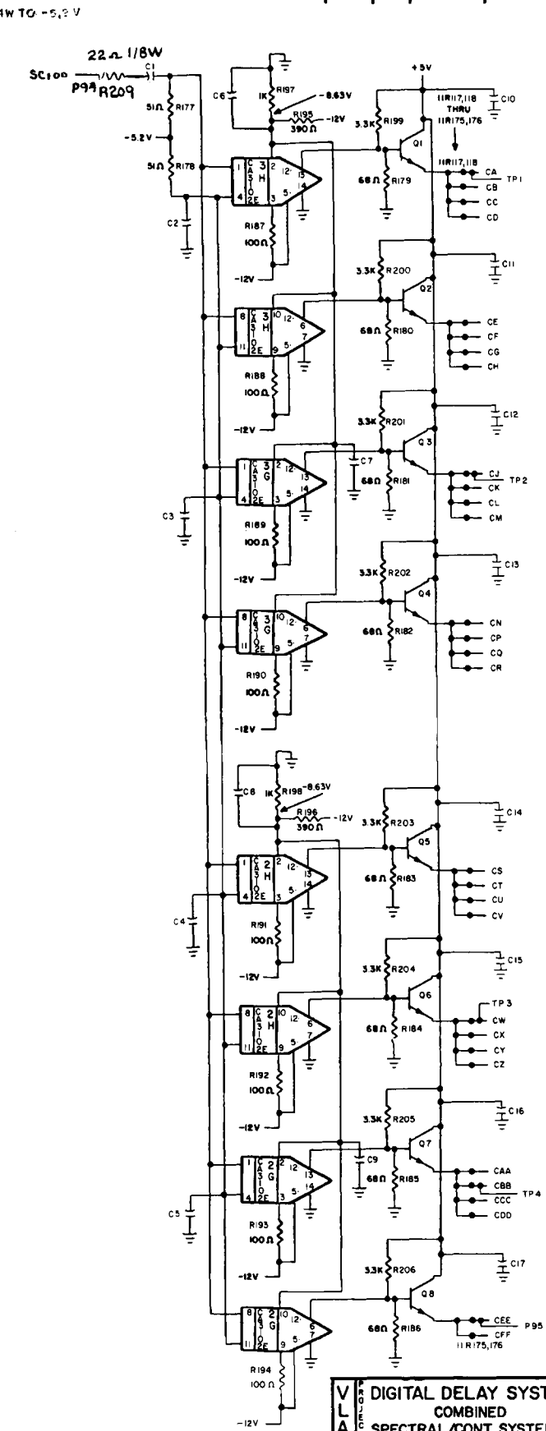
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE 3-16-77
DESIGNED BY | DATE 4-18-77
APPROVED BY | DATE 4-18-77

SHEET NUMBER 1 of 2 | DRAWING NUMBER D13800L4 | REV. C | SCALE







NOTES:

1. ALL RESISTORS ARE 1/4W ±5% UNLESS OTHERWISE SPECIFIED
2. ALL CAPACITORS = 0.1 µf UNLESS OTHERWISE SPECIFIED
3. RESISTOR DESIGNATIONS:
   6R = 390Ω 1/4W TO -5.2V
   11RX,Y: X=82Ω 1/4W TO GND
   Y=130Ω 1/4W TO -5.2V
4. TP1 (EXAMPLE) REFERS TO TEST POINTS FOR SCOPE PROBE ADAPTOR = TEKTRONIX P/N 013-0085-00
5. LAST R=
   C=
   TP=4

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

1	GND
2	GND
3	OUT 1
4	OUT 2
5	OUT 3
6	OUT 4
7	OUT 5
8	OUT 6
9	+5V
10	+5V
11	OUT 7
12	OUT 8
13	OUT 9
14	MODE
15	TRI STATE EN
16	+5V
17	SHIFT OUT CLOCK
18	+5V
19	GND
20	GND
21	+5V
22	+5V
23	1 +To
24	1 -To
25	2 +To
26	2 -To
27	3 +To
28	3 -To
29	+5V
30	+5V
31	4 +To
32	4 -To
33	5 +To
34	5 -To
35	6 +To
36	6 -To
37	7 +To
38	7 -To
39	8 +To
40	8 -To
41	9 +To
42	9 -To
43	-12V
44	-12V
45	1 +TM
46	1 -TM
47	
48	
49	-5.2V
50	-5.2V
51	2 +TM
52	2 -TM
53	
54	
55	
56	
57	3 +TM
58	3 -TM
59	GND
60	GND
61	
62	
63	
64	
65	4 +TM
66	4 -TM
67	
68	
69	-5.2V
70	-5.2V
71	5 +TM
72	5 -TM
73	
74	-5.2V
75	-5.2V
76	
77	6 +TM
78	6 -TM
79	GND
80	GND
81	
82	
83	
84	
85	7 +TM
86	7 -TM
87	
88	
89	-5.2V
90	-5.2V
91	8 +TM
92	8 -TM
93	
94	SC100
95	CEE
96	
97	9 +TM
98	9 -TM
99	GND
100	GND

VLA PROJECT: DIGITAL DELAY SYSTEM COMBINED SPECTRAL/CONT SYSTEM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

TITLE: MULTIPLIER

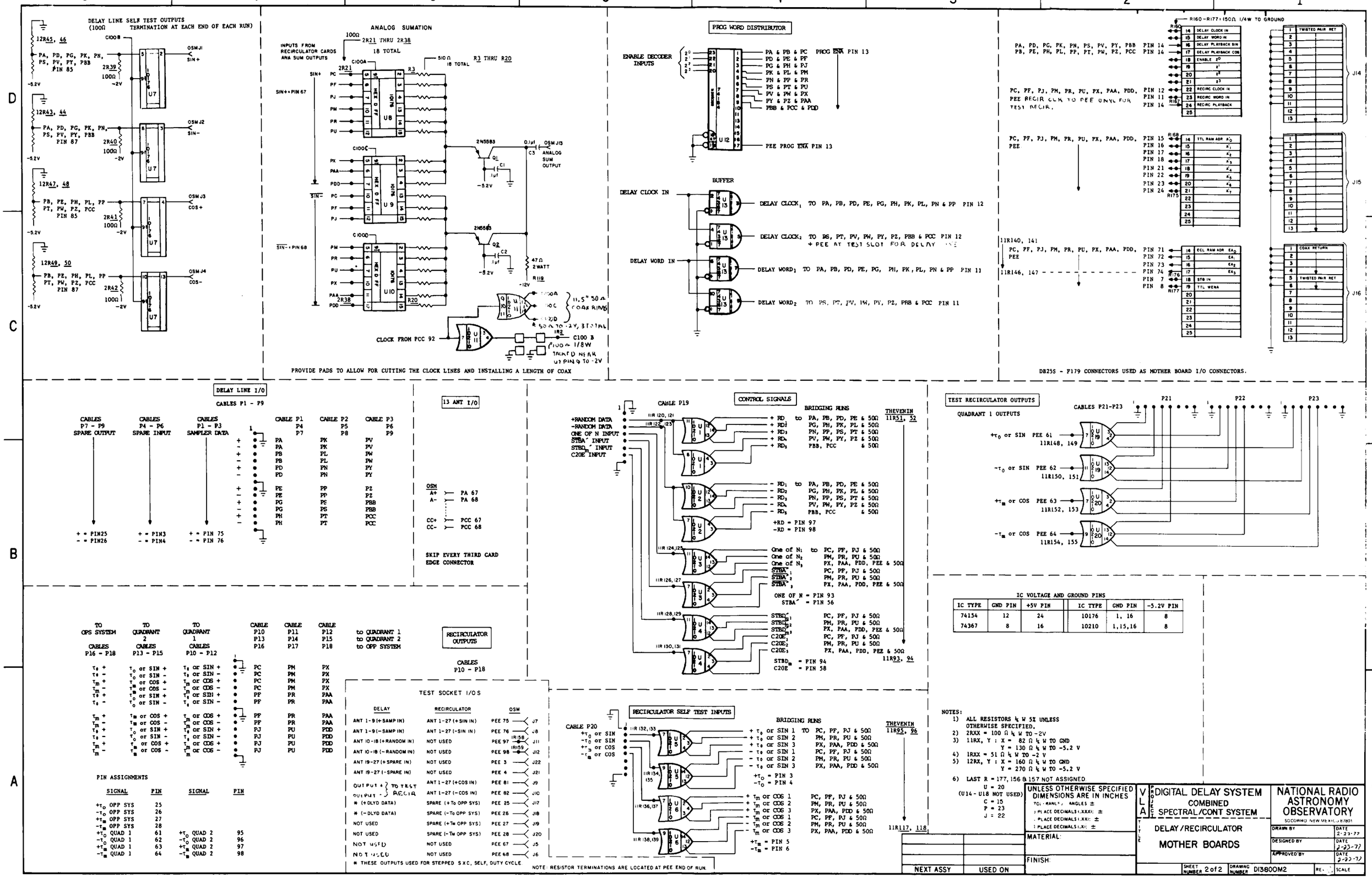
DRAWN BY	DATE 3-19-77
DESIGNED BY	DATE 4-18-77
APPROVED BY	DATE 4-18-77

SHEET NUMBER 2of2 | DRAWING NUMBER D13800L4 | REV C | SCALE

MATERIAL:

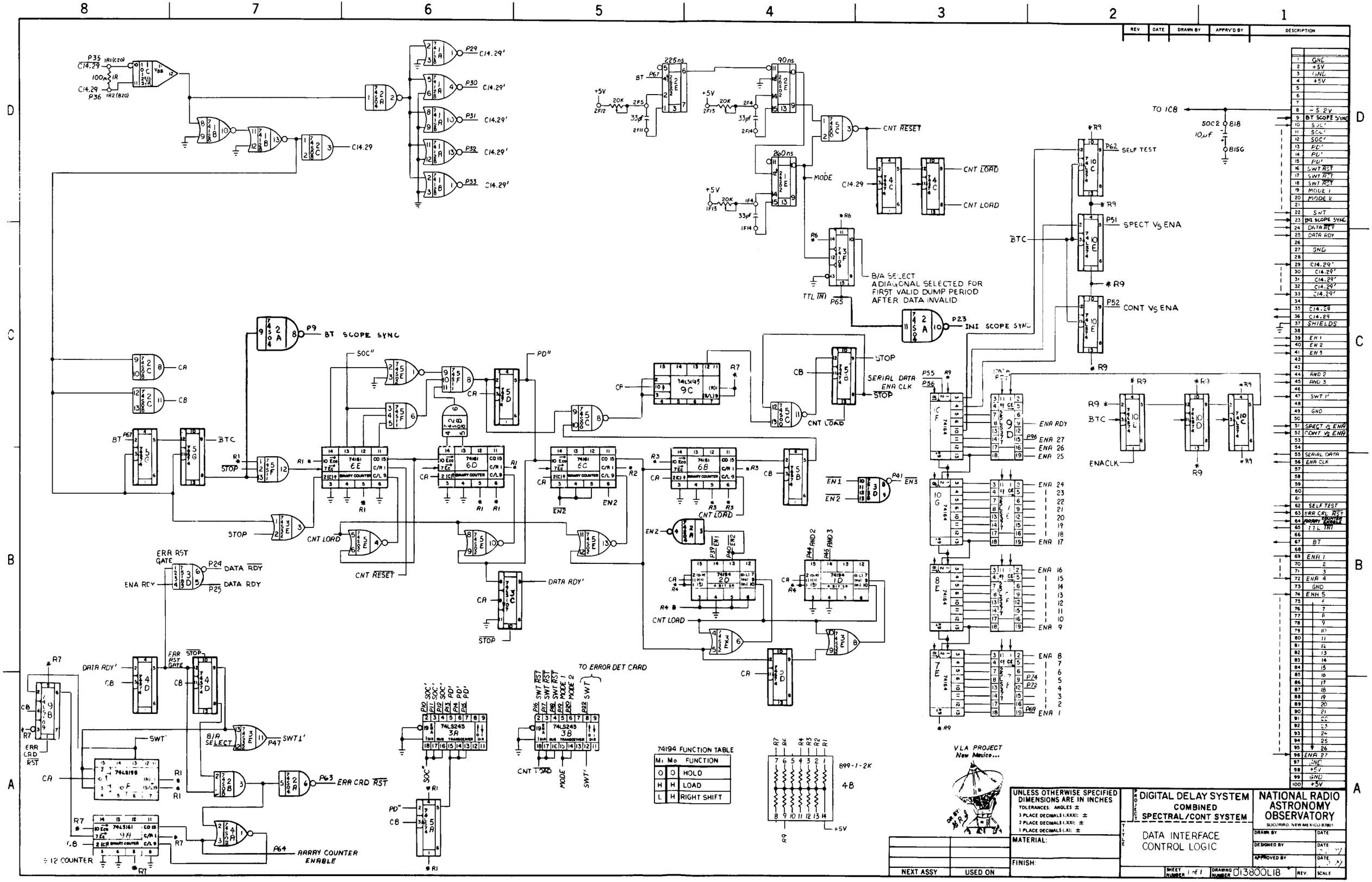
FINISH:

NEXT ASSY | USED ON


DELAY LINE SELF TEST OUTPUTS (100Ω TERMINATION AT EACH END OF EACH RUN)
ANALOG SUMATION
INPUTS FROM RECIRCULATOR CARDS ANA SUM OUTPUTS
PROVIDE PADS TO ALLOW FOR CUTTING THE CLOCK LINES AND INSTALLING A LENGTH OF COAX
PROG WORD DISTRIBUTOR
ENABLE DECODER INPUTS
BUFFER
DELAY CLOCK IN
DELAY WORD IN
R160 - R177: 150Ω 1/4W TO GROUND
DB25S - F179 CONNECTORS USED AS MOTHER BOARD I/O CONNECTORS.
DELAY LINE I/O
CABLES P1 - P9
13 ANT I/O
SKIP EVERY THIRD CARD EDGE CONNECTOR
CONTROL SIGNALS
BRIDGING RUNS
THEVENIN
TEST RECIRCULATOR OUTPUTS
QUADRANT 1 OUTPUTS
CABLES P21-P23
RECIRCULATOR OUTPUTS
CABLES P10 - P18
TEST SOCKET I/OS
RECIRCULATOR SELF TEST INPUTS
PIN ASSIGNMENTS
IC VOLTAGE AND GROUND PINS
NOTES:
1) ALL RESISTORS ¼ W 5% UNLESS OTHERWISE SPECIFIED.
2) 2RXX = 100 Ω ¼ W TO -2V
3) 11RX, Y : X = 82 Ω ¼ W TO GND
Y = 130 Ω ¼ W TO -5.2 V
4) 1RXX = 51 Ω ¼ W TO -2 V
5) 12RX, Y : X = 160 Ω ¼ W TO GND
Y = 270 Ω ¼ W TO -5.2 V
6) LAST R = 177, 156 & 157 NOT ASSIGNED.
U = 20
(U14 - U18 NOT USED)
C = 15
F = 23
J = 22
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL:
FINISH:
NEXT ASSY
USED ON
VLA PROJECT
DIGITAL DELAY SYSTEM
COMBINED SPECTRAL/CONT SYSTEM
DELAY/RECIRCULATOR MOTHER BOARDS
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO NEW MEXICO 87801
DRAWN BY
DATE 2-23-77
DESIGNED BY
DATE 2-23-77
APPROVED BY
DATE 2-23-77
SHEET NUMBER 2 of 2
DRAWING NUMBER D13800M2
SCALE

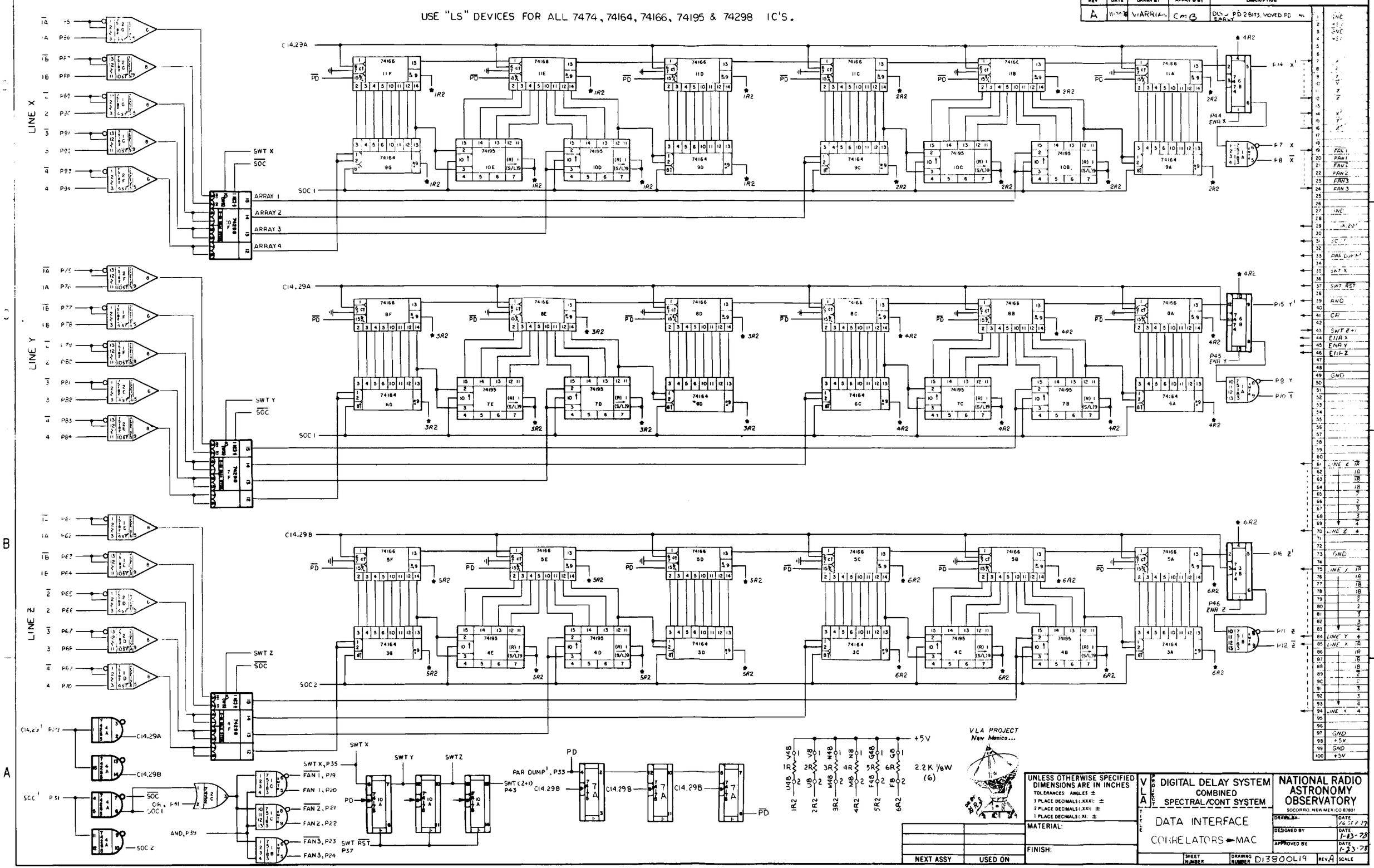
DRAWING SECTION 2 Drawings related to the delay/multiplier control and interface logic

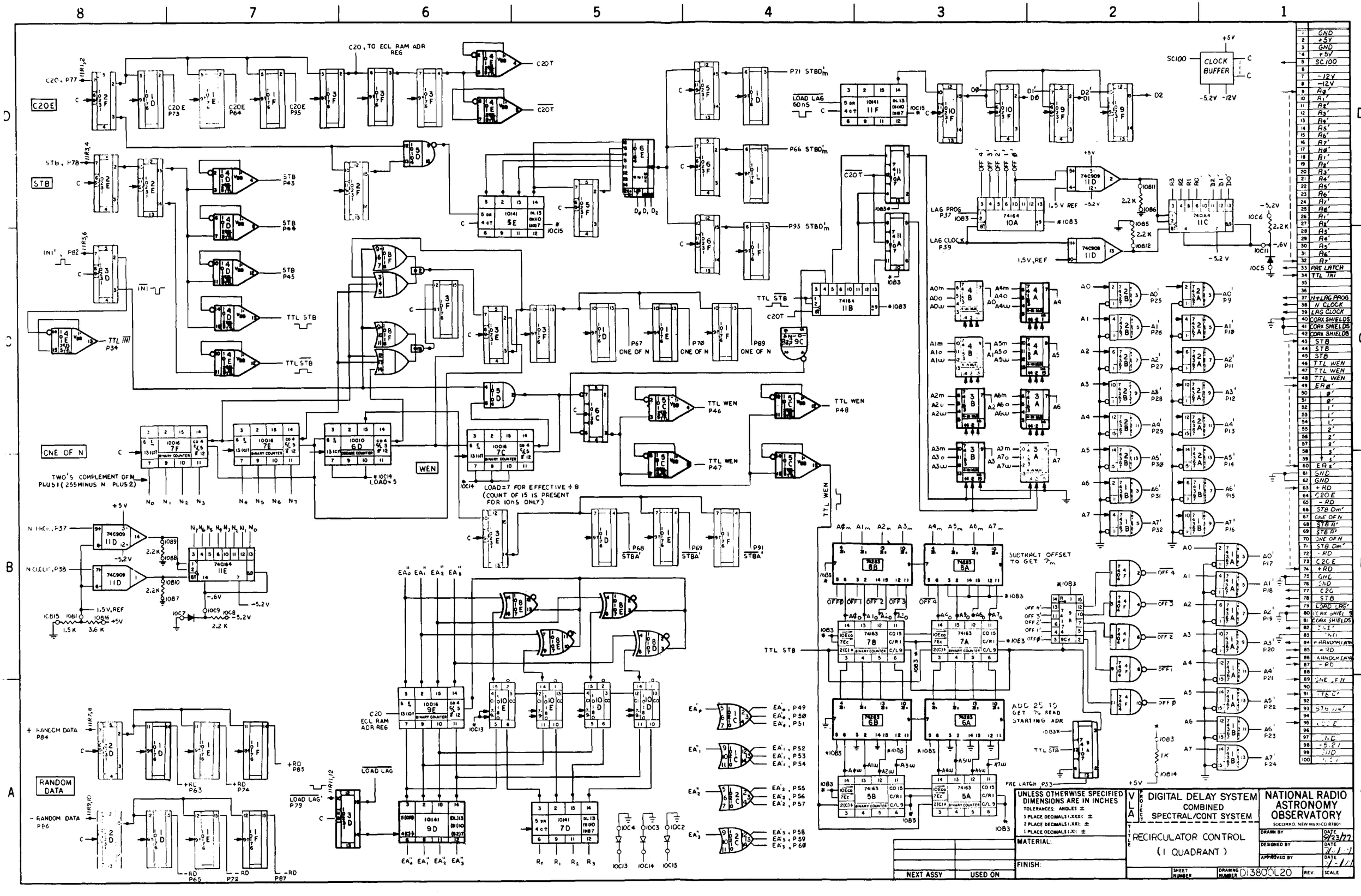
D13800L18
D13800L19
D13800L20
D13800L21
D13800L23
D13800L24
D13800L25
D13800L26

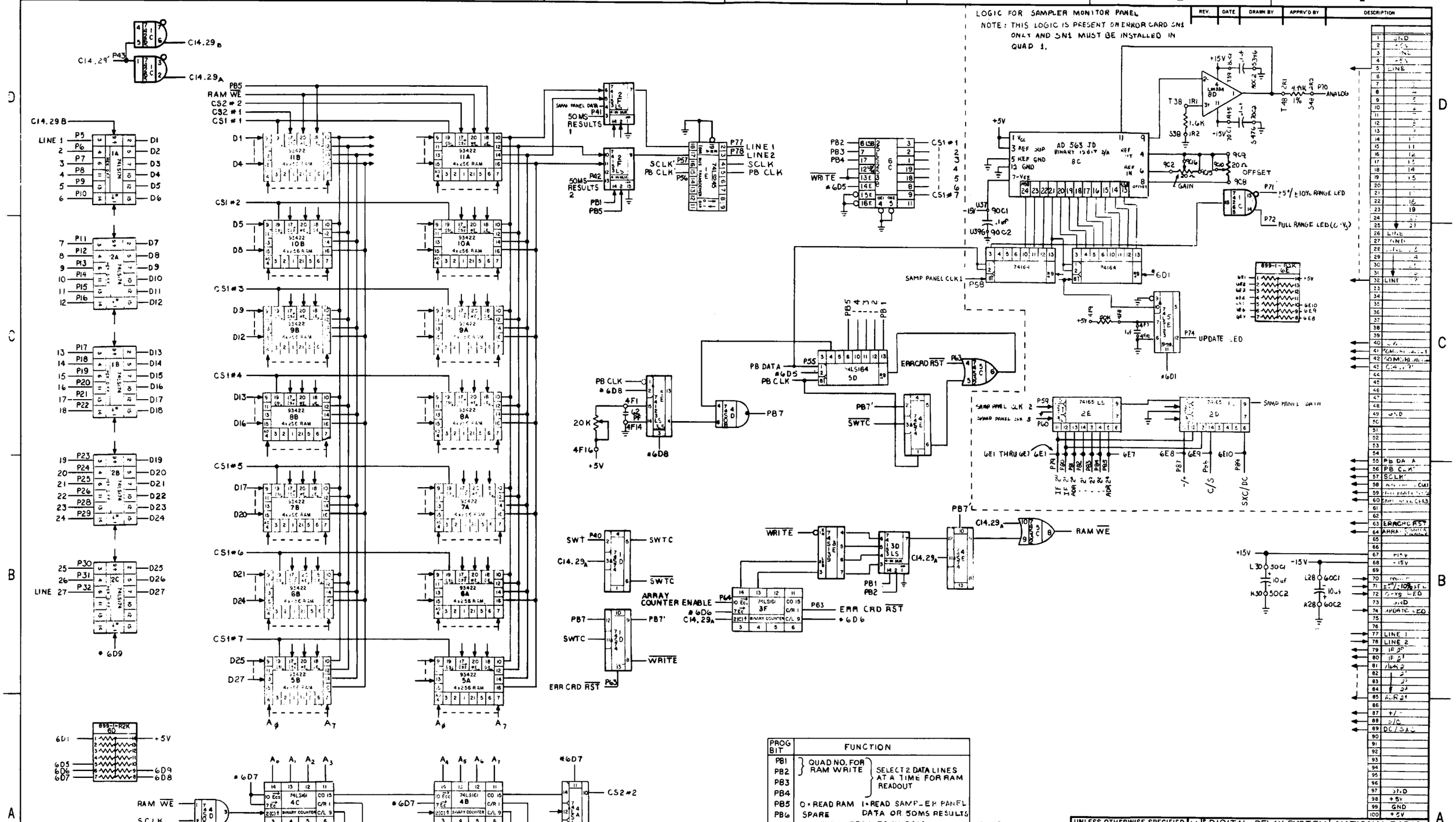

8
7
6
5
4
3
2
1
D
C
B
A
REV.
DATE
DRAWN BY
APPRV'D BY
DESCRIPTION
P35
C14.29
100Ω 1R
C14.29
P36
1R1(220)
1R2(820)
P29
P30
P31
P32
P33
C14.29'
C14.29
225ns
90ns
260ns
BT
P67
+5V
20K
33pf
2F12
2F5
2F11
2F13
2F4
2F14
1F13
1F4
1F14
CNT RESET
CNT LOAD
MODE
R6
B/A SELECT
A DIAGONAL SELECTED FOR
FIRST VALID DUMP PERIOD
AFTER DATA INVALID
TTL INI
P65
P23
INI SCOPE SYNC
TO IC8
50C2
8.8
10μf
B15G
R9
P62
SELF TEST
P51
SPECT VS ENA
P52
CONT VS ENA
BTC
P9
BT SCOPE SYNC
CA
CB
SOC"
PD"
STOP
SERIAL DATA
ENA CLK
P55
P56
ENA RDY
P96
ENA 27
ENA 26
ENA 25
ENA 24
ENA 17
ENA 16
ENA 9
ENA 8
ENA 1
P74
P72
P69
ENACLK
EN1
EN2
EN3
P41
CNT LOAD
ERR RST GATE
P24
DATA RDY
P25
DATA RDY'
ENA RDY
SWT'
SWT1'
P47
8/A SELECT
ERR CRD RST
P63
ARRAY COUNTER ENABLE
÷12 COUNTER
TO ERROR DET CARD
SWT
MODE 1
MODE 2
AND 2
AND 3
P44
P45
74194 FUNCTION TABLE
M1 M0 FUNCTION
0 0 HOLD
H H LOAD
L H RIGHT SHIFT
899-1-2K
4B
+5V
VLA PROJECT
New Mexico...
GND
+5V
BT SCOPE SYNC
SOC'
PD'
SWT RST
DATA RDY
SWT
ENA 4
ENA 5
ENA 27
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
PROJECT
DIGITAL DELAY SYSTEM
COMBINED
SPECTRAL/CONT SYSTEM
TITLE
DATA INTERFACE
CONTROL LOGIC
NATIONAL RADIO
ASTRONOMY
OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DESIGNED BY
APPROVED BY
DATE
SHEET NUMBER 1 of 1
DRAWING NUMBER D13800L18
REV.
SCALE

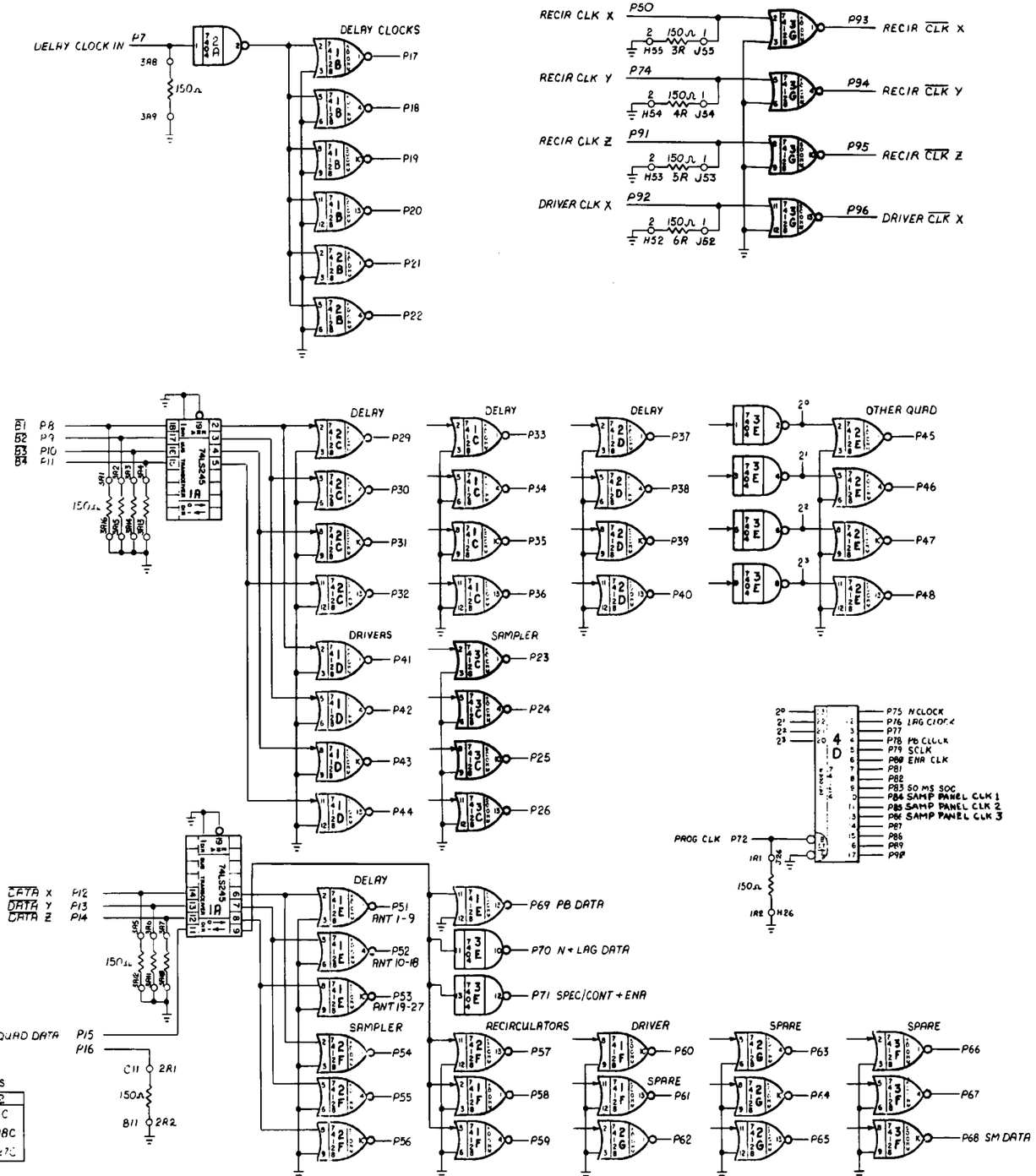
REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	11-20-78	W. ARRIZA	CMB	DLY PD 2 BITS, MOVED PD [illegible] EARLY

USE "LS" DEVICES FOR ALL 7474, 74164, 74166, 74195 & 74298 IC'S.




C20E
STB
ONE OF N
WEN
RANDOM DATA
CLOCK BUFFER
SC100
LOAD LAG 60nS
TTL STB
TTL WEN
PRE LATCH P33
SUBTRACT OFFSET TO GET Tm
ADD 25 TO GET Tm READ STARTING ADR
LOAD LAG
C20 ECL RAM ADR REG
TWO'S COMPLEMENT OF N PLUS 1 (255 MINUS N PLUS 2)
LOAD=7 FOR EFFECTIVE ÷8 (COUNT OF 15 IS PRESENT FOR 10nS ONLY)
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
VLA PROJECT
DIGITAL DELAY SYSTEM
COMBINED SPECTRAL/CONT SYSTEM
RECIRCULATOR CONTROL
(1 QUADRANT)
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DESIGNED BY
APPROVED BY
DATE 9/23/77
SHEET NUMBER
DRAWING NUMBER D138001L20
REV.
SCALE


LOGIC FOR SAMPLER MONITOR PANEL
NOTE: THIS LOGIC IS PRESENT ON ERROR CARD SN1 ONLY AND SN1 MUST BE INSTALLED IN QUAD 1.
REV. DATE DRAWN BY APPRV'D BY DESCRIPTION
AD 563 JD BINARY 12 BIT D/A
OFFSET
GAIN
±5V/±10% RANGE LED
FULL RANGE LED
UPDATE LED
SAMP PANEL CLK 1
SAMP PANEL CLK 2
SAMP PANEL DATA
ERRCRD RST
RAM WE
ARRAY COUNTER ENABLE
ERR CRD RST
PB CLK
SCLK
SWTC
WRITE
PB7
PB7'
LINE 1
LINE 2
50MS RESULTS 1
50MS RESULTS 2
CS1#1
CS1#2
CS1#3
CS1#4
CS1#5
CS1#6
CS1#7
CS2#1
CS2#2
PROG BIT
FUNCTION
PB1
PB2
PB3
PB4
QUAD NO. FOR RAM WRITE
SELECT 2 DATA LINES AT A TIME FOR RAM READOUT
PB5 0=READ RAM 1=READ SAMPLER PANEL
PB6 SPARE DATA OR 50MS RESULTS
PB7 1=WRITE RESULTS IN RAM
93422 +5V=PIN 22 GND=PIN 8
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
VLA PROJECT
DIGITAL DELAY SYSTEM
COMBINED SPECTRAL/CONT SYSTEM
TITLE
ERROR CARD
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DESIGNED BY
APPROVED BY
DATE
SHEET NUMBER
DRAWING NUMBER D13860L21
REV.
SCALE



SAMPLER DATA ASSIGNMENTS

	QUAD 1	QUAD 2
P54	ANT 1-9A	ANT 1-9C
P55	ANT 10-18A	ANT 10-18C
P56	ANT 19-27A	ANT 19-27C

1	GND
2	+5V
3	GND
4	+5V
5	
6	
7	DLY CLK IN
8	B1
9	B2
10	B3
11	B4
12	DATA X
13	DATA Y
14	DATA Z
15	QUAD DATA
16	150 Ω TERM
17	DLY CLK OUT
18	
19	
20	
21	
22	DLY CLK OUT
23	2⁰
24	2¹
25	2²
26	2³
27	GND
28	
29	2⁰
30	2¹
31	2²
32	2³
33	2⁰
34	2¹
35	2²
36	2³
37	2⁰
38	2¹
39	2²
40	2³
41	2⁰
42	2¹
43	2²
44	2³
45	2⁰
46	2¹
47	2²
48	2³
49	GND
50	RECIR CLK X
51	DELAY X
52	DELAY Y
53	DELAY Z
54	SAMPLER X
55	SAMPLER Y
56	SAMPLER Z
57	RECL X
58	RECL Y
59	RECL Z
60	DRIVER X
61	DRIVER Y
62	Z
63	X
64	Y
65	Z
66	X
67	SPARE Y
68	SM DATA
69	PB DATA
70	N+LAG DATA
71	SPEC/CONT+ENA
72	PROG CLOCK
73	GND
74	RECIR CLK Y
75	N CLOCK
76	LAG CLOCK
77	
78	PB CLK
79	SCLK
80	ENA CLK
81	SM CLK 1
82	SM CLK 2
83	CLK
84	
85	
86	
87	
88	
89	
90	CLK
91	RECIR CLK Z
92	DRIVER CLK X
93	RECIR CLK X
94	RECIR CLK Y
95	RECIR CLK Z
96	DRIVER CLK X
97	GND
98	+5V
99	GND
100	+5V

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

VLA PROJECT
New Mexico...

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

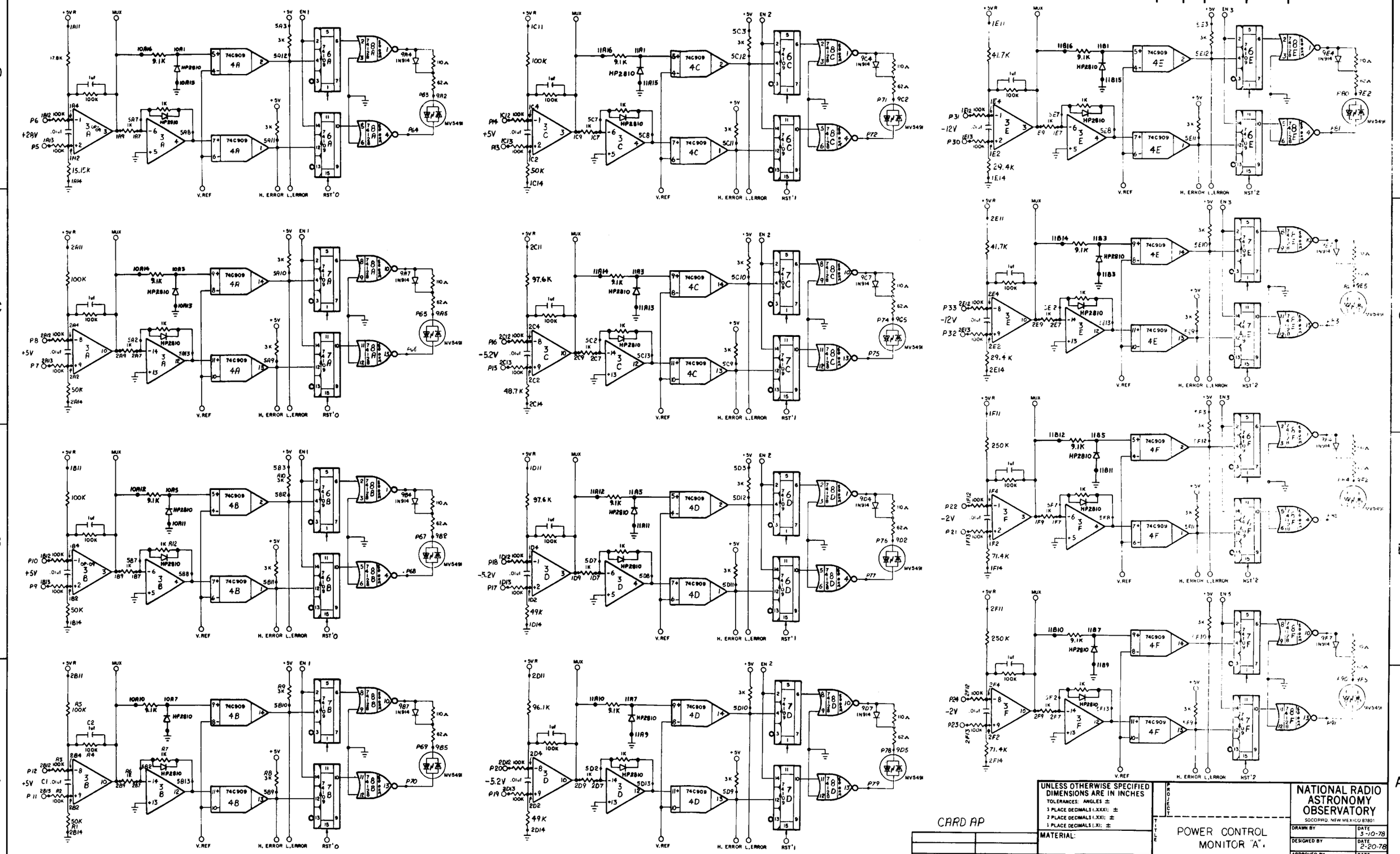
NEXT ASSY	USED ON

PROJECT: DIGITAL DELAY SYSTEM COMBINED SPECTRAL/CONT SYSTEM

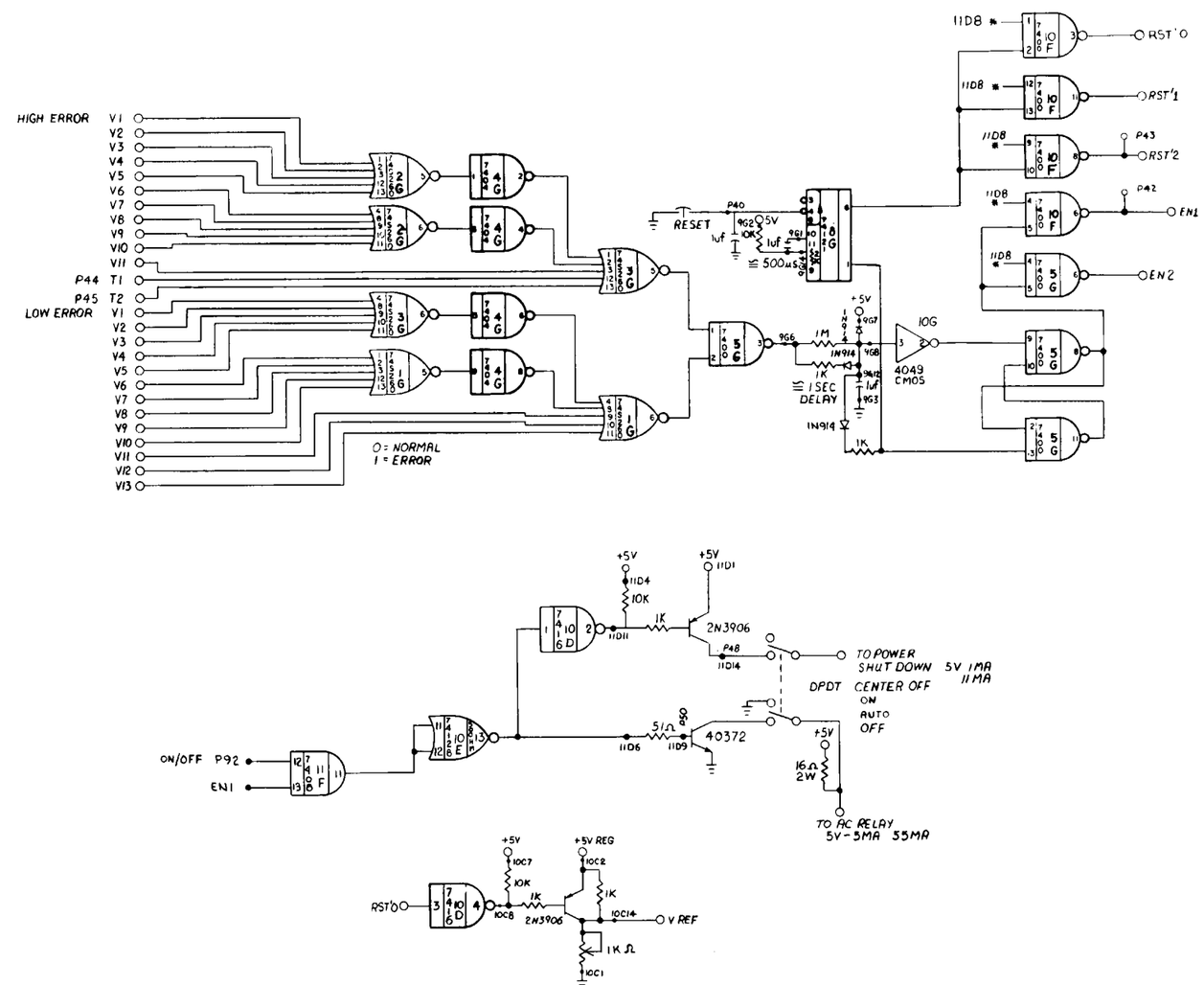
TITLE: PROG FAN OUT

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY		DATE	4-22-78
DESIGNED BY		DATE	[illegible]
APPROVED BY		DATE	[illegible]
SHEET NUMBER	DRAWING NUMBER D13800L23	REV.	SCALE


8
7
6
5
4
3
2
1
D
C
B
A
REV.
DATE
DRAWN BY
APPRV'D BY
DESCRIPTION
74C909
HP2810
MV5491
V.REF
H. ERROR
L.ERROR
RST'0
RST'1
RST'2
EN 1
EN 2
EN 3
MUX
+5V R
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
CARD AP
NEXT ASSY
USED ON
PROJECT
TITLE
POWER CONTROL MONITOR "A".
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DATE 3-10-78
DESIGNED BY
DATE 2-20-78
APPROVED BY
DATE
SHEET NUMBER 1 of 2
DRAWING NUMBER D13800L24
REV.
SCALE
NOTE: ALL OP AMPS ARE OP-09E

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



1	GND
2	VCC +5V
3	GND
4	VCC +5V
5	+28V A
6	-COMP
7	+5V B
8	-COMP
9	+5V C
10	-COMP
11	+5V D
12	-COMP
13	+5V E
14	-COMP
15	- A
16	+5.2V COMP
17	- B
18	+5.2V COMP
19	- C1
20	+5.2V COMP
21	-
22	+2V COMP
23	-
24	+2V COMP
25	
26	
27	GND
28	
29	
30	- C
31	+12V COMP
32	- D
33	+12V COMP
34	
35	+5V REG
36	+15V
37	+15V
38	-15V
39	
40	ON/OFF HEATER
41	
42	EN 1
43	EN 2
44	TEMP 1 ERR
45	TEMP 2 ERR
46	
47	
48	1 SHUT DN
49	NC
50	2 SHUT DN
51	+5V MUX B
52	+5V MUX C
53	+5V MUX D
54	+5V MUX E
55	+28V MUX A
56	-2V MUX C
57	-2V MUX D
58	-5.2V MUX A
59	-5.2V MUX B
60	-5.2V MUX C
61	-12V MUX C
62	-12V MUX D
63	+LED +28V
64	-LED +28V
65	+LED +5V
66	-LED +5V
67	+LED +5V
68	-LED +5V
69	+LED +5V
70	-LED +5V
71	+LED +5V
72	-LED +5V
73	NC
74	+LED -5.2V
75	-LED -5.2V
76	+LED -5.2V
77	-LED -5.2V
78	+LED -5.2V
79	-LED -5.2V
80	+LED -12V
81	-LED -12V
82	+LED -12V
83	-LED -12V
84	+LED -2V
85	-LED -2V
86	+15V
87	+15V
88	-15V
89	-15V
90	+LED -2V
91	-LED -2V
92	ON/OFF
93	
94	
95	
96	
97	GND
98	VCC +5V
99	GND
100	VCC +5V

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON

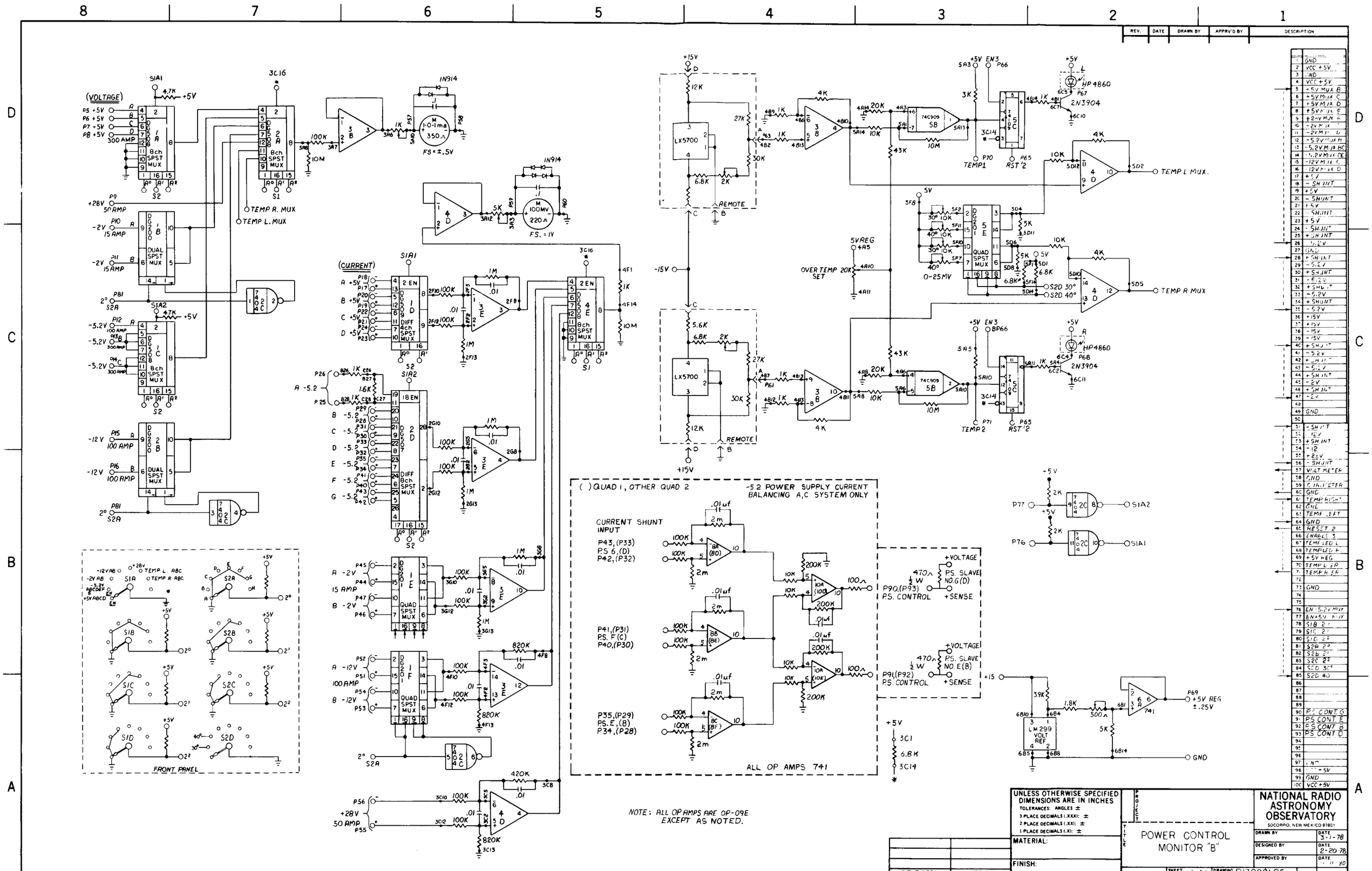
PROJECT

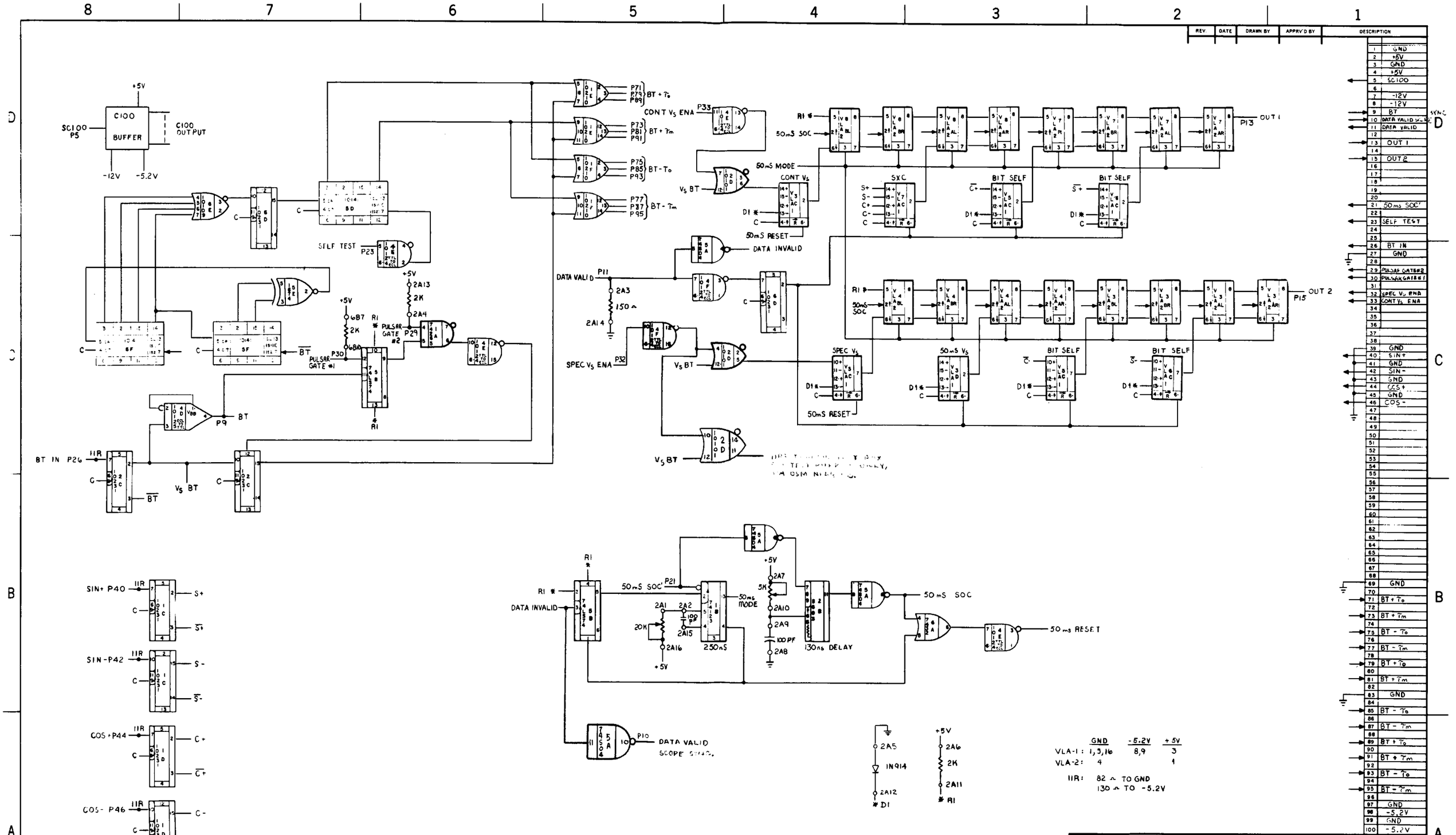
TITLE: POWER CONTROL MONITOR "A"

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY		DATE 4-19-78
DESIGNED BY		DATE 2-20-78
APPROVED BY		DATE

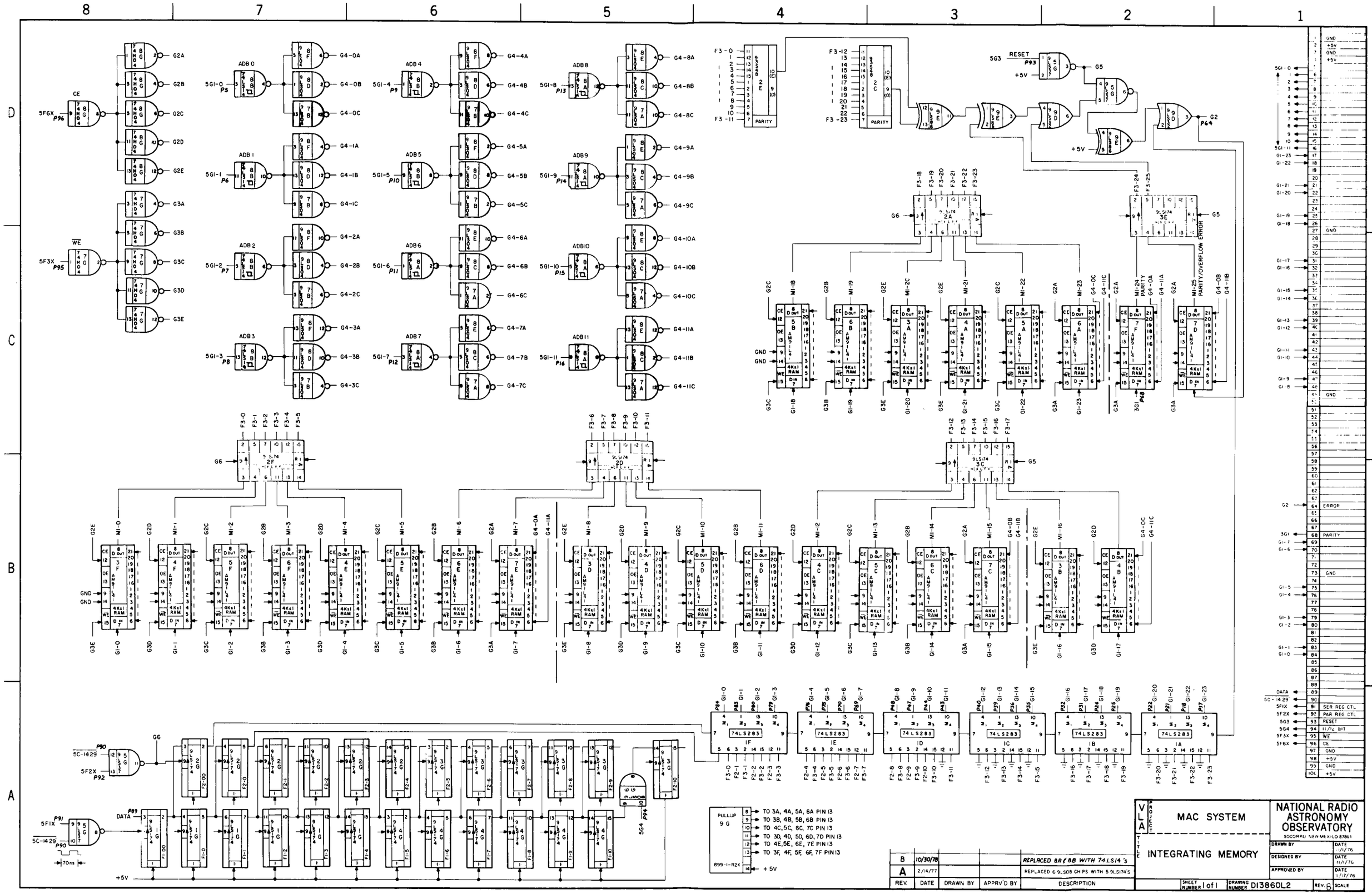
SHEET NUMBER 2 OF 2 | DRAWING NUMBER D13800L24 | REV. | SCALE


(VOLTAGE)
(CURRENT)
8ch SPST MUX
DUAL SPST MUX
DIFF 8ch SPST MUX
QUAD SPST MUX
TEMP R. MUX
TEMP L. MUX
FS = ±.5V
FS. = 1V
LX5700
REMOTE
74C909
HP4860
2N3904
TEMP1
TEMP2
RST '2
TEMP L MUX.
TEMP R MUX
0-25MV
OVER TEMP SET
5VREG
FRONT PANEL
QUAD 1, OTHER QUAD 2
-5.2 POWER SUPPLY CURRENT BALANCING A,C SYSTEM ONLY
CURRENT SHUNT INPUT
P43,(P33) P.S. 6,(D) P42,(P32)
P41,(P31) P.S. F(C) P40,(P30)
P35,(P29) P.S. E,(B) P34,(P28)
+VOLTAGE
P.S. SLAVE NO.G(D)
P90,(P93) P.S. CONTROL
+SENSE
P.S. SLAVE NO.E(B)
P91,(P92) P.S. CONTROL
ALL OP AMPS 741
LM 299 VOLT REF
741
+5V REG ±.25V
GND
NOTE: ALL OP AMPS ARE OP-09E EXCEPT AS NOTED.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
PROJECT
TITLE
POWER CONTROL MONITOR "B"
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DATE 3-1-78
DESIGNED BY
DATE 2-20-78
APPROVED BY
SHEET NUMBER 1 of 1
DRAWING NUMBER D13800L25
REV.
SCALE
REV. DATE DRAWN BY APPRV'D BY DESCRIPTION

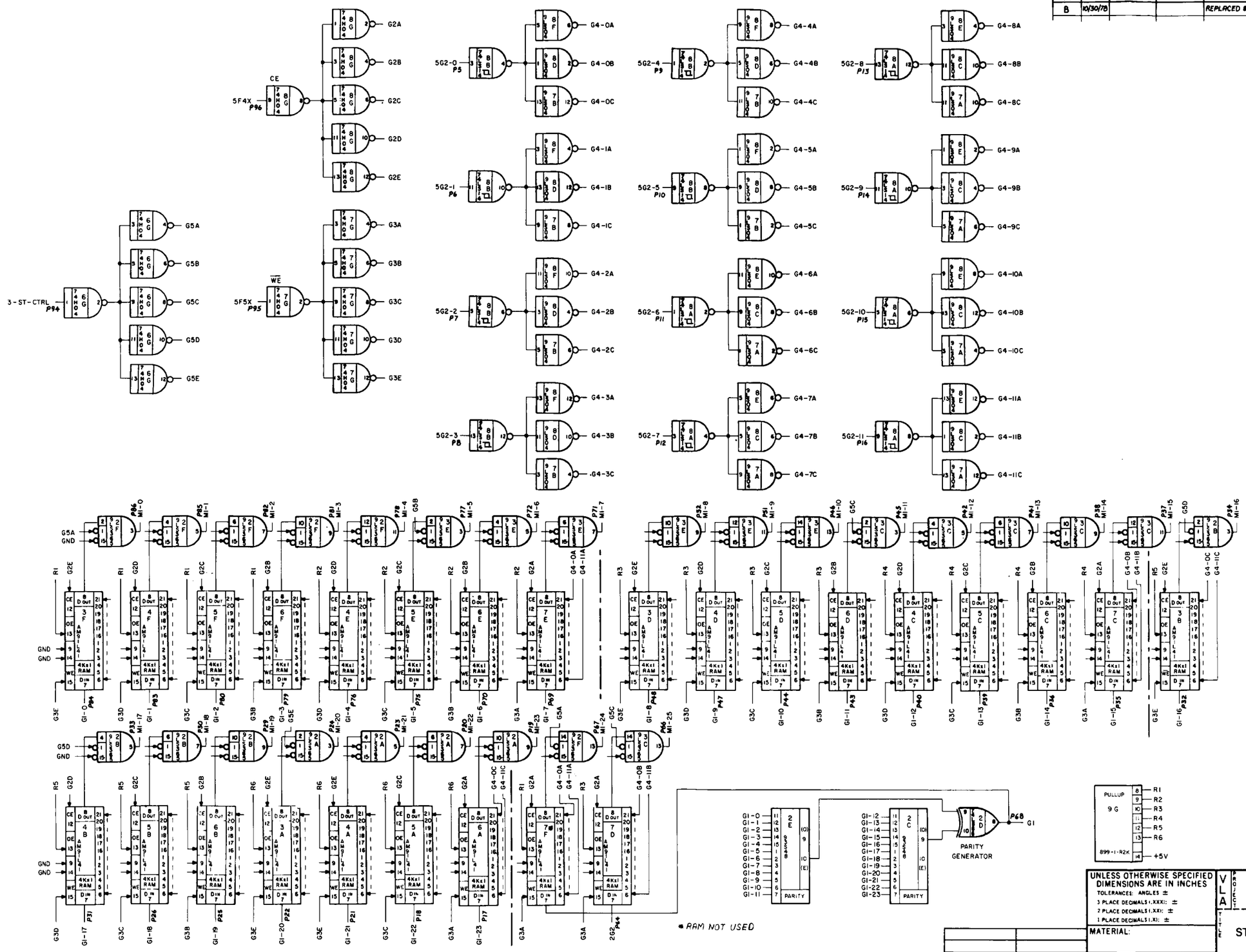

C100 BUFFER
SC100 P5
C100 OUTPUT
+5V
-12V
-5.2V
SELF TEST
P23
P71 P79 P89 BT + To
P73 P81 P91 BT + Tm
P75 P85 P93 BT - To
P77 P87 P95 BT - Tm
CONT Vs ENA
P33
CONT Vs
Vs BT
D1 *
50mS RESET
DATA INVALID
DATA VALID
P11
2A3
150 Ω
2A14
SPEC Vs ENA
P32
R1 *
50mS SOC
50mS MODE
OUT 1
P13
SXC
BIT SELF
OUT 2
P15
SPEC Vs
50mS Vs
2A13
2K
2A4
6B7
6B10
P29
PULSAR GATE #2
P30
PULSAR GATE #1
P9
BT
BT IN P26
Vs BT
SIN+ P40
SIN-P42
COS+P44
COS- P46
S+
S-
C+
C-
50mS SOC'
P21
2A1
2A2
100 PF
2A15
20K
2A16
250nS
2A7
5K
2A10
2A9
100 PF
2A8
130ns DELAY
50mS SOC
50mS RESET
P10
DATA VALID
SCOPE
2A5
IN914
2A12
2A6
2K
2A11
GND
-5.2V
+5V
VLA-1: 1,5,16 8,9 3
VLA-2: 4 1
IIR: 82 Ω TO GND
130 Ω TO -5.2V
SYNC
GND
BT
DATA VALID
DATA VALID
OUT 1
OUT 2
50ms SOC'
SELF TEST
BT IN
PULSAR GATE#2
PULSAR GATE#1
SPEC Vs ENA
CONT Vs ENA
SIN+
SIN-
COS+
COS-
BT + To
BT + Tm
BT - To
BT - Tm
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
VLA PROJECT
DIGITAL DELAY SYSTEM
COMBINED SPECTRAL/CONT SYSTEM
TITLE
SELF TEST & BT
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DATE
DESIGNED BY
APPROVED BY
SHEET NUMBER 1 OF 1
DRAWING NUMBER D13800L26
REV.
SCALE

DRAWING SECTION 3 Drawings related to the integrator

D13860L2
D13860L3
D13860L4
D13860L5
D13860L6
D13860L7
D13860L8
D13860L31
D13860L32
D13860L35
D13860L36
D13860L37


8
7
6
5
4
3
2
1
D
C
B
A
CE
5F6X P96
WE
5F3X P95
ADB 0
ADB 1
ADB 2
ADB 3
ADB 4
ADB 5
ADB 6
ADB 7
ADB 8
ADB 9
ADB 10
ADB 11
5G1-0 P5
5G1-1 P6
5G1-2 P7
5G1-3 P8
5G1-4 P9
5G1-5 P10
5G1-6 P11
5G1-7 P12
5G1-8 P13
5G1-9 P14
5G1-10 P15
5G1-11 P16
G2A
G2B
G2C
G2D
G2E
G3A
G3B
G3C
G3D
G3E
G4-0A
G4-0B
G4-0C
G4-1A
G4-1B
G4-1C
G4-2A
G4-2B
G4-2C
G4-3A
G4-3B
G4-3C
G4-4A
G4-4B
G4-4C
G4-5A
G4-5B
G4-5C
G4-6A
G4-6B
G4-6C
G4-7A
G4-7B
G4-7C
G4-8A
G4-8B
G4-8C
G4-9A
G4-9B
G4-9C
G4-10A
G4-10B
G4-10C
G4-11A
G4-11B
G4-11C
F3-0
F3-11
F3-12
F3-23
PARITY
5G3 RESET P93
+5V
G5
G2 P64
G6
9-5174 2A
9-5174 3E
9-5174 2F
9-5174 2D
9-5174 3C
F3-24
F3-25
PARITY/OVERFLOW ERROR
MI-18
MI-19
MI-20
MI-21
MI-22
MI-23
MI-24 PARITY
MI-25 PARITY/OVERFLOW ERROR
MI-0
MI-1
MI-2
MI-3
MI-4
MI-5
MI-6
MI-7
MI-8
MI-9
MI-10
MI-11
MI-12
MI-13
MI-14
MI-15
MI-16
MI-17
GND
4Kx1 RAM
GND +5V GND +5V
5G1-0
5G1-11
G1-23
G1-22
G1-21
G1-20
G1-19
G1-18
G1-17
G1-16
G1-15
G1-14
G1-13
G1-12
G1-11
G1-10
G1-9
G1-8
G2 ERROR
3G1 PARITY
G1-7
G1-6
G1-5
G1-4
G1-3
G1-2
G1-1
G1-0
DATA
5C-1429
5F1X SER REG CTL
5F2X PAR REG CTL
5G3 RESET
5G4 11/12 BIT
5F3X WE
5F6X CE
GND
+5V
5C-1429 P90
5F2X P92
5F1X P91
DATA P89
70ns
+5V
F2-00
F2-0
F2-1
F2-2
F2-3
F2-4
F2-5
F2-6
F2-7
F2-8
F2-9
F2-10
F1-00
F1-0
F1-1
F1-2
F1-3
F1-4
F1-5
F1-6
F1-7
F1-8
F1-9
F1-10
5G4 P84
74LS283
1F
1E
1D
1C
1B
1A
PULLUP 9 G
899-1-R2K
TO 3A, 4A, 5A, 6A PIN 13
TO 3B, 4B, 5B, 6B PIN 13
TO 4C, 5C, 6C, 7C PIN 13
TO 3D, 4D, 5D, 6D, 7D PIN 13
TO 4E, 5E, 6E, 7E PIN 13
TO 3F, 4F, 5F, 6F, 7F PIN 13
+ 5V
B 10/30/78 REPLACED 8RF 8B WITH 74LS14's
A 2/14/77 REPLACED 6 9LS08 CHIPS WITH 5 9LS174'S
REV. DATE DRAWN BY APPRV'D BY DESCRIPTION
VLA PROJECT
MAC SYSTEM
TITLE
INTEGRATING MEMORY
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO NEW MEXICO 87801
DRAWN BY DATE 1/1/76
DESIGNED BY DATE 11/1/76
APPROVED BY DATE 11/17/76
SHEET NUMBER 1 of 1
DRAWING NUMBER D13860L2
REV. B
SCALE

REV.	DATE	DRAWN BY	APPVR'D BY	DESCRIPTION
A	2/7/77			ADDED 9LS365 CHIPS
B	10/30/78			REPLACED 8A & 8B WITH 74LS14's



1	GND
2	+5V
3	GND
4	+5V
5	5G2-0
6	1
7	2
8	3
9	4
10	5
11	6
12	7
13	8
14	9
15	10
16	5G2-11
17	2GI-23
18	2GI-22
19	MI-23
20	MI-22
21	2GI-21
22	2GI-20
23	MI-21
24	MI-20
25	2GI-19
26	2GI-18
27	GND
28	
29	MI-19
30	MI-18
31	2GI-17
32	2GI-16
33	MI-17
34	MI-16
35	2GI-15
36	2GI-14
37	MI-15
38	MI-14
39	2GI-13
40	2GI-12
41	MI-13
42	MI-12
43	2GI-11
44	2GI-10
45	MI-11
46	MI-10
47	2GI-9
48	2GI-8
49	GND
50	
51	MI-9
52	MI-8
53	
54	
55	
56	
57	
58	
59	
60	
61	
62	
63	
64	2G2
65	
66	MI-25
67	MI-24
68	G1
69	2GI-7
70	2GI-6
71	MI-7
72	MI-6
73	GND
74	
75	2GI-5
76	2GI-4
77	MI-5
78	MI-4
79	2GI-3
80	2GI-2
81	MI-3
82	MI-2
83	2GI-1
84	2GI-0
85	MI-1
86	MI-0
87	
88	
89	
90	
91	
92	
93	
94	3-ST-CTL
95	5F5X WE
96	5F4X CE
97	GND
98	+5V
99	GND
100	+5V

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON

VLA PROJECT

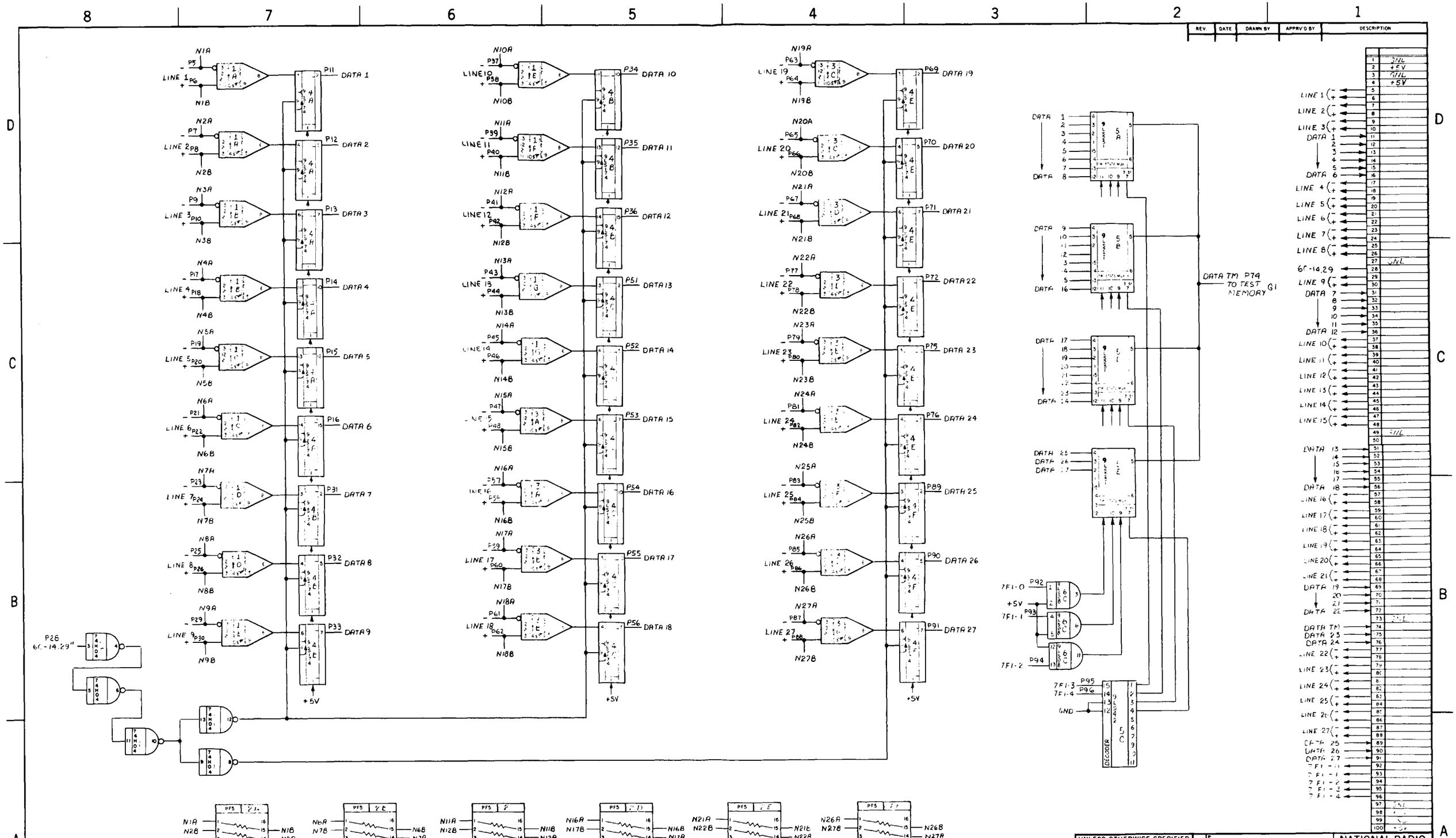
MAC SYSTEM

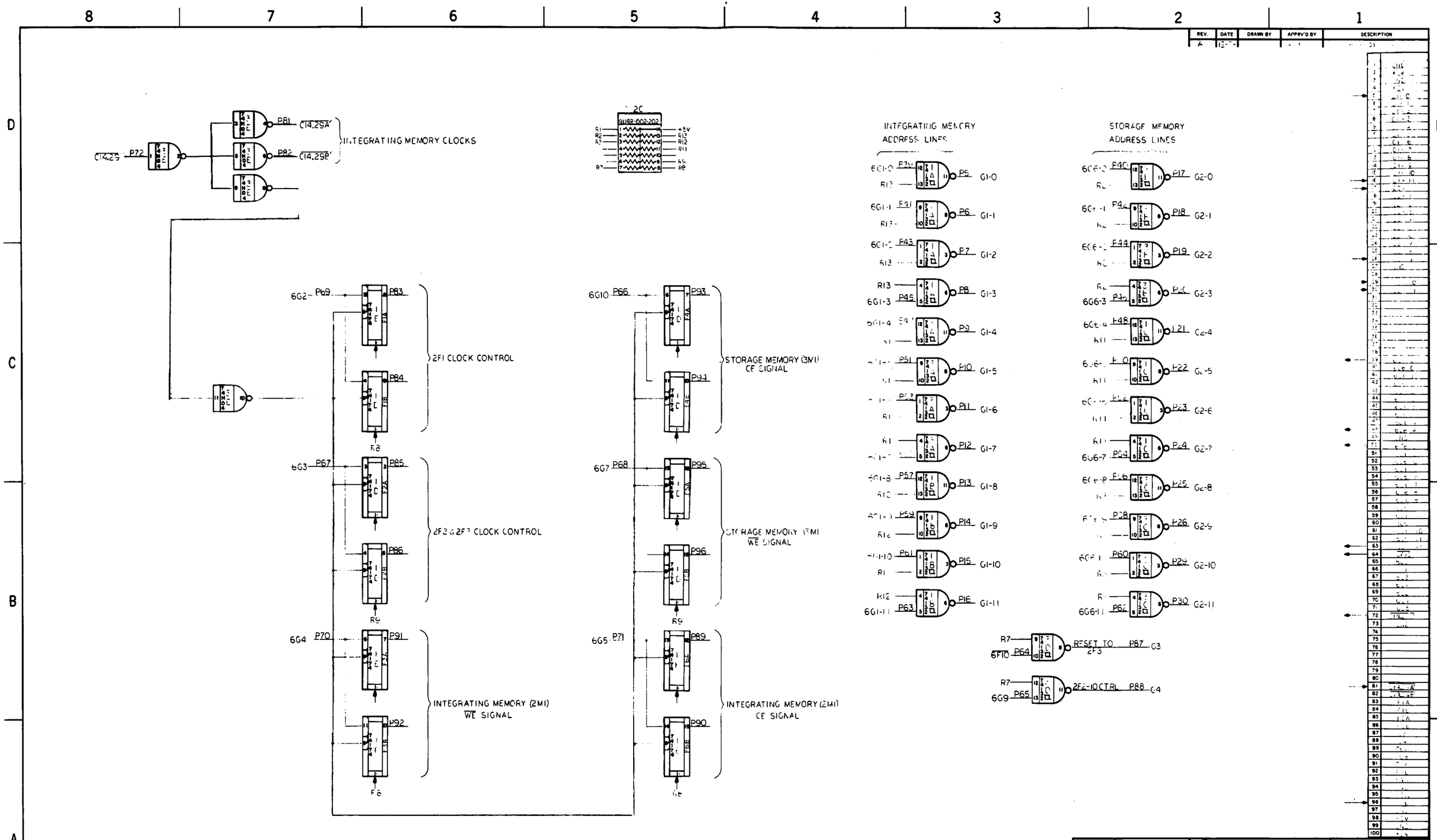
TITLE: STORAGE MEMORY

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 11/1/76
DESIGNED BY	DATE 11/1/76
APPROVED BY	DATE 11/17/76

SHEET NUMBER 1 of 1 | DRAWING NUMBER D13860L3 | REV. B | SCALE


8
7
6
5
4
3
2
1
D
C
B
A
REV.
DATE
DRAWN BY
APPRV'D BY
DESCRIPTION
LINE 1
LINE 2
LINE 3
LINE 4
LINE 5
LINE 6
LINE 7
LINE 8
LINE 9
LINE 10
LINE 11
LINE 12
LINE 13
LINE 14
LINE 15
LINE 16
LINE 17
LINE 18
LINE 19
LINE 20
LINE 21
LINE 22
LINE 23
LINE 24
LINE 25
LINE 26
LINE 27
DATA 1
DATA 2
DATA 3
DATA 4
DATA 5
DATA 6
DATA 7
DATA 8
DATA 9
DATA 10
DATA 11
DATA 12
DATA 13
DATA 14
DATA 15
DATA 16
DATA 17
DATA 18
DATA 19
DATA 20
DATA 21
DATA 22
DATA 23
DATA 24
DATA 25
DATA 26
DATA 27
+5V
GND
DATA TM P74 TO TEST MEMORY G1
DECODER
NOTE: ALL RESISTORS ARE 100Ω
* NOT USED
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
PROJECT
VLA
MAC SYSTEM
TITLE
DATA MULTIPLEXER
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DATE
DESIGNED BY
APPROVED BY
SHEET NUMBER 1 of 1
DRAWING NUMBER D1556.1.4
REV.
SCALE



REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	12-[illegible]			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY | USED ON

PROJECT: MAC SYSTEM

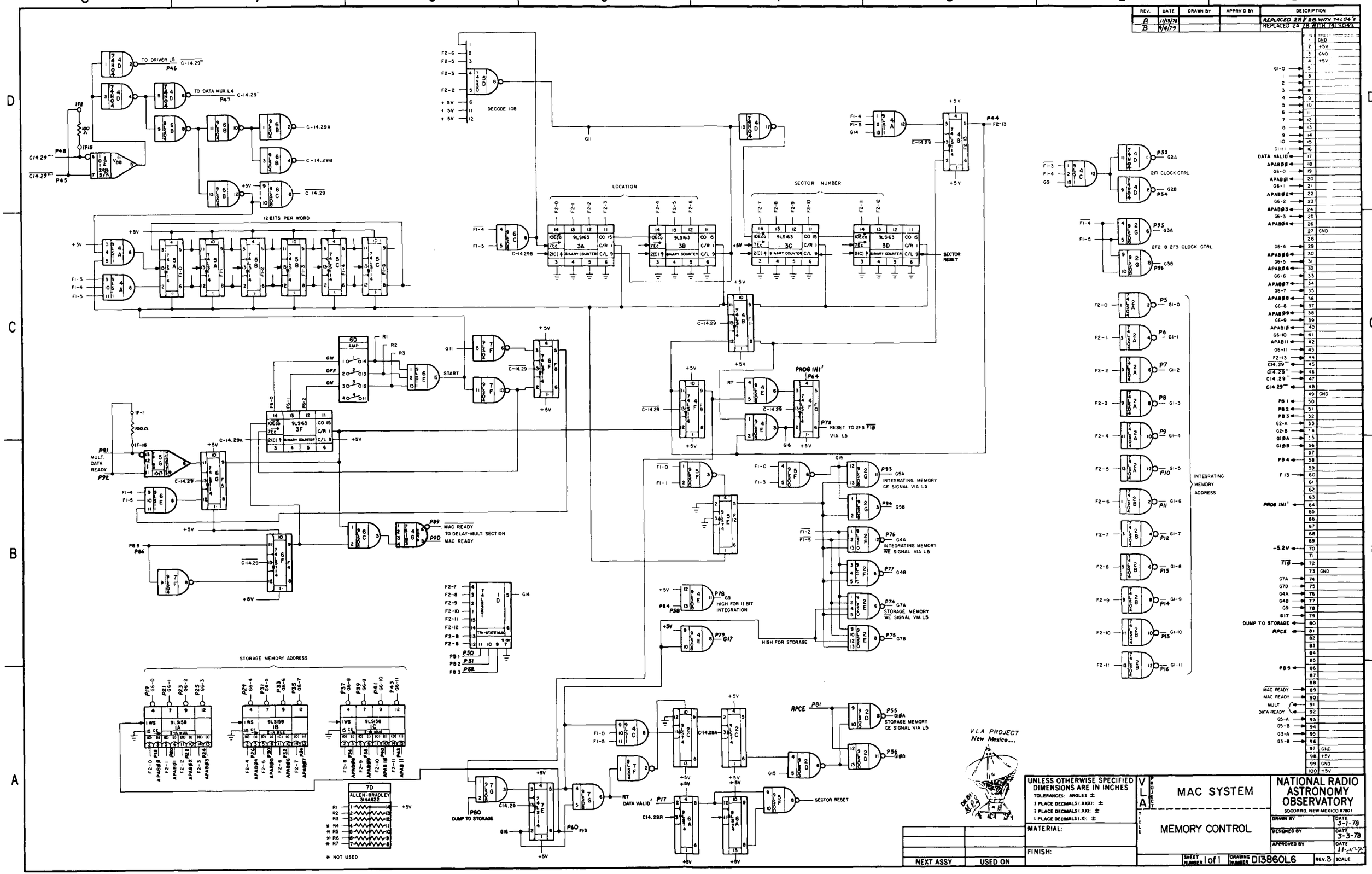
TITLE: DRIVER

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE 12-21-78
DESIGNED BY | DATE 12-21-78
APPROVED BY | DATE

SHEET NUMBER 1 of 1 | DRAWING NUMBER D138601-5 | REV. A | SCALE

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	11/13/78			REPLACED 2A & 2B WITH 74LS04's
B	4/6/79			REPLACED 2A 2B WITH 74LS04's



VLA PROJECT New Mexico...

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY | USED ON

VLA PROJECT

TITLE: MAC SYSTEM

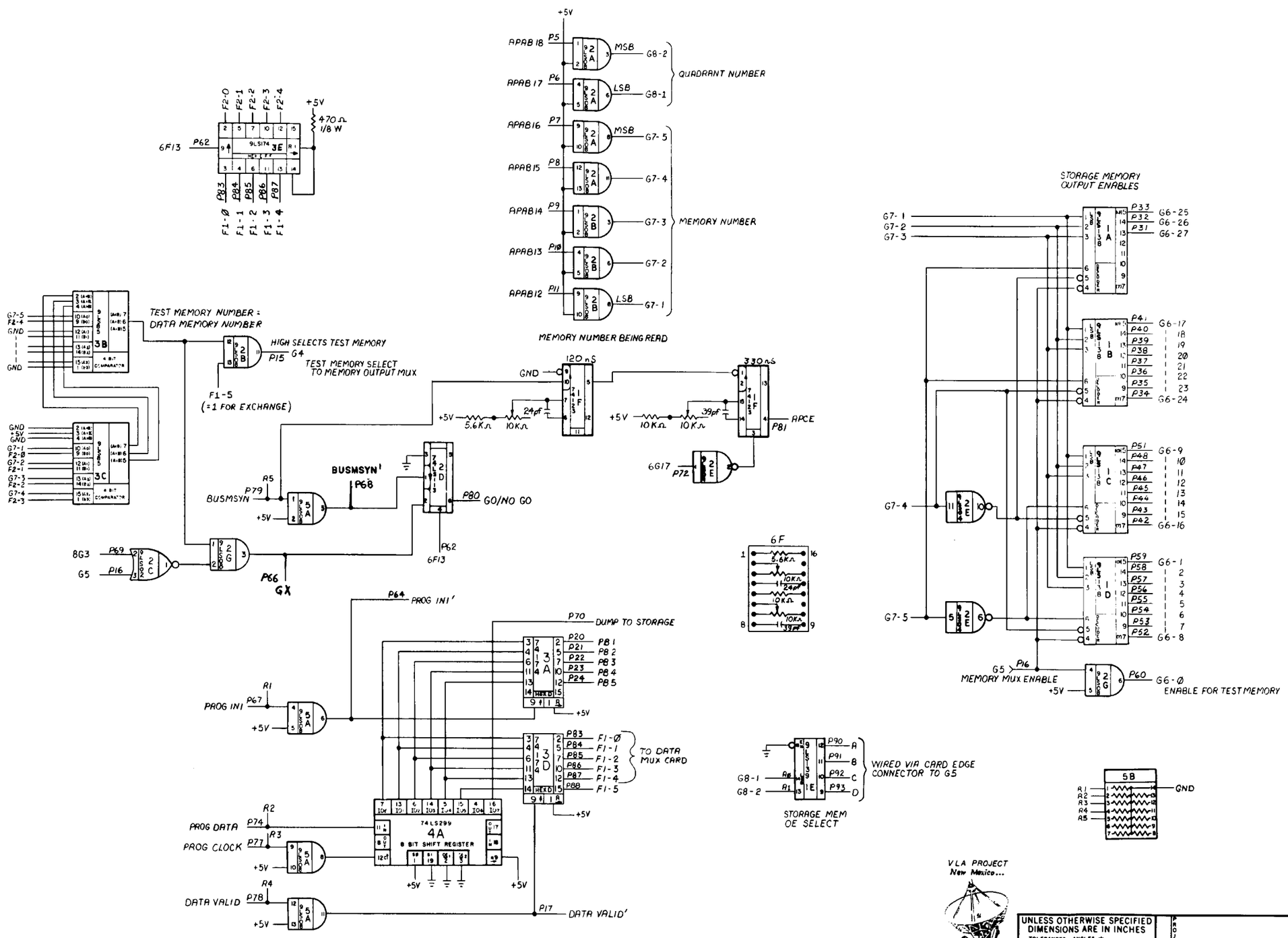
MEMORY CONTROL

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

		DATE
DRAWN BY		3-1-78
DESIGNED BY		3-3-78
APPROVED BY		11-[illegible]

SHEET NUMBER 1 of 1 | DRAWING NUMBER D13860L6 | REV. B | SCALE

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	4/4/79			APPRD FIRST [illegible]



VLA PROJECT New Mexico...

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY | USED ON

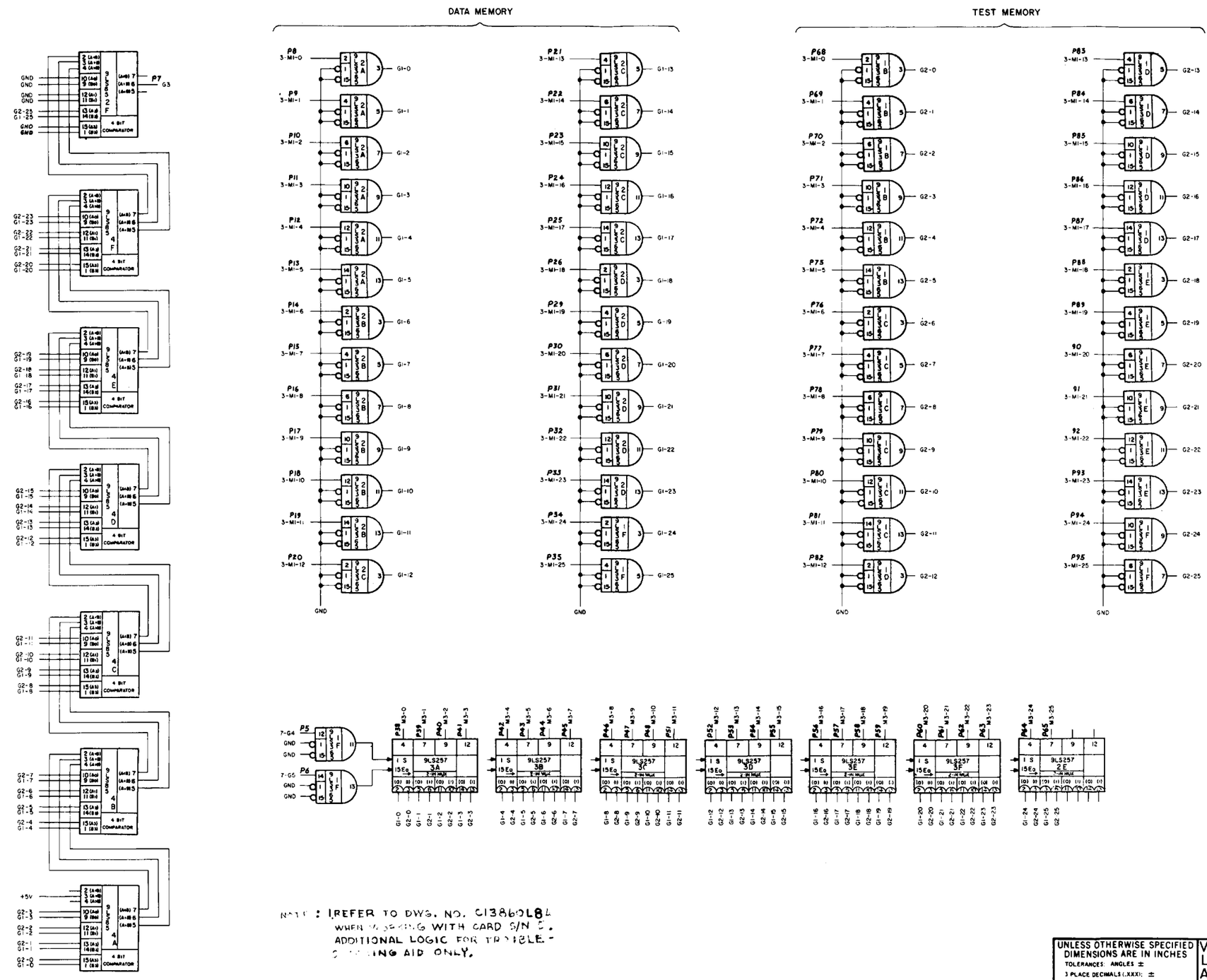
PROJECT

TITLE: TEST MEMORY CONTROL

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY		DATE
DESIGNED BY		DATE 9-6-78
APPROVED BY		DATE 11-20-78

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D13860L7 | REV. A | SCALE



NOTE: REFER TO DWG. NO. D13860L8L WHEN WORKING WITH CARD S/N [illegible]. ADDITIONAL LOGIC FOR TROUBLE-SHOOTING AID ONLY.

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

1	GND
2	+5V
3	GND
4	+5V
5	7-G4
6	7-G5
7	G3
8	3MI-0
9	-1
10	-2
11	-3
12	-4
13	-5
14	-6
15	-7
16	-8
17	-9
18	-10
19	-11
20	-12
21	-13
22	-14
23	-15
24	-16
25	-17
26	-18
27	GND
28	
29	-19
30	-20
31	-21
32	-22
33	-23
34	-24
35	3MI-25
36	
37	
38	M3-0
39	-1
40	-2
41	-3
42	-4
43	-5
44	-6
45	-7
46	-8
47	-9
48	-10
49	GND
50	
51	-11
52	-12
53	-13
54	-14
55	-15
56	-16
57	-17
58	-18
59	-19
60	-20
61	-21
62	-22
63	-23
64	-24
65	M3-25
66	
67	
68	3MI-0
69	-1
70	-2
71	-3
72	-4
73	GND
74	
75	-5
76	-6
77	-7
78	-8
79	-9
80	-10
81	-11
82	-12
83	-13
84	-14
85	-15
86	-16
87	-17
88	-18
89	-19
90	-20
91	-21
92	-22
93	-23
94	-24
95	3MI-25
96	
97	GND
98	+5V
99	GND
100	+5V

DATA MEMORY

TEST MEMORY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON

PROJECT: VLA

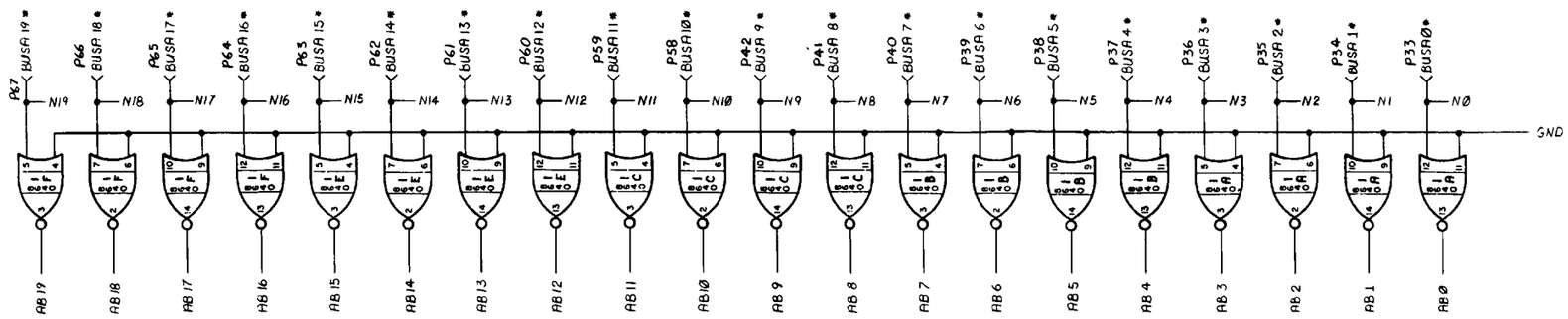
MAC SYSTEM

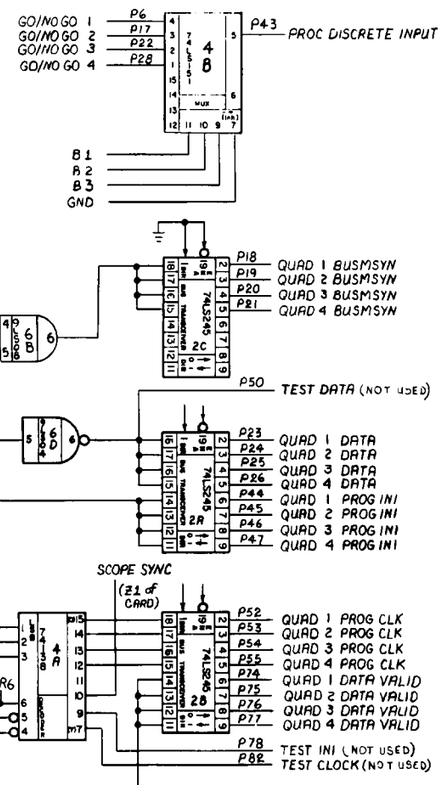
TITLE: MEMORY OUTPUT MUX

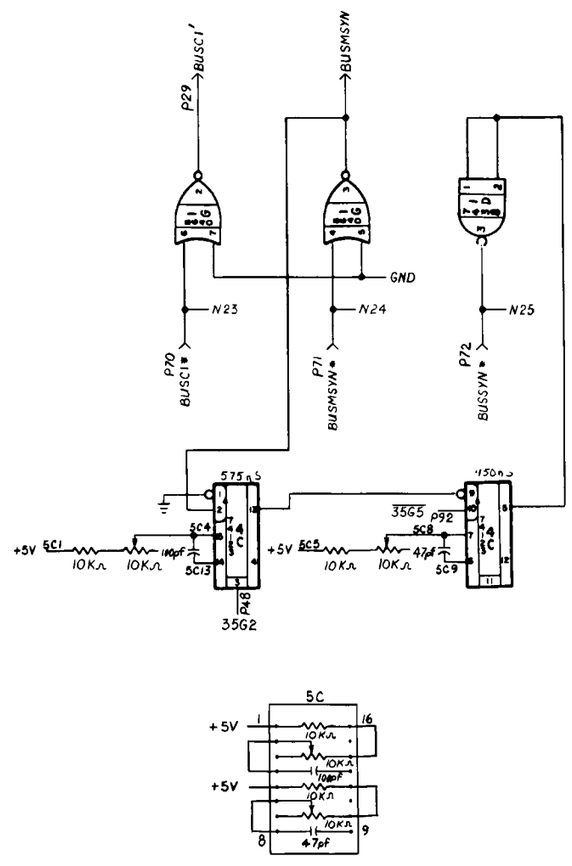
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

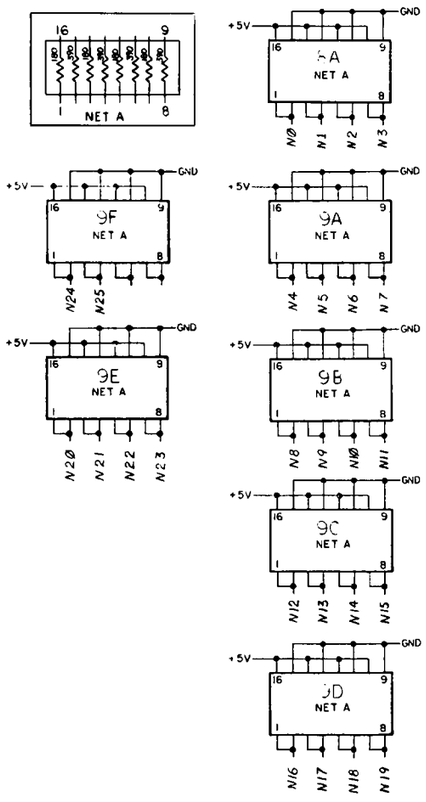
DRAWN BY		DATE 09-05-77
DESIGNED BY		DATE [illegible]
APPROVED BY		DATE [illegible]
SHEET NUMBER 1 of 1	DRAWING NUMBER D13860L8	REV. / SCALE

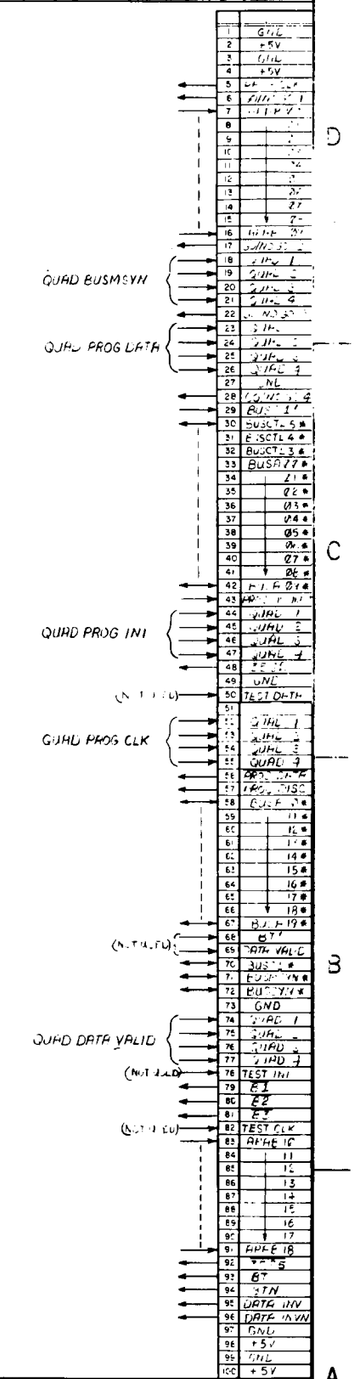
REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	5.79			[illegible]











VLA PROJECT
New Mexico...

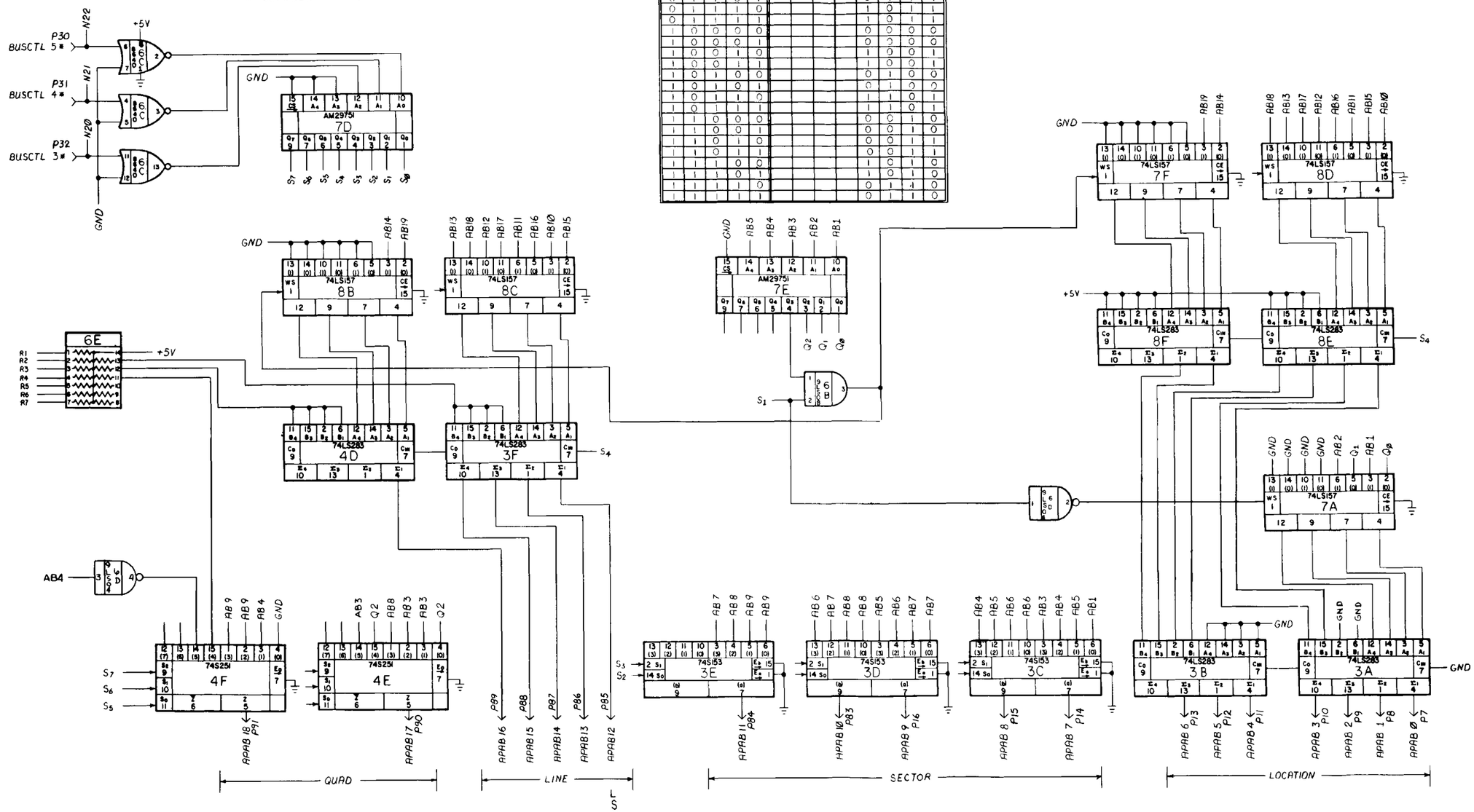
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		PROJECT	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801
TOLERANCES: ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ±		TITLE FPS ADDRESS BUS BUFFER DECODER	DRAWN BY — DATE 5-3-78
MATERIAL:			DESIGNED BY — DATE 5-7-78
FINISH:			APPROVED BY — DATE [illegible]
NEXT ASSY	USED ON	SHEET NUMBER 1 OF 2	DRAWING NUMBER D13860L31 REV. A SCALE

MODE	NO	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0
CONTINUUM (AC)	0	0	0	0	0	0	0	1	0
CONTINUUM (BD)	1	1	0	0	0	0	0	1	0
SINGLE BAND SPECTRAL LINE (A or C)	2	0	0	1	0	0	1	0	1
DUAL BAND SPECTRAL LINE	3	0	1	0	0	1	0	0	1
FOUR BAND SPECTRAL LINE	4	0	1	1	0	1	1	0	1
SINGLE BAND SPECTRAL (B or D)	5	1	0	1	0	0	1	0	1
RESERVED FOR OUTPUT TO CORE A *	6	–	–	–	–	–	–	–	–
" " " " " B *	7	–	–	–	–	–	–	–	–

* = DECODED ON L35

AM29751 TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0					1	0	0	0
0	0	0	0	1					1	0	0	0
0	0	0	1	0					0	0	0	1
0	0	0	1	1					0	0	0	1
0	0	1	0	0					1	1	0	0
0	0	1	0	1					1	1	0	0
0	0	1	1	0					0	1	0	1
0	0	1	1	1					0	1	0	1
0	1	0	0	0					1	1	1	1
0	1	0	0	1					1	1	1	1
0	1	0	1	0					1	1	1	0
0	1	0	1	1					1	1	1	0
0	1	1	0	0					0	1	1	1
0	1	1	0	1					0	1	1	1
0	1	1	1	0					1	0	1	1
0	1	1	1	1					1	0	1	1
1	0	0	0	0					0	0	0	0
1	0	0	0	1					0	0	0	0
1	0	0	1	0					1	0	0	1
1	0	0	1	1					1	0	0	1
1	0	1	0	0					0	1	0	0
1	0	1	0	1					0	1	0	0
1	0	1	1	0					1	1	0	1
1	0	1	1	1					1	1	0	1
1	1	0	0	0					0	0	1	0
1	1	0	0	1					0	0	1	0
1	1	0	1	0					0	0	1	1
1	1	0	1	1					0	0	1	1
1	1	1	0	0					1	0	1	0
1	1	1	0	1					1	0	1	0
1	1	1	1	0					0	1	1	0
1	1	1	1	1					0	1	1	0



NOTE: REFER TO DWG. NO. C13860L31A WHEN WORKING WITH CARD S/N 1. ADDITIONAL LOGIC FOR TROUBLE-SHOOTING AID ONLY.

VLA PROJECT
New Mexico...

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

1	GND
2	+5V
3	GND
4	+5V
27	GND
49	GND
73	GND
97	GND
98	+5V
99	GND
100	+5V

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY | USED ON

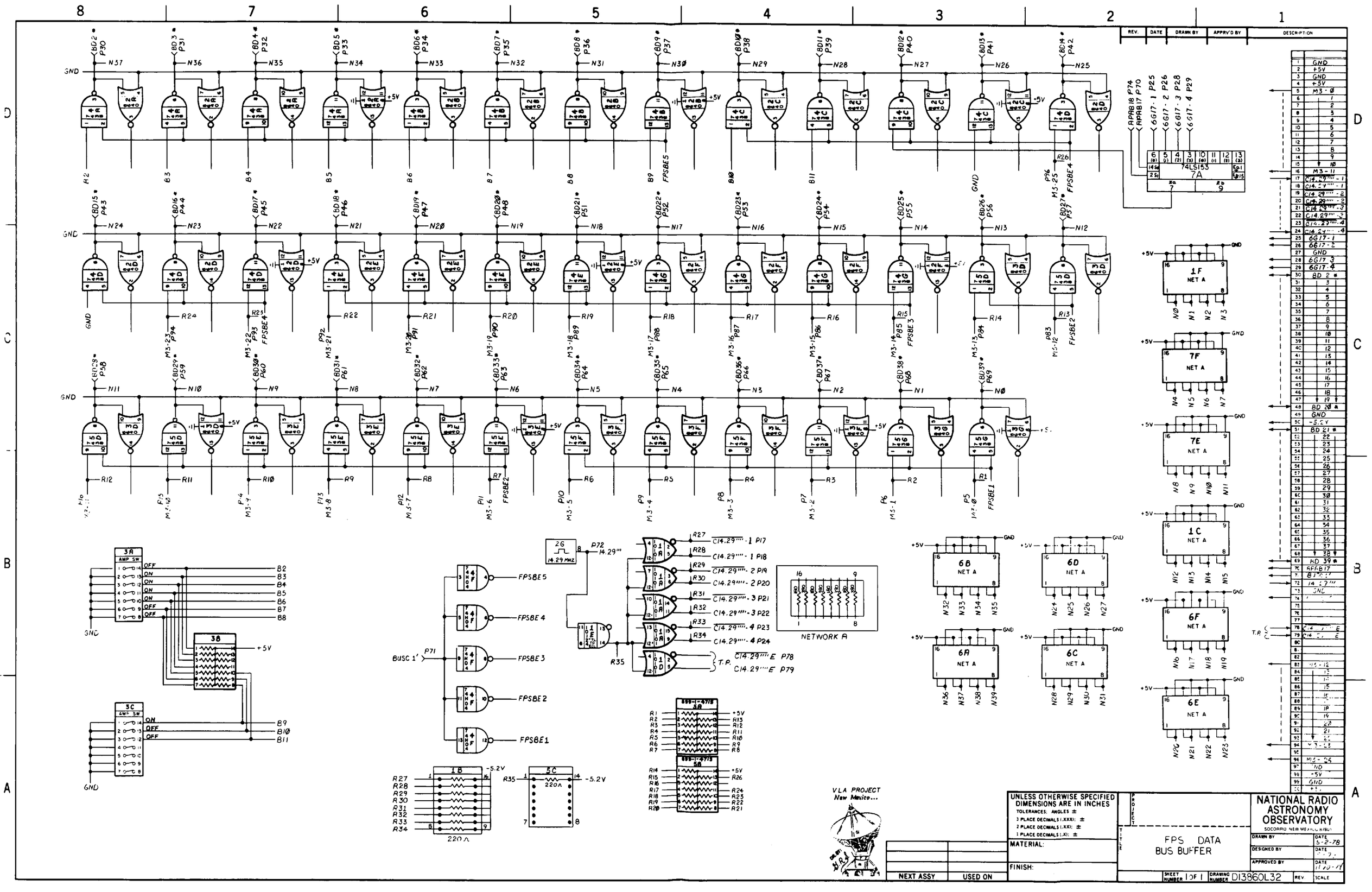
PROJECT

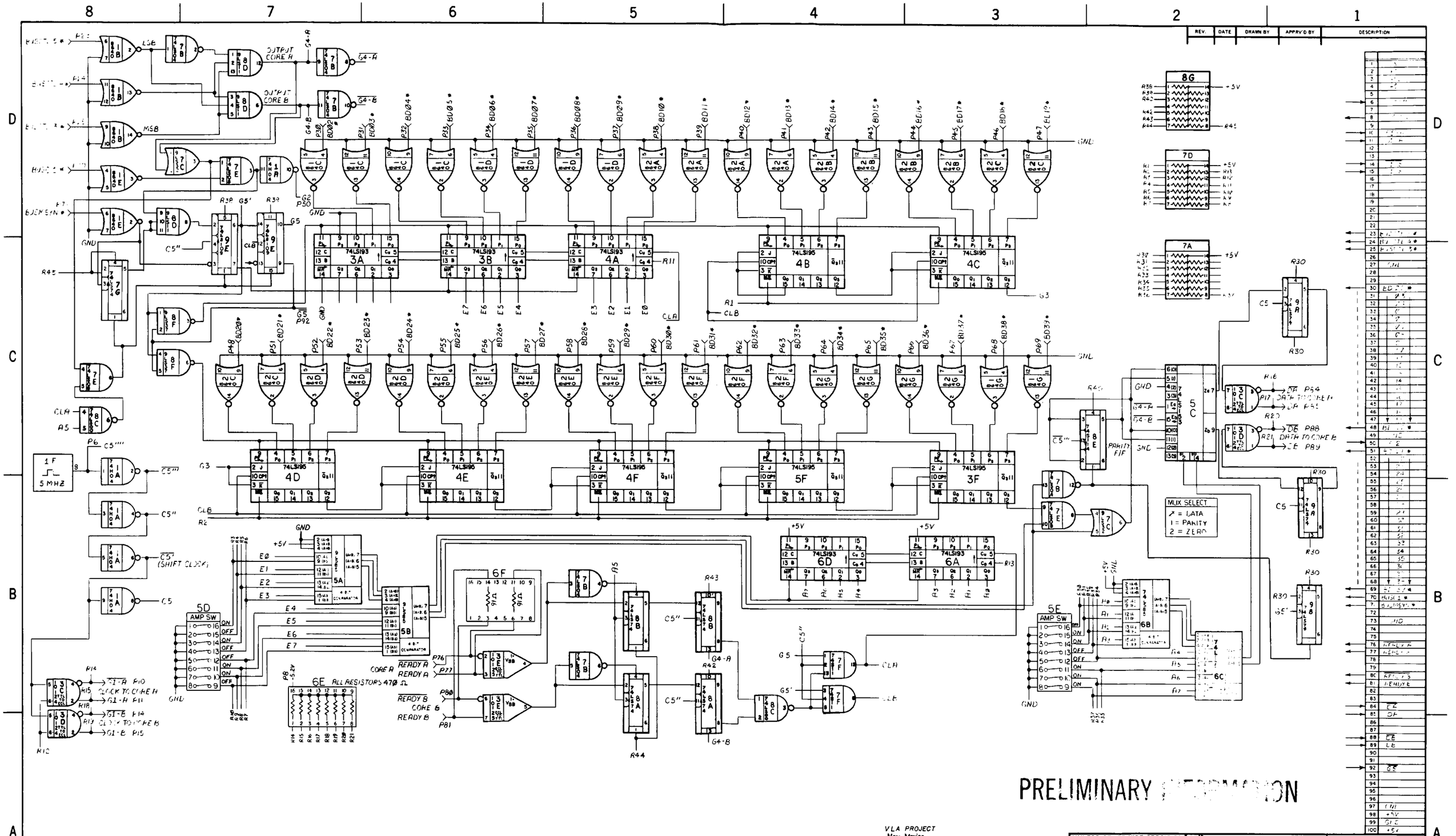
TITLE: FPS ADDRESS BUS BUFFER/DECODER

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE
DESIGNED BY | DATE 7-78
APPROVED BY | DATE 11-20-78

SHEET NUMBER 2 OF 2 | DRAWING NUMBER D13860L31 | REV. A | SCALE


8 7 6 5 4 3 2 1
D C B A
GND
+5V
74LS153
7A
1F NET A
7F NET A
7E NET A
1C NET A
6F NET A
6E NET A
6B NET A
6D NET A
6A NET A
6C NET A
NETWORK A
3A AMP SW
3C AMP SW
3B
1B
5C
220Ω
BUSC 1'
P71
P72
14.29 MHZ
FPSBE5
FPSBE4
FPSBE3
FPSBE2
FPSBE1
T.P.
VLA PROJECT
New Mexico...
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
TITLE
FPS DATA
BUS BUFFER
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO NEW MEXICO 87801
DRAWN BY
DATE 5-2-78
DESIGNED BY
APPROVED BY
SHEET NUMBER 1 OF 1
DRAWING NUMBER D13860L32
REV.
SCALE



REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

VLA PROJECT
New Mexico...

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON

PROJECT

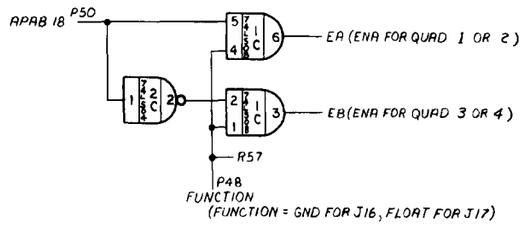
TITLE: FPS TO MODCOMP FORMATTER (LOCATION 2-J5)

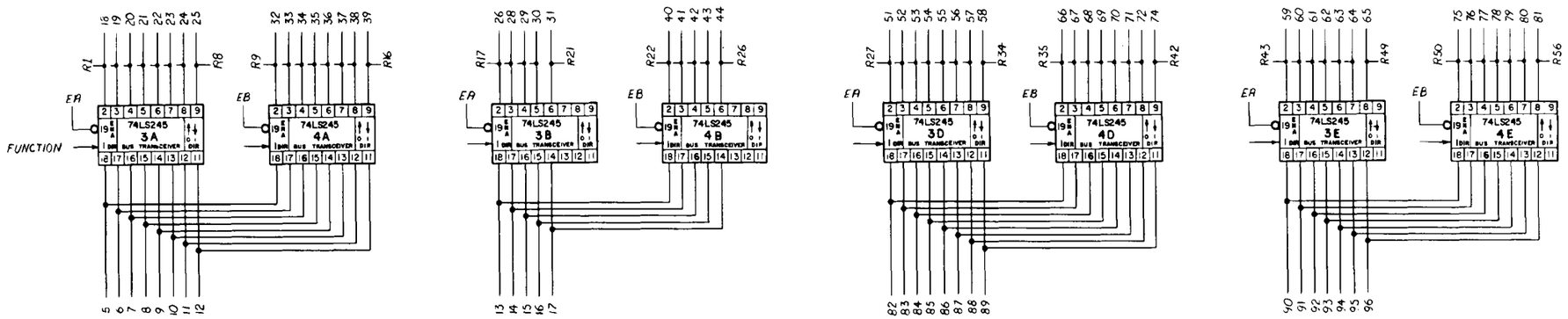
SHEET NUMBER | DRAWING NUMBER D13860L35 | REV. | SCALE

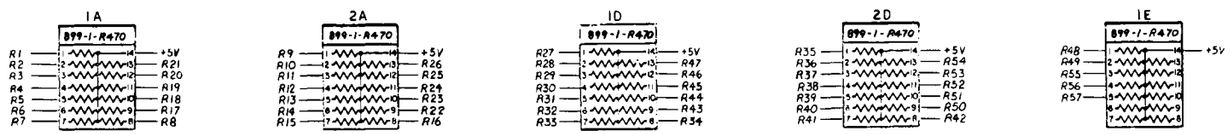
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY		DATE 5-26-78
DESIGNED BY		DATE 7-6-78
APPROVED BY		DATE 9-1-78

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION







NOTE:
RESISTORS ON ALL UPPER I/O PINS
EXCEPT APAB18 (IN ROW)

	J16		J17
1	GND		GND
2	+5V		+5V
3	GND		GND
4	+5V		+5V
5			[illegible]
6			
7	[illegible]		[illegible]
8			[illegible]
9			[illegible]
10			[illegible]
11			[illegible]
12			[illegible]
13			[illegible]
14			[illegible]
15			[illegible]
16	[illegible]		M3-11
17			
18			M3-[illegible]-A
19			[illegible]
20	APAB-0-A		[illegible]
21			[illegible]
22			[illegible]
23			[illegible]
24			[illegible]
25			[illegible]
26	APAB-1-A		M3-[illegible]-A
27	GND		GND
28	APAB-7-A		M3-9-A
29	APAB-3-A		M3-10-A
30	APAB-[illegible]-A		M3-11-A
31			
32			M3-[illegible]-B
33			
34	APAB-1-B		[illegible]
35			[illegible]
36			[illegible]
37			[illegible]
38			[illegible]
39			[illegible]
40			[illegible]
41			[illegible]
42			[illegible]
43	APAB-[illegible]-B		M3-11-B
44			
45			
46			
47			
48	FUNCTION		FUNCTION
49	GND		GND
50			APAB-10
51			
52	[illegible]-17-A		[illegible]-A
53			[illegible]
54			12
55			13
56			14
57			15
58			[illegible]
59			17
60	APAB-[illegible]-A		[illegible]
61	COMP-A		[illegible]
62			[illegible]
63			[illegible]
64			[illegible]
65			M3-[illegible]-A
66			
67	APAB-[illegible]-B		M3-[illegible]-B
68			[illegible]
69			14
70			15
71			[illegible]
72	APAB-[illegible]-B		M3-[illegible]-B
73	GND		GND
74	[illegible]		M3-[illegible]-B
75	[illegible]		[illegible]
76	[illegible]		[illegible]
77	COMP-B		21
78			22
79			23
80			24
81			M3-[illegible]-B
82			
83	[illegible]		M3-12
84			[illegible]
85			14
86			15
87			[illegible]
88			[illegible]
89			[illegible]
90			[illegible]
91	APAB-[illegible]		[illegible]
92	COMP		[illegible]
93			
94			23
95			24
96			M3-25
97	GND		GND
98	+5V		+5V
99	GND		GND
100	+5V		+5V

VLA PROJECT
New Mexico...

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

PROJECT

TITLE: QUADRANT FAN OUT/FAN IN

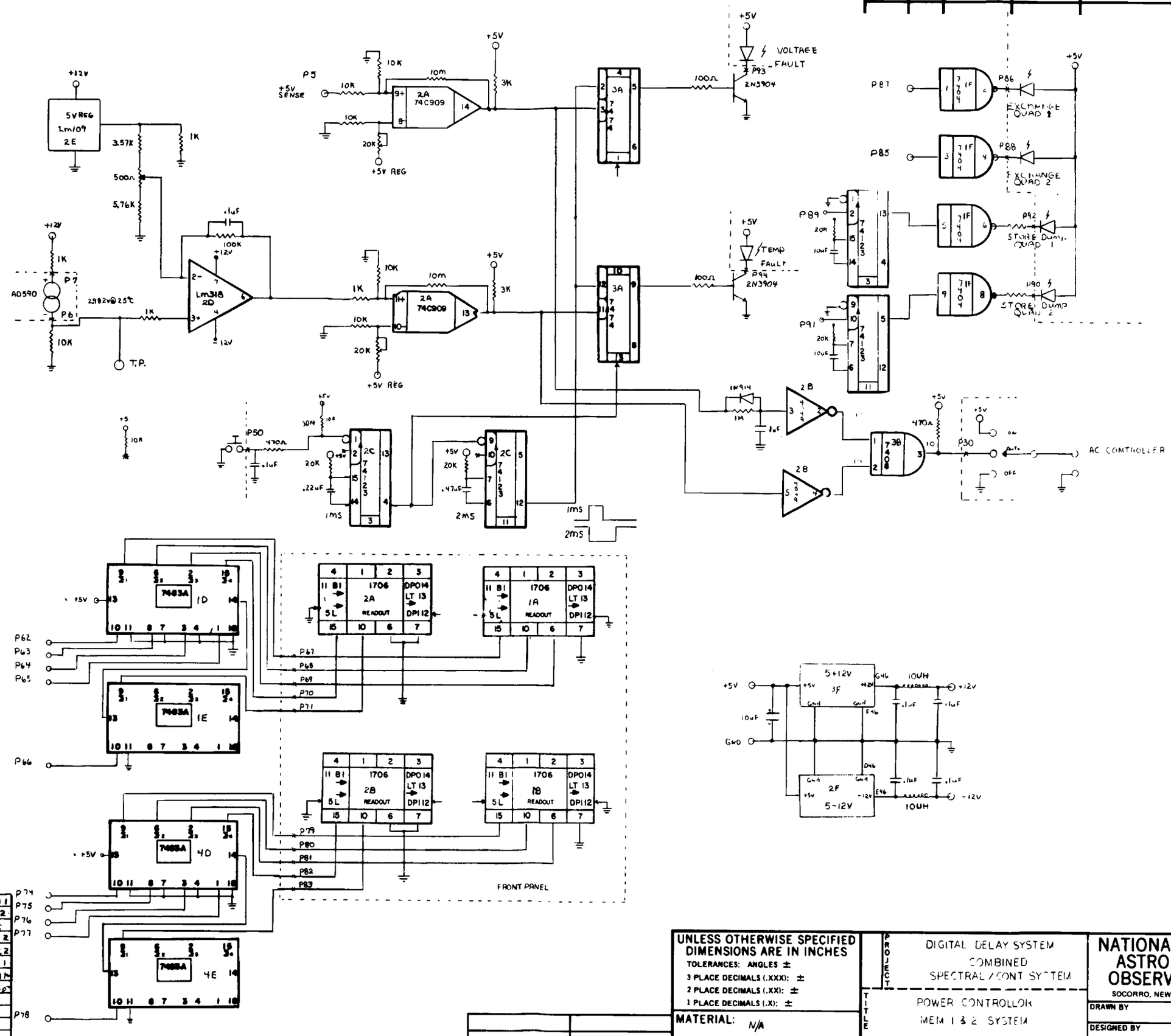
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 5-22-78
DESIGNED BY	DATE 5-6-78
APPROVED BY	DATE 7-6-78

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D13860L36 | REV | SCALE

1	GND
2	+5V
3	GND
4	+5V
5	+5V SENSE
6	Temp Sense −
7	Temp Sense +
8	GND CASE
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	GND
28	
29	
30	Auto SW
31	
32	
33	
34	
35	
36	
37	
38	
39	
40	
41	
42	
43	
44	
45	
46	
47	
48	
49	
50	RESET SW
51	
52	
53	
54	
55	
56	
57	
58	
59	
60	
61	
62	FI-0 Quad 1
63	FI-1
64	FI-2
65	FI-3
66	FI-4
67	1B1
68	1B2
69	1B4
70	1B1
71	1B2
72	
73	GND
74	FI-0 Quad 2
75	FI-1
76	FI-2
77	FI-3
78	FI-4
79	2B1
80	2B2
81	2B4
82	2B1
83	2B2
84	
85	Exchange Quad 2
86	LED " " 1

87	Exchange Quad 1 1
88	LED " " 2
89	Store Dump Quad
90	LED " " 2
91	Store Dump Quad 2
92	LED " " 1
93	LED Fault Volt
94	LED Fault Temp
95	
96	
97	GND
98	+5V
99	GND
100	+5V



REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL: N/A

FINISH: N/A

NEXT ASSY	USED ON

PROJECT: DIGITAL DELAY SYSTEM COMBINED SPECTRAL / CONT SYSTEM

TITLE: POWER CONTROLLOR MEM 1 & 2 SYSTEM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

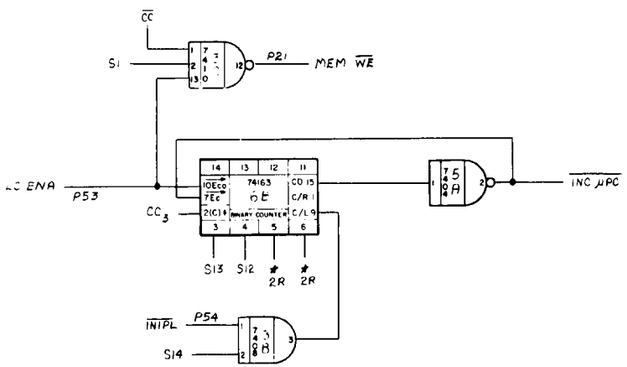
DRAWN BY	DATE 4/2/79
DESIGNED BY	DATE 3/25/79
APPROVED BY	DATE 2/1/[illegible]

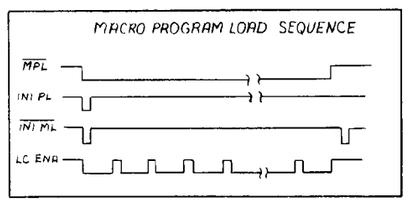
SHEET NUMBER 1 OF 1 | DRAWING NUMBER C 13860 L37 | REV. | SCALE

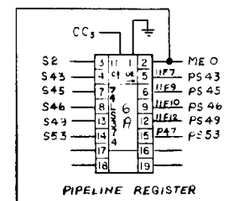
DRAWING SECTION 4 Drawings related to the system controller

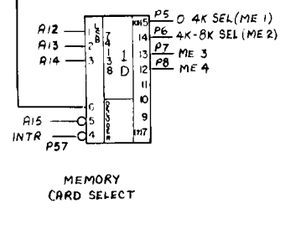
D13800L11
D13800L12
D13800L13
D13800L14
D13800L15
D13800L16
D13800L17
D13800L22
D13800L28

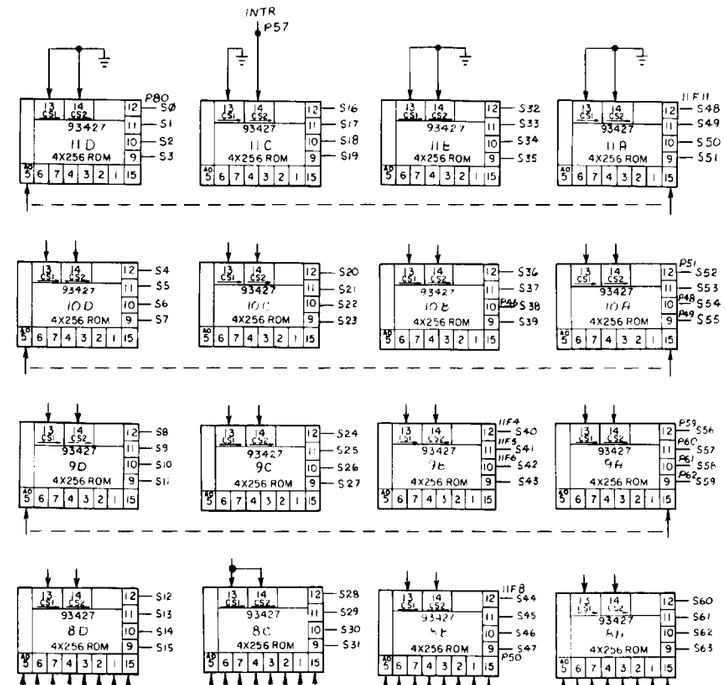
REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

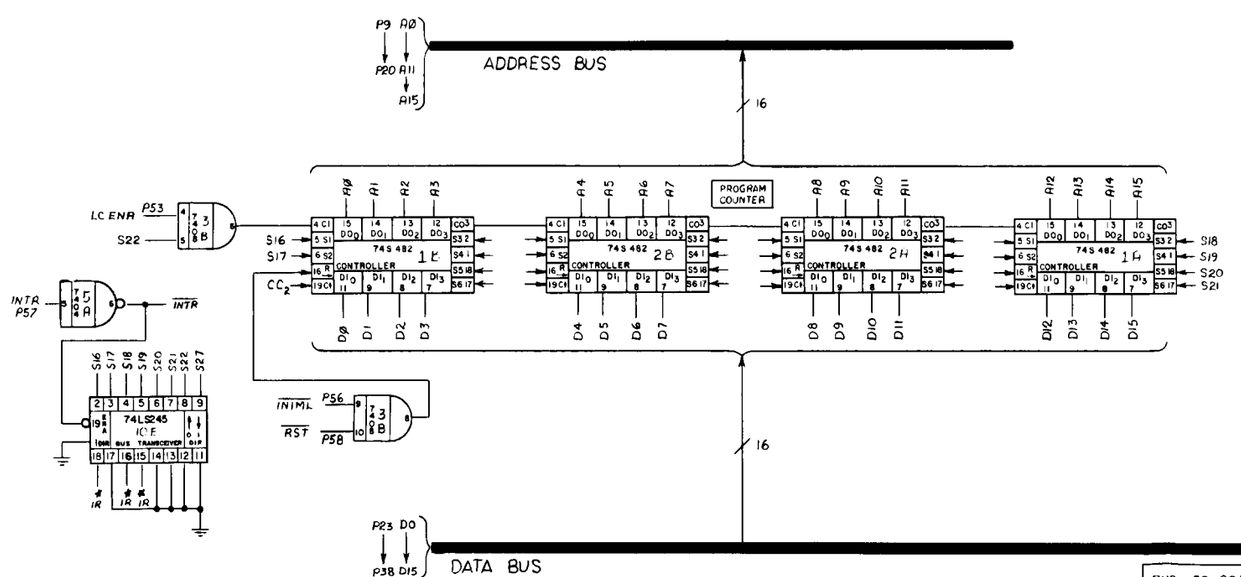


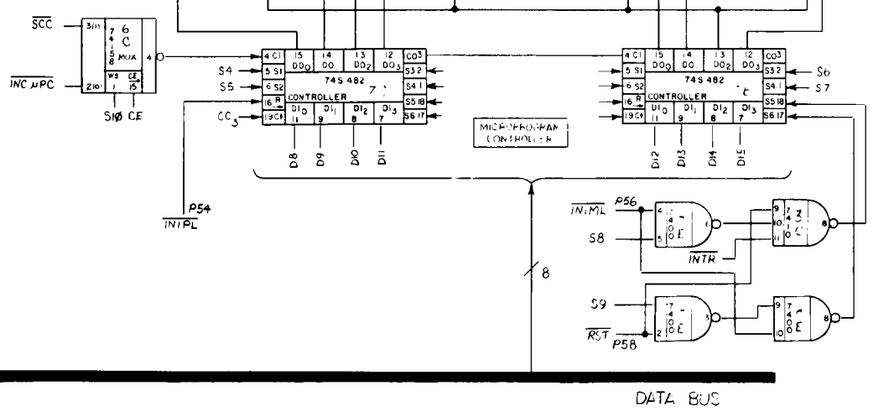




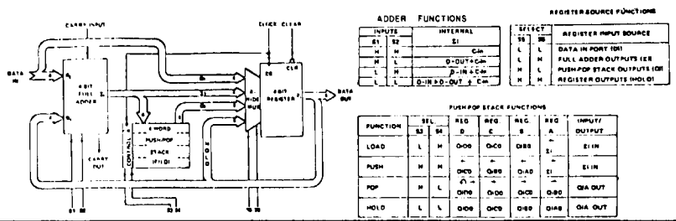








I/O CONNECTOR TO RESISTER CARD PLATFORM AT 11F			
PIN	SIGNAL	PIN	SIGNAL
1	S31	9	PS45
2	S27	10	PS46
3	S30	11	S48
4	S40	12	PS49
5	S41	13	GND
6	S42	14	GND
7	PS43	15	CRY
8	S44	16	CONDITION



74S482 CONTROLLER

BUS SOURCES

DATA BUS	
DE0	+ REGISTER CARD
DE1	MEM → DATA BUS
DE2	CONDITION REGISTER
DE3	* I/O CARDS
DE4	CONTROL CARD
DE5	
DE6	
DE7	

* ALSO NEEDS S52 = 0
\+ ALSO NEEDS S27 = 0

AUX DATA BUS	
AE0	* REGISTER CARD
AE1	ACCUMULATOR
AE2	
AE3	

* ALSO NEEDS S30 = 0

MEMORY DATA BUS	
ME0	DATA → MEMORY BUS
ME1	0-4K MEMORY
ME2	4-8K MEMORY
ME3	SPARE MEMORY
ME4	SPARE MEMORY

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

VLA PROJECT

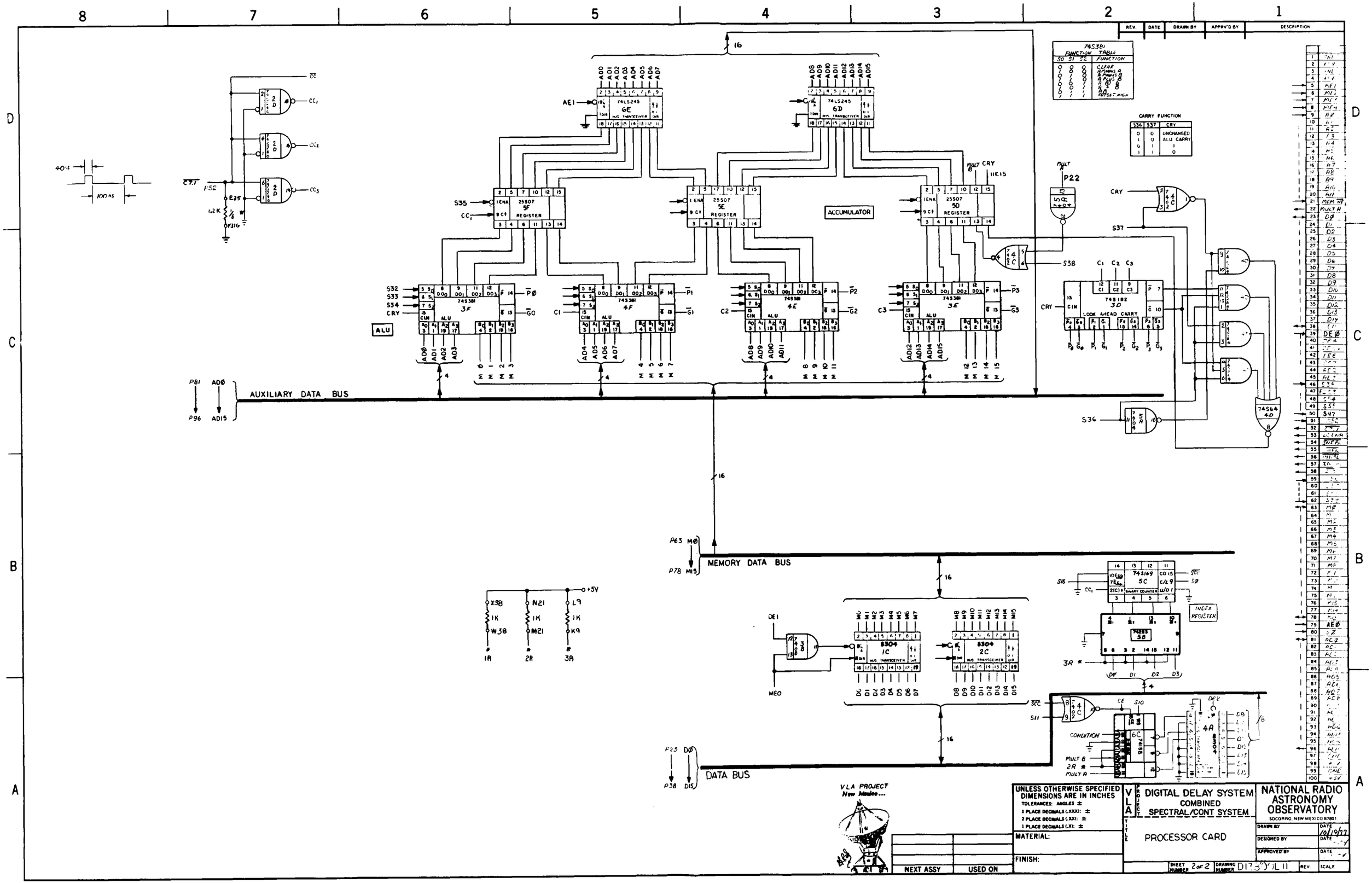
DIGITAL DELAY SYSTEM
COMBINED
SPECTRAL/CONT SYSTEM

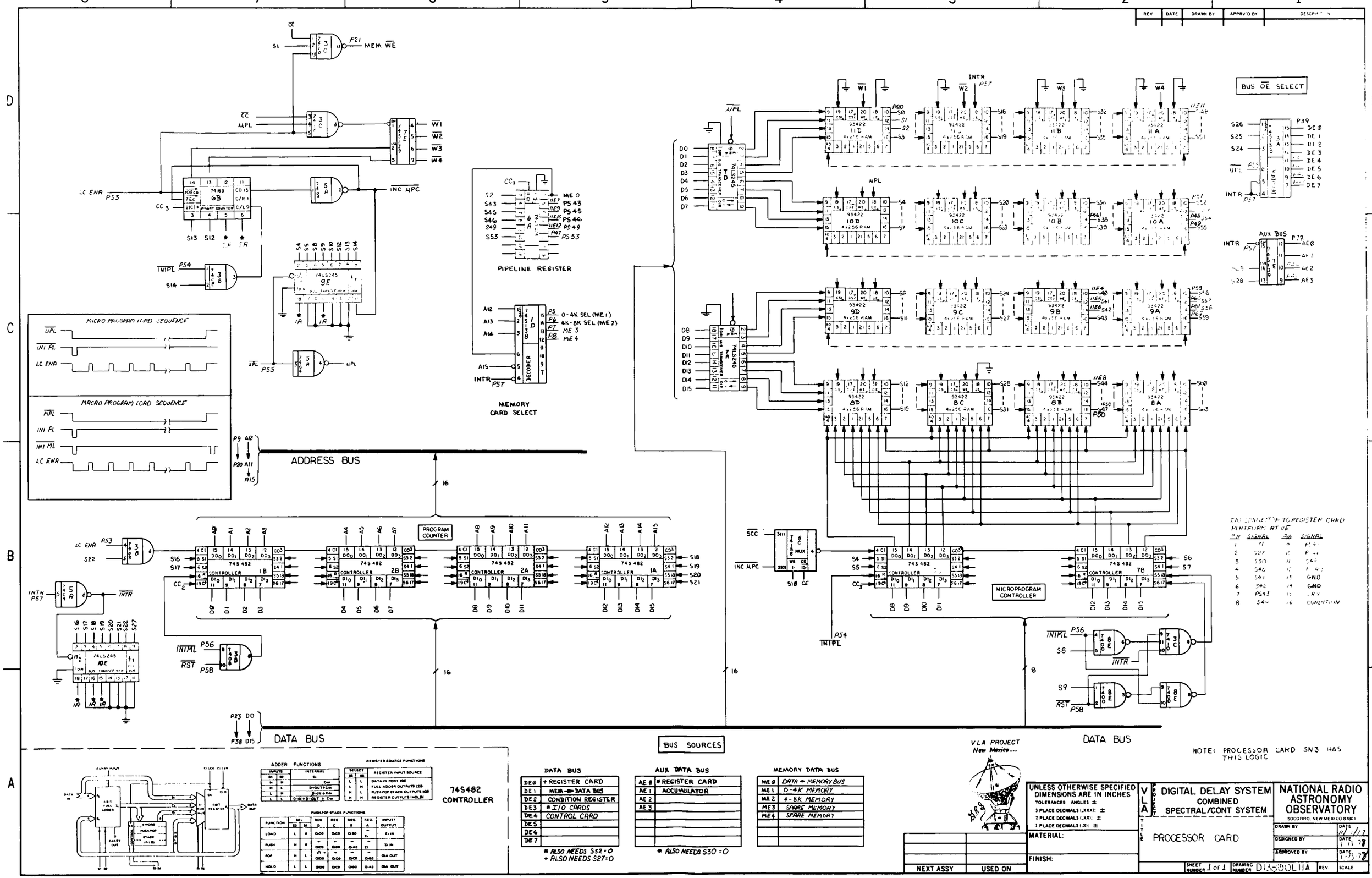
TITLE: PROCESSOR CARD

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

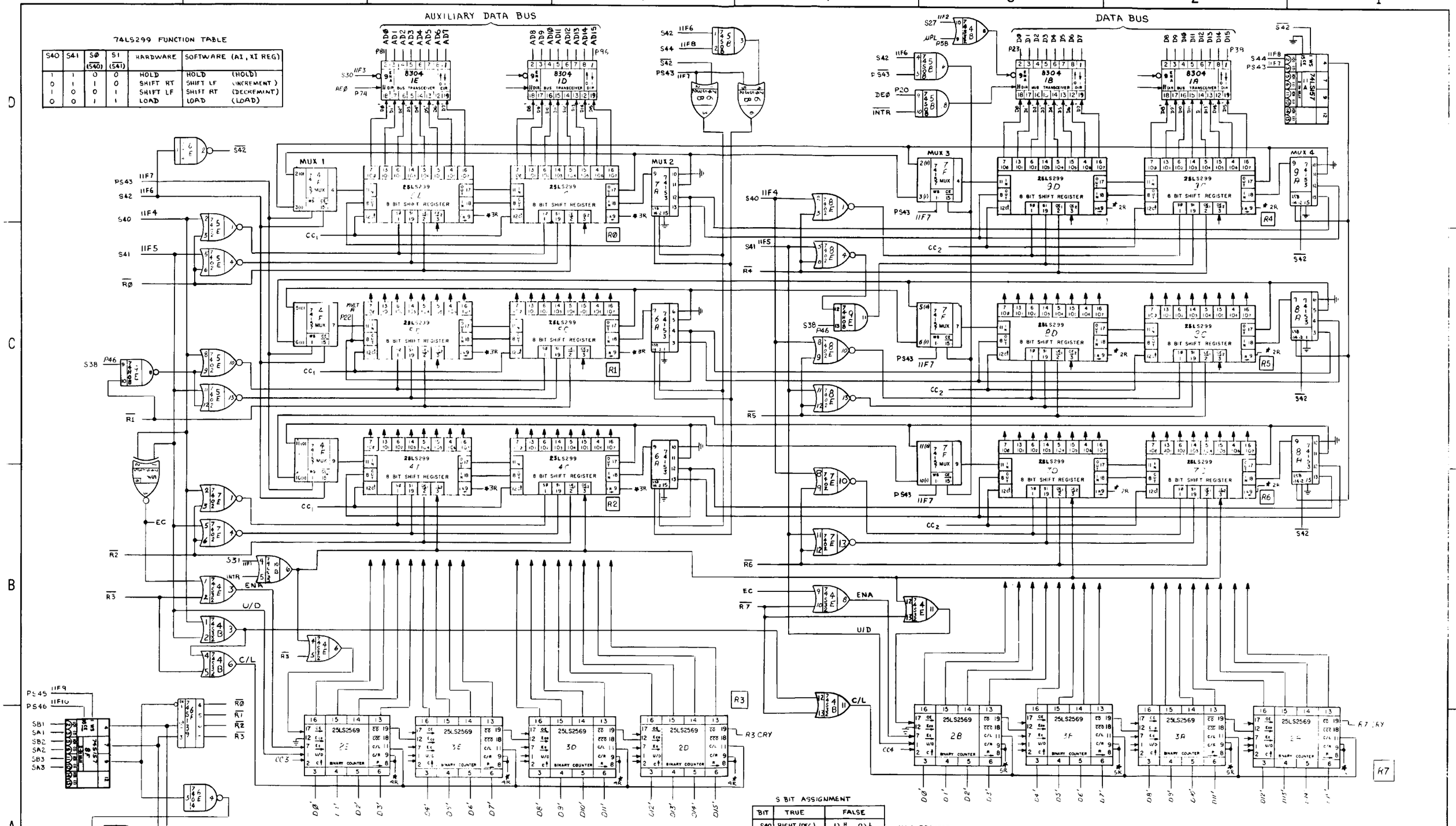
DRAWN BY		DATE	12/15/78
DESIGNED BY		DATE	/ /
APPROVED BY		DATE	/ /

SHEET NUMBER 1 OF 2 | DRAWING NUMBER D13800L11 | REV. | SCALE


REV. | DATE | DRAWN BY | APPRV'D BY | DESCRIPTION
74S381 FUNCTION TABLE
CARRY FUNCTION
ACCUMULATOR
ALU
AUXILIARY DATA BUS
MEMORY DATA BUS
DATA BUS
INDEX REGISTER
VLA PROJECT New Mexico...
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
VLA
DIGITAL DELAY SYSTEM
COMBINED SPECTRAL/CONT SYSTEM
TITLE
PROCESSOR CARD
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DATE 10/19/77
DESIGNED BY
APPROVED BY
SHEET NUMBER 2 OF 2
DRAWING NUMBER D173701L11
REV.
SCALE



NOTE: PROCESSOR CARD SN3 HAS THIS LOGIC



74LS299 FUNCTION TABLE

S40	S41	S0 (S40)	S1 (S41)	HARDWARE	SOFTWARE (A1, X1 REG)	
1	1	0	0	HOLD	HOLD	(HOLD)
0	1	1	0	SHIFT RT	SHIFT LF	(INCREMENT)
1	0	0	1	SHIFT LF	SHIFT RT	(DECREMENT)
0	0	1	1	LOAD	LOAD	(LOAD)

S BIT ASSIGNMENT

BIT	TRUE	FALSE
S40	RIGHT (DEC)	1) HOLD 0) LOAD
S41	LEFT (INC)	1) HOLD 0) LOAD
S42	SHIFT	ROTATE
PS43	DOUBLE PREC	SINGLE
S44	ARITHMETIC	LOGICAL
PS45	REG = SA BITS	REG = SB BITS
PS46	SEL REG Ø	NORMAL
(P)S48	NORMAL	TEST INTRR
PS49	INTRR PROG	NORMAL

MUX 1 AND MUX 3

S42	PS43	FUNCTION	
0	0	ROT	SINGLE
0	1	ROT	DOUBLE
1	0	SHIFT	SINGLE
1	1	SHIFT	DOUBLE

MUX 2

S42	PS43	S44	FUNCTION
1	0	0	LOGIC SHIFT
1	0	1	ARITH SHIFT
0	0	0	ROT
X	1	X	DOUBLE

MUX 4

S42	PS43	S44	FUNCTION
1	X	0	LOGIC SHIFT
1	X	1	ARITH SHIFT
0	0	X	ROT
X	1	X	DOUBLE

VLA PROJECT New Mexico...

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

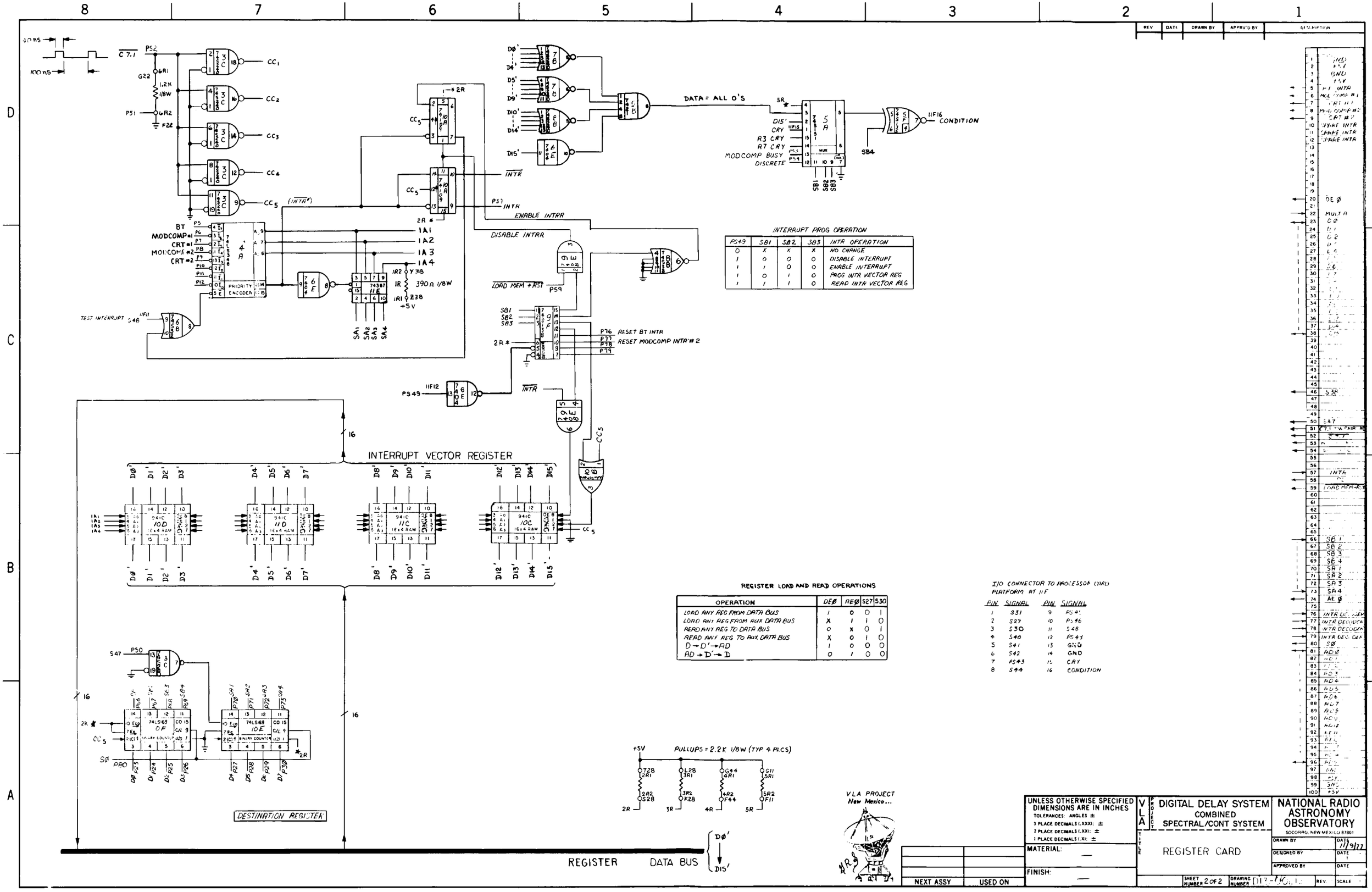
VLA PROJECT: DIGITAL DELAY SYSTEM COMBINED SPECTRAL/CONT SYSTEM

TITLE: REGISTER CARD

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE
DESIGNED BY | DATE
APPROVED BY | DATE

SHEET NUMBER 1 OF 2 | DRAWING NUMBER D17-46-0-1 | REV — | SCALE —



INTERRUPT PROG OPERATION

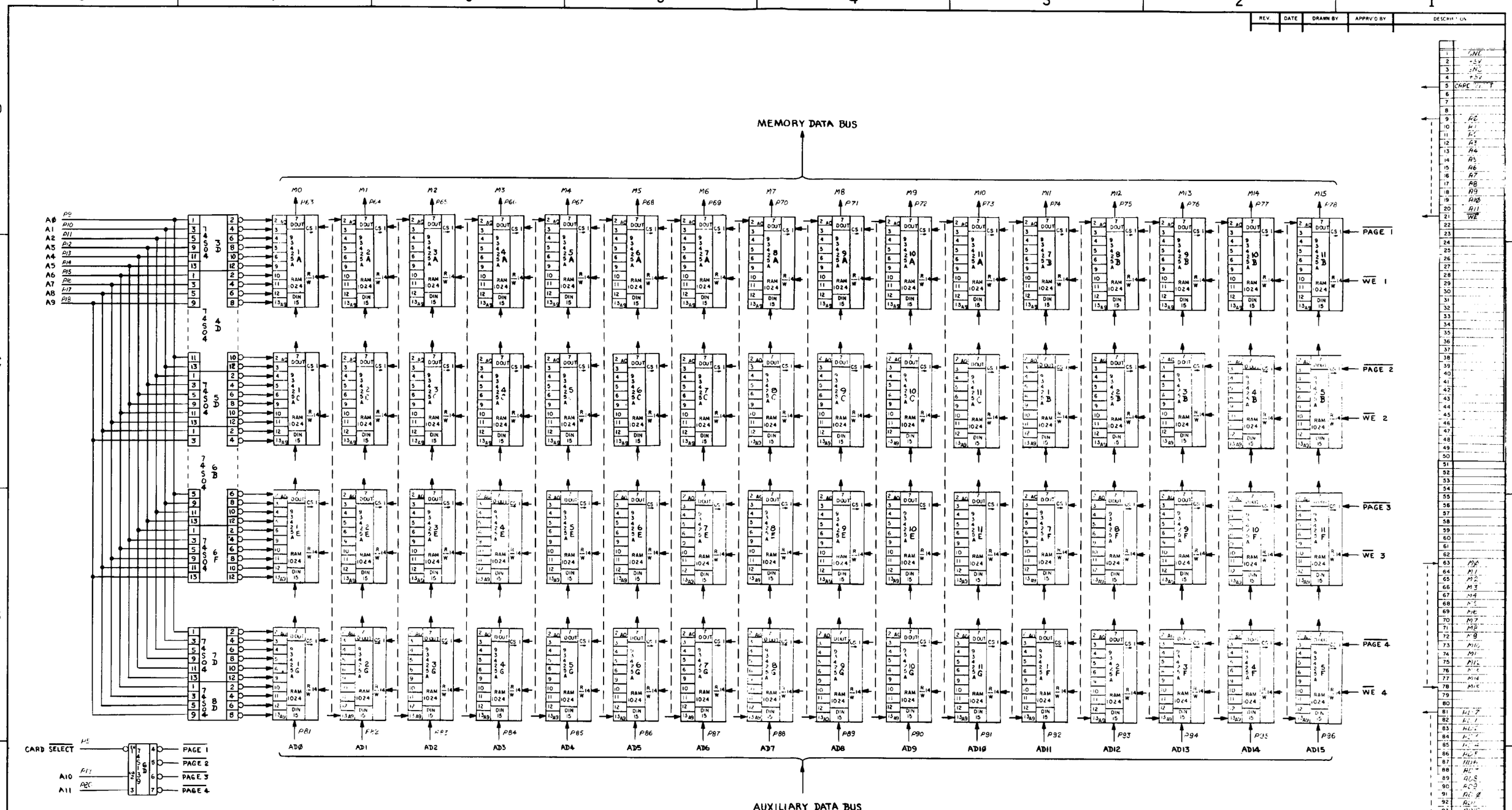
PS49	SB1	SB2	SB3	INTR OPERATION
0	X	X	X	NO CHANGE
1	0	0	0	DISABLE INTERRUPT
1	1	0	0	ENABLE INTERRUPT
1	0	1	0	PROG INTR VECTOR REG
1	1	1	0	READ INTR VECTOR REG

REGISTER LOAD AND READ OPERATIONS

OPERATION	DEØ	REØ	S27	S30
LOAD ANY REG FROM DATA BUS	1	0	0	1
LOAD ANY REG FROM AUX DATA BUS	X	1	1	0
READ ANY REG TO DATA BUS	0	X	0	1
READ ANY REG TO AUX DATA BUS	X	0	1	0
D → D' → AD	1	0	0	0
AD → D' → D	0	1	0	0

I/O CONNECTOR TO PROCESSOR (ARD)
PLATFORM AT 11F

PIN	SIGNAL	PIN	SIGNAL
1	S31	9	PS41
2	S27	10	PS46
3	S30	11	S48
4	S40	12	PS43
5	S41	13	GND
6	S42	14	GND
7	PS43	15	CRY
8	S44	16	CONDITION



REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY | USED ON

VLA PROJECT

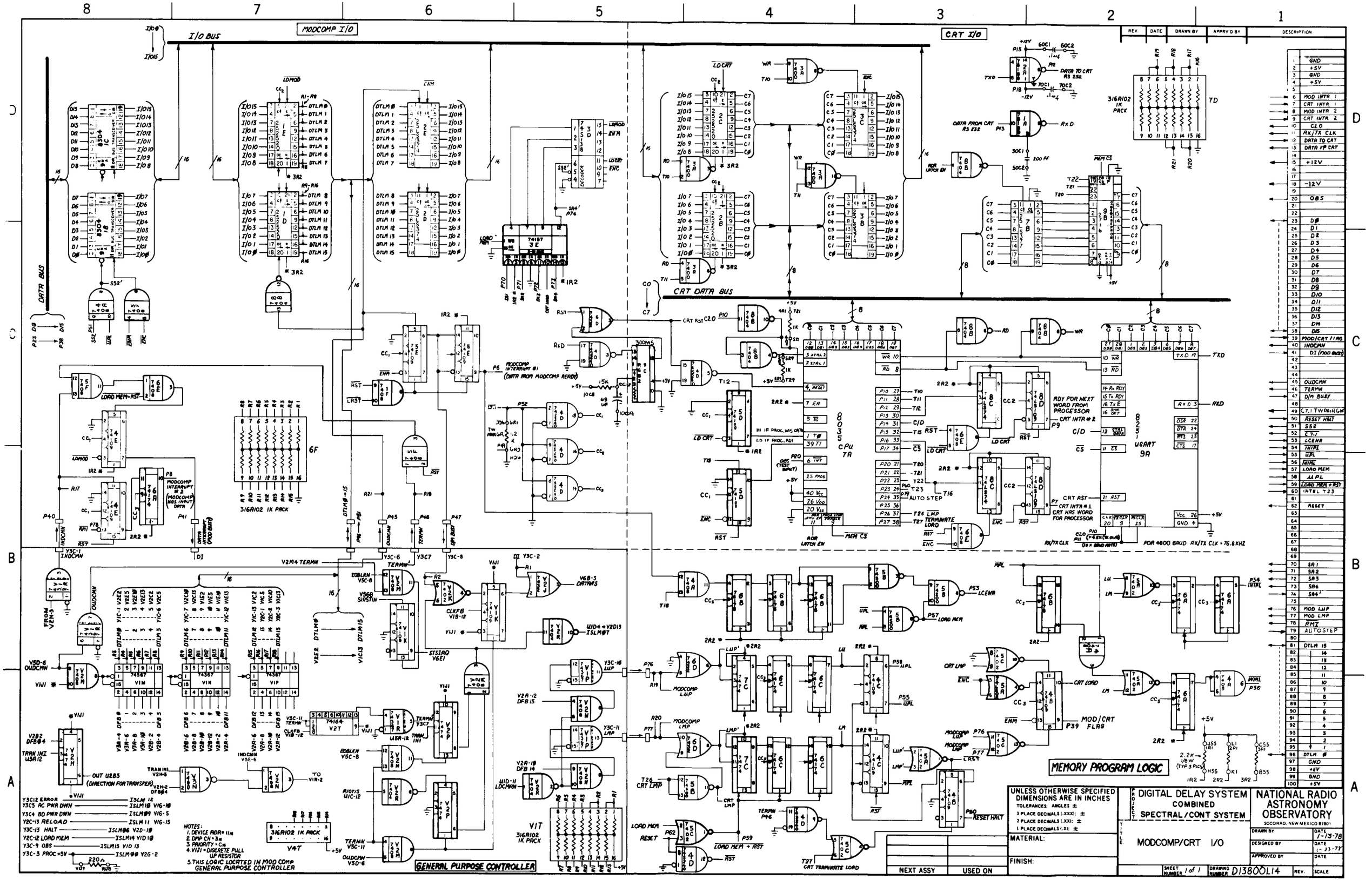
DIGITAL DELAY SYSTEM
COMBINED
SPECTRAL/CONT SYSTEM

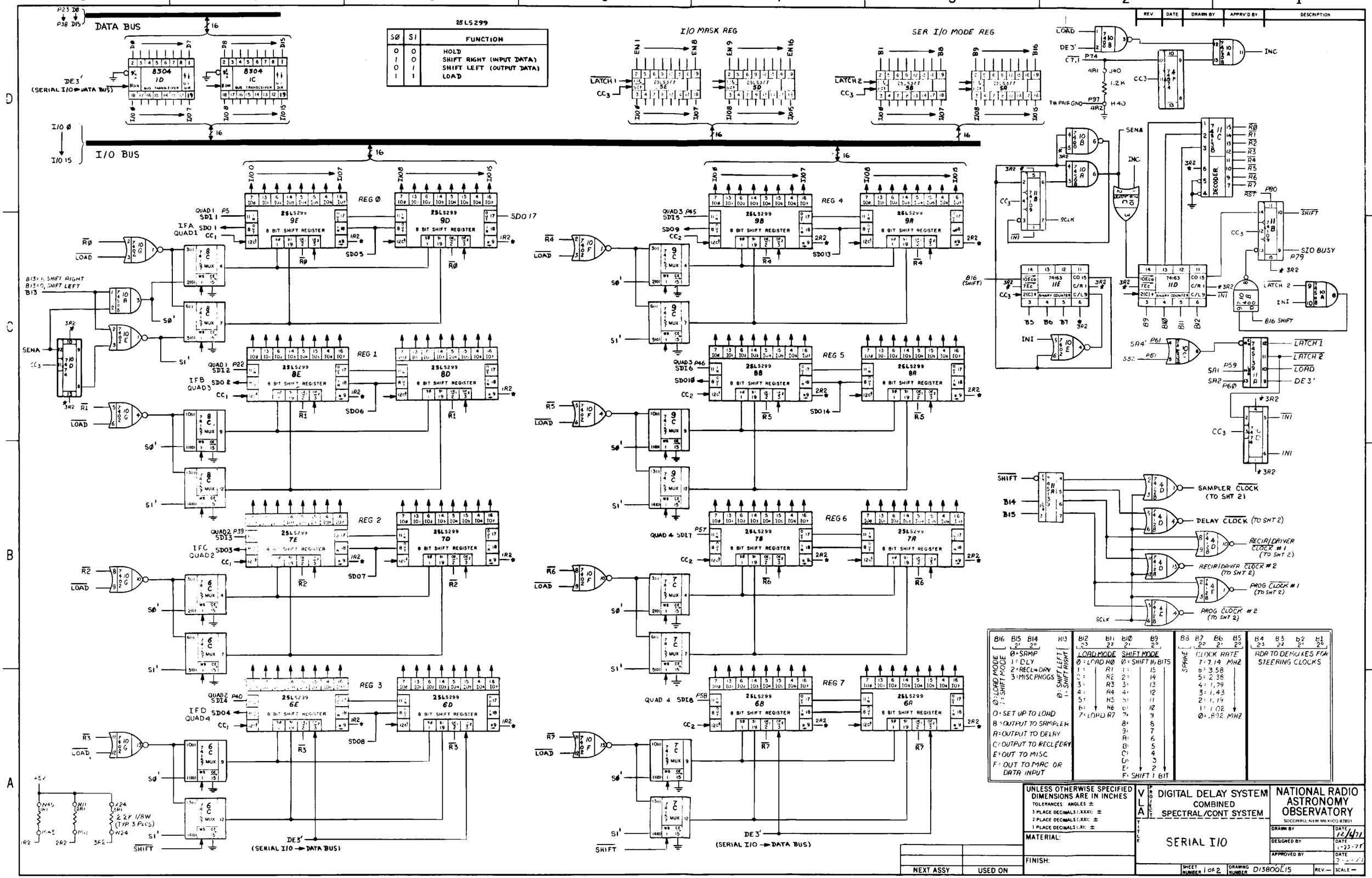
TITLE MEMORY CARD

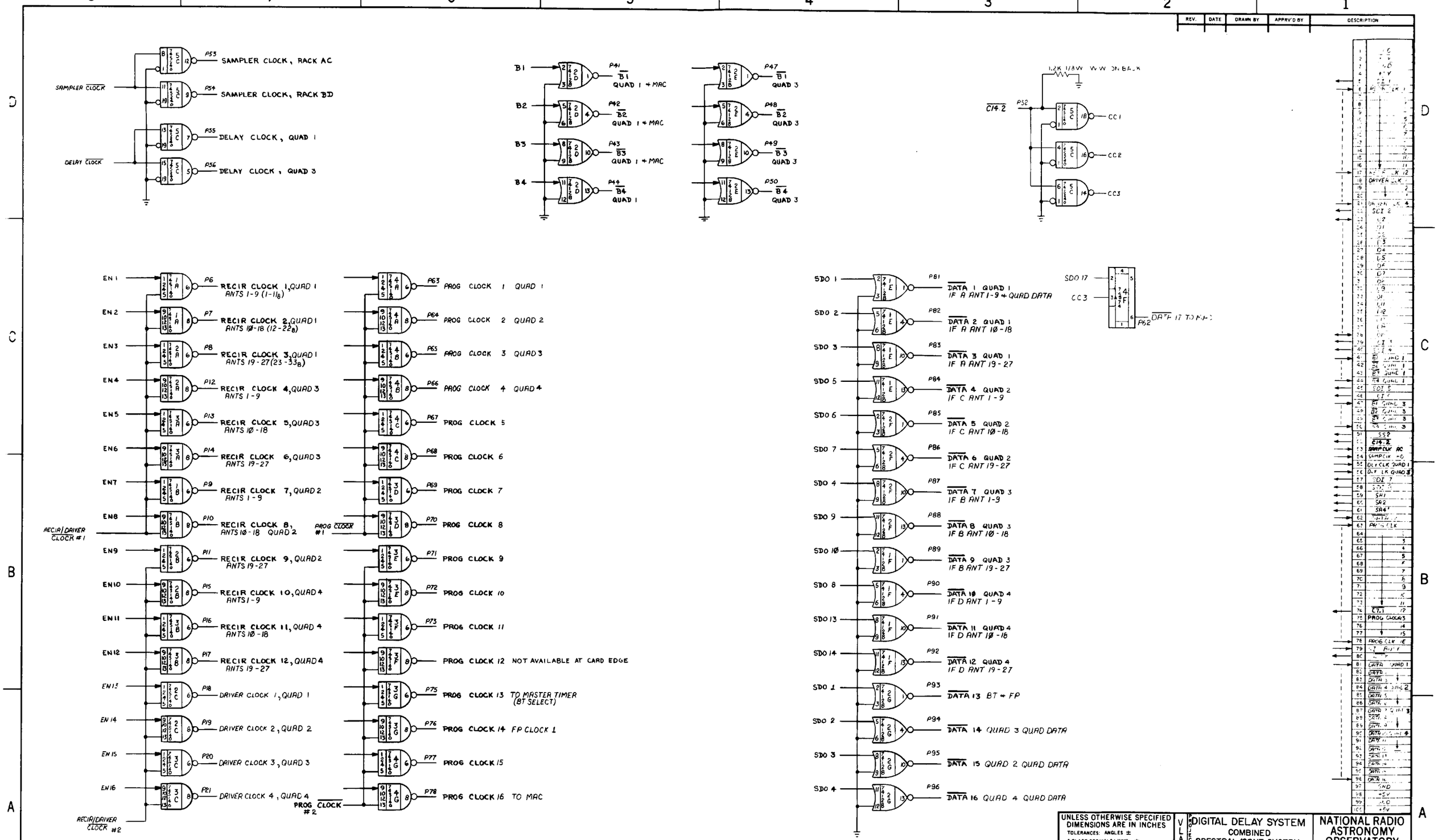
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

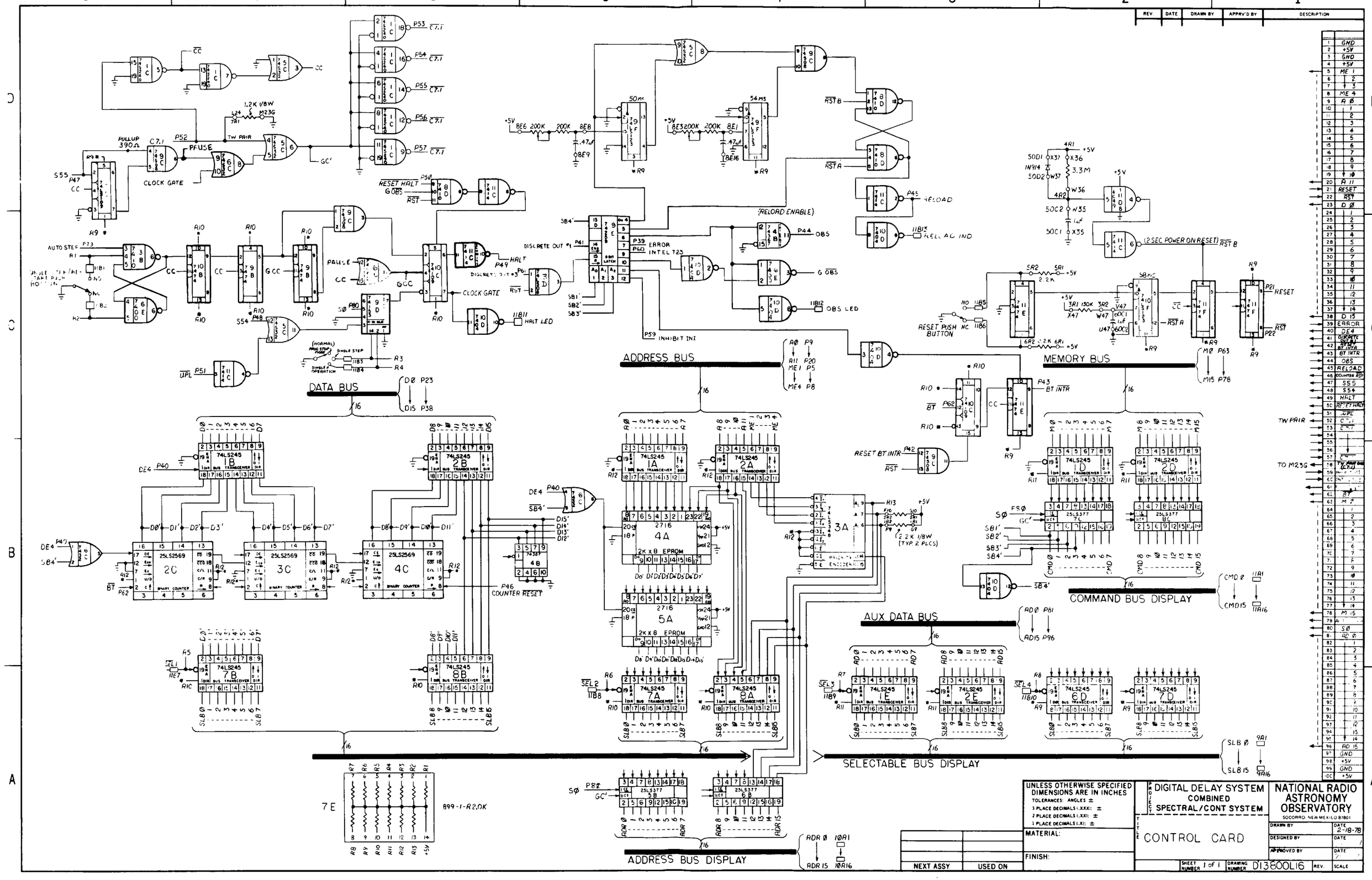
DRAWN BY | DATE 12/1/77
DESIGNED BY | DATE
APPROVED BY | DATE

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D17300L17 | REV. | SCALE —


MODCOMP I/O
CRT I/O
I/O BUS
DATA BUS
CRT DATA BUS
8304 IC
8304 IC
74157 3E
74157 3D
74157 2E
74157 2D
74157 2C
74157 2B
74157 3C
74157 3B
74157 VIM
74157 VIN
74157 VIP
74164 V2T
316A102 1K PACK
8035 CPU 7A
8251 USART 9A
DATA TO CRT RS 232
DATA FROM CRT RS 232
RDY FOR NEXT WORD FROM PROCESSOR
CRT INTR #2
CRT INTR #1
CRT HRS WORD FOR PROCESSOR
AUTO STEP
TERMINATE LOAD
CRT TERMINATE LOAD
MODCOMP INTERRUPT #2 (MODCOMP HAS INPUT DATA)
MODCOMP INTERRUPT #1 (DATA FROM MODCOMP READY)
FROM V2N-3
OUT U28S (DIRECTION FOR TRANSFER)
Y3C12 ERROR — I3LM 12
Y3C5 AC PWR DWN — ISLM10 VIG-10
Y3C4 DC PWR DWN — ISLM09 VIG-5
Y2C-13 RELOAD — ISLM 11 VIG-15
Y3C-13 HALT — ISLM06 V2D-10
Y2C-12 LOAD MEM — ISLM14 VID10
Y3C-9 OBS — ISLM15 VID 13
Y3C-3 PROC +5V — ISLM08 V2G-2
NOTES:
1. DEVICE ADR = 11H
2. DMP CH = 3H
3. PRIORITY = CH
4. VIN1 = DISCRETE PULL UP RESISTOR
5. THIS LOGIC LOCATED IN MOD COMP GENERAL PURPOSE CONTROLLER
GENERAL PURPOSE CONTROLLER
MEMORY PROGRAM LOGIC
REV. | DATE | DRAWN BY | APPRV'D BY | DESCRIPTION
1 GND
2 +5V
3 GND
4 +5V
6 MOD INTR 1
7 CRT INTR 1
8 MOD INTR 2
9 CRT INTR 2
10 CZ0
11 RX/TX CLK
12 DATA TO CRT
13 DATA FR CRT
15 +12V
18 -12V
20 OBS
23 D0
24 D1
25 D2
26 D3
27 D4
28 D5
29 D6
30 D7
31 D8
32 D9
33 D10
34 D11
35 D12
36 D13
37 DM
38 DIS
39 MOD/CRT ?/RQ
40 INDCMN
41 DI (MOD BUSY)
45 OUDCMN
46 TERMN
47 D/M BUSY
49 C7.1 TW PAIR GND
50 RESET HALT
51 SS2
52 C7.1
53 LCENR
54 INTPL
55 UPL
56 INIML
57 LOAD MEM
58 LL PL
59 LOAD MEM + RST
60 INTEL Y23
62 RESET
70 SR1
71 SR2
72 SR3
73 SR4
74 SR4'
76 MOD LUP
77 MOD LMP
78 RMZ
79 AUTO STEP
81 DTLM 15
82 14
83 13
84 12
85 11
86 10
87 9
88 8
89 7
90 6
91 5
92 4
93 3
94 2
95 1
96 DTLM 0
97 GND
98 +5V
99 GND
100 +5V
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
PROJECT: DIGITAL DELAY SYSTEM COMBINED SPECTRAL/CONT SYSTEM
TITLE: MODCOMP/CRT I/O
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DATE 1-13-78
DESIGNED BY
DATE 1-23-78
APPROVED BY
DATE
SHEET NUMBER 1 of 1
DRAWING NUMBER D13800L14
REV.
SCALE


DATA BUS
I/O BUS
8304 1D
8304 1C
BUS TRANSCEIVER
DE3' (SERIAL I/O → DATA BUS)
I/O MASK REG
SER I/O MODE REG
25LS299
8 BIT SHIFT REGISTER
REG Ø
REG 1
REG 2
REG 3
REG 4
REG 5
REG 6
REG 7
B13=1, SHIFT RIGHT
B13=0, SHIFT LEFT
SENA
INC
LOAD
DE3'
SAMPLER CLOCK (TO SHT 2)
DELAY CLOCK (TO SHT 2)
RECIR/DRIVER CLOCK #1 (TO SHT 2)
RECIR/DRIVER CLOCK #2 (TO SHT 2)
PROG CLOCK #1 (TO SHT 2)
PROG CLOCK #2 (TO SHT 2)
SIO BUSY
B16 (SHIFT)
B16 SHIFT
74163 11E
74163 11D
BINARY COUNTER
DECODER
B16 B15 B14 B13
Ø=LOAD MODE
1=SHIFT MODE
Ø=SAMP
1=DLY
2=RECL&DRV
3=MISC PROGS
Ø=SHIFT LEFT
1=SHIFT RIGHT
O=SET UP TO LOAD
B=OUTPUT TO SAMPLER
A=OUTPUT TO DELAY
C=OUTPUT TO RECL&DRV
E=OUT TO MISC
F=OUT TO MAC OR DATA INPUT
B12 B11 B10 B9
LOAD MODE
SHIFT MODE
Ø=LOAD RØ
1=R1
2=R2
3=R3
4=R4
5=R5
6=R6
7=LOAD R7
Ø=SHIFT 16 BITS
1=15
2=14
3=13
4=12
5=11
6=10
7=9
8=8
9=7
A=6
B=5
C=4
D=3
E=2
F=SHIFT 1 BIT
B8 B7 B6 B5
SPARE
CLOCK RATE
7=7.14 MHZ
6=3.58
5=2.38
4=1.79
3=1.43
2=1.19
1=1.02
Ø=.802 MHZ
B4 B3 B2 B1
ADR TO DEMUXES FOR STEERING CLOCKS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
VLA PROJECT
DIGITAL DELAY SYSTEM
COMBINED SPECTRAL/CONT SYSTEM
TITLE
SERIAL I/O
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DATE 12/4/71
DESIGNED BY
APPROVED BY
SHEET NUMBER 1 OF 2
DRAWING NUMBER D138006L15
REV.
SCALE


SAMPLER CLOCK
DELAY CLOCK
P53 SAMPLER CLOCK, RACK AC
P54 SAMPLER CLOCK, RACK BD
P55 DELAY CLOCK, QUAD 1
P56 DELAY CLOCK, QUAD 3
B1
B2
B3
B4
P41 B1 QUAD 1 + MAC
P42 B2 QUAD 1 + MAC
P43 B3 QUAD 1 + MAC
P44 B4 QUAD 1
P47 B1 QUAD 3
P48 B2 QUAD 3
P49 B3 QUAD 3
P50 B4 QUAD 3
C14 2
P52
CC1
CC2
CC3
EN1
EN2
EN3
EN4
EN5
EN6
EN7
EN8
EN9
EN10
EN11
EN12
EN13
EN14
EN15
EN16
RECIR/DRIVER CLOCK #1
RECIR/DRIVER CLOCK #2
P6 RECIR CLOCK 1, QUAD 1 ANTS 1-9 (1-11₈)
P7 RECIR CLOCK 2, QUAD 1 ANTS 10-18 (12-22₈)
P8 RECIR CLOCK 3, QUAD 1 ANTS 19-27 (23-33₈)
P12 RECIR CLOCK 4, QUAD 3 ANTS 1-9
P13 RECIR CLOCK 5, QUAD 3 ANTS 10-18
P14 RECIR CLOCK 6, QUAD 3 ANTS 19-27
P9 RECIR CLOCK 7, QUAD 2 ANTS 1-9
P10 RECIR CLOCK 8, ANTS 10-18 QUAD 2
P11 RECIR CLOCK 9, QUAD 2 ANTS 19-27
P15 RECIR CLOCK 10, QUAD 4 ANTS 1-9
P16 RECIR CLOCK 11, QUAD 4 ANTS 10-18
P17 RECIR CLOCK 12, QUAD 4 ANTS 19-27
P18 DRIVER CLOCK 1, QUAD 1
P19 DRIVER CLOCK 2, QUAD 2
P20 DRIVER CLOCK 3, QUAD 3
P21 DRIVER CLOCK 4, QUAD 4
PROG CLOCK #1
PROG CLOCK #2
P63 PROG CLOCK 1 QUAD 1
P64 PROG CLOCK 2 QUAD 2
P65 PROG CLOCK 3 QUAD 3
P66 PROG CLOCK 4 QUAD 4
P67 PROG CLOCK 5
P68 PROG CLOCK 6
P69 PROG CLOCK 7
P70 PROG CLOCK 8
P71 PROG CLOCK 9
P72 PROG CLOCK 10
P73 PROG CLOCK 11
PROG CLOCK 12 NOT AVAILABLE AT CARD EDGE
P75 PROG CLOCK 13 TO MASTER TIMER (BT SELECT)
P76 PROG CLOCK 14 FP CLOCK 1
P77 PROG CLOCK 15
P78 PROG CLOCK 16 TO MAC
SDO 1
SDO 2
SDO 3
SDO 5
SDO 6
SDO 7
SDO 4
SDO 9
SDO 10
SDO 8
SDO 13
SDO 14
SDO 1
SDO 2
SDO 3
SDO 4
P81 DATA 1 QUAD 1 IF A ANT 1-9 + QUAD DATA
P82 DATA 2 QUAD 1 IF A ANT 10-18
P83 DATA 3 QUAD 1 IF A ANT 19-27
P84 DATA 4 QUAD 2 IF C ANT 1-9
P85 DATA 5 QUAD 2 IF C ANT 10-18
P86 DATA 6 QUAD 2 IF C ANT 19-27
P87 DATA 7 QUAD 3 IF B ANT 1-9
P88 DATA 8 QUAD 3 IF B ANT 10-18
P89 DATA 9 QUAD 3 IF B ANT 19-27
P90 DATA 10 QUAD 4 IF D ANT 1-9
P91 DATA 11 QUAD 4 IF D ANT 10-18
P92 DATA 12 QUAD 4 IF D ANT 19-27
P93 DATA 13 BT + FP
P94 DATA 14 QUAD 3 QUAD DATA
P95 DATA 15 QUAD 2 QUAD DATA
P96 DATA 16 QUAD 4 QUAD DATA
SDO 17
CC3
P62 DATA 17 TO MAC
REV.
DATE
DRAWN BY
APPRV'D BY
DESCRIPTION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
VLA PROJECT
DIGITAL DELAY SYSTEM
COMBINED SPECTRAL/CONT SYSTEM
TITLE
SERIAL I/O
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DATE 12/5/77
DESIGNED BY
DATE 1-23-77
APPROVED BY
DATE
SHEET NUMBER 2 OF 2
DRAWING NUMBER D138001.15
REV.
SCALE



REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON

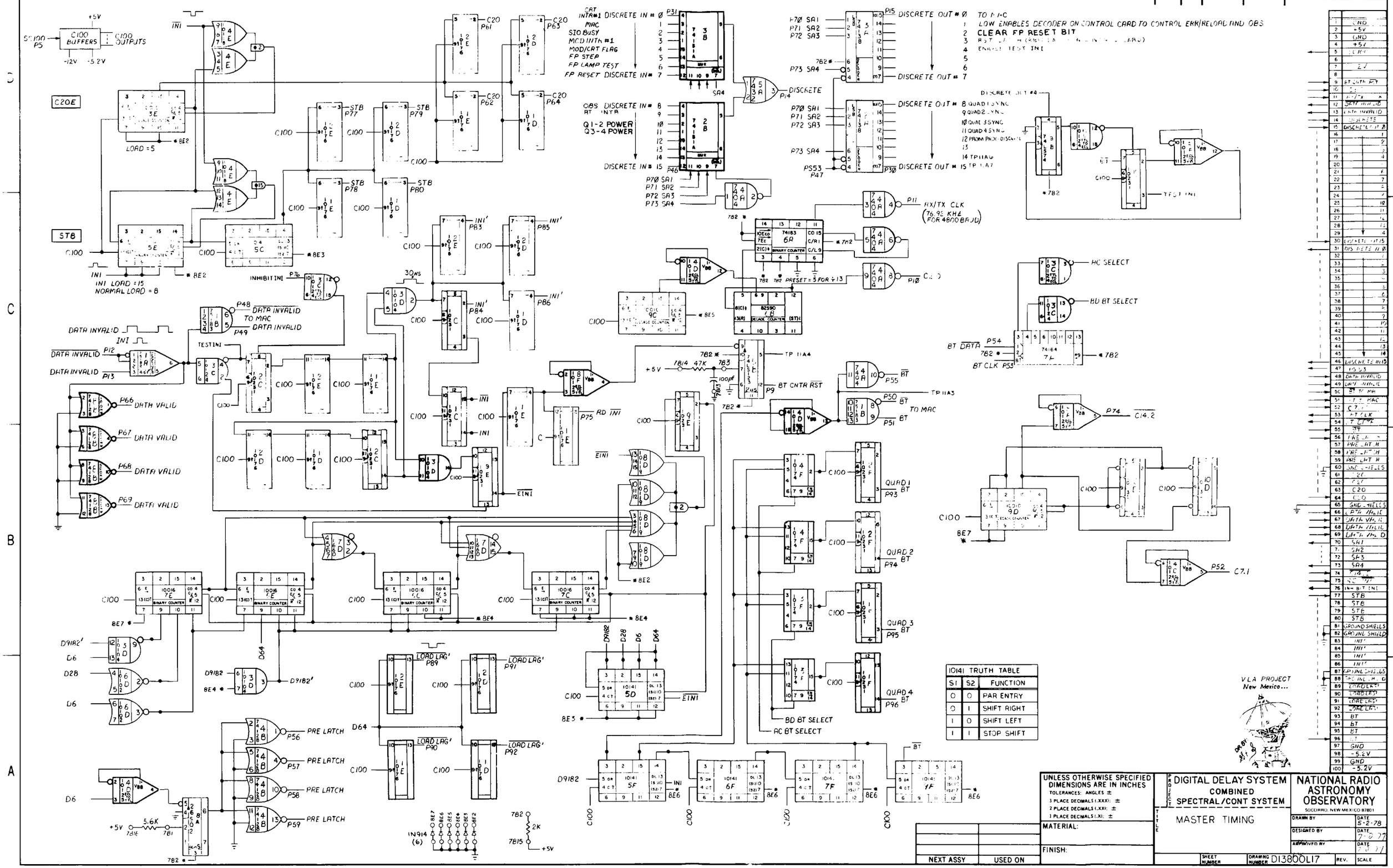
PROJECT: DIGITAL DELAY SYSTEM COMBINED SPECTRAL/CONT SYSTEM

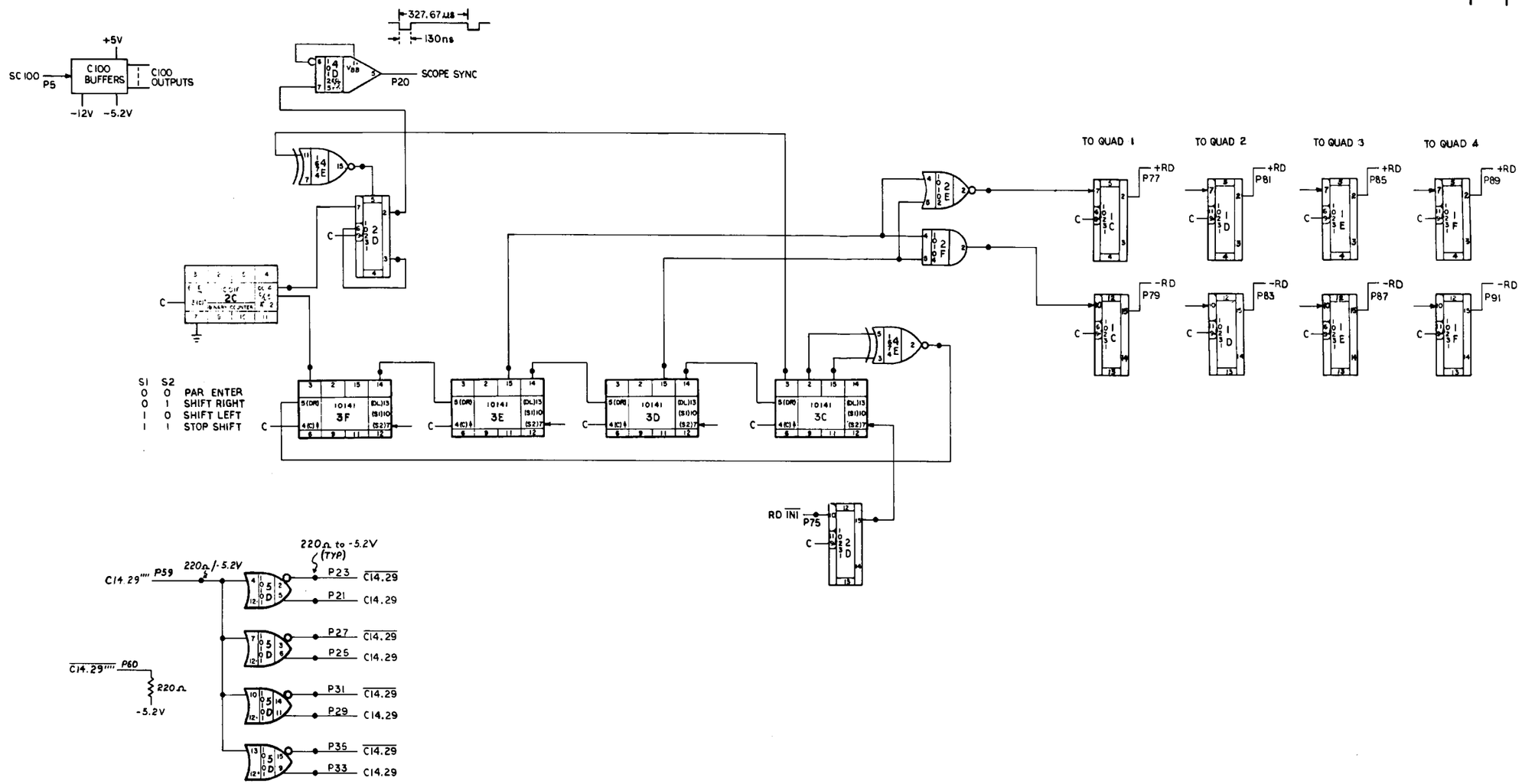
TITLE: CONTROL CARD

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 2-18-78
DESIGNED BY	DATE
APPROVED BY	DATE

SHEET NUMBER 1 of 1 | DRAWING NUMBER D13800L16 | REV. | SCALE


C100 BUFFERS
C100 OUTPUTS
SC100 P5
+5V
-12V
-5.2V
C20E
STB
LOAD = 5
INI LOAD = 15
NORMAL LOAD = 8
INHIBIT INI
DATA INVALID TO MAC
DATA INVALID
TESTINI
DATA VALID
CRT INTR#1
MAC
SIO BUSY
MOD INTR #1
MOD/CRT FLAG
FP STEP
FP LAMP TEST
FP RESET
DISCRETE IN # 0
DISCRETE IN # 7
OBS BT INTR
Q1-2 POWER
Q3-4 POWER
DISCRETE IN # 8
DISCRETE IN # 15
DISCRETE OUT # 0
DISCRETE OUT # 7
DISCRETE OUT # 8
DISCRETE OUT # 15
TO MAC
LOW ENABLES DECODER ON CONTROL CARD TO CONTROL ERR/RELOAD AND OBS
CLEAR FP RESET BIT
QUAD 1 SYNC
QUAD 2 SYNC
QUAD 3 SYNC
QUAD 4 SYNC
PROM PROG DISCRETE
TP 11A6
TP 11A7
TEST INI
RX/TX CLK (76.95 KHZ FOR 4800 BAUD)
PRESET = 5 FOR ÷13
BT CNTR RST
TP 11A4
TP 11A5
TO MAC
HC SELECT
BD BT SELECT
AC BT SELECT
QUAD 1 BT
QUAD 2 BT
QUAD 3 BT
QUAD 4 BT
PRE LATCH
RD INI
EINI
LOAD LAG'
IN914 (6)
2K
5.6K
10141 TRUTH TABLE
S1 S2 FUNCTION
0 0 PAR ENTRY
0 1 SHIFT RIGHT
1 0 SHIFT LEFT
1 1 STOP SHIFT
VLA PROJECT New Mexico...
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
DIGITAL DELAY SYSTEM
COMBINED SPECTRAL/CONT SYSTEM
MASTER TIMING
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DATE 5-2-78
DESIGNED BY
APPROVED BY
SHEET NUMBER
DRAWING NUMBER D13800L17
REV.
SCALE



1	GND
2	+5V
3	GND
4	+5V
5	SC 100
7	-12V
20	SCOPE SYNC
21	C14.29
22	SHIELD
23	C14.29
24	SHIELD
25	C14.29
26	SHIELD
27	C14.29
28	SHIELD
29	C14.29
30	SHIELD
31	C14.29
32	SHIELD
33	C14.29
34	SHIELD
35	C14.29
36	SHIELD
59	C14.29''''
60	C14.29''''
75	RD INT
77	+RD
78	CORX SHIELD
79	-RD
80	CORX SHIELD
81	+RD
82	CORX SHIELD
83	-RD
84	CORX SHIELD
85	+RD
86	CORX SHIELD
87	-RD
88	CORX SHIELD
89	+RD
90	CORX SHIELD
91	-RD
92	CORX SHIELD
97	GND
98	-5.2V
99	GND
100	-5.2V

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

VLA PROJECT
New Mexico...

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY | USED ON

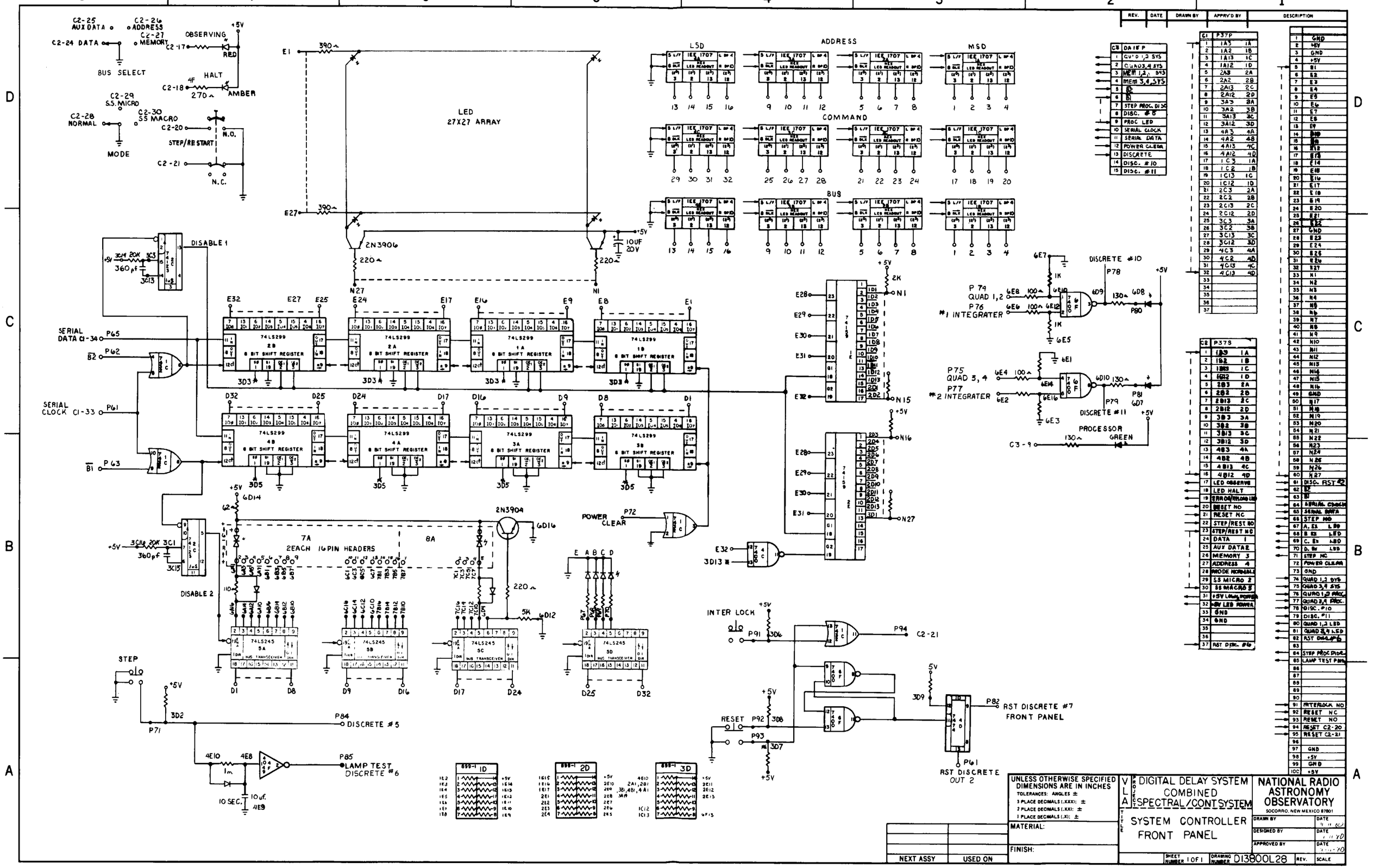
PROJECT

TITLE: DATA GENERATOR

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE
DESIGNED BY | DATE
APPROVED BY | DATE

SHEET NUMBER | DRAWING NUMBER D13800L22 | REV. | SCALE


LED 27X27 ARRAY
LSD
ADDRESS
MSD
COMMAND
BUS
IEE 1707
BUS SELECT
MODE
STEP/RESTART
N.O.
N.C.
OBSERVING
RED
HALT
AMBER
DISABLE 1
DISABLE 2
SERIAL DATA
SERIAL CLOCK
74LS299
8 BIT SHIFT REGISTER
74LS245
BUS TRANSCEIVER
2N3906
2N3904
POWER CLEAR
7A
8A
2EACH 16PIN HEADERS
STEP
LAMP TEST DISCRETE #6
DISCRETE #5
INTER LOCK
RESET
RST DISCRETE #7 FRONT PANEL
RST DISCRETE OUT 2
DISCRETE #10
DISCRETE #11
PROCESSOR GREEN
P 79 QUAD 1,2
P76 #1 INTEGRATER
P75 QUAD 3,4
P77 #2 INTEGRATER
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
VLA PROJECT
DIGITAL DELAY SYSTEM
COMBINED SPECTRAL/CONT SYSTEM
TITLE
SYSTEM CONTROLLER FRONT PANEL
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DESIGNED BY
APPROVED BY
DATE
SHEET NUMBER 1 OF 1
DRAWING NUMBER D13800L28
REV.
SCALE

DRAWING SECTION 5 Miscellaneous drawings

E13500S8
B13800L1
B13540S1
D13500L40
D13500L41
B13800S1
D13800S1
D13800B1
D13800B2
D13800B3
D13800B4
D13800B5
D13800B6
D13800B7
D13800B8
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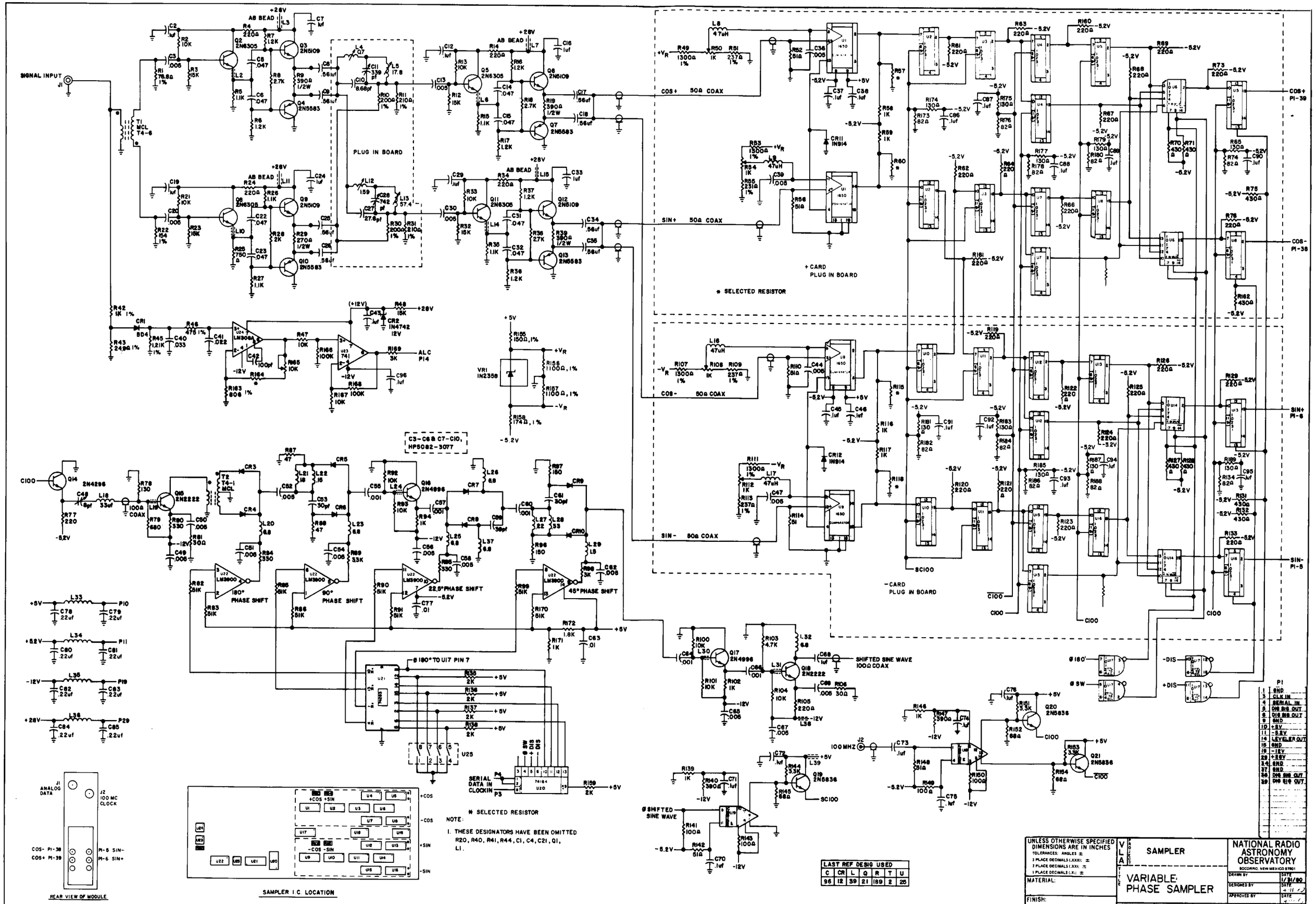
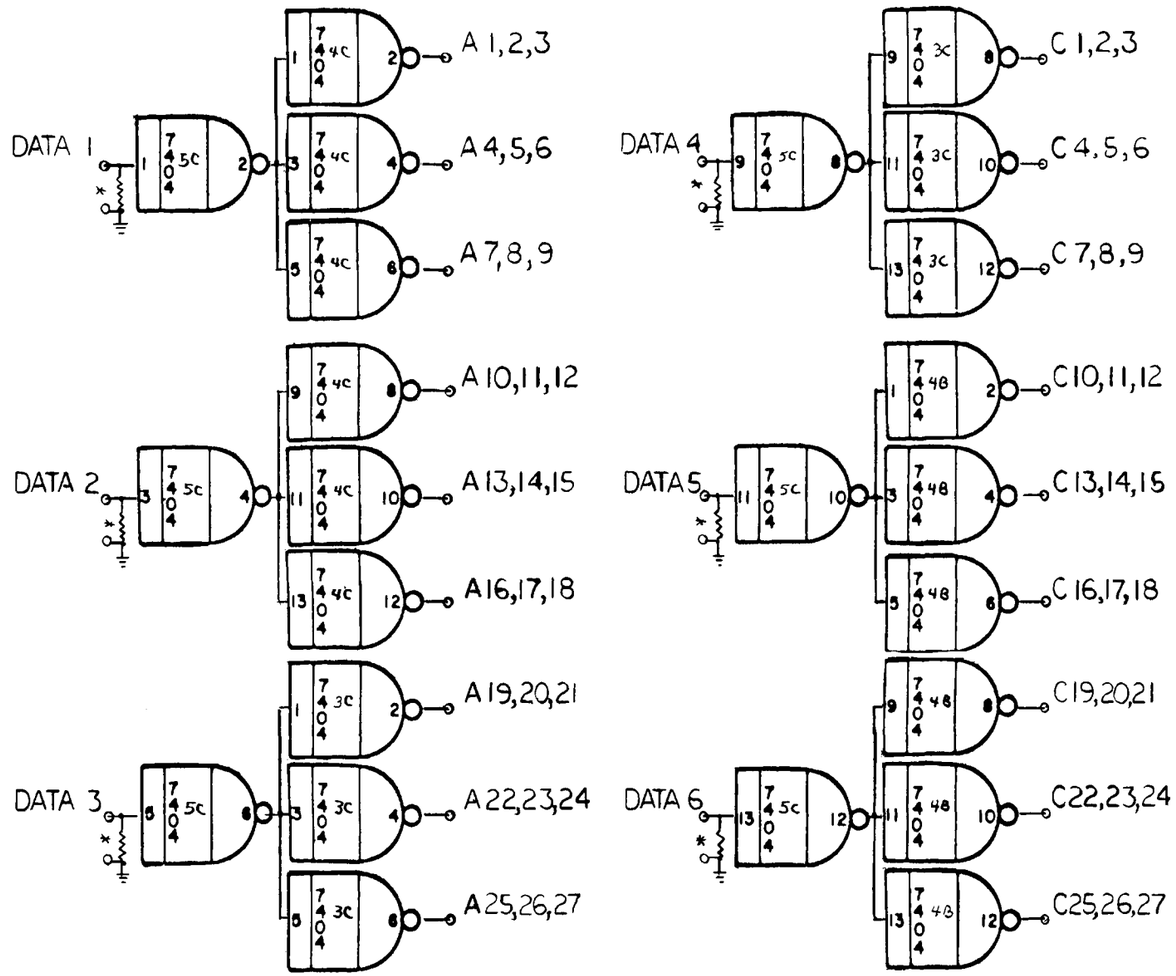
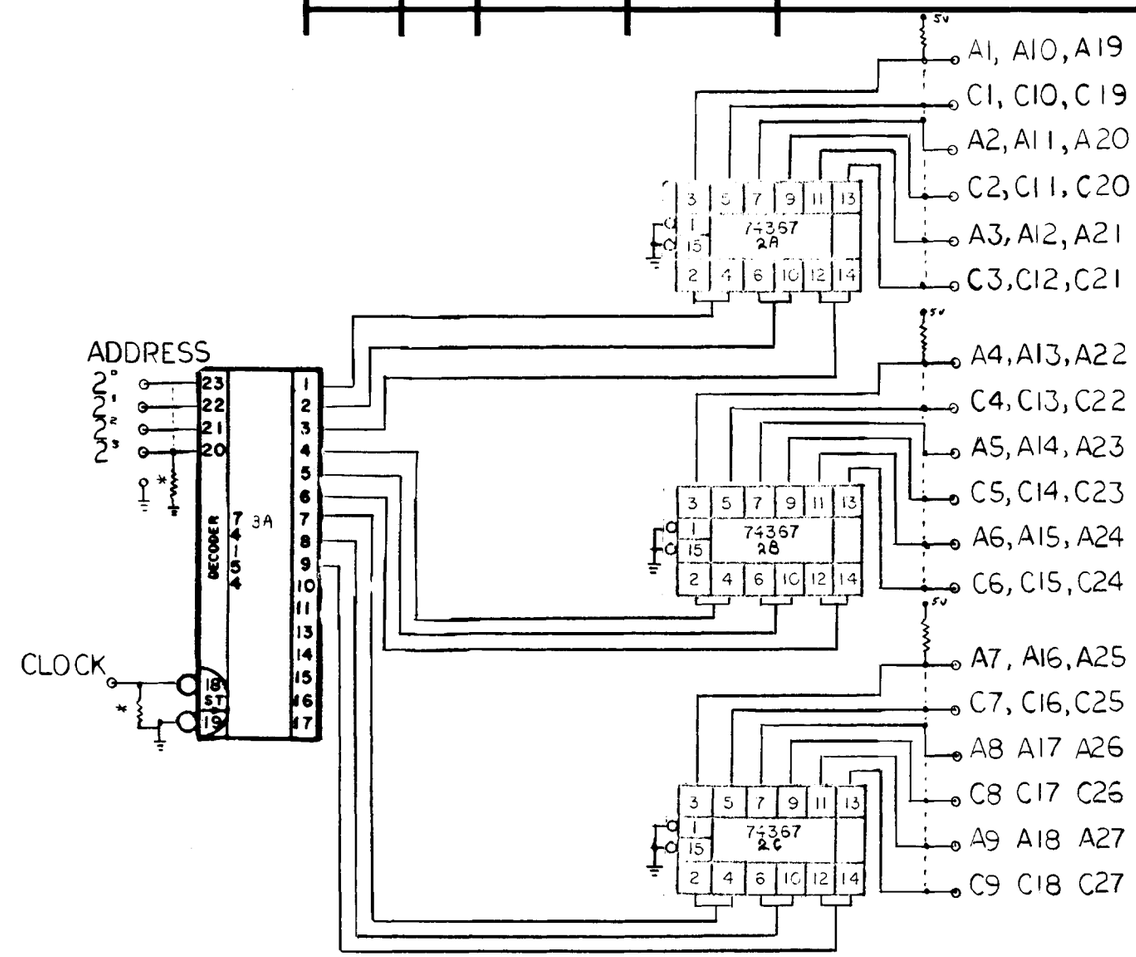
B13800B13
B13800B14
D13860B2
D13800B15

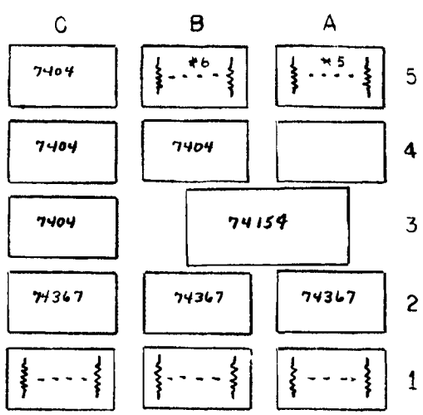

SIGNAL INPUT
J1
T1 MCL T4-6
PLUG IN BOARD
COS+ 50Ω COAX
SIN+ 50Ω COAX
COS- 50Ω COAX
SIN- 50Ω COAX
+ CARD PLUG IN BOARD
* SELECTED RESISTOR
- CARD PLUG IN BOARD
C3-C8 & C7-C10, HP5082-3077
180° PHASE SHIFT
90° PHASE SHIFT
22.5° PHASE SHIFT
45° PHASE SHIFT
ALC P14
COS+ P1-39
COS- P1-38
SIN+ P1-6
SIN- P1-5
SHIFTED SINE WAVE 100Ω COAX
100 MHZ
SERIAL DATA IN CLOCKIN
ANALOG DATA
100 MC CLOCK
REAR VIEW OF MODULE
SAMPLER I.C. LOCATION
NOTE:
1. THESE DESIGNATORS HAVE BEEN OMITTED R20, R40, R41, R44, C1, C4, C21, Q1, L1.
LAST REF DESIG USED
C CR L Q R T U
96 12 39 21 189 2 25
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL:
FINISH:
SAMPLER
VARIABLE PHASE SAMPLER
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DESIGNED BY
APPROVED BY
DATE 1/31/80
SHEET NUMBER 1 of 1
DRAWING NUMBER E1350S8
REV.
SCALE



DATA DELAY WORD



GATED CLOCK



* 100Ω

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

PROJECT: DIGITAL DELAY SYSTEM COMBINED SPECTRAL /CONT SYSTEM

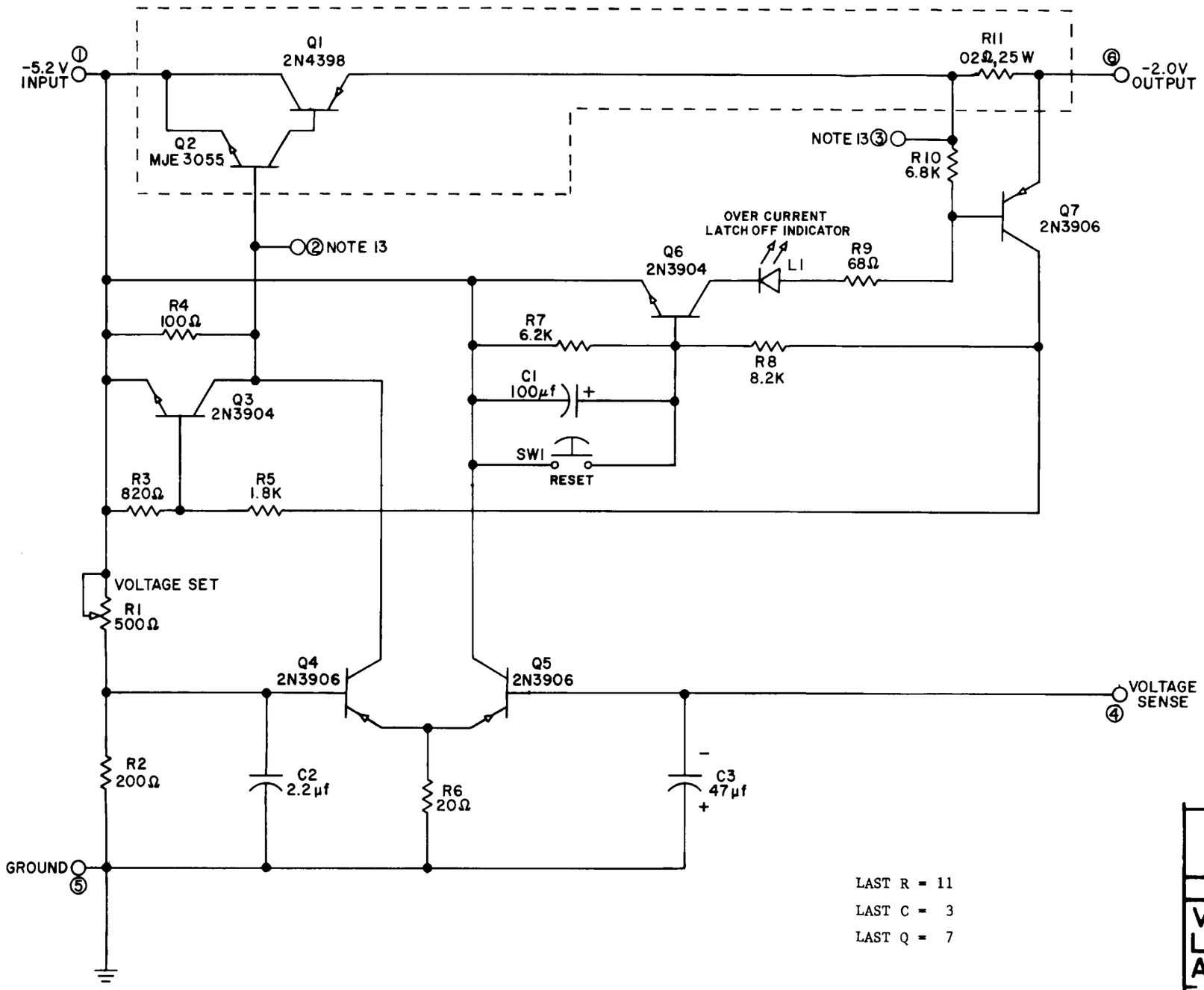
TITLE: DELAY WORD DISTRIBUTION

SAMPLER

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 3 NOV 77
DESIGNED BY	DATE
APPROVED BY	DATE 2-26-80

SHEET NUMBER 1 of 1 | DRAWING NUMBER B13800L1 | REV. | SCALE



NOTES:

1. ALL RESISTORS 1/4 W UNLESS OTHERWISE SPECIFIED.
2. R1 = BECKMAN HELIPOT 62 PA R500 RH.
3. L1 = MONSANTO MV 5024.
4. C1 = SPRAGUE 150D,100uf,20V.
5. C2 = ERIE 8141-050-651-225M 50 VOLT.
6. C3 = KEMET CS 13BE476K 20 VOLT.
7. R11 = DALE RH25,25 W, 3%.
8. SW1 = GRAYHILL 30-1.
9. ⓧ DENOTES BARRIER STRIP ASSIGNMENTS.
10. COMPONENTS IN DASHED LINES MOUNTED ON HEAT SINK.
11. PRINTED CIRCUIT DRAWING NO. IS C13540AB1
12. CONNECTING TERMINALS: KULKA 601-Y-6 SIX TERMINAL, 20 AMP BARRIER STRIP. TERMINAL NUMBERS ETCHED ON PC CARD WHICH MOUNTS TO SIDE OF HEAT SINK.
13. NOT FOR EXTERNAL CONNECTIONS.
14. HEAT SINK = THERMALLOY 6441B-2.
15. BERYLLIUM OXIDE INSULATOR = THERMALLOY 4003.
16. HEAT SINK COMPOUND FOR 2N4398 = DOW CORNING 340 SILICONE.

LAST R = 11
LAST C = 3
LAST Q = 7

9/75 JE

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	12-1-75			NOTE 4 WAS ERIE 8121 -050-651-223M 50V; R3 WAS 33K; R5 WAS 1.8K; R7 WAS 33K; R8 WAS 1K; R10 WAS 39Ω; C1 WAS .022 uf

VLA PROJECT

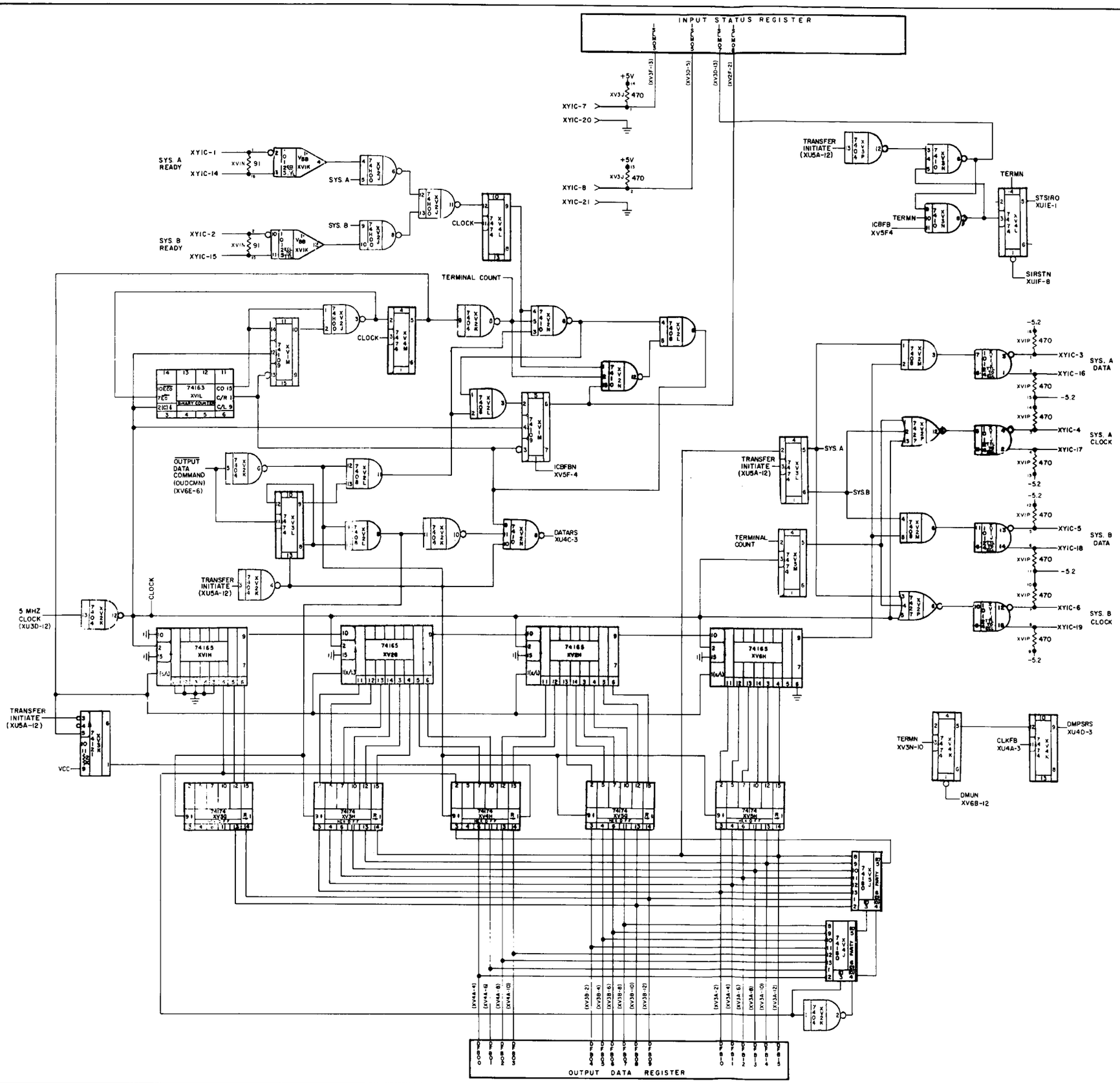
DIGITAL DELAY SYSTEM
MULTIPLIER SECTION

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

TITLE: -2V/15 AMP REGULATOR

DRAWN BY	DATE 7/9/74
DESIGNED BY	DATE 8/1/74
APPROVED BY	DATE 8/1/74

SHEET NUMBER | DRAWING NUMBER B13540S1 | REV. A | SCALE



REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

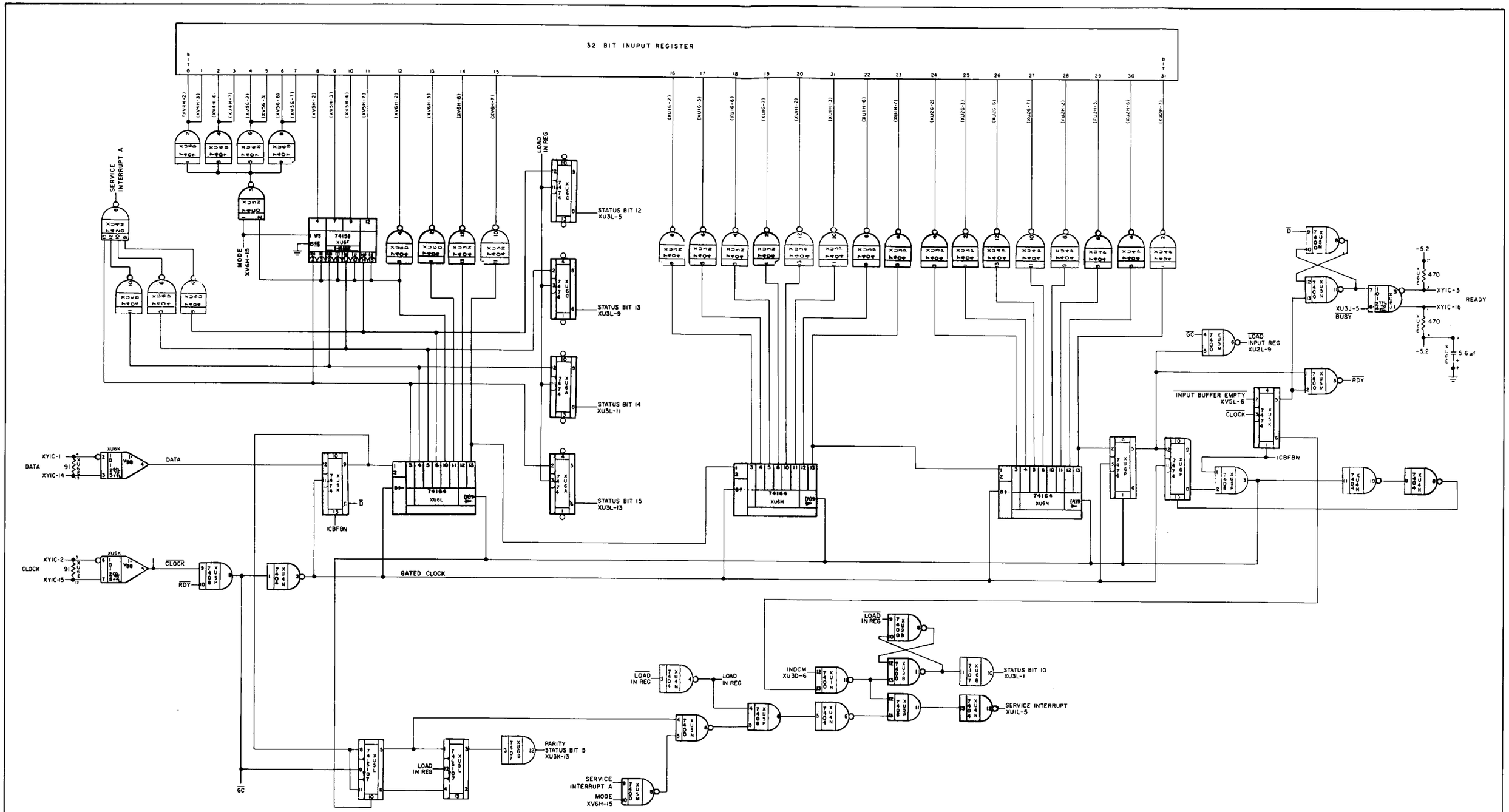
VLA

TITLE: VLAC TO SYSTEM CONTROLLER INTERFACE

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA 22901

DRAWN BY		DATE 3-25-75
DESIGNED BY		DATE 3/25/75
APPROVED BY		DATE 12/9/75

SHEET NUMBER | DRAWING NUMBER D35006L40 | REV | SCALE



REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

VLA PROJECT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA 22901

TITLE: CORRELATOR TO VLAC

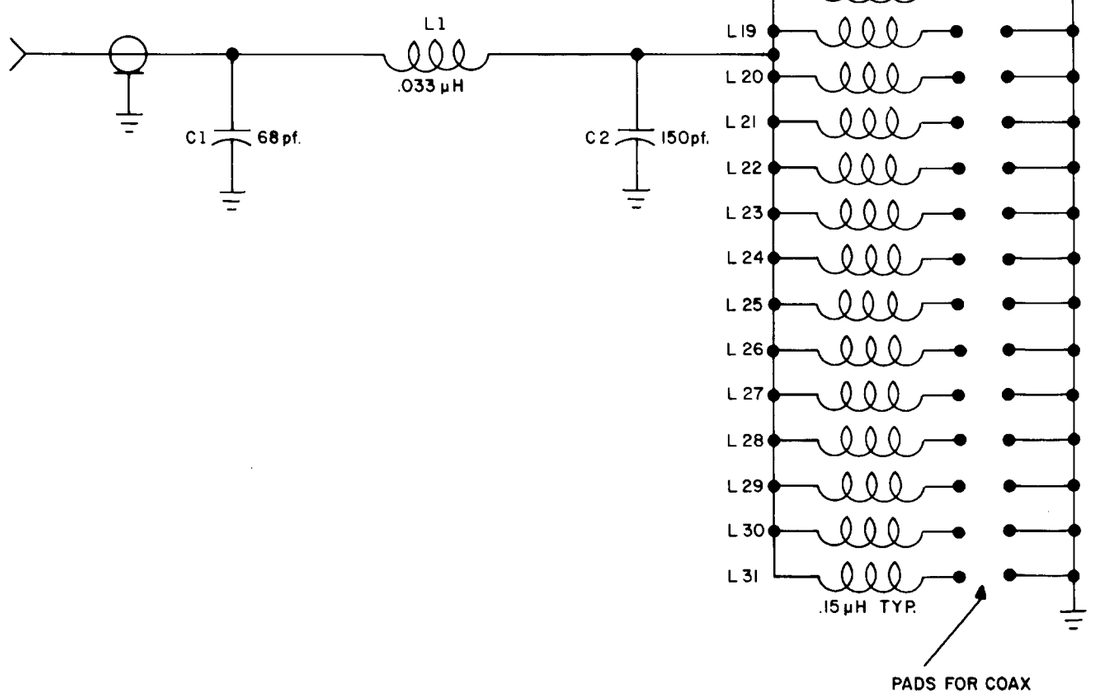
DRAWN BY		DATE 6-11-75
DESIGNED BY		DATE 6-11-75
APPROVED BY		DATE

SHEET NUMBER | DRAWING NUMBER D13500L41 | REV | SCALE

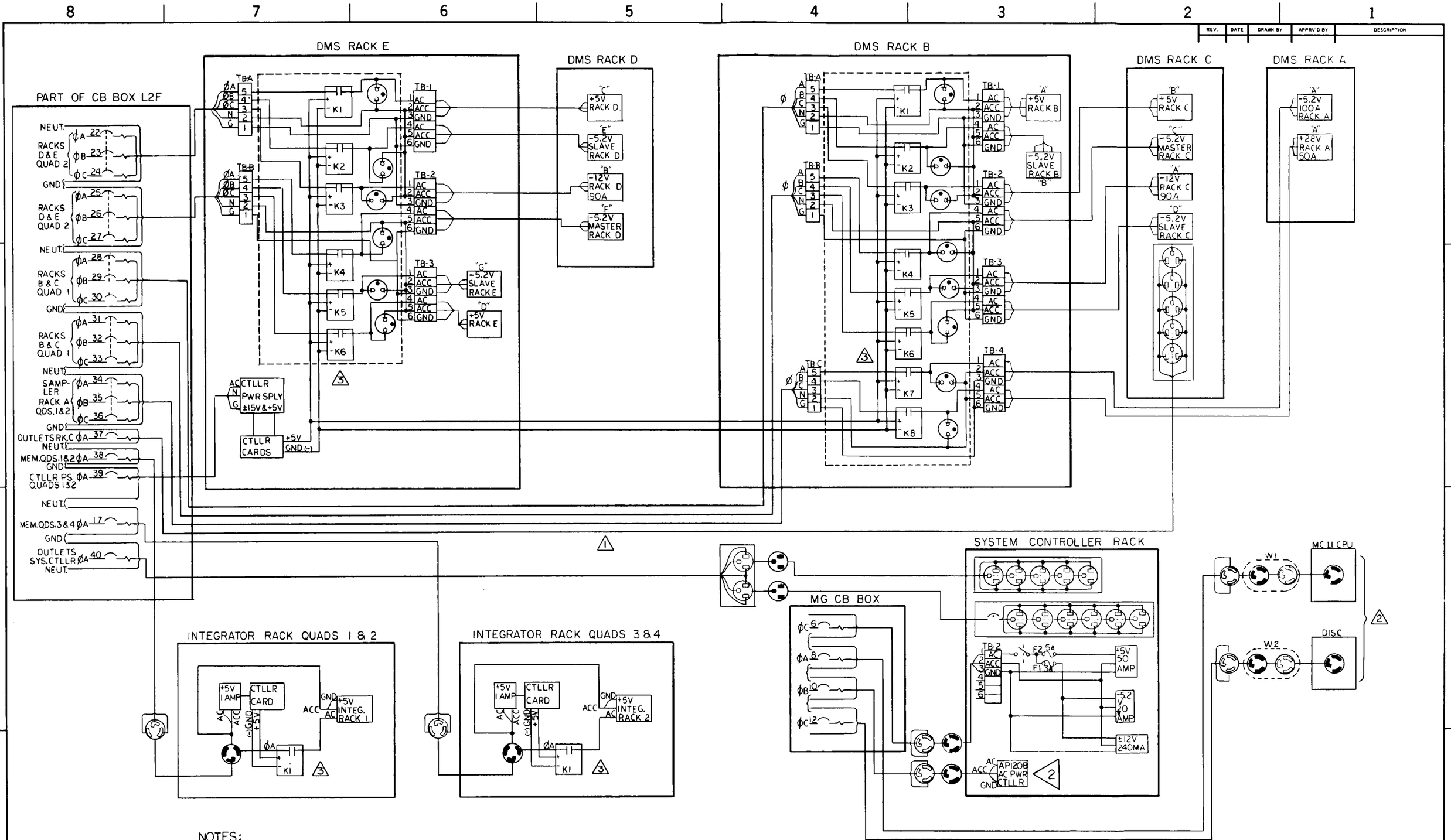
REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:

1. L1 = VANGUARD SERIES 91, TYPE 9107.
2. C1 = ERIE RED CAP 8121-100-COGO-680K.
3. C2 = ERIE RED CAP 8121-100-COGO-151K.
4. L2-L31 = .15 μH J W MILLER TYPE 9230-00. FED SYMMETRICALLY FROM L1.
5. 1/16" G10 DOUBLE CLAD BOARD.
6. PC LAYOUT DWG. NO. = D13800AD1.



VLA PROJECT	DIGITAL DELAY SYSTEM COMBINED SPECTRAL/CONT SYSTEM	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801	
TITLE	CLOCK POWER DIVIDER	DRAWN BY	DATE 6-1-77
		DESIGNED BY	DATE 7-12-79
		APPROVED BY	DATE 7-12-79
	SHEET NUMBER 1 of 1	DRAWING NUMBER B13800S1	REV. / SCALE



NOTES:

1. AC TO DMS RACKS VIA PLUGS (NOT SHOWN). HUBBELL TYPES 2823, 2821, 2313, & 2311.
2. REFER TO EQUIP. MANUAL FOR DETAILED DIST.
3. ALL RELAYS: TELEDYNE 611-6H, SPST/NO.

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

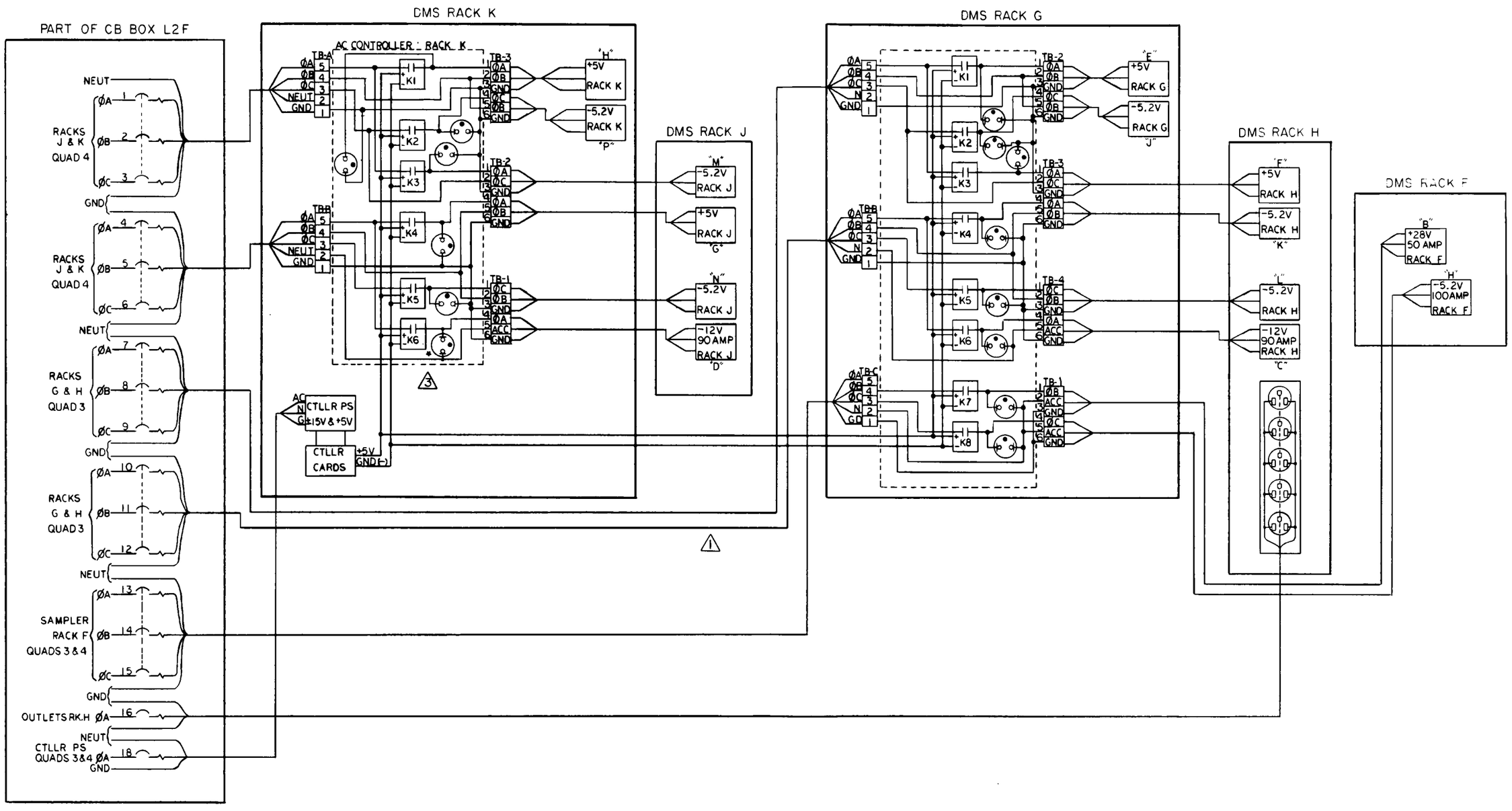
NEXT ASSY	USED ON

PROJECT: DIGITAL DELAY SYSTEM COMBINED SPECTRAL/CONT. SYSTEM

TITLE: AC POWER DIST.

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY		DATE 2-19-80
DESIGNED BY		DATE 2-19-80
APPROVED BY		DATE 2-27-80
SHEET NUMBER 1 of 2	DRAWING NUMBER D13800S1	REV.
SCALE		



REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON

PROJECT: DIGITAL DELAY SYSTEM COMBINED SPECTRAL/CONT SYSTEM

TITLE: AC POWER DIST.

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

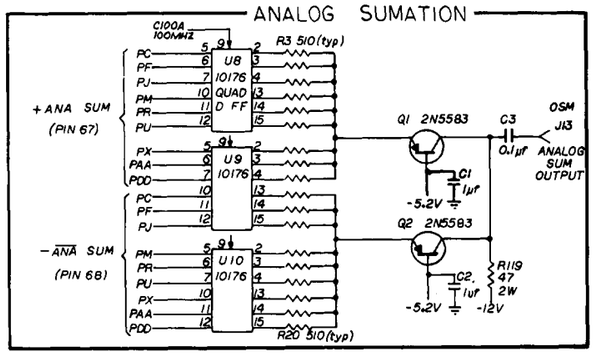
DRAWN BY	DATE 2/11/80
DESIGNED BY	DATE
APPROVED BY	DATE

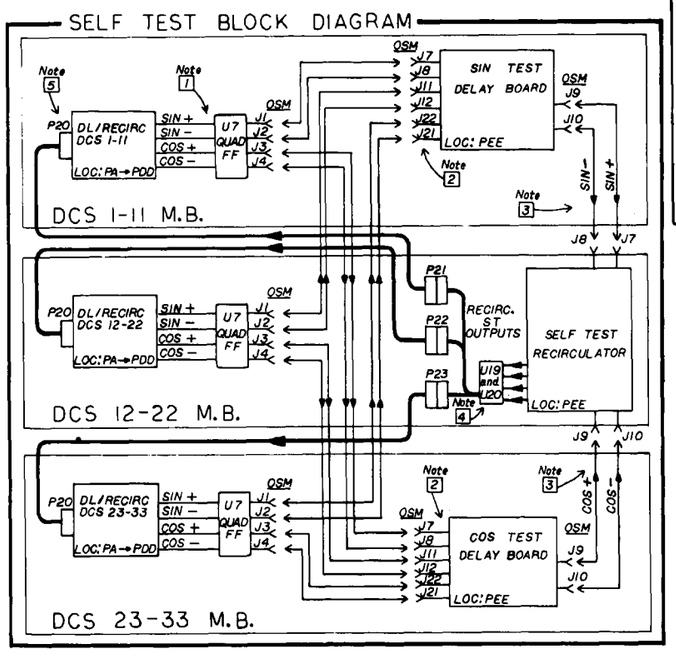
SHEET NUMBER 2 of 2 | DRAWING NUMBER D1380051 | REV. | SCALE

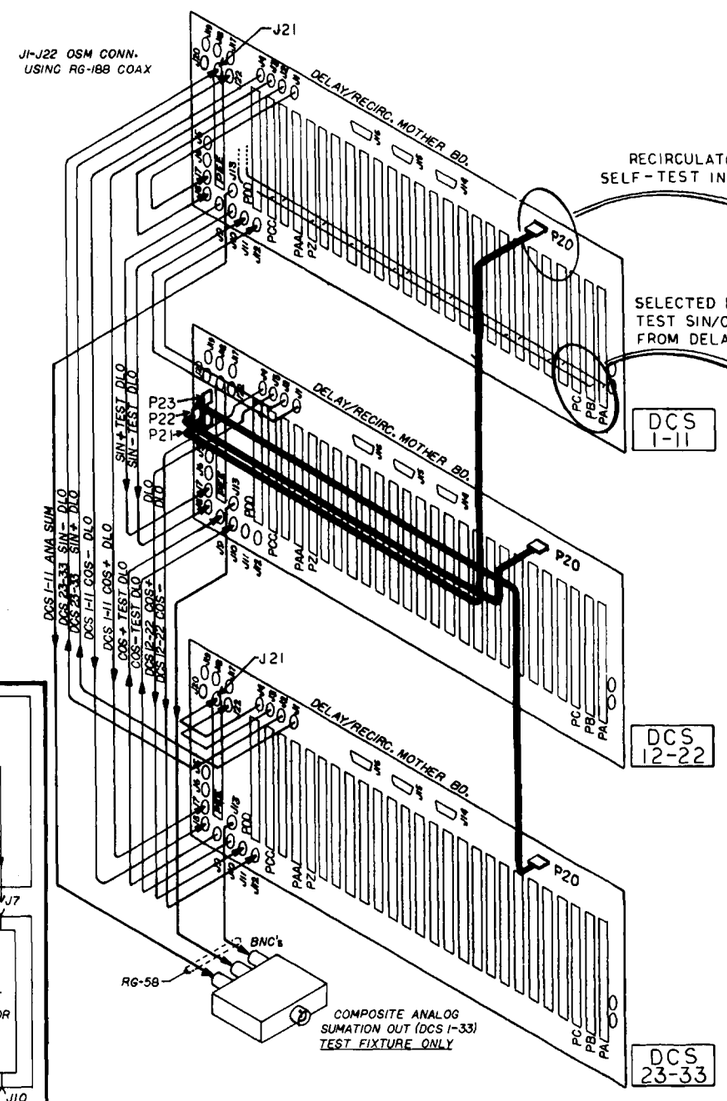
REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

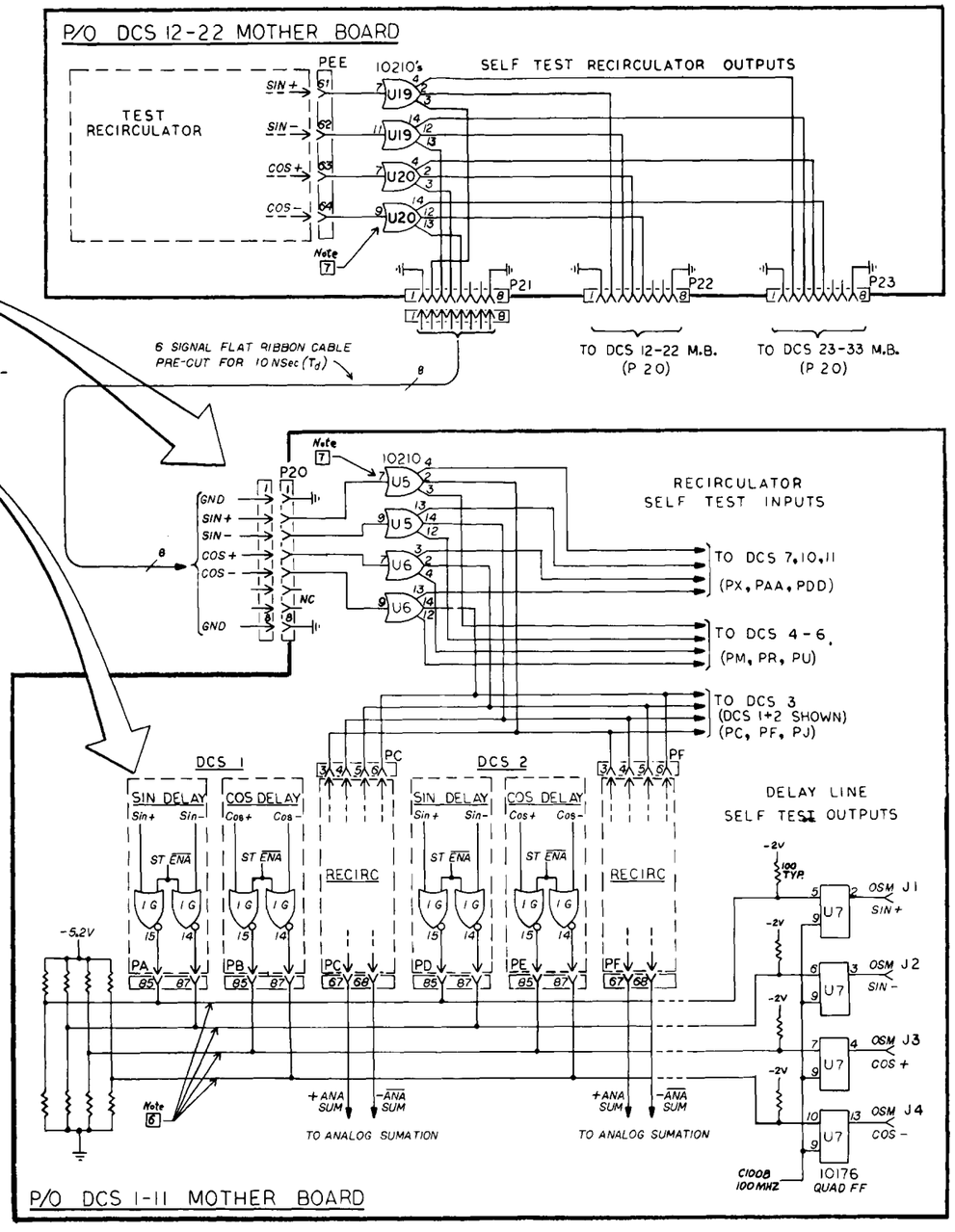
NOTES

1. 3-STATE OUTPUT OF DELAY LINE IS SELECTED TO DRIVE TEST DELAY LINE
2. INPUT TO TEST DELAY LINE; ONE MOTHER BOARD OUTPUT IS SELECTED BY THE TEST DELAY LINE INPUT MULTIPLEXER (MUX)
3. OUTPUT OF TEST DELAY LINE IS CABLED TO INPUT OF TEST RECIRCULATOR
4. OUTPUT OF TEST RECIRCULATOR IS FANNED-OUT TO DRIVE ALL MOTHER BOARDS
5. OUTPUT OF TEST RECIRCULATOR DRIVES RECIRCULATOR OUTPUT STAGES WHICH CAN BE PROGRAMMED TO SUBSTITUTE THE TEST RECIRCULATORS' DATA FOR IT'S OWN
6. 3-STATE BUS IS TERMINATED ON BOTH ENDS IN 100 OHMS. ENABLE TERM (ST ENA) IS SUPPLIED BY THE SYSTEM CONTROLLER TO ENABLE ONE EACH OF THE NINE SIN AND NINE COS DELAY LINES ON A MOTHER BOARD TO DRIVE THIS BUS. ONLY TWO (OF NINE) DELAY LINES ARE SHOWN ON THIS BUS.
7. FAN-OUT OF THE TEST RECIRCULATOR OUTPUT ALLOWS IT TO DRIVE ALL 27 ANTENNA RECIRCULATOR OUTPUT STAGES ON THREE (3) MOTHER BOARDS. THE SYSTEM CONTROLLER CAN PROGRAM ANY RECIRCULATOR TO SUBSTITUTE THE TEST RECIRCULATORS OUTPUT FOR IT'S OWN.

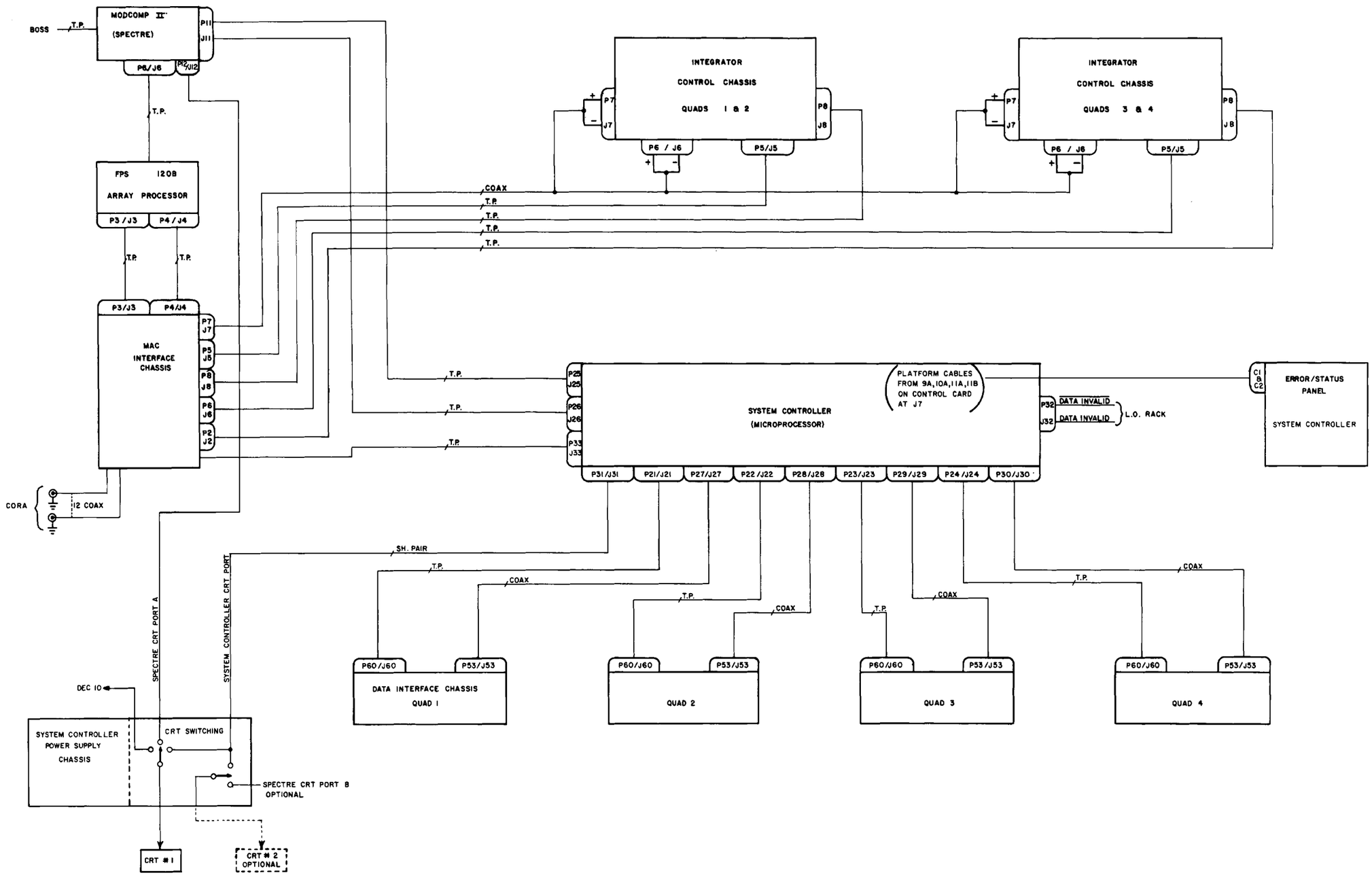








UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	PROJECT	NATIONAL RADIO ASTRONOMY OBSERVATORY
TOLERANCES: ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ±	TITLE: DELAY RACK TEST LOGIC INTERCONNECT DIAGRAM	SOCORRO, NEW MEXICO 87801
MATERIAL:		DRAWN BY / DATE 9-79
FINISH:		DESIGNED BY / DATE 4/23/82
NEXT ASSY / USED ON		APPROVED BY / DATE 4/23/82
	SHEET NUMBER / DRAWING NUMBER D13800B1	REV. / SCALE



REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON

PROJECT: DIGITAL DELAY SYSTEM COMBINED SPECTRAL/CONT. SYSTEM

TITLE: MASTER INTERCONNECTION DIAGRAM

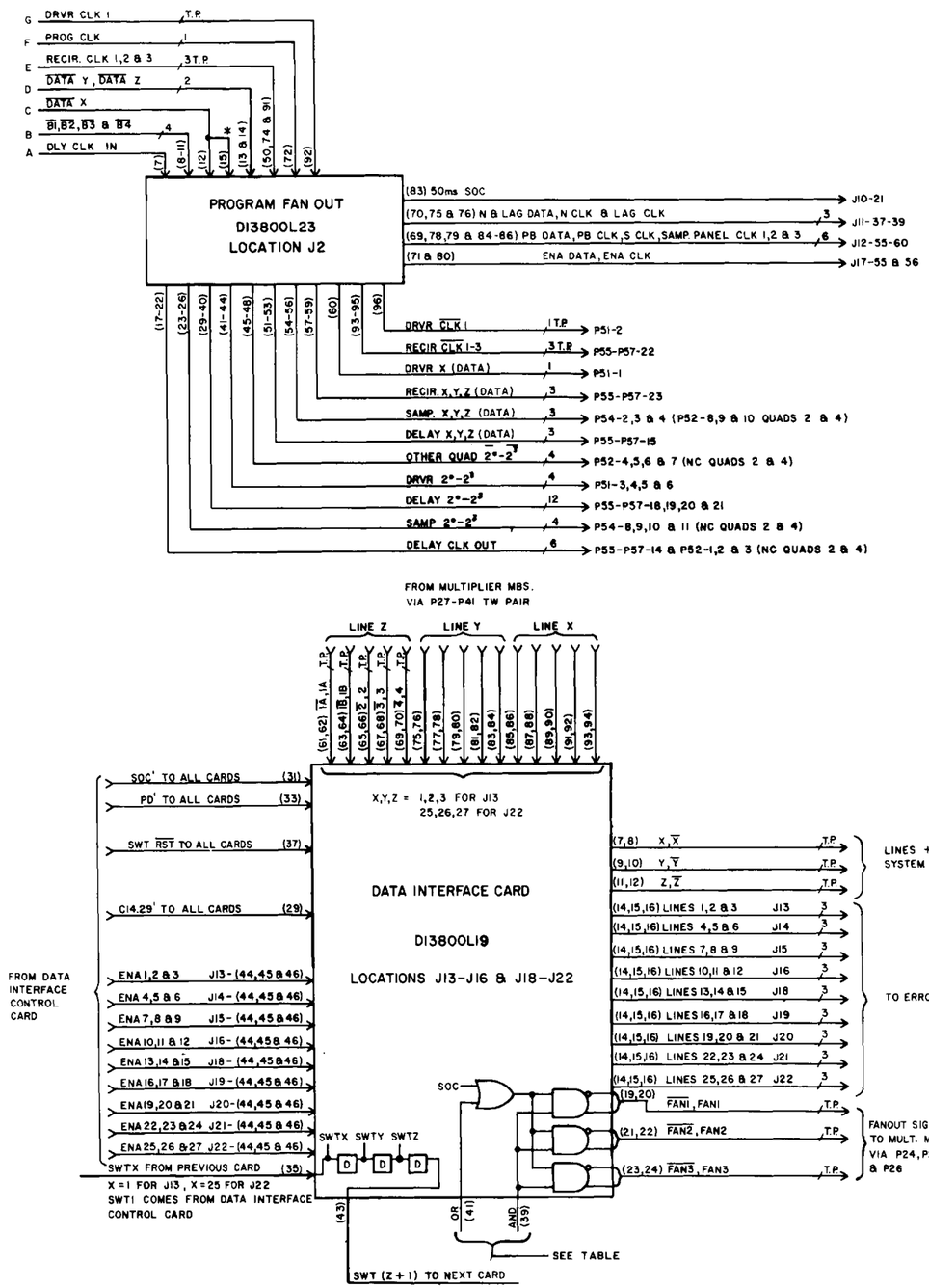
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY — DATE 11/6/79
DESIGNED BY — DATE
APPROVED BY — DATE

SHEET NUMBER — DRAWING NUMBER D13800B2 — REV. — SCALE

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

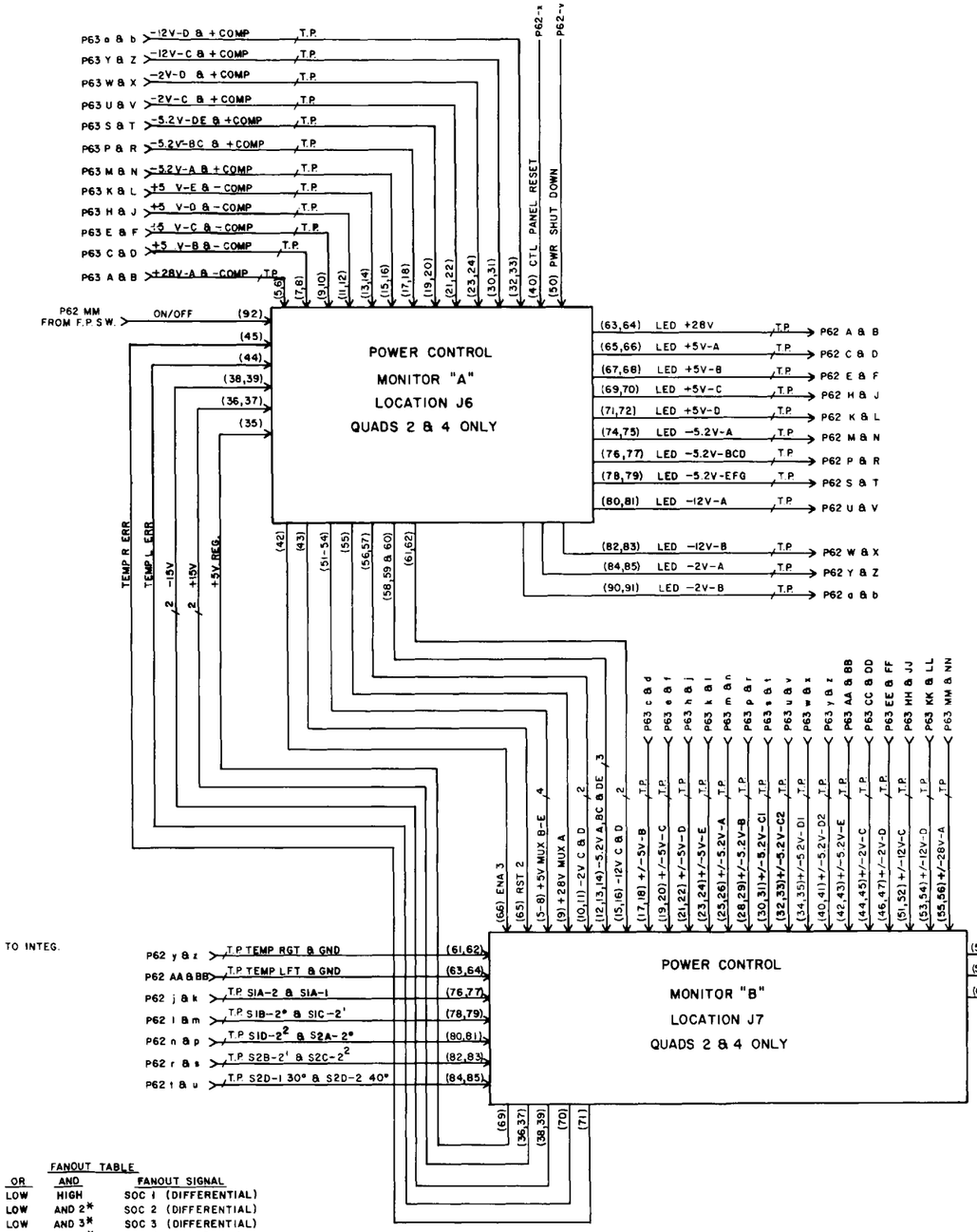
G-P60-H (DRVR CLK 2,3,4 QUADS 2,3,4)
F-P60-Y
E-P60-A,C & E (RECIR. CLK 4,5,6,7,8,9,10,11,12 QUADS 2,3 & 4)
D-P60-c & e
C-P60-a
B-P60-K,M,P & S QUADS 1 & 3 : P52-4,5,6 & 7 QUADS 2 & 4
A-P60-W QUADS 1 & 3 : NC QUADS 2 & 4
*-P60-S TO PINS 15 & 16 QUADS 2,3 & 4 ONLY -SIG
NAME-QUAD DATA



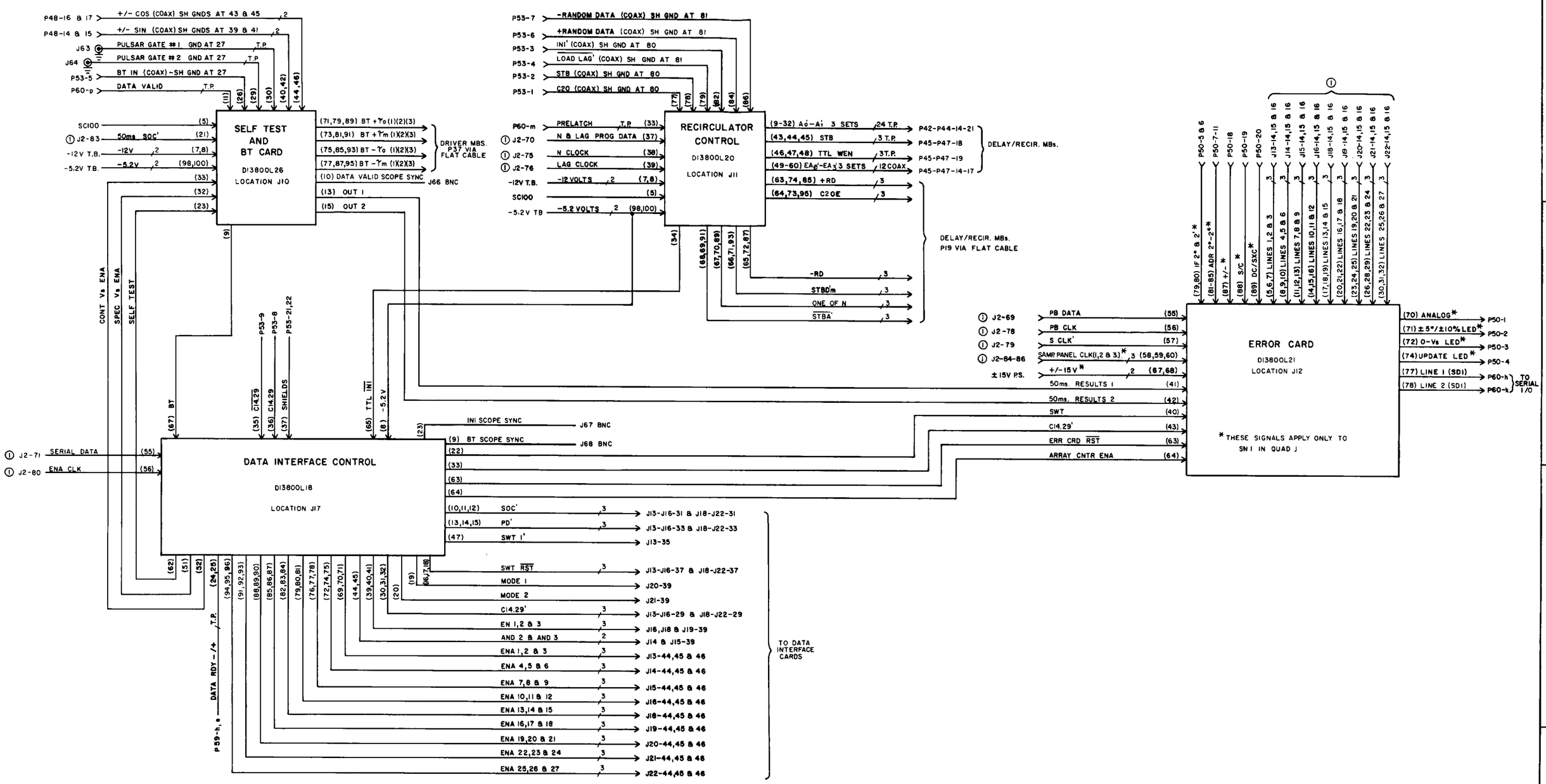
CARD	OR	AND	FANOUT SIGNAL
J13	LOW	HIGH	SOC 1 (DIFFERENTIAL)
J14	LOW	AND 2*	SOC 2 (DIFFERENTIAL)
J15	LOW	AND 3*	SOC 3 (DIFFERENTIAL)
J16	HIGH	EN 1*	EN 1 (SINGLE ENDED)
J18	HIGH	EN 2*	EN 2 (SINGLE ENDED)
J19	HIGH	EN 3*	EN 3 (SINGLE ENDED)
J20	HIGH	MODE 1*	MODE 1 (DIFFERENTIAL)
J21	HIGH	MODE 2*	MODE 2 (DIFFERENTIAL)
J22	NOT USED		

FANOUT TABLE

* = FROM DATA INTERFACE CONTROL CARD



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	VLA PROJECT	DIGITAL DELAY SYSTEM COMBINED SPECTRAL/CONT SYSTEM	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801
TOLERANCES: ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ±	TITLE	INTERFACE CHASSIS INTERCONNECTION DIAGRAM	DRAWN BY / DATE 11-22-79
MATERIAL:			DESIGNED BY / DATE
FINISH:			APPROVED BY / DATE
NEXT ASSY / USED ON		SHEET NUMBER 1/2 DRAWING NUMBER D13800B3	REV. / SCALE



NOTES:

1. ① = SIGNAL FROM SHEET 1

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY | USED ON

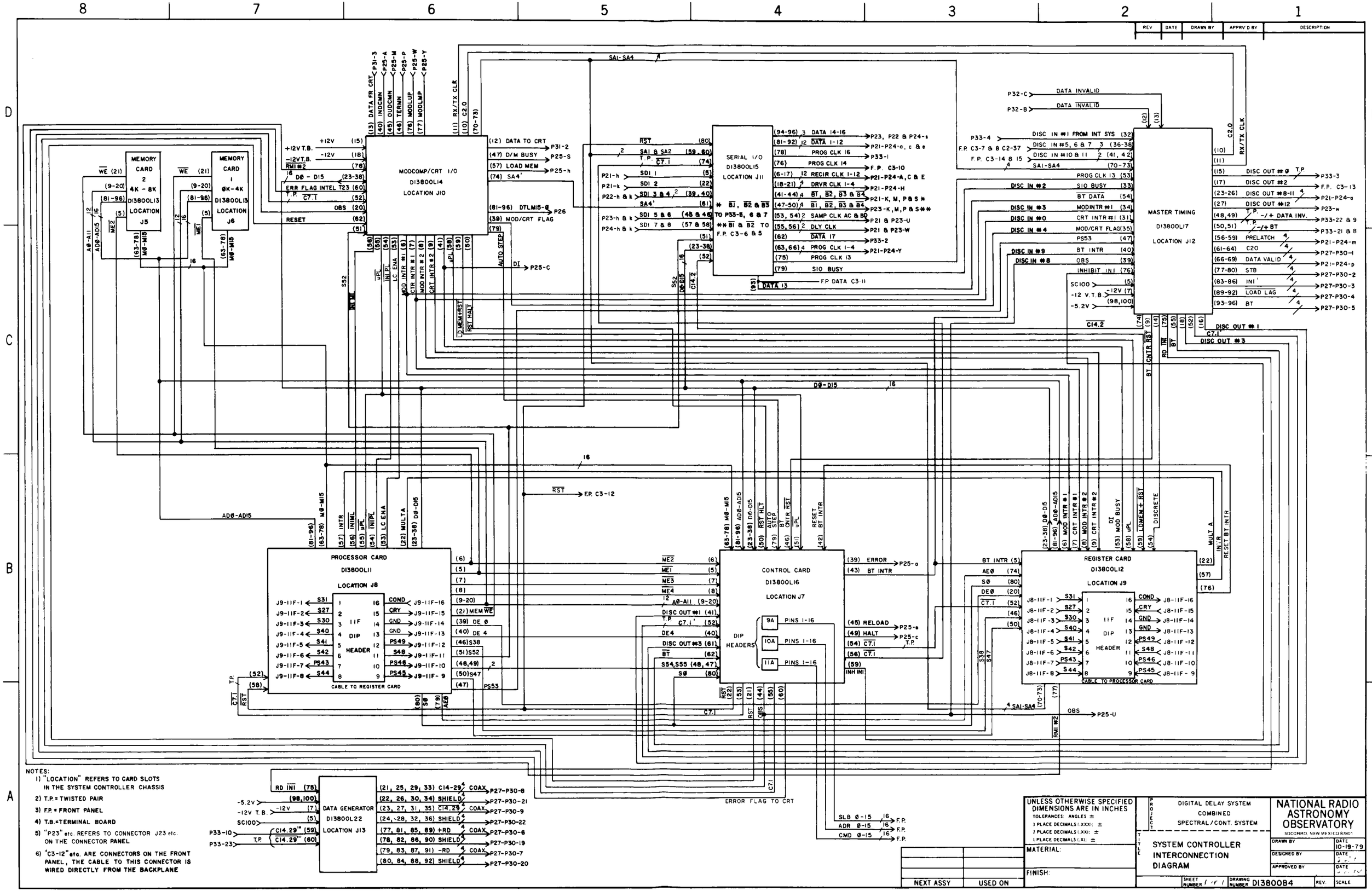
PROJECT: DIGITAL DELAY SYSTEM COMBINED SPECTRAL/CONT SYSTEM

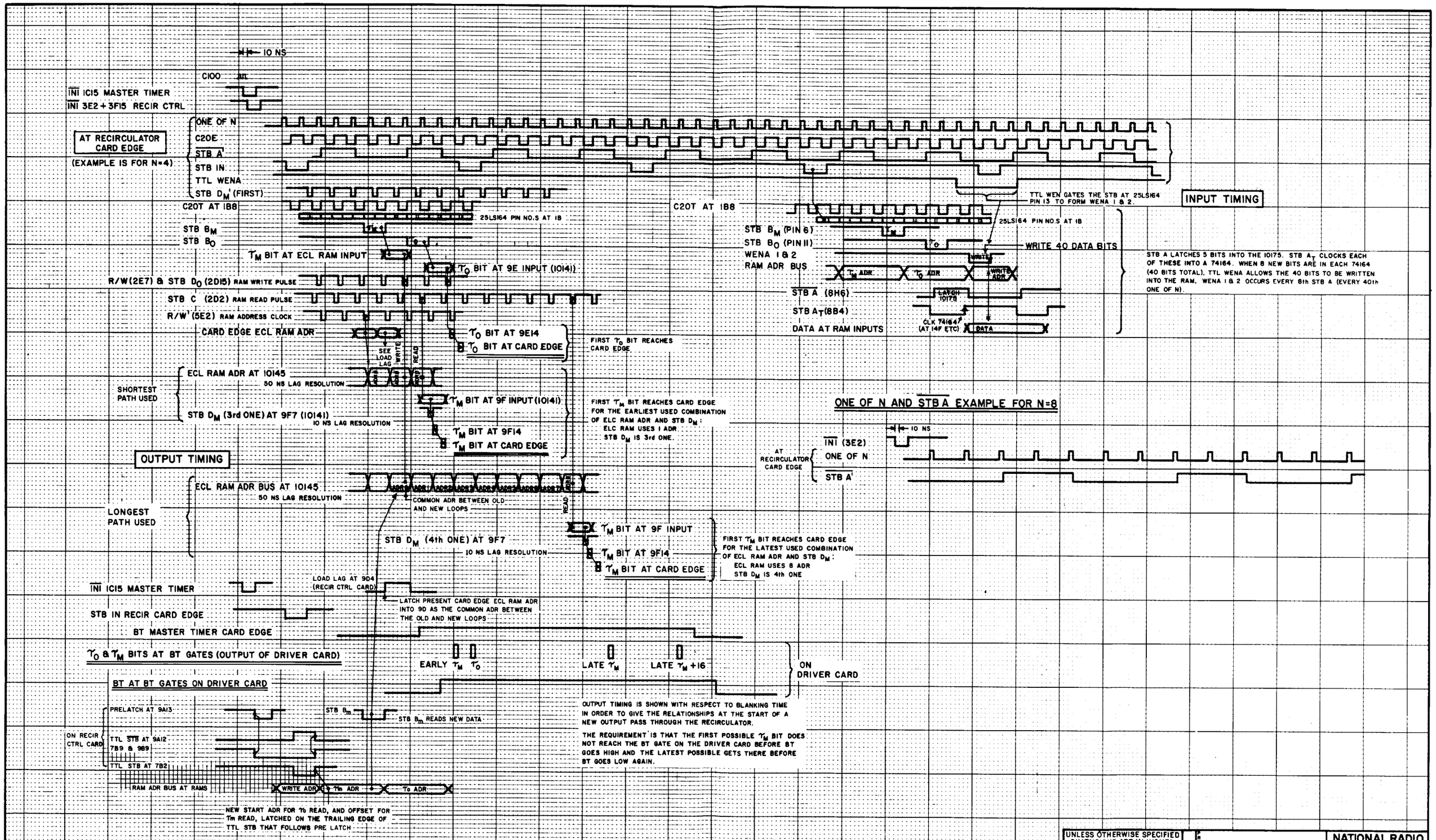
TITLE: INTERFACE CHASSIS INTERCONNECTION DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE 11-24-79
DESIGNED BY | DATE
APPROVED BY | DATE

SHEET NUMBER 2/2 | DRAWING NUMBER D13800B3 | REV. | SCALE


MODCOMP/CRT I/O
D13800L14
LOCATION J10
MEMORY CARD 2
4K - 8K
D13800L13
LOCATION J5
MEMORY CARD 1
0K-4K
D13800L13
LOCATION J6
SERIAL I/O
D13800L15
LOCATION J11
MASTER TIMING
D13800L17
LOCATION J12
PROCESSOR CARD
D13800L11
LOCATION J8
CONTROL CARD
D13800L16
LOCATION J7
REGISTER CARD
D13800L12
LOCATION J9
DIP HEADERS
CABLE TO REGISTER CARD
CABLE TO PROCESSOR CARD
DATA GENERATOR
D13800L22
LOCATION J13
ERROR FLAG TO CRT
NOTES:
1) "LOCATION" REFERS TO CARD SLOTS IN THE SYSTEM CONTROLLER CHASSIS
2) T.P. = TWISTED PAIR
3) F.P. = FRONT PANEL
4) T.B. = TERMINAL BOARD
5) "P23" etc. REFERS TO CONNECTOR J23 etc. ON THE CONNECTOR PANEL
6) "C3-12" etc. ARE CONNECTORS ON THE FRONT PANEL, THE CABLE TO THIS CONNECTOR IS WIRED DIRECTLY FROM THE BACKPLANE
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
DIGITAL DELAY SYSTEM
COMBINED
SPECTRAL/CONT. SYSTEM
SYSTEM CONTROLLER
INTERCONNECTION
DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DATE 10-19-79
DESIGNED BY
APPROVED BY
SHEET NUMBER 1 OF 1
DRAWING NUMBER D13800B4
REV.
SCALE



NOTE:
ALL IC DESIGNATIONS REFER TO ICs ON THE RECIRCULATOR CARD UNLESS OTHERWISE INDICATED.

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

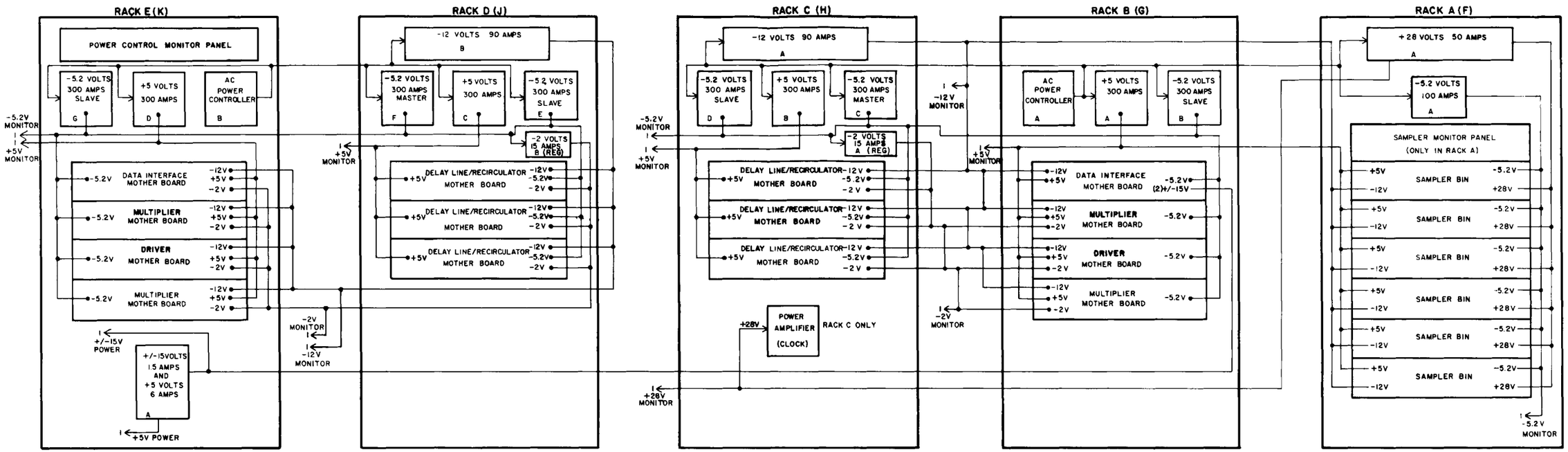
FINISH:

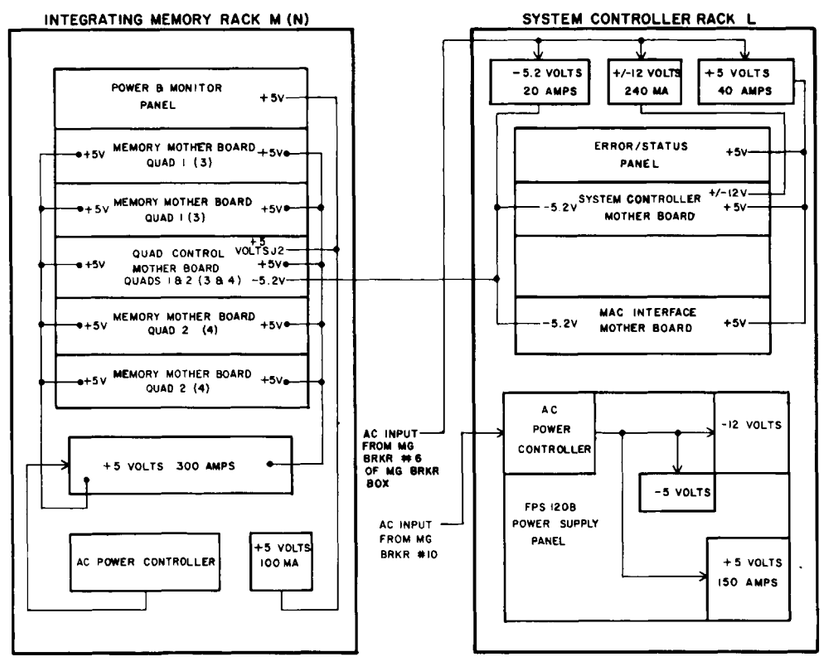
PROJECT

TITLE: RECIRCULATOR CARD TIMING

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY		DATE	12-05-79
DESIGNED BY		DATE	
APPROVED BY		DATE	
SHEET NUMBER	DRAWING NUMBER D13800B5	REV.	SCALE





NOTES:

( ) DESIGNATION FOR QUADS 3 & 4.

1. SIGNALS OR POWER TO J6 & J7 OF DATA INTERFACE MOTHER BOARD IN QUADS 2 & 4, RACKS E & K. (POWER MONITOR CARDS)
2. ONLY TO QUAD 1, RACK B, FOR SAMPLER MONITOR PANEL.

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

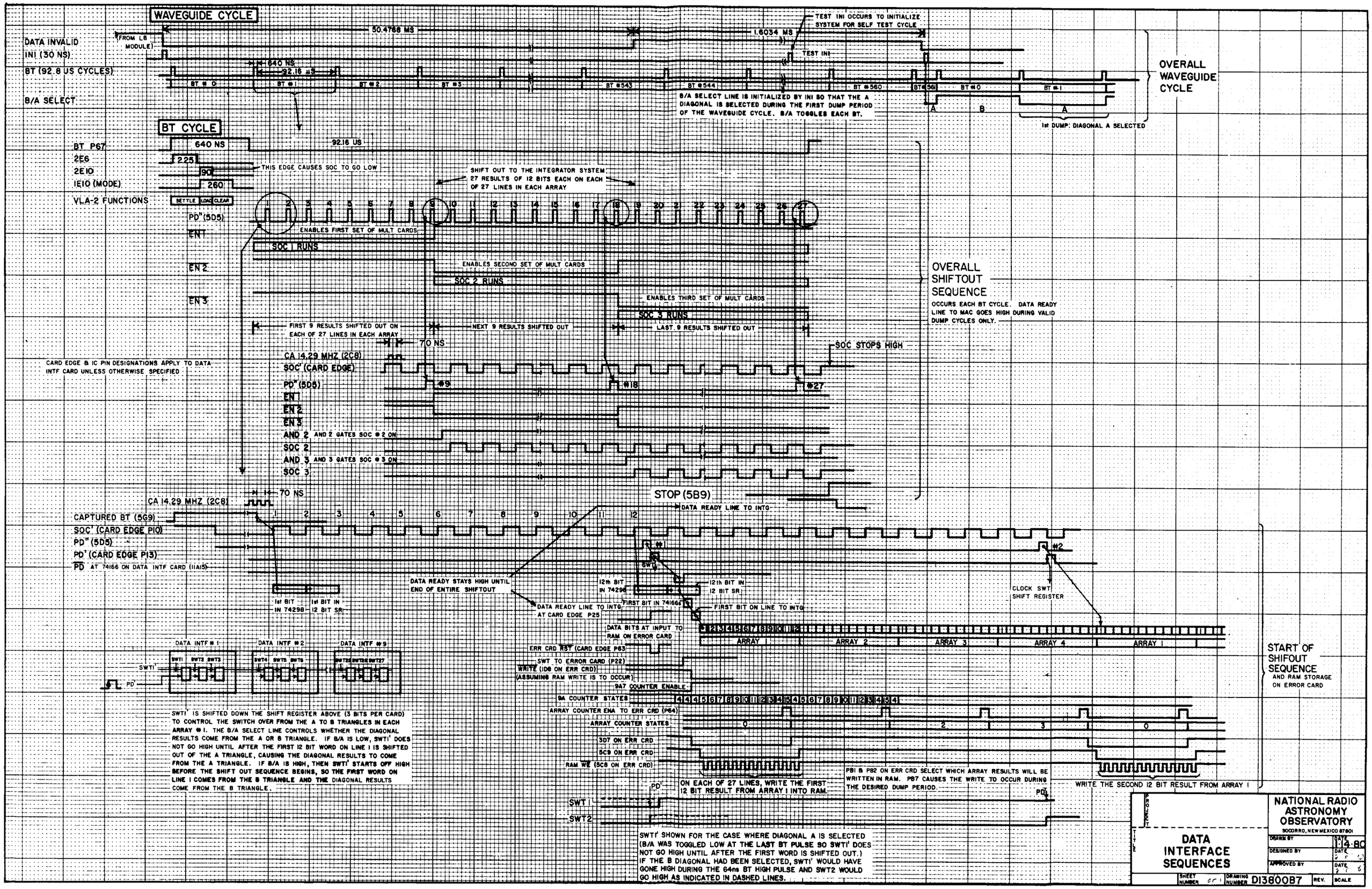
VLA PROJECT: DIGITAL DELAY SYSTEM COMBINED SPECTRAL/CONT. SYSTEM

TITLE: DC POWER DISTRIBUTION (DELAY/MULT. SYSTEM)

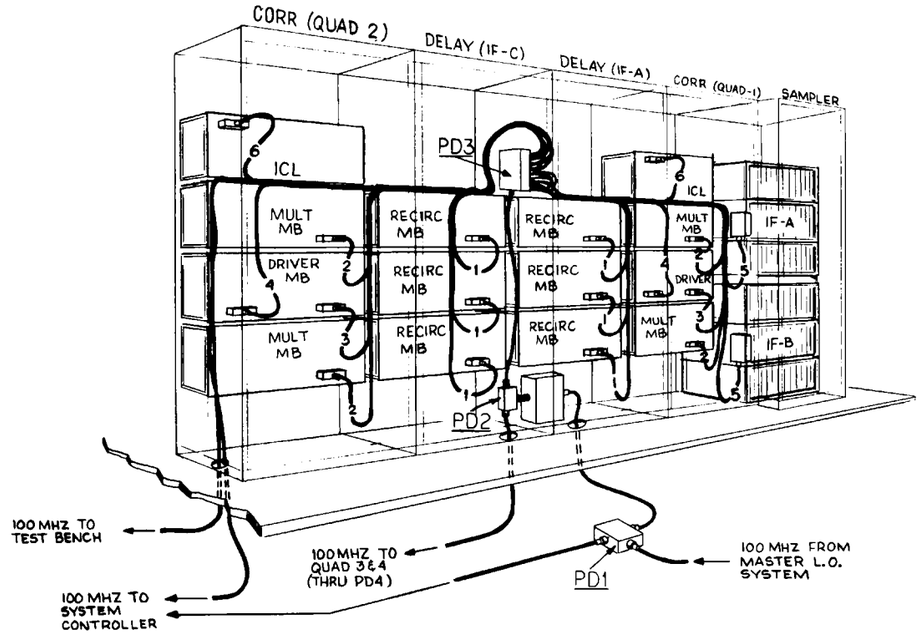
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO NEW MEXICO 87801

DRAWN BY		DATE	11/3/79
DESIGNED BY		DATE	
APPROVED BY		DATE	

SHEET NUMBER 1 | DRAWING NUMBER D13800B6 | REV. | SCALE


WAVEGUIDE CYCLE
DATA INVALID (FROM LB MODULE)
INI (30 NS)
BT (92.8 US CYCLES)
B/A SELECT
50.4766 MS
1.6034 MS
640 NS
92.16 µS
BT # 0
BT #1
BT #2
BT #3
BT #543
BT #544
BT #560
BT #561
TEST INI OCCURS TO INITIALIZE SYSTEM FOR SELF TEST CYCLE
TEST INI
B/A SELECT LINE IS INITIALIZED BY INI SO THAT THE A DIAGONAL IS SELECTED DURING THE FIRST DUMP PERIOD OF THE WAVEGUIDE CYCLE. B/A TOGGLES EACH BT.
A
B
A
1st DUMP: DIAGONAL A SELECTED
OVERALL WAVEGUIDE CYCLE
BT CYCLE
BT P67
2E6
2E10
1E10 (MODE)
VLA-2 FUNCTIONS
640 NS
92.16 US
225
90
260
SETTLE
LOAD
CLEAR
THIS EDGE CAUSES SOC TO GO LOW
SHIFT OUT TO THE INTEGRATOR SYSTEM 27 RESULTS OF 12 BITS EACH ON EACH OF 27 LINES IN EACH ARRAY
PD" (5D5)
EN1
ENABLES FIRST SET OF MULT CARDS
SOC 1 RUNS
EN2
ENABLES SECOND SET OF MULT CARDS
SOC 2 RUNS
EN3
ENABLES THIRD SET OF MULT CARDS
SOC 3 RUNS
FIRST 9 RESULTS SHIFTED OUT ON EACH OF 27 LINES IN EACH ARRAY
NEXT 9 RESULTS SHIFTED OUT
LAST 9 RESULTS SHIFTED OUT
70 NS
SOC STOPS HIGH
OVERALL SHIFTOUT SEQUENCE
OCCURS EACH BT CYCLE. DATA READY LINE TO MAC GOES HIGH DURING VALID DUMP CYCLES ONLY.
CARD EDGE & IC PIN DESIGNATIONS APPLY TO DATA INTF CARD UNLESS OTHERWISE SPECIFIED
CA 14.29 MHZ (2C8)
SOC' (CARD EDGE)
PD" (5D5)
EN1
EN2
EN3
AND 2 AND 2 GATES SOC #2 ON
SOC 2
AND 3 AND 3 GATES SOC #3 ON
SOC 3
#9
#18
#27
CA 14.29 MHZ (2C8)
70 NS
STOP (5B9)
DATA READY LINE TO INTG
CAPTURED BT (5G9)
SOC' (CARD EDGE P10)
PD" (5D5)
PD' (CARD EDGE P13)
PD AT 74166 ON DATA INTF CARD (11A15)
#1
SWT1
#2
CLOCK SWT SHIFT REGISTER
DATA READY STAYS HIGH UNTIL END OF ENTIRE SHIFTOUT
1st BIT IN 74298
1st BIT IN 12 BIT SR
12th BIT IN 74298
12th BIT IN 12 BIT SR
DATA READY LINE TO INTG AT CARD EDGE P25
FIRST BIT IN 74166
FIRST BIT ON LINE TO INTG
DATA BITS AT INPUT TO RAM ON ERROR CARD
ARRAY 1
ARRAY 2
ARRAY 3
ARRAY 4
ARRAY 1
START OF SHIFOUT SEQUENCE AND RAM STORAGE ON ERROR CARD
DATA INTF #1
DATA INTF #2
DATA INTF #9
SWT1
SWT2
SWT3
SWT4
SWT5
SWT6
SWT25
SWT26
SWT27
SWT1'
PD'
ERR CRD RST (CARD EDGE P63)
SWT TO ERROR CARD (P22)
WRITE (1D6 ON ERR CRD) (ASSUMING RAM WRITE IS TO OCCUR)
9A7 COUNTER ENABLE
9A COUNTER STATES
ARRAY COUNTER ENA TO ERR CRD (P64)
ARRAY COUNTER STATES
3D7 ON ERR CRD
5C9 ON ERR CRD
RAM WE (5C8 ON ERR CRD)
PD'
SWT1
SWT2
ON EACH OF 27 LINES, WRITE THE FIRST 12 BIT RESULT FROM ARRAY 1 INTO RAM.
PB1 & PB2 ON ERR CRD SELECT WHICH ARRAY RESULTS WILL BE WRITTEN IN RAM. PB7 CAUSES THE WRITE TO OCCUR DURING THE DESIRED DUMP PERIOD.
PD'
WRITE THE SECOND 12 BIT RESULT FROM ARRAY 1
SWT1' IS SHIFTED DOWN THE SHIFT REGISTER ABOVE (3 BITS PER CARD) TO CONTROL THE SWITCH OVER FROM THE A TO B TRIANGLES IN EACH ARRAY #1. THE B/A SELECT LINE CONTROLS WHETHER THE DIAGONAL RESULTS COME FROM THE A OR B TRIANGLE. IF B/A IS LOW, SWT1' DOES NOT GO HIGH UNTIL AFTER THE FIRST 12 BIT WORD ON LINE 1 IS SHIFTED OUT OF THE A TRIANGLE, CAUSING THE DIAGONAL RESULTS TO COME FROM THE A TRIANGLE. IF B/A IS HIGH, THEN SWT1' STARTS OFF HIGH BEFORE THE SHIFT OUT SEQUENCE BEGINS, SO THE FIRST WORD ON LINE 1 COMES FROM THE B TRIANGLE AND THE DIAGONAL RESULTS COME FROM THE B TRIANGLE.
SWT1' SHOWN FOR THE CASE WHERE DIAGONAL A IS SELECTED (B/A WAS TOGGLED LOW AT THE LAST BT PULSE SO SWT1' DOES NOT GO HIGH UNTIL AFTER THE FIRST WORD IS SHIFTED OUT.) IF THE B DIAGONAL HAD BEEN SELECTED, SWT1' WOULD HAVE GONE HIGH DURING THE 64ns BT HIGH PULSE AND SWT2 WOULD GO HIGH AS INDICATED IN DASHED LINES.
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
TITLE
DATA INTERFACE SEQUENCES
DRAWN BY
DATE 1-4-80
DESIGNED BY
APPROVED BY
SHEET NUMBER
DRAWING NUMBER D13800B7
REV.
SCALE

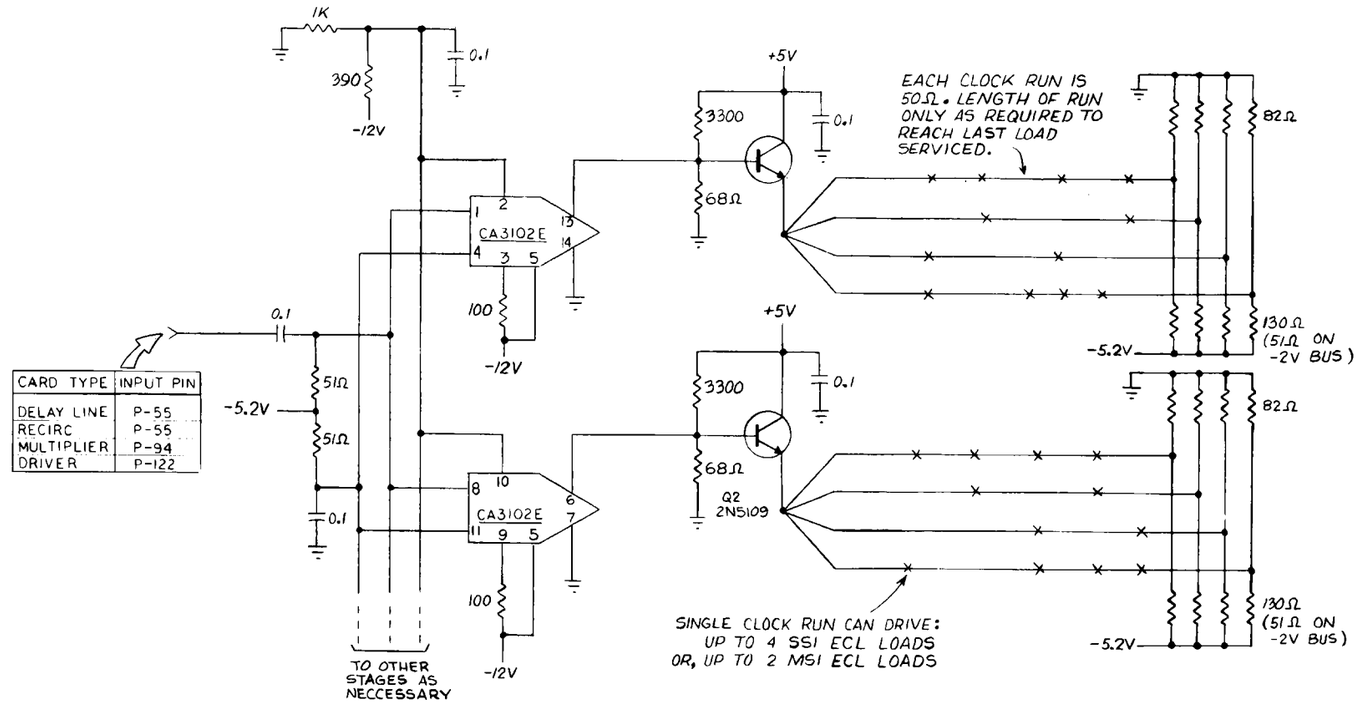
REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



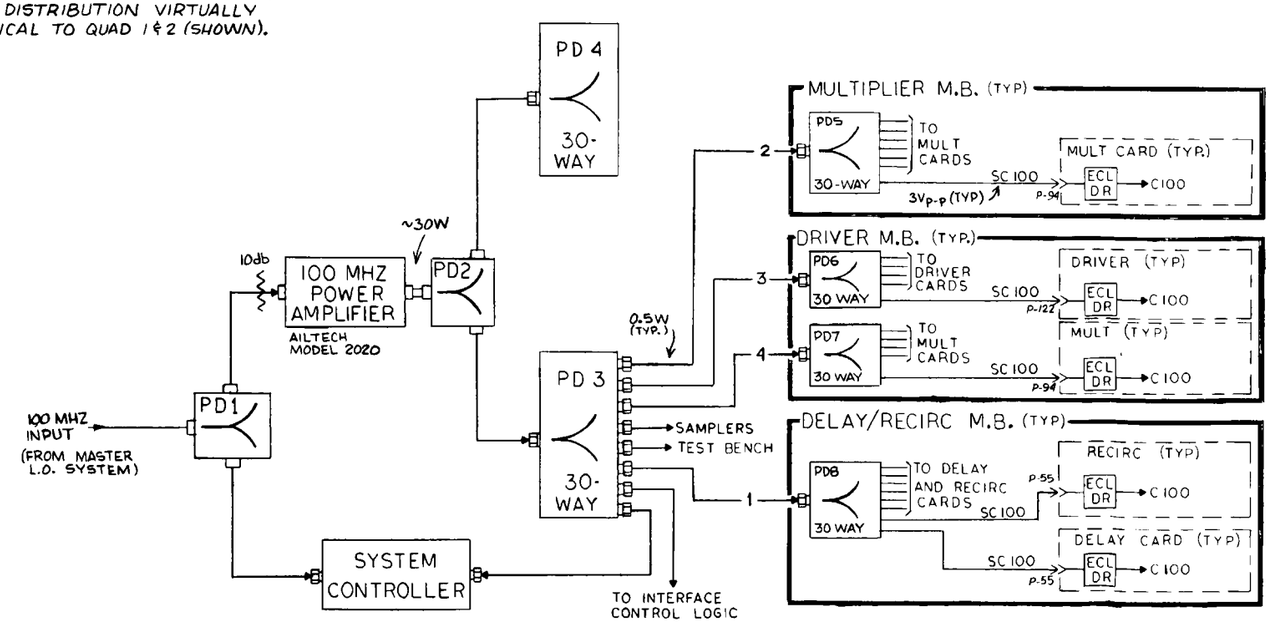
100MHZ DISTRIBUTION QUADS 1 and 2, PICTORAL

LEGEND →
PD = POWER DIVIDER. DESIGNATIONS FOR ILLUSTRATION PUPOSES ONLY. QUAD 3 & 4 DISTRIBUTION VIRTUALLY IDENTICAL TO QUAD 1 & 2 (SHOWN).

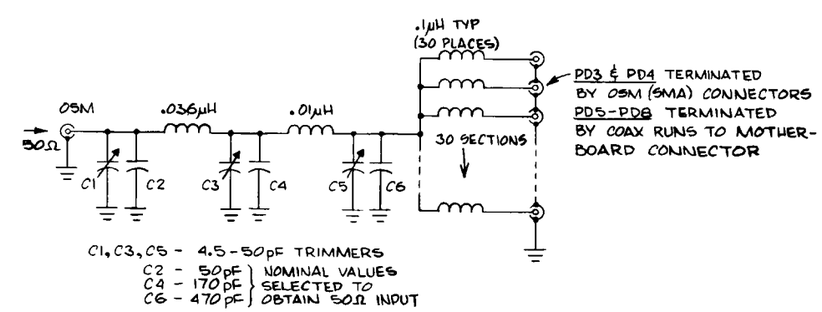
100MHZ E-C-L CLOCK DRIVER



CARD TYPE	INPUT PIN
DELAY LINE	P-55
RECIRC	P-55
MULTIPLIER	P-94
DRIVER	P-122



100 MHZ 30-WAY POWER DIVIDER DETAIL



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY | USED ON

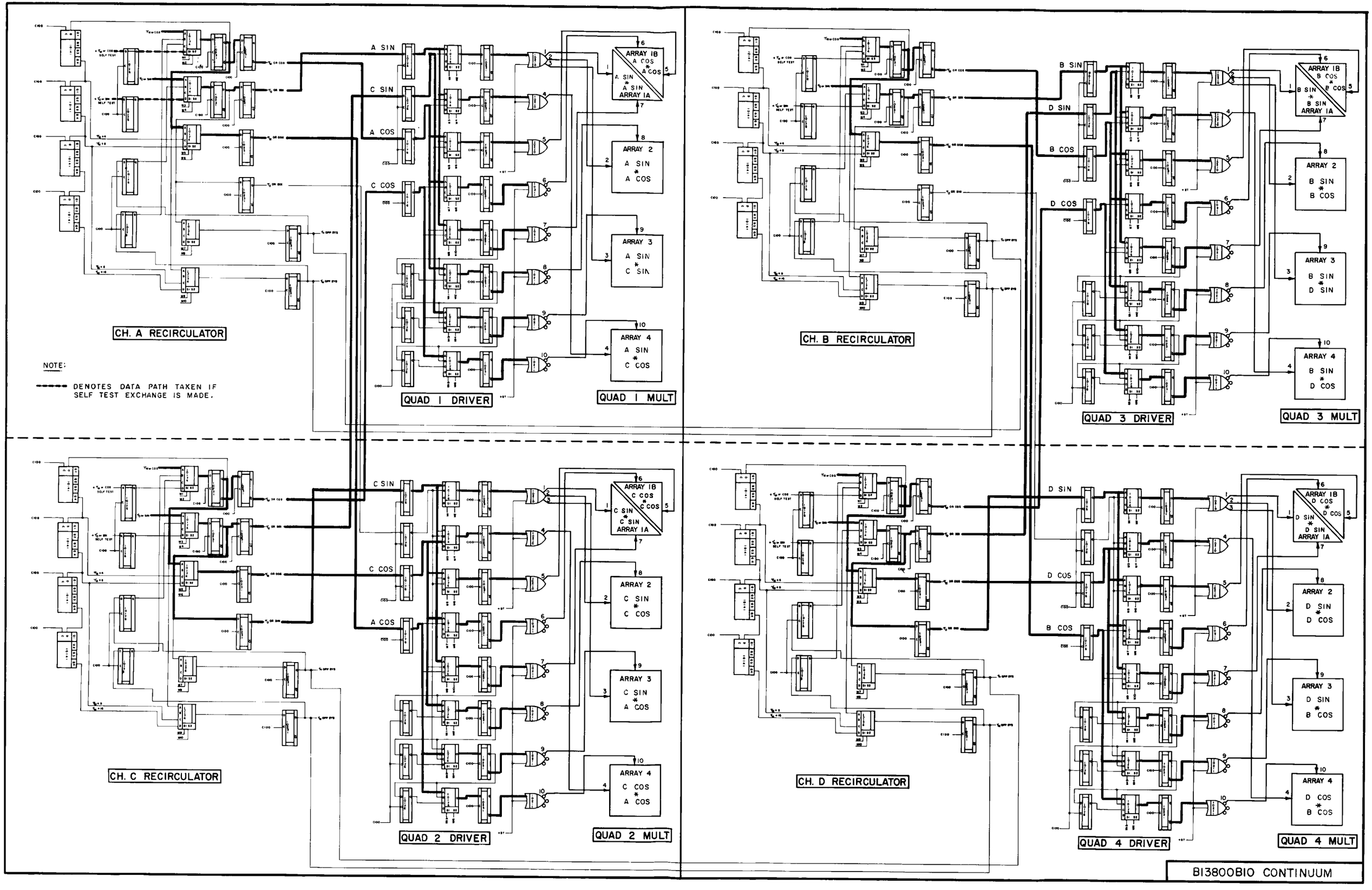
PROJECT: VLA — CORRELATOR SYSTEM

TITLE: CLOCK DISTRIBUTION

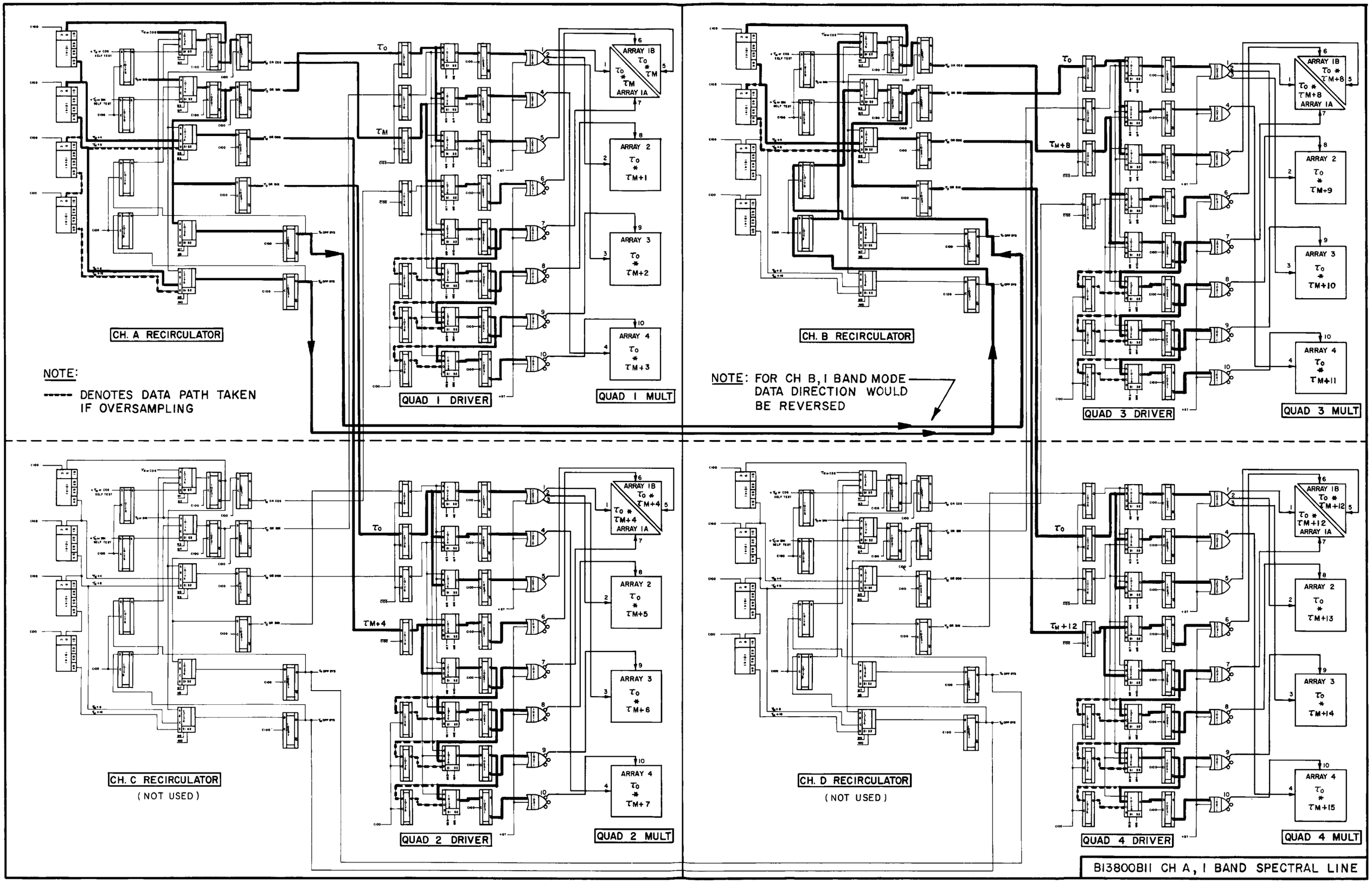
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

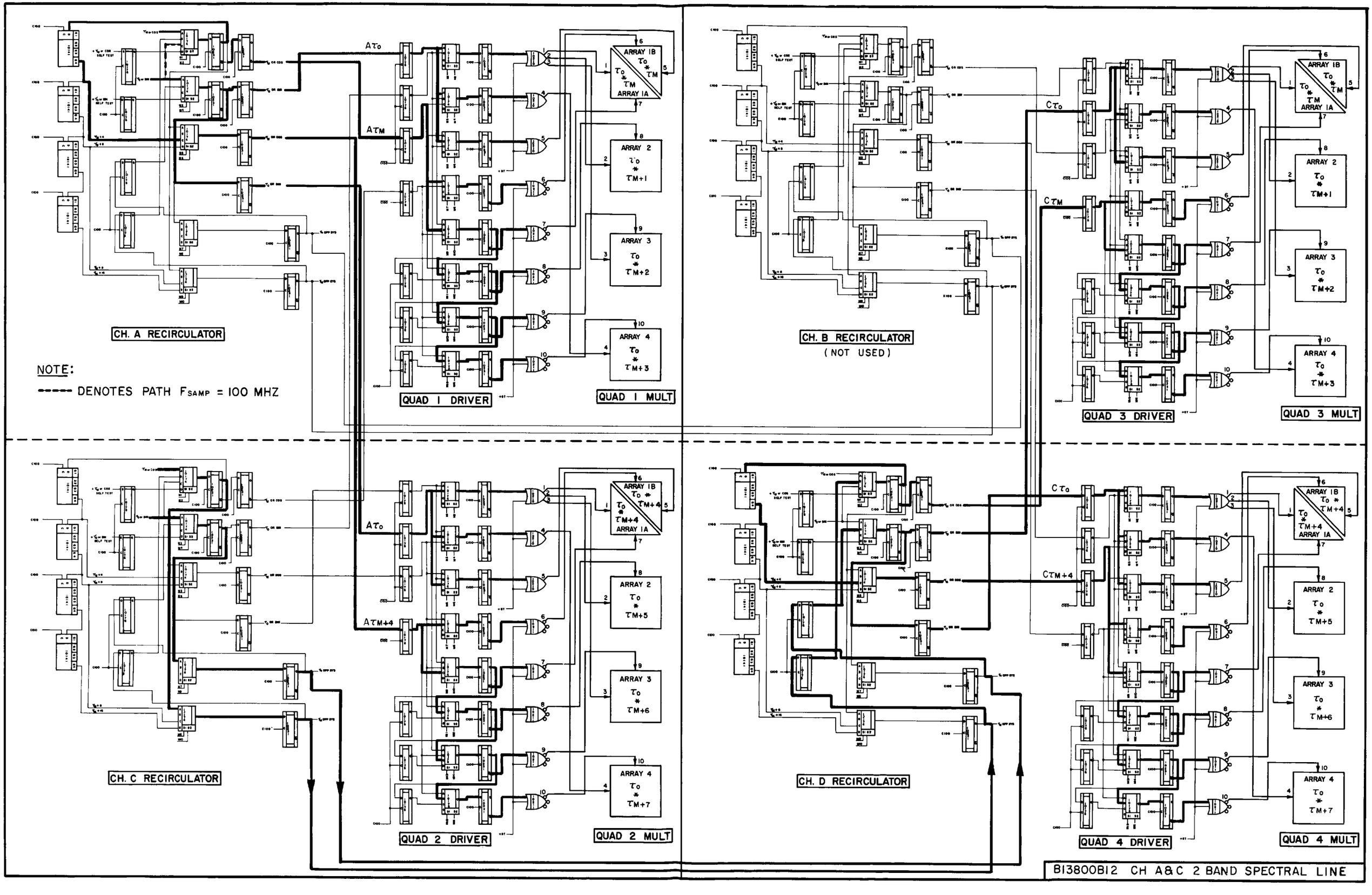
DRAWN BY		DATE JAN 80
DESIGNED BY		DATE 4-14-80
APPROVED BY		DATE 4-14-80

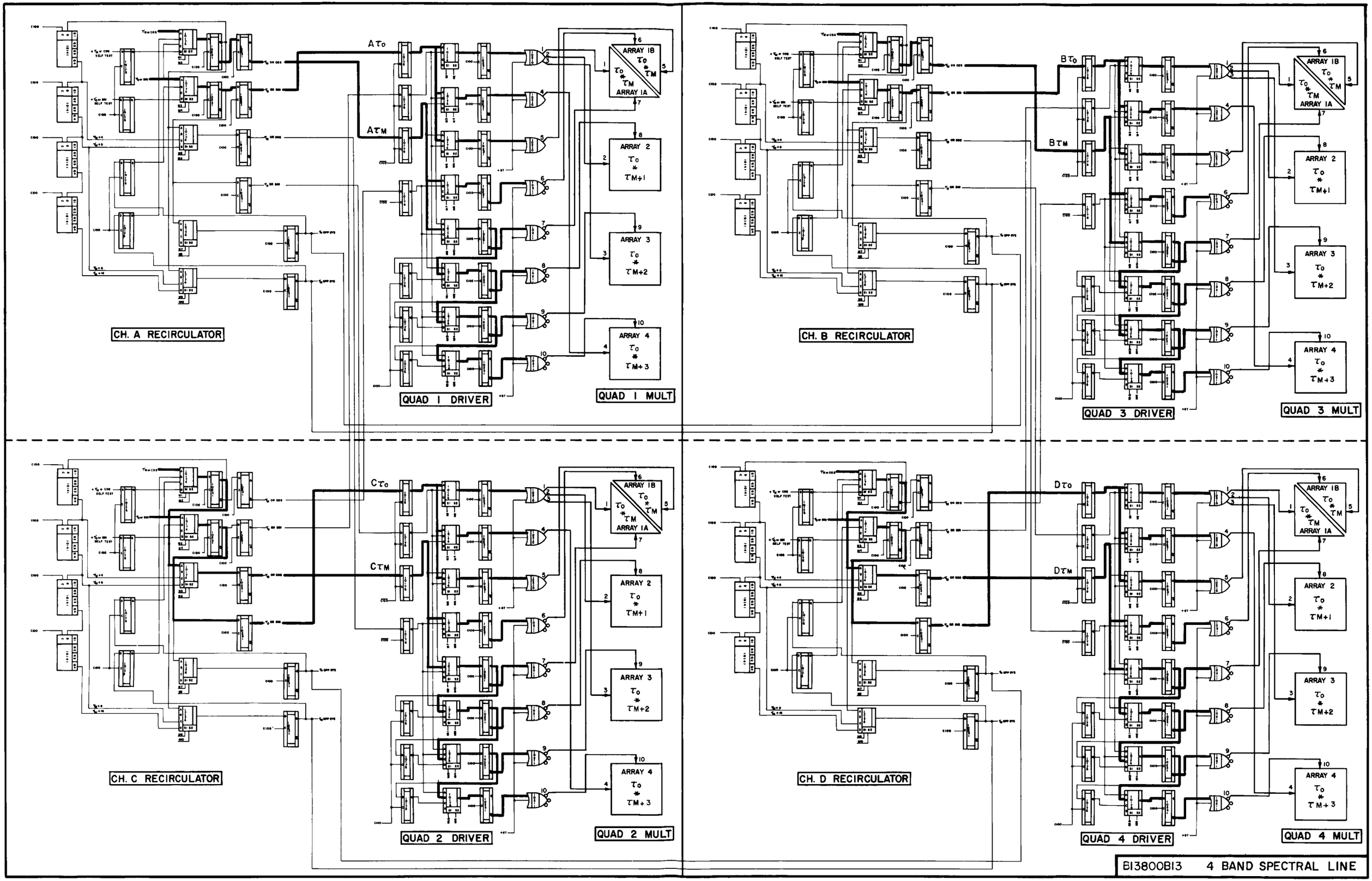
SHEET NUMBER 1 OF 1 | DRAWING NUMBER D13800B8 | REV. | SCALE



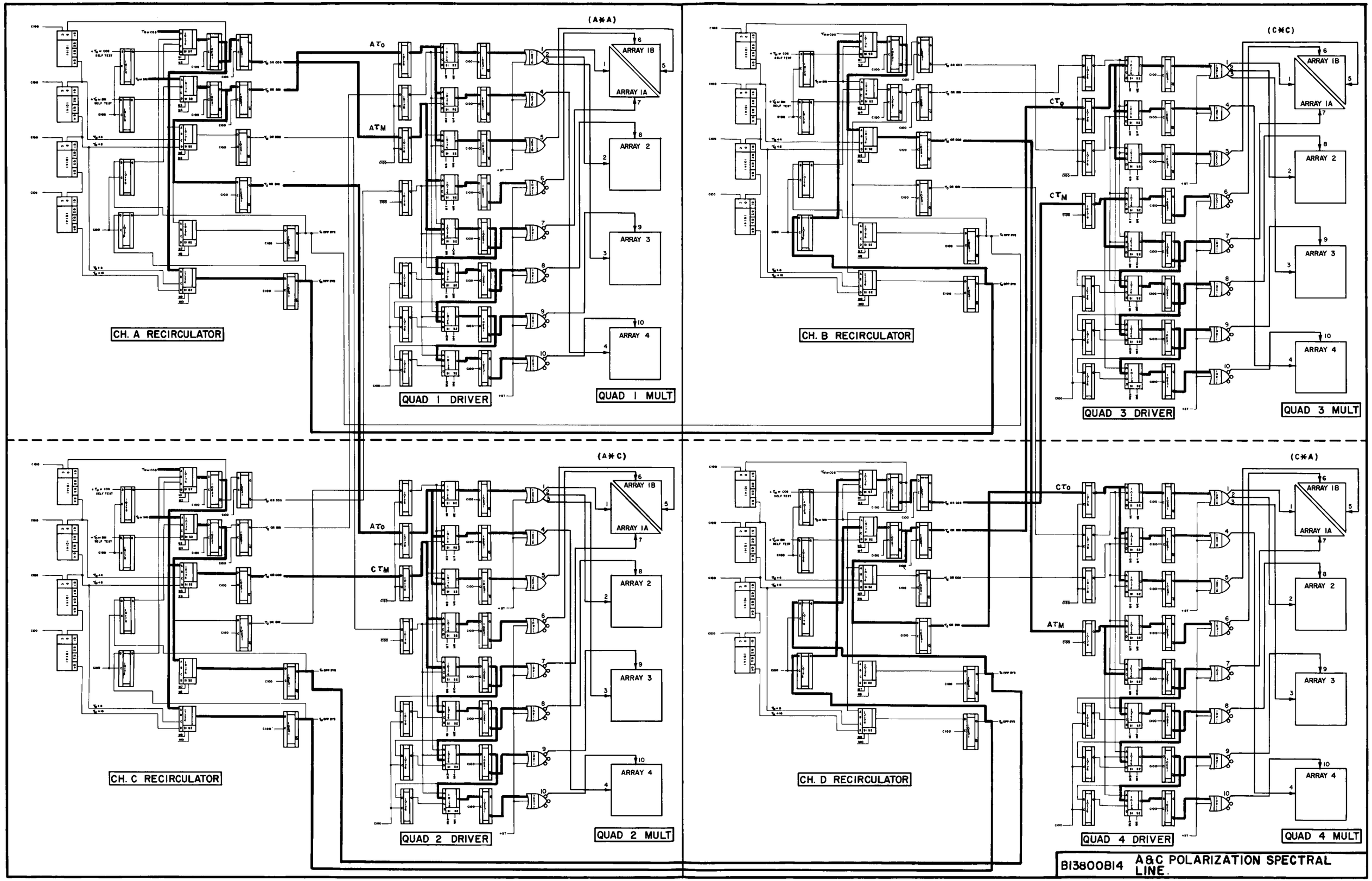
B13800B10 CONTINUUM


CH. A RECIRCULATOR
CH. B RECIRCULATOR
CH. C RECIRCULATOR
(NOT USED)
CH. D RECIRCULATOR
(NOT USED)
QUAD 1 DRIVER
QUAD 1 MULT
QUAD 2 DRIVER
QUAD 2 MULT
QUAD 3 DRIVER
QUAD 3 MULT
QUAD 4 DRIVER
QUAD 4 MULT
ARRAY 1A
ARRAY 1B
ARRAY 2
ARRAY 3
ARRAY 4
NOTE:
DENOTES DATA PATH TAKEN IF OVERSAMPLING
NOTE: FOR CH B, I BAND MODE DATA DIRECTION WOULD BE REVERSED
B13800B11 CH A, I BAND SPECTRAL LINE

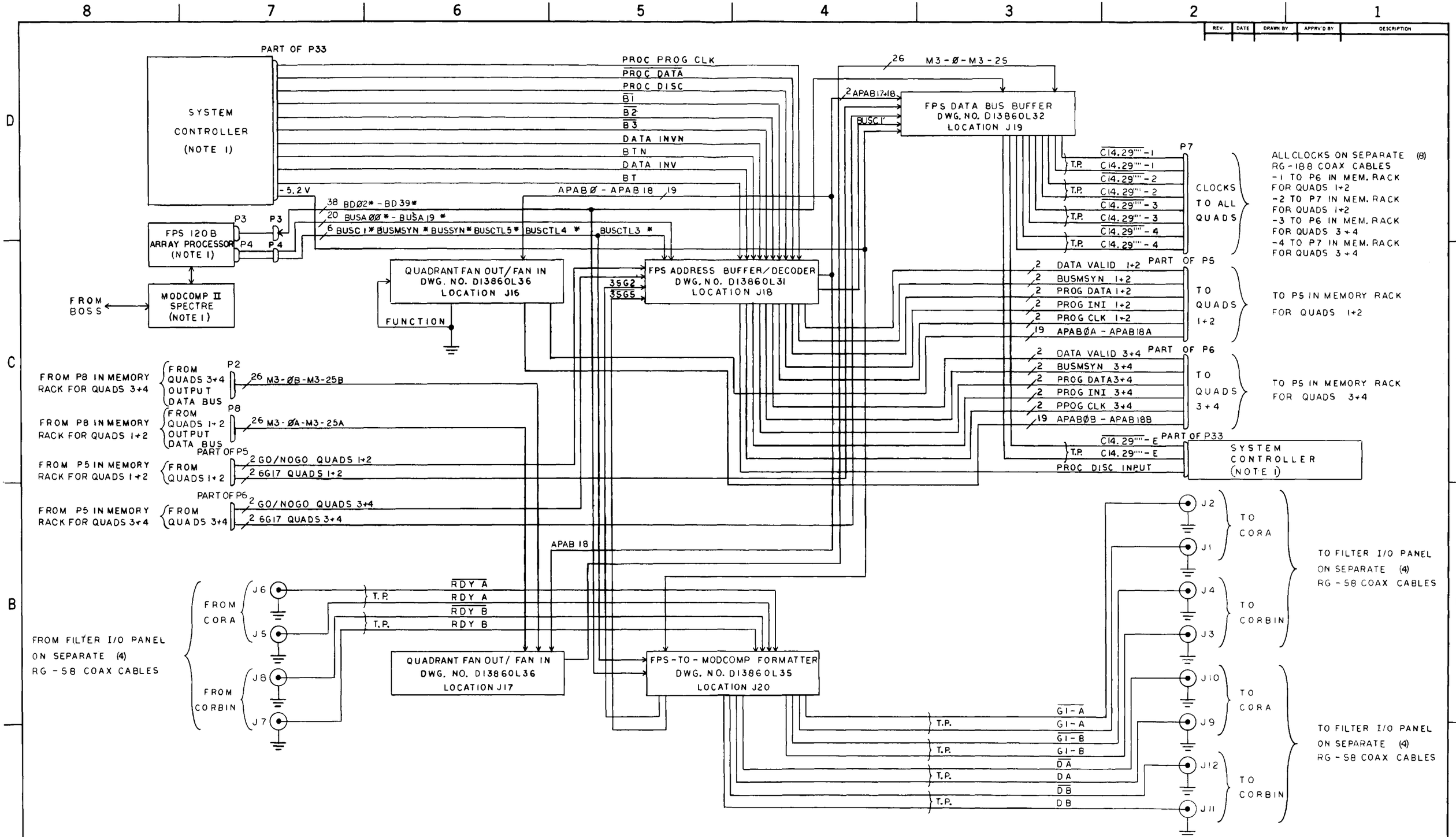

CH. A RECIRCULATOR
CH. B RECIRCULATOR
(NOT USED)
CH. C RECIRCULATOR
CH. D RECIRCULATOR
QUAD 1 DRIVER
QUAD 2 DRIVER
QUAD 3 DRIVER
QUAD 4 DRIVER
QUAD 1 MULT
QUAD 2 MULT
QUAD 3 MULT
QUAD 4 MULT
ARRAY 1A
ARRAY 1B
ARRAY 2
ARRAY 3
ARRAY 4
NOTE:
DENOTES PATH FSAMP = 100 MHZ
B13800B12 CH A&C 2 BAND SPECTRAL LINE

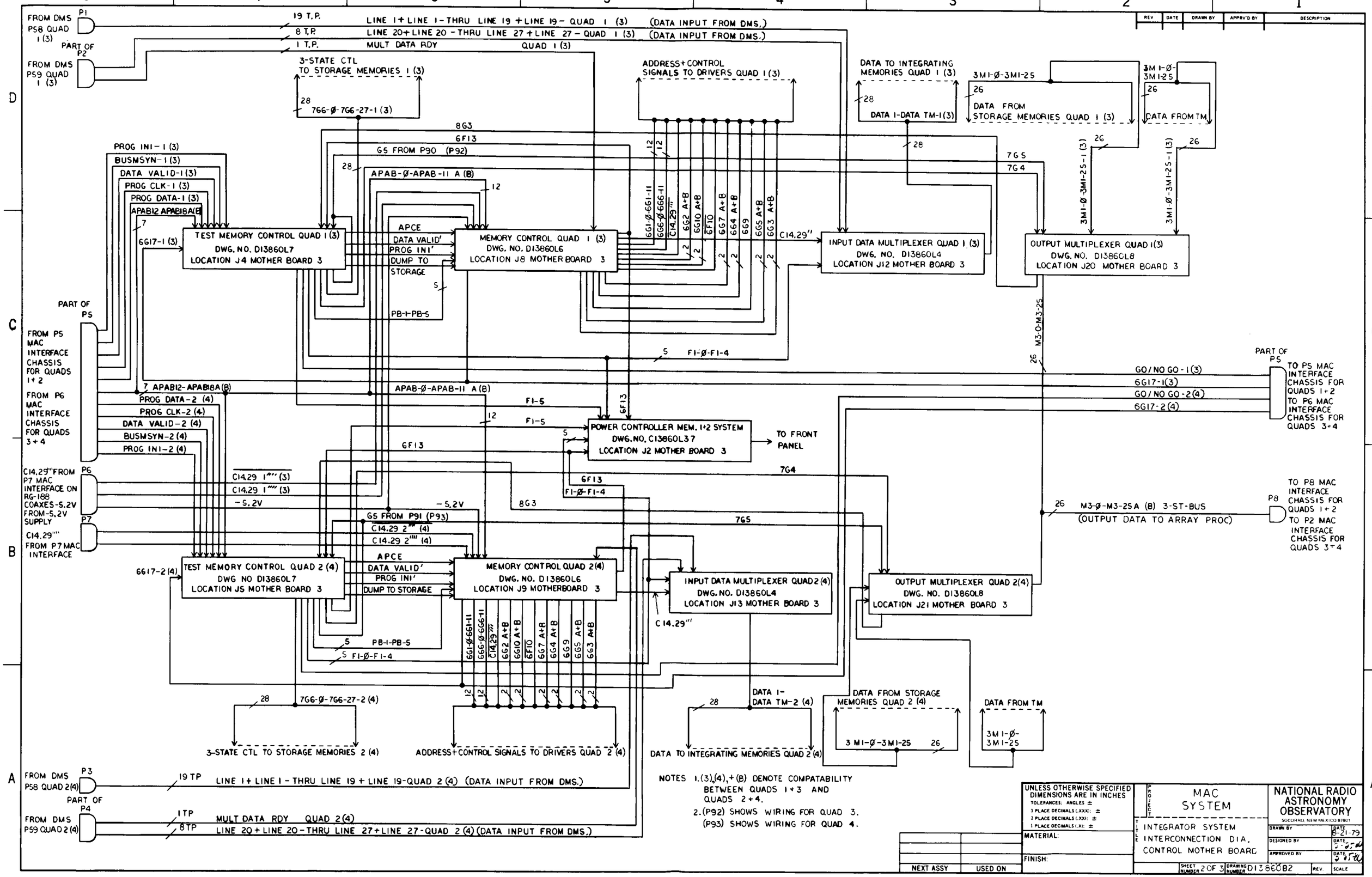


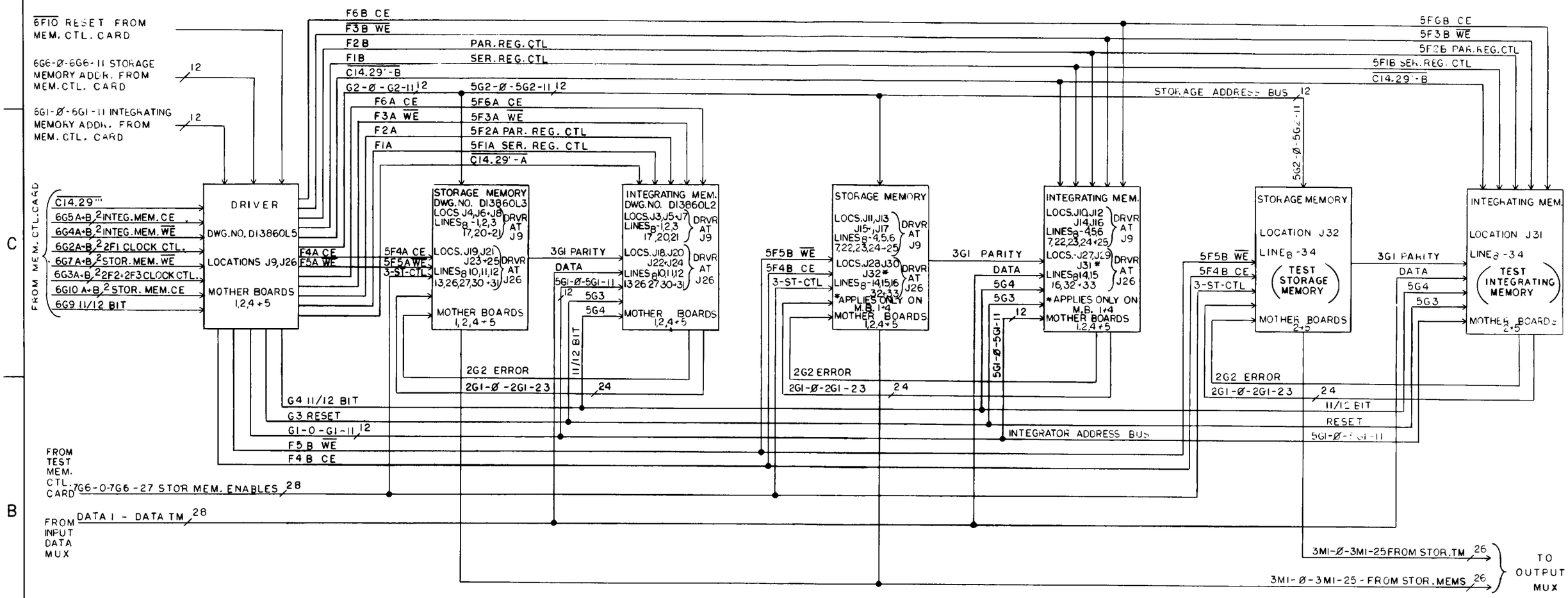
B13800B13 4 BAND SPECTRAL LINE



B13800B14 A&C POLARIZATION SPECTRAL LINE.


PART OF P33
SYSTEM CONTROLLER (NOTE 1)
PROC PROG CLK
PROC DATA
PROC DISC
B1
B2
B3
DATA INVN
BTN
DATA INV
BT
APABØ - APAB18
19
-5.2V
38 BDØ2* - BD39*
20 BUSAØØ* - BUSA19*
6 BUSC1* BUSMSYN* BUSSYN* BUSCTL5* BUSCTL4* BUSCTL3*
26 M3-Ø-M3-25
2 APAB17,18
BUSC1*
FPS DATA BUS BUFFER DWG. NO. D13860L32 LOCATION J19
FPS 120B ARRAY PROCESSOR (NOTE 1)
P3
P4
MODCOMP II SPECTRE (NOTE 1)
FROM BOSS
QUADRANT FAN OUT/FAN IN DWG. NO. D13860L36 LOCATION J16
FUNCTION
FPS ADDRESS BUFFER/DECODER DWG. NO. D13860L31 LOCATION J18
3SG2
3SG5
P7
C14.29''''-1
C14.29''''-2
C14.29''''-3
C14.29''''-4
T.P.
CLOCKS TO ALL QUADS
ALL CLOCKS ON SEPARATE RG-188 COAX CABLES (8)
-1 TO P6 IN MEM. RACK FOR QUADS 1+2
-2 TO P7 IN MEM. RACK FOR QUADS 1+2
-3 TO P6 IN MEM. RACK FOR QUADS 3+4
-4 TO P7 IN MEM. RACK FOR QUADS 3+4
PART OF P5
2 DATA VALID 1+2
2 BUSMSYN 1+2
2 PROG DATA 1+2
2 PROG INI 1+2
2 PROG CLK 1+2
19 APABØA - APAB18A
TO QUADS 1+2
TO PS IN MEMORY RACK FOR QUADS 1+2
PART OF P6
2 DATA VALID 3+4
2 BUSMSYN 3+4
2 PROG DATA 3+4
2 PROG INI 3+4
2 PPOG CLK 3+4
19 APABØB - APAB18B
TO QUADS 3+4
TO PS IN MEMORY RACK FOR QUADS 3+4
FROM P8 IN MEMORY RACK FOR QUADS 3+4
FROM QUADS 3+4 OUTPUT DATA BUS
P2
26 M3-ØB-M3-25B
FROM P8 IN MEMORY RACK FOR QUADS 1+2
FROM QUADS 1+2 OUTPUT DATA BUS
P8
26 M3-ØA-M3-25A
FROM P5 IN MEMORY RACK FOR QUADS 1+2
FROM QUADS 1+2
PART OF P5
2 GO/NOGO QUADS 1+2
2 6G17 QUADS 1+2
FROM P5 IN MEMORY RACK FOR QUADS 3+4
FROM QUADS 3+4
PART OF P6
2 GO/NOGO QUADS 3+4
2 6G17 QUADS 3+4
PART OF P33
C14.29''''-E
PROC DISC INPUT
SYSTEM CONTROLLER (NOTE 1)
APAB 18
FROM FILTER I/O PANEL ON SEPARATE (4) RG-58 COAX CABLES
FROM CORA
J6
J5
FROM CORBIN
J8
J7
RDY A
RDY B
QUADRANT FAN OUT/ FAN IN DWG. NO. D13860L36 LOCATION J17
FPS-TO-MODCOMP FORMATTER DWG. NO. D13860L35 LOCATION J20
G1-A
G1-B
DA
DB
J2
J1
J4
J3
J10
J9
J12
J11
TO CORA
TO CORBIN
TO FILTER I/O PANEL ON SEPARATE (4) RG-58 COAX CABLES
NOTE 1: SHOWN FOR CLARITY
REV. DATE DRAWN BY APPRV'D BY DESCRIPTION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
PROJECT MAC SYSTEM
TITLE INTEGRATOR SYSTEM INTERCONNECTION DIA. MAC INTERFACE CHASSIS
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DESIGNED BY
APPROVED BY
SHEET NUMBER 1 of 3
DRAWING NUMBER D13860B2
REV.
SCALE


FROM DMS PS8 QUAD 1 (3)
P1
PART OF P2
FROM DMS PS9 QUAD 1 (3)
19 T.P.
LINE 1+ LINE 1- THRU LINE 19 + LINE 19- QUAD 1 (3) (DATA INPUT FROM DMS.)
8 T.P.
LINE 20+ LINE 20 - THRU LINE 27 + LINE 27 - QUAD 1 (3) (DATA INPUT FROM DMS.)
1 T.P.
MULT DATA RDY QUAD 1 (3)
3-STATE CTL TO STORAGE MEMORIES 1 (3)
7G6-Ø-7G6-27-1 (3)
ADDRESS+CONTROL SIGNALS TO DRIVERS QUAD 1 (3)
DATA TO INTEGRATING MEMORIES QUAD 1 (3)
DATA 1-DATA TM-1(3)
3M1-Ø-3M1-25
DATA FROM STORAGE MEMORIES QUAD 1 (3)
3M1-Ø-3M1-25
DATA FROM TM
8G3
6F13
G5 FROM P90 (P92)
PROG INI-1 (3)
BUSMSYN-1 (3)
DATA VALID-1 (3)
PROG CLK-1 (3)
PROG DATA-1 (3)
APAB12 APAB18A(B)
APAB-Ø-APAB-11 A (B)
7G5
7G4
3M1-Ø-3M1-25-1 (3)
3M1-Ø-3M1-25-1 (3)
6G17-1 (3)
TEST MEMORY CONTROL QUAD 1 (3)
DWG. NO. D13860L7
LOCATION J4 MOTHER BOARD 3
APCE
DATA VALID'
PROG INI'
DUMP TO STORAGE
MEMORY CONTROL QUAD 1 (3)
DWG. NO. D13860L6
LOCATION J8 MOTHER BOARD 3
6G1-Ø-6G1-11
6G6-Ø-6G6-11
C14.29'''
6G2 A+B
6G10 A+B
6F10
6G7 A+B
6G4 A+B
6G9
6G5 A+B
6G3 A+B
C14.29''
INPUT DATA MULTIPLEXER QUAD 1 (3)
DWG. NO. D13860L4
LOCATION J12 MOTHER BOARD 3
OUTPUT MULTIPLEXER QUAD 1(3)
DWG. NO. D13860L8
LOCATION J20 MOTHER BOARD 3
PART OF P5
FROM P5 MAC INTERFACE CHASSIS FOR QUADS 1+2
PB-1-PB-5
F1-Ø-F1-4
M3-Ø-M3-25
GO/NO GO-1 (3)
6G17-1(3)
GO/NO GO-2(4)
6G17-2(4)
PART OF P5
TO P5 MAC INTERFACE CHASSIS FOR QUADS 1+2
TO P6 MAC INTERFACE CHASSIS FOR QUADS 3+4
FROM P6 MAC INTERFACE CHASSIS FOR QUADS 3+4
7 APAB12-APAB18A(B)
APAB-Ø-APAB-11 A (B)
PROG DATA-2 (4)
PROG CLK-2 (4)
DATA VALID-2 (4)
BUSMSYN-2 (4)
PROG INI-2 (4)
F1-5
F1-5
POWER CONTROLLER MEM. 1+2 SYSTEM
DWG. NO. C13860L37
LOCATION J2 MOTHER BOARD 3
TO FRONT PANEL
6F13
7G4
F1-Ø-F1-4
C14.29'''' FROM P7 MAC INTERFACE ON RG-188 COAXES-5.2V FROM-5.2V SUPPLY
P6
C14.29 1''''(3)
C14.29 1''''(3)
-5.2V
P7
C14.29''''
FROM P7 MAC INTERFACE
-5.2V
8G3
G5 FROM P91 (P93)
C14.29 2''''(4)
C14.29 2''''(4)
7G5
M3-Ø-M3-25A (B) 3-ST-BUS
(OUTPUT DATA TO ARRAY PROC)
P8
TO P8 MAC INTERFACE CHASSIS FOR QUADS 1+2
TO P2 MAC INTERFACE CHASSIS FOR QUADS 3+4
6G17-2(4)
TEST MEMORY CONTROL QUAD 2 (4)
DWG NO D13860L7
LOCATION J5 MOTHER BOARD 3
APCE
DATA VALID'
PROG INI'
DUMP TO STORAGE
MEMORY CONTROL QUAD 2(4)
DWG. NO. D13860L6
LOCATION J9 MOTHERBOARD 3
6G1-Ø-6G1-11
6G6-Ø-6G6-11
C14.29'''
6G2 A+B
6G10 A+B
6F10
6G7 A+B
6G4 A+B
6G9
6G5 A+B
6G3 A+B
INPUT DATA MULTIPLEXER QUAD 2(4)
DWG. NO. D13860L4
LOCATION J13 MOTHER BOARD 3
C14.29'''
OUTPUT MULTIPLEXER QUAD 2(4)
DWG. NO. D13860L8
LOCATION J21 MOTHER BOARD 3
PB-1-PB-5
F1-Ø-F1-4
7G6-Ø-7G6-27-2 (4)
3-STATE CTL TO STORAGE MEMORIES 2 (4)
ADDRESS+CONTROL SIGNALS TO DRIVERS QUAD 2 (4)
DATA 1-DATA TM-2 (4)
DATA TO INTEGRATING MEMORIES QUAD 2 (4)
DATA FROM STORAGE MEMORIES QUAD 2 (4)
3M1-Ø-3M1-25
DATA FROM TM
3M1-Ø-3M1-25
FROM DMS PS58 QUAD 2(4)
P3
19 TP
LINE 1+ LINE 1 - THRU LINE 19 + LINE 19-QUAD 2 (4) (DATA INPUT FROM DMS.)
PART OF P4
FROM DMS PS9 QUAD 2(4)
1TP
MULT DATA RDY QUAD 2(4)
8TP
LINE 20+ LINE 20-THRU LINE 27+LINE 27-QUAD 2 (4) (DATA INPUT FROM DMS.)
NOTES 1.(3),(4),+(B) DENOTE COMPATABILITY BETWEEN QUADS 1+3 AND QUADS 2+4.
2.(P92) SHOWS WIRING FOR QUAD 3.
(P93) SHOWS WIRING FOR QUAD 4.
REV
DATE
DRAWN BY
APPRV'D BY
DESCRIPTION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
PROJECT
MAC SYSTEM
TITLE
INTEGRATOR SYSTEM INTERCONNECTION DIA. CONTROL MOTHER BOARD
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DATE 5-21-79
DESIGNED BY
APPROVED BY
SHEET NUMBER 2 OF 3
DRAWING NUMBER D13860B2
REV.
SCALE



REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON

PROJECT: MAC SYSTEM

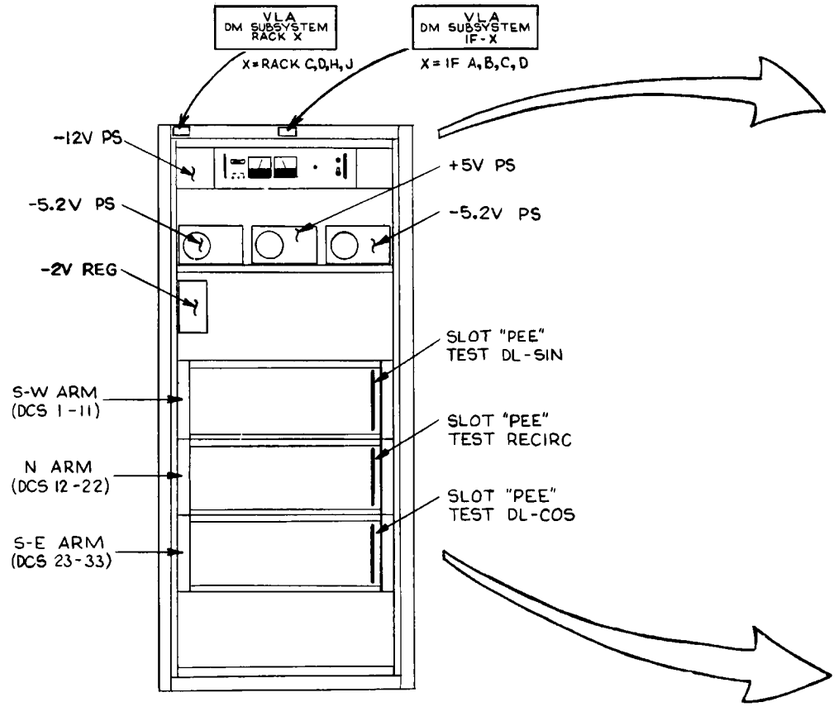
TITLE: INTEGRATOR SYSTEM INTERCONNECTION DIA. MEMORY MOTHER BOARDS

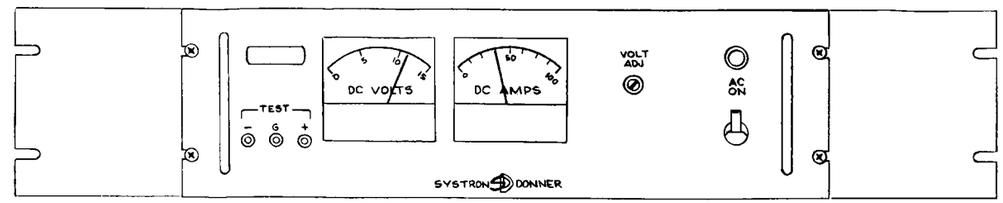
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

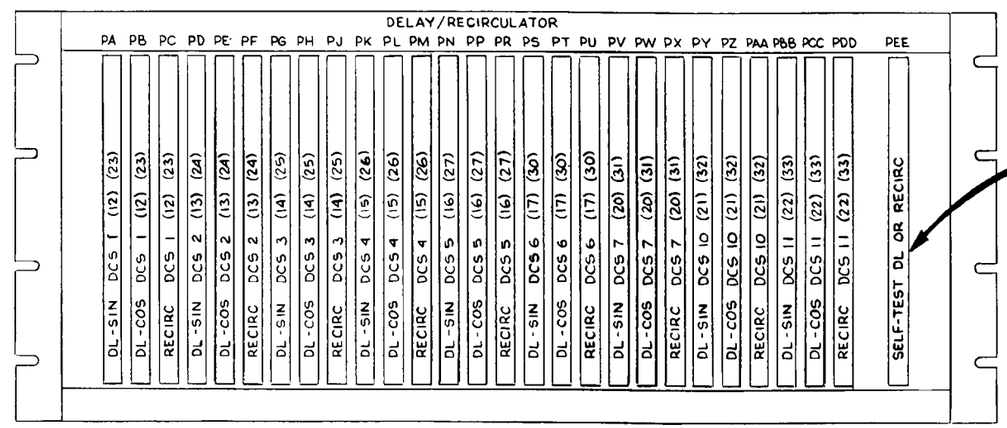
DRAWN BY — DATE
DESIGNED BY — DATE
APPROVED BY — DATE

SHEET NUMBER 3 of 3 DRAWING NUMBER D13860B2 REV. SCALE

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

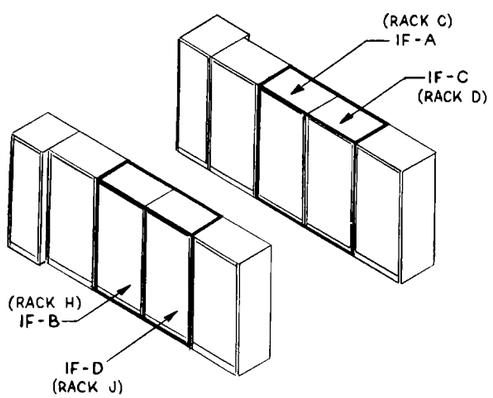


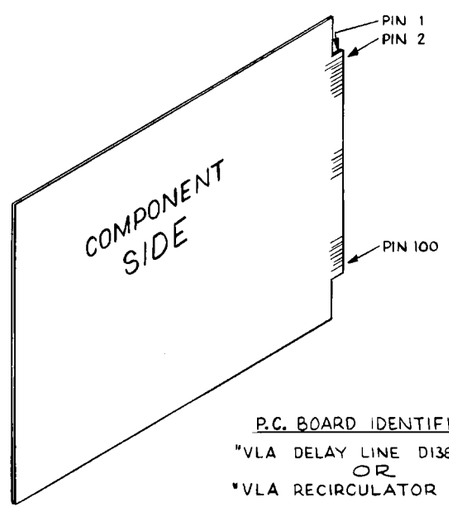




SELF-TEST BOARD	LOCATION
DELAY LINE - SIN	DCS 1-11 BIN
RECIRCULATOR	DCS 12-22 BIN
DELAY LINE - COS	DCS 23-33 BIN

SCREEN ROOM LAYOUT





P.C. BOARD IDENTIFICATION

"VLA DELAY LINE D13800L1"

OR

"VLA RECIRCULATOR D13800L2"

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

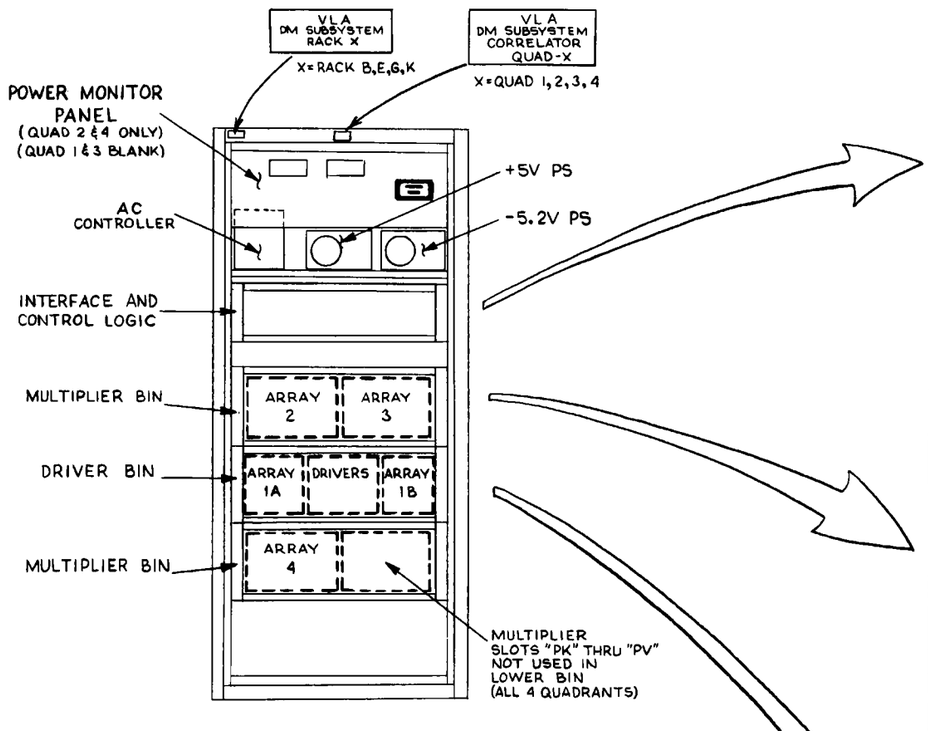
PROJECT: VLA — CORRELATOR SYSTEM

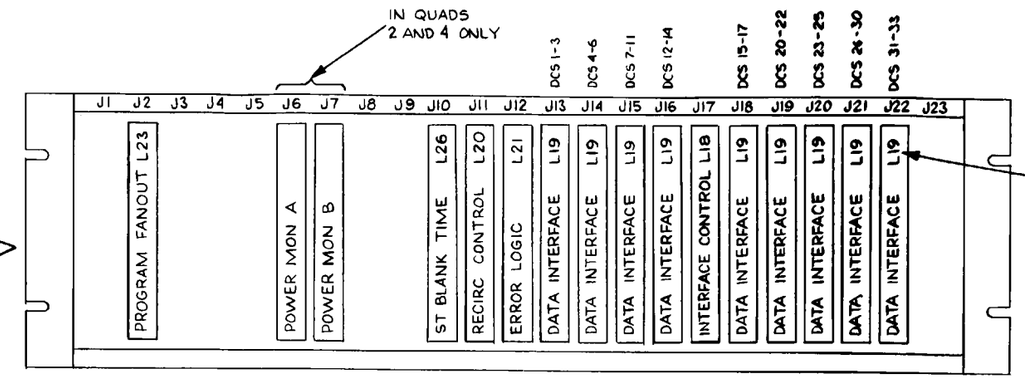
TITLE: RACK LAYOUT

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY		DATE APR 80
DESIGNED BY		DATE
APPROVED BY		DATE 4-21-80

SHEET NUMBER 1 OF 3 DRAWING NUMBER D13800B15 REV. SCALE

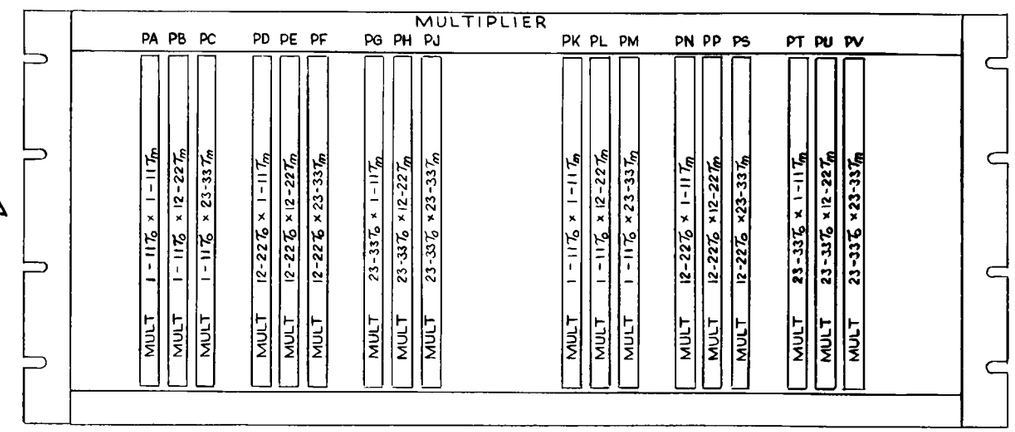




INTERFACE & CONTROL CHASSIS

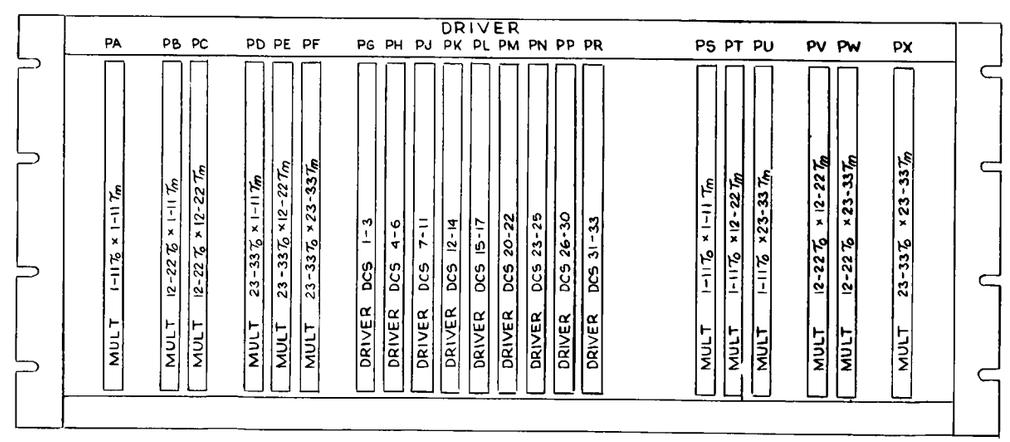
LOGIC BOARD IDENTIFICATION: D13800L00

WIRE-WRAPPED LOGIC BOARDS



MULTIPLIER BINS (2 PER RACK)

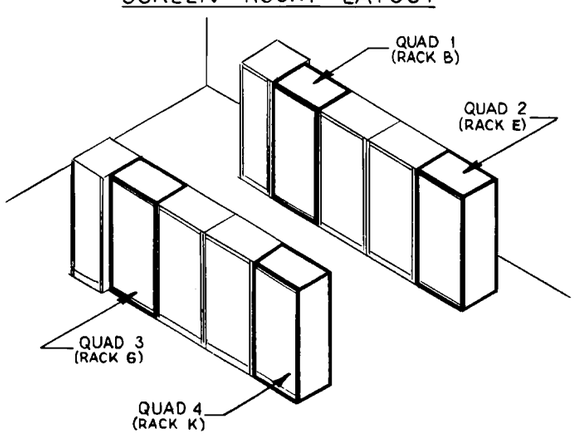
P.C. BOARD IDENTIFICATION: "VLA MULTIPLIER D13800L4"

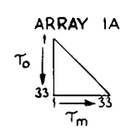


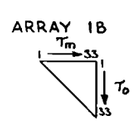
DRIVER BIN

P.C. BOARD IDENTIFICATION: "VLA MULTIPLIER D13800L4" OR "VLA DRIVER CARD D13800L3"

SCREEN ROOM LAYOUT







REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
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2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY | USED ON

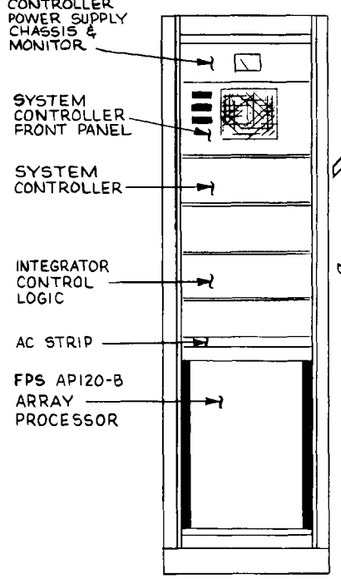
PROJECT: VLA

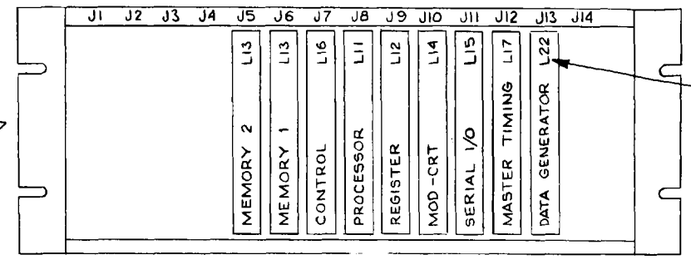
TITLE: CORRELATOR SYSTEM — RACK LAYOUT

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE APR 1980
DESIGNED BY | DATE
APPROVED BY | DATE 4-21-80

SHEET NUMBER 2 OF 3 | DRAWING NUMBER D13800B15 | REV. | SCALE

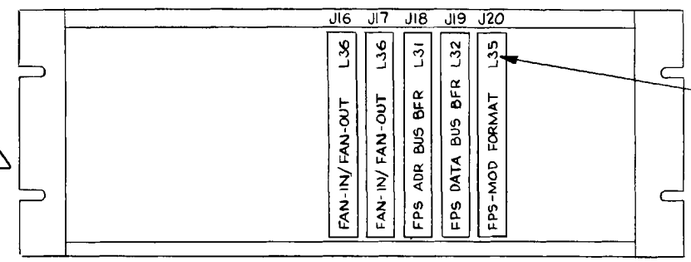




SYSTEM CONTROLLER BIN

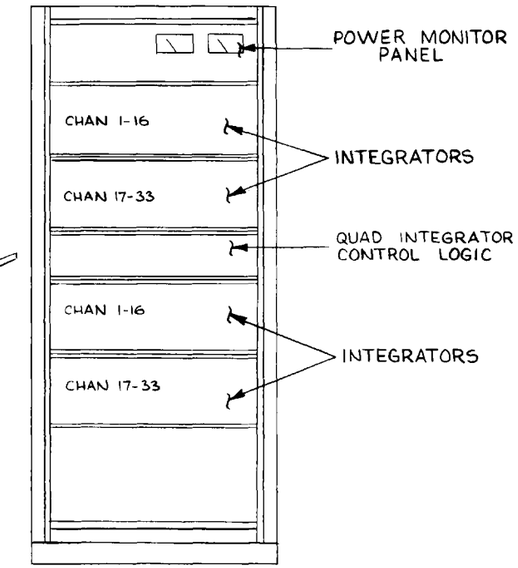
LOGIC BOARD IDENTIFICATION: "D13800L00"

(WIRE WRAP CARDS)



MASTER INTEGRATOR CONTROL BIN

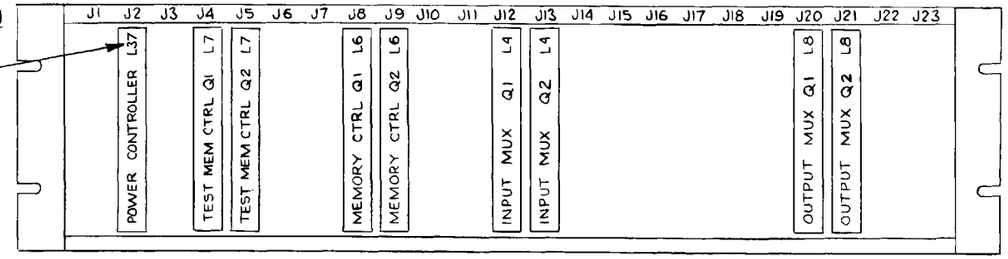
LOGIC BOARD IDENTIFICATION: "D13860L00"

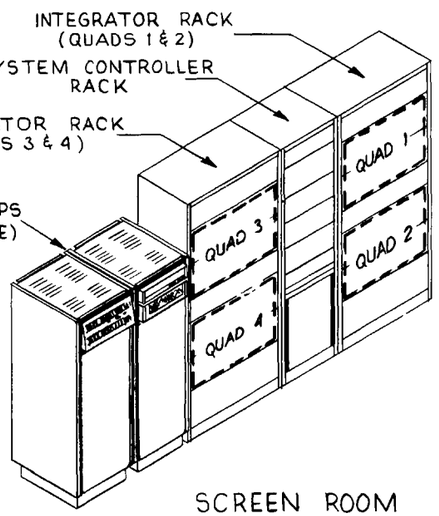


QUAD INTEGRATOR CONTROL BIN

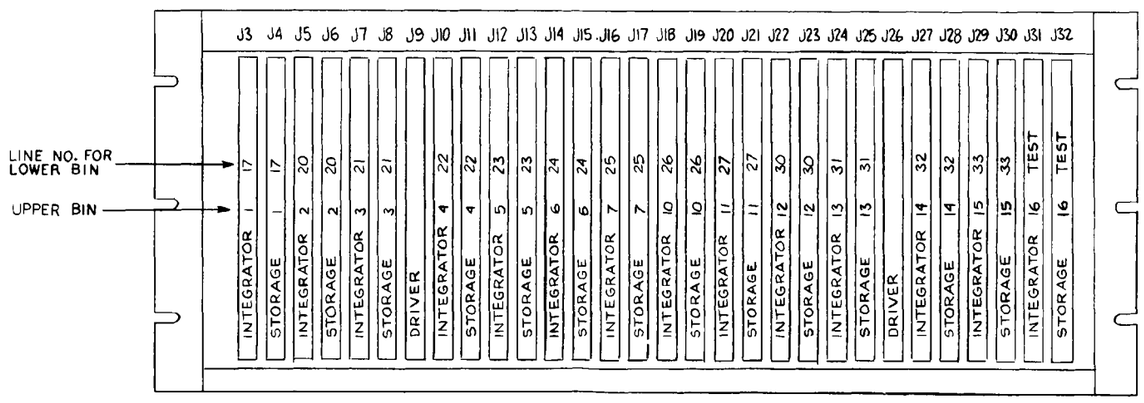
LOGIC BOARD IDENTIFICATION: "D13860L00"

(WIRE WRAP CARDS)





SCREEN ROOM LAYOUT



INTEGRATOR BIN

P.C. BOARD IDENTIFICATION:

"INTEGRATING MEMORY D13860L2"
"STORAGE MEMORY D13860L3"
"INTEGRATOR DRIVER D13860L5"

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

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1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON

PROJECT: VLA — CORRELATOR SYSTEM

TITLE: RACK LAYOUT

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY — DATE APR 80
DESIGNED BY — DATE
APPROVED BY — DATE 4-22-80

SHEET NUMBER 3 OF 3 DRAWING NUMBER D13800B15 REV. SCALE