VLA Technical Report No. 46

MODULE L17D SYNTHESIZER PHASE-LOCK
And
MODULE L21A SYNTHESIZER PHASE-LOCK EMERGENCY POWER

W.E. Dumke
November 1980

TABLE OF CONTENTS

L17 SYNTHESIZER PHASE-LOCK

1.0	GENERAL DESCRIPTION	1
2.0	THEORY OF OPERATION	2
3.0	MODULE DESCRIPTION	8
	3.1 Possible Improvements	9
4.0	CIRCUIT DETAILS	12
	4.1 Voltage Regulator	12
	4.2 5-400 MHz Amplifier	12
	4.3 50-350 MHz Multiplier	12
	4.4 Phase-Locked Loop	13
	4.5 Wire Harness	18
5.0	FRONT PANEL INDICATORS AND CONTROLS	20
6.0	PRELIMINARY MODULE ADJUSTMENTS	23
7.0	MEASUREMENTS	24
8.0	DRAWING LIST	25
9.0	DATA SHEETS	26

L21 SYNTHESIZER PHASE-LOCK EMERGENCY POWER

1.0	DESCRIPTION	27
2.0	CIRCUIT DETAILS	27
3.0	DRAWING LIST	27
4.0	BILL OF MATERIALS	27
5.0	DATA SHEETS	28

MODULE L17D SYNTHESIZER PHASE-LOCK

1.0 GENERAL DESCRIPTION

Four frequency synthesized signals are distributed to the T3 "IF to Baseband Converter" modules to provide a fine tuning capability across the four IF passbands. The tuning ranges of the signals are 125 ± 25 MHz, 225 ± 25 MHz, 225 ± 25MHz, and 125 ± 25 MHz for IF channels A, B, C, and D respectively. The signals are obtained from four Fluke Model 6160B Frequency Synthesizers with those for channels B and C requiring frequency doubling. The frequencies are thus tuneable in 1 or 2 Hz steps.

Operation in the polarization mode requires coherence between channels A and C and between channels B and D. To achieve this the synthesizers for channels A and C are phase-locked so that the sum of the output frequencies is 350 MHz phase referenced to the master LO system.

The synthesizers require an external 5 MHz reference frequency. The synthesizer for channel C is supplied with 5 MHz from the master LO system. The synthesizer for channel A is supplied with 5 MHz from a voltage controlled crystal oscillator (VCXO). The frequencies from the synthesizers are summed in a mixer and then phase compared with a 350 HMz reference derived from the master LO system. The output of the phase detector is used to close a phase-locked loop that controls the VCXO. An identical system is used with channels B and D.

The L17D module contains the following circuitry to control each synthesizer pair: a frequency doubler, mixer, 50-350 MHz frequency multiplier, 350 MHz phase detector, and 5 MHz VCXO. It also contains switching so that all synthesizers can be directly referenced to the master LO for observations requiring independent tuning of the four channels.

2.0 THEORY OF OPERATION

A modem IF spectrum received by the Central Electronics Room T1 and T2 is shown in Figure 2.1. The A_{IF} and C_{IF} noise passbands are orthogonal right and left circular polarizations of the same front end passband. If the relative amplitudes and phase of each passband are known, then a quantitative measurement can be made on the polarization characteristics of the source.

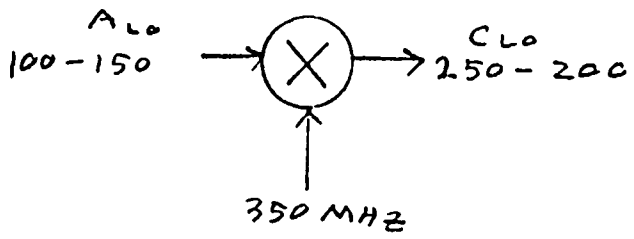
Because both right and left circular polarizations are required to be measured simultaneously, separate receiver systems for the right and left circular antenna feed outputs must be used. Since only one modem 1-2 GHz IF transmission system passband at one time is transmitted from each antenna the two front end IF passbands must be translated to two seperate modem IF channels. This is done with coherent (with the antenna local oscillator chain) local oscillator signals in the front end "A" rack.

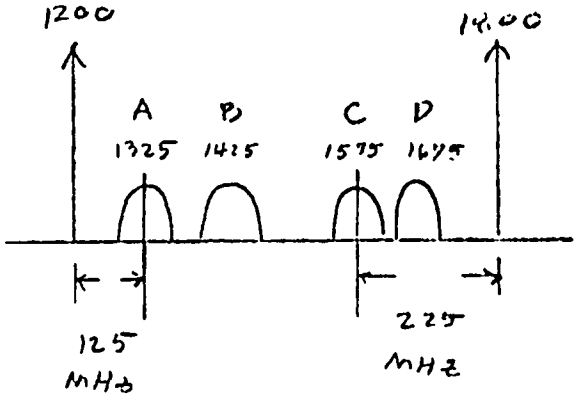
The A_{IF}, B_{IF}, C_{IF}, and D_{IF} signals are transmitted through the waveguide and modem transmission system as shown by Figure 2.1.

Note that the A_{IF} and B_{IF} passbands are closer in frequency to the 1200 MHz LO reference carrier and the C_{IF} and D_{IF} passbands are closer to the 1800 MHz LO reference carrier. All 4 "IF" passbands must be converted to a 200 KHz to 50 MHz baseband frequency range in order to be sampled and converted to digital information in the D1 sampler module.

The A_{IF} and C_{IF} signals are right and left circularly polarized signals of the same front end frequency band.

The B_{IF} and D_{IF} signals are right and left circularly polarized signals of a different front end frequency band. Note that the phase integrity between A_{IF} and C_{IF} signals as well as B_{IF} and D_{IF} signals must be maintained. Low pass filters do the final analog filtering in the T4 Baseband Filter module. Therefore an image reject mixer system must be used in the T3 "IF to Baseband





$$A_{LO} = 350 - C_{LO}$$

$$A_{OUT} = 1200 + A_{LO}$$

$$C_{OUT} = 1800 - C_{LO}$$

A_{OUT} TRACKS C_{OUT}

Figure 2.1

FINE TUNING LO PHASE NOISE CANCELLATION

Converter" module to prevent aliasing. The T3 module does this in two steps. First, the A_{IF} and B_{IF} passbands are mixed with the 1200 MHz reference to provide a lower "IF" easier to convert to the baseband 200 KHz to 50 MHz frequency range. These intermediate IF's are then converted to baseband in an image rejection mixer using a frequency synthesizer local oscillator. A similar situation exists for the C_{IF} and D_{IF} signals referenced to the 1800 MHz LO signal.

The low and high frequency band edges of each IF singal are given in Figure 2.1. Note that the sum of the A_{LO} and C_{LO} fine tuning signals result in 350 MHz. If the C_{LO} signal was to be derived from the A_{LO} frequency synthesizer by use of a simple mixer, note that positive phase jitter of the A_{LO} synthesizer sould result in negative phase jitter of the C_{LO} signal. Since the A_{LO} signal is effectively added to that of the 1200 MHz carrier, and the C_{LO} signal is effectively subtracted from the 1800 MHz carrier, the A_{LO} phase jitter would be cancelled. This is shown in Figure 2.1.

Unfortunately spurious signals would be generated in a mixer scheme which would prohibit its use. This is especially true since the C_{LO} frequency range contains second harmonics of portions of the A_{LO} frequency range.

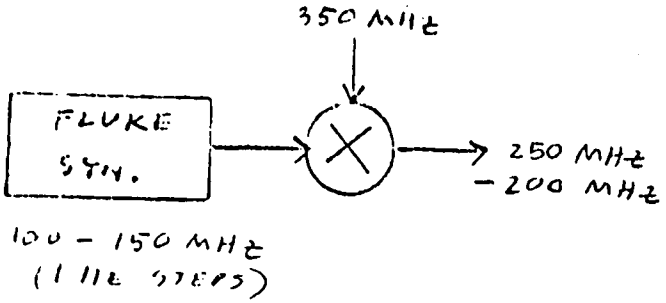
Another simple method of deriving A_{LO} and C_{LO} would be to use seperate frequency synthesizers. The spurious response level would be dependent on the synthesizers, assuming proper filtering was utilized in the frequency doubler on the C_{LO} side. Phase coherence would be maintained with the system because both synthesizers would be operated from the system 5 MHz assuming the frequencies of each were properly set.

Unfortunately this method has a major flaw in that the absolute phase difference between A_{LO} and C_{LO} (or the resultant A and C baseband signals) would change each time power failed or frequency was changed. This results from the unpredictability of

the initial states of the synthesizers' programable dividers. Also relative phase jitter of the A_{LO} and C_{LO} synthesizer outputs would not cancel, but instead triple. For these two reasons this scheme of fine tuning local oscillator signal generation was also rejected. This is shown in Figure 2.2.

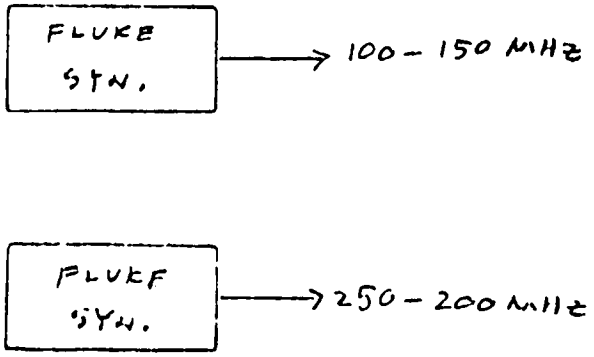
The system for generation of the A_{LO} and C_{LO} used with the L17D Synthesizer Phase-Lock module is shown in Figure 2.3. The L17 simulates the action of a mixer but without the generation of spurious mixer responses. Even though seperate synthesizers are required, the phase relationship between the A_{IF} and C_{IF} channels is always a known constant.

Because the Fluke synthesizers cannot tune above 150 MHz a doubler is required to generate the C_{LO} band from 250-200 MHz. The two Fluke synthesizers are set in frequency by computer control such that $A_{LO} + C_{LO} = 350$ MHz. Some of each synthesizer's output is sampled and fed to a mixer with adequate isolation (either power dividers, attenuators, or amplifiers) such that mixer spurious products do not appear at either output. This mixer takes the 350 MHz sum signal and phase compares it to a 350 MHz signal derived from the system through a multiplier chain. The phase detector and loop filter then phase-locks the $C_{LO} \div 2$ synthesizer to a constant phase relationship with frequency changes and be restored to the initial relationship in the event of system disruption. Because the system simulates the action of a mixer, relative phase noise between the two synthesizers will be cancelled to some extent within the loop bandwidth.



Advantages - Relative phase noise cancels.
- Only one synthesizer required.

Disadvantage - Spurious signals would be prohibitive.

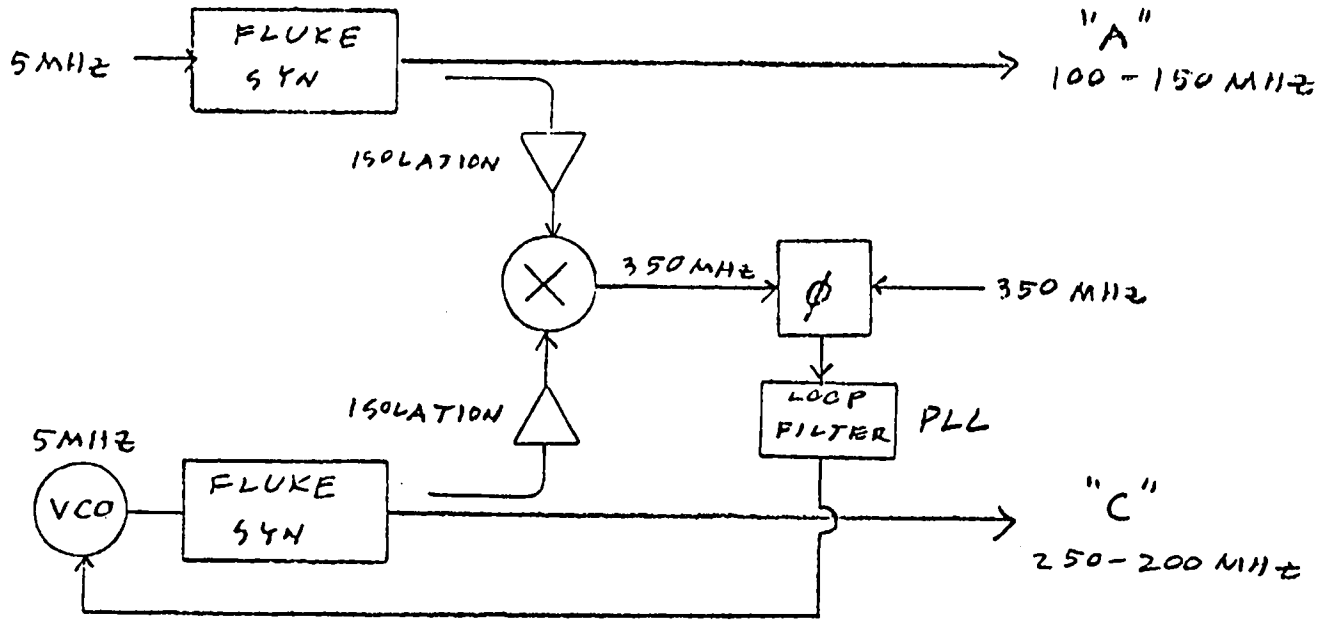


Advantage - No spurs.

Disadvantages - Relative phase noise does not cancel.
- Must recalibrate absolute phase difference with interrupted power and change in frequency.
- Two fine tuning synthesizers are required.

11/16/77 - WED

Figure 2.2
FINE TUNING LO GENERATION SCHEMES



Advantages - Relative phase noise cancels (3.5 Hz loop BW).
- No spurs (dependent on isolation).

11/16/77 - WED

Figure 2.3
L17 SCHEME

3.0 MODULE DESCRIPTION

The block diagram of the L17D Synthesizer Phase-Lock module is given in drawing D13220B2C. Typical power levels are also included. Because of the critical tolerances on LO input levels to the T3 IF to Baseband Converter module image reject mixers, these values may deviate somewhat from what is shown in the diagram.

These levels are currently set at the "D" rack input connectors using the Fluke synthesizer output level control as an adjustment. The phase detector output voltages will be affected somewhat by this adjustment. The natural frequency and damping factor should be checked after drastic changes in these levels. Attenuation may be added to the L18 "Variable Frequency Driver" to increase the L17 level if necessary.

Notice that no adjustments, with the exception of the A2 voltage regulator assembly, are necessary internal to the module. The EFC control of the HP voltage controlled crystal oscillator is a front panel adjustment, as opposed to earlier L1 designs which required the front panel to be removed for access to the EFC control. This should be periodically adjusted to compensate for oscillator aging.

No adjustments are necessary on the phase-locked loop board either. This is due to the use of a precision low input offset voltage and input bias/offset current bipolar operational amplifier, the AD517LH. This op amp will remain stable in these parameters unlike JFET op amps which will age considerably with time.

Because of the crowding in the L17 module it was necessary to place the battery backup supply for the crystal oscillator oven in a seperate L21 "Synthesizer Phase-Lock Emergency Power" module. Therefore when the L17 is to be removed or transferred to another rack or bin position, rapidity of transfer is required to prevent the oscillator from cooling down. The drift rate can be monitored with the "Lock Warn" LED with warm-up.

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
B	1/28/78			RE-DRAWN
C	10/1/80			MADE CORRECTIONS

NOTES

1. ONE L17 IS REQUIRED FOR EACH OF 2 SYNTHESIZER COMBINATIONS. THE FIRST LETTER OF A FREQUENCY DESIGNATOR CORRESPONDS TO THE A AND C SYNTHESIZER COMBINATION. THE SECOND LETTER CORRESPONDS TO THE B AND D SYNTHESIZER COMBINATION. THE L17 MODULES FOR EACH COMBINATION ARE INTERCHANGEABLE.
2. NOTATIONS GIVEN IN BLOCKS ARE FRONT PANEL LABELS.
3. RELAY IS SHOWN IN ACTIVATED POSITION.
4. LOCKED/AUTO/INDEPENDENT SWITCH IS SHOWN IN AUTO POSITION.

FREQUENCY CHART

A+C = 350 MHZ
B+D = 350 MHZ

A, 100 - 150 MHZ
B, 200 - 250 MHZ
C, 250 - 200 MHZ
D, 150 - 100 MHZ

5MHZ FROM MASTER LO
+0dBm
SYNTHESIZER C÷2/B÷2
C÷2/B÷2, 100-125 MHZ +10dBm
J9
A
D
-10dB
DCG-10-4 ANZAC
C
IN X2 OUT
DI-4 ANZAC DOUBLER
IN A4 OUT
GPD 402/402/403 AVANTEK
+15V
IN 2 WAY OUT
1
2
3
J15 +10dBm C/B OUTPUT TO L18
4B120-225/60-0 K+L
200-250 MHZ
PDM-20-165 MERRIMAC
10dB MECA
-10dBm
C÷2/B÷2
WATKINS/JOHNSON MIA
0dBm
Ø DET
+10 dBm
R
L
K+L 6B120-350/25-0
350 MHZ
-12dBm
I
MIE WATKINS/JOHNSON
+15 VDC
A5
GPD 402/402/403 AVANTEK
0dBm
350 MIXER
-10dB MECA
IN 3 WAY
PDM-30-250 MERRIMAC
PDM-30-250 MERRIMAC
+15 VDC
91Ω 5% 1W
IN4733
+5VDC
50 MHZ FROM MASTER LO +10dBm
J7
50 MHZ
4B51-50/20-0 K+L
A3
50 TO 350 MHZ MULTIPLIER
MC 1662
350 MHZ
6B120-350/25-0 K+L
+15 VDC
A6
GPD 402/402/403 AVANTEK
IN 3 WAY
PDM-30-250 MERRIMAC
-10dB MECA
350 MULT
-10dBm
EFC TO M10, P1-23
OVDC. TYP.
EFC
P1-15 GND
-15 VDC
+5VDC
+15VDC
EFC GND TO M10 P1-13
BUFFER AMPLIFIER
SECOND ORDER LOOP FILTER
fn ≈ 3.5 Hz
δ ≈ 0.8
PHASELOCK LOOP PC BOARD A1
IN PHASE
QUAD PHASE
LOCK INDICATOR
DELAY LINE 90° @ 350 MHZ
-10dB MECA
LOCKED
AUTO
INDEPENDENT
S1A
NC
RED
AUTO WARN
+5V
S1B
P1-1 LOCKED/IND. COMMAND FROM M10 (HIGH = LOCKED)
YEL
IND
AUTO WARN TO M10, P1-14 (HIGH = MANUAL)
LOCK WARN TO M10, P1-4 (LOW = LOCKED)
LOCK WARN
RED
+5VDC
LOOP OPEN
N.O.
0dBm R Ø DET L +10dBm
MIA WATKINS/JOHNSON
I
FREQ ADJ
919C70100 TRANSCO
IN4005
+28V
N.O.
N.C.
5MHZ OUTPUT
IN
J1
A/D 5MHZ 0dBm ≥
SYNTHESIZER A/D
A/D 100-150 MHZ +10dBm
J8
-10dB MECA
-10dBm
A/D
A
C
IN 2 WAY
D
-10dB
DCG-10-4 ANZAC
PDM-20-165 MERRIMAC
100-150 MHZ
4B120-125/60-0 K+L
J16
A/D OUTPUT +10dBm
TO L18
+28VDC P1-29 > FL > +28 VDC
+15VDC P1-16 > FL > +15 VDC
+5VDC P1-10 > FL > +5 VDC
-15VDC P1-17 > FL > -15VDC
GND P1-34 > GND
+28 VDC
E1
E5
E4
VOLTAGE REGULATOR P.C. BOARD A2
REG OUTPUT E3
EFC
+20.7 VDC
200Ω
+12 VDC
IN4742A
5MHZ VCXO
HEATER
RED
BATT
+BATT FROM L21, P1-20
-BATT FROM L21, P1-35
J2
5MHZ FROM MASTER LO
≥ +0dBm

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:

NEXT ASSY	USED ON

VLA PROJECT

TITLE: L17 SYNTHESIZER PHASE LOCK (MODEL "D")
BLOCK DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 1/28/78
DESIGNED BY	DATE 7/11/78
APPROVED BY	DATE 7/11/78

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D13220B2 | REV C | SCALE ~

3.1 POSSIBLE IMPROVEMENTS

3.1.1 L17 Phase Detector Beatnote Feedthru

Normally: $A_{LO} + C_{LO}$ 350 MHz

Where 100 MHz $\leq$ A $\leq$ 150 MHz

250 MHz $\geq$ C $\geq$ 200 MHz

Actually: $A_{LO} + 2\ (C_{LO} \div 2) = 350$ MHz

Where 100 MHz $\leq A_{LO} \leq$ 150 MHz

125 MHz $\geq C_{LO} \div 2 \geq$ 100 MHz

Therefore: A beatnote can appear at the phase detector and can result in FM of the voltage controlled crystal oscillator when

$$A_{LO} \cong C_{LO} \div 2 \cong \frac{350 \text{ MHz}}{3} \cong 116.666667 \text{ MHz}$$

Example: Let A = 116.666666 MHz

A + 2 (C ÷ 2) = 350.000000 MHz

∴ C ÷ 2 = 116.666667 MHz

3A = 349.999998 MHz

3 (C ÷ 2) = 350.000001 MHz

The 3A and 3 (C ÷ 2) signals will mix with the normal 350 MHz to generate 1 Hz and 2 Hz signals frequency modulating the L17 5 MHz VCXO which controls the A synthesizer.

Cause 1. Non-linearity in the 350 MHz summing mixer can create a third harmonic of the A_{LO} from the synthesizer. Also the synthesizer output itself contains a considerable amount of harmonic power (although the non-harmonically related spurious output is extremely good). This cause of the beatnote requires two solutions. First, a low pass filter for the A_{LO} synthesizer output should be installed in the input line to eliminate A_{LO} harmonics from the synthesizer. Second, the 350 MHz mixer should be made linear with respect to

the A_{LO} input to eliminate harmonics generated in the A_{LO} side. This could be done by lowering the level to the mixer while possibly increasing the C_{LO} level. However, it would be important to note that modifications to the isolation between the A_{LO} and C_{LO} outputs and the 350 mixer do not result in increases in spurious responses. Additional isolation may be required, especially in the C_{LO} side.

Cause 2. C ÷ 2 and 3 (C ÷ 2) feedthru from the C_{LO} frequency doubler. This would require a bandpass filter for the C_{LO} frequency range at the C_{LO} doubler output. Its characteristics would have to be carefully chosen for temperature stability.

Other Effects: Note that this previously described problem does not occur at just one frequency setting combination but actually occurs over a wide range of frequencies in the vicinity of these settings. The actual range would be determined by system requirements, and bandwidth limitations due to the loop filter and crystal oscillator "Q". If perfect op amps and a first order loop filter (integrator) were used, the amplitude of the beatnote would decrease at the rate of 20 dB per decade of frequency difference. However, a first order phase-lock loop filter will not track in phase and so therefore is unusable.

A second order loop filter will have a maximum rejection dependent on the ratio of

the two timing resistances (this assumes the reactance of the loop filter capacitor is near zero at high beatnotes). Thus the ultimate rejection caused by a second order filter is severely limited.

System measurements and a system requirements study have not been completed at this time. However, it is doubtful that the previous solutions will completely cure these effects.

3.1.2 Output Filter Phase Shift Versus Frequency

Cause: The A_{LO} and C_{LO} output bandpass filters are not inside the loop. Therefore a changing relative phase shift between the A_{IF} and C_{IF} channels will result with changes in A_{LO} and C_{LO} frequency. Refer to D13220B2, the L17 Block Diagram.

A possible solution would be to move the filters to the input of the two-way power splitters that feed both the 350 MHz mixer as well as the output connectors. However, a danger might exist in out of band products from the mixer appearing at the output connectors through the output isolation of the splitter. If this method were to be employed, additonal isolation (also phase constant with frequency) might have to be added to the mixer inputs.

A second possible solution would be to use phase matched filters at both outputs of each two way splitter. However, the mixer imput impedance may not be a very good match and could also result in phase differences between the two filters. Also temperature

matching (by physical position) would have to be observed.

All previous measurements have been taken with respect to phase error at the L17 phase detector with variations of synthesizer frequencies. Thus the effect has not yet been measured with respect to actual L17 output signals.

4.0 CIRCUIT DETAILS

4.1 Voltage Regulator (Assembly A2)

Refer to Schematic B13230S5. Note that the regulator is the same one used in the L1 module. Regulator pot R4 should be adjusted to give 20.70 VDC under a 200 mA load (warm oscillator).

Note that the pass transistor will be hot to the touch when power is first applied to a cold oscillator. At this time the series pass transistor will still be operating within specified safe limits.

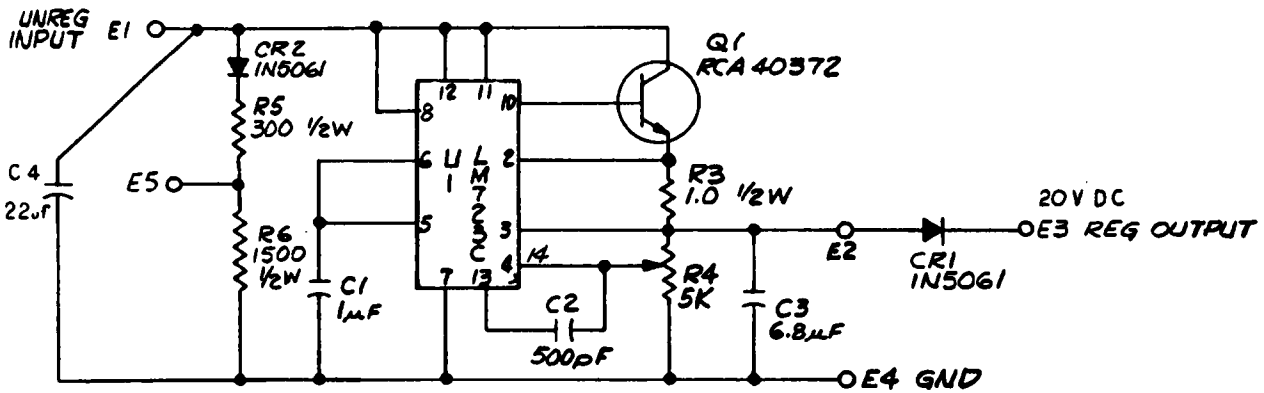
4.2 5-400 MHz Amplifier (Assemblies A4, A5, A6)

Refer to Schematic B13220S5. General purpose broadband amplifiers using cascaded GPD 402, 402, 403 stages are utilized in the module. 35 dB of gain is available with the amplifier operating in the linear mode. Phase stability at 350 MHz at +10 dBm output was measured at 0.1° phase/°C.

4.3 50-350 MHz Multiplier (Assembly A3)

Refer to Schematic B13220S7. A unique form of comb generator is constructed using an MC1662 MECL III chip. When a 50 MHz sine wave of sufficient amplitude (> +8 dBm) is applied to the first gate, the bias network R1, C2, and R2 provides DC feedback which adjusts the bias voltage to provide a 50% duty cycle at the output.

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	4/27/76			ADDED CR2
B	6/29/76			ADDED C4 PER CO - 143
C	11/3/80			ADDED (L17, A2) IN PROJECT BOX



LAST COMPONENT DESIG. USED						
C	E	Q	R	U	CR	
4	5	1	6	1	2	

COMPONENT DESIG NOT USED

5/76. HJ. A

A13230Z20	A13230E1
NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

VLA PROJECT: LOCAL OSCILLATOR LI (L17, A2)

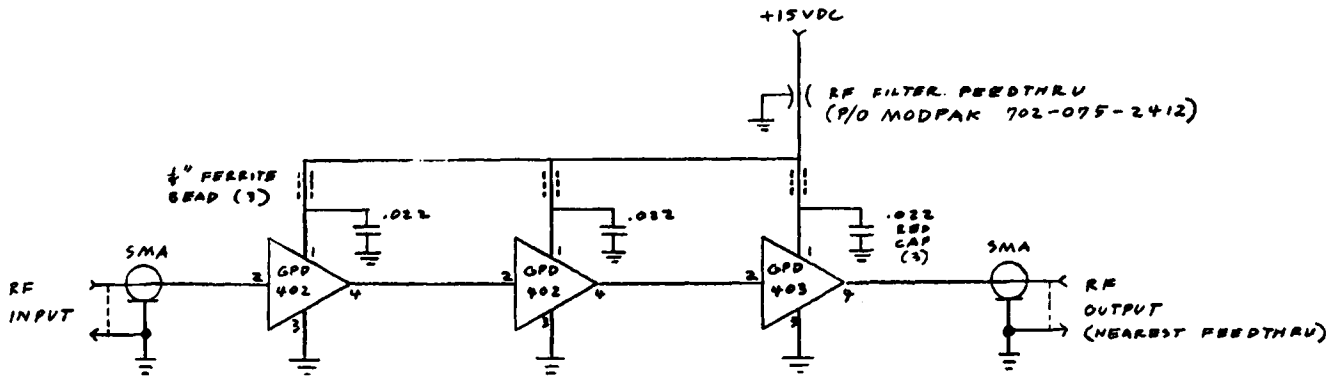
TITLE: VOLTAGE REGULATOR BATTERY CHARGER SCHEMATIC

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

DRAWN BY	DATE 8 MAY 75	
DESIGNED BY	DATE 5-20-75	
APPROVED BY	DATE 5-20-75	
SHEET NUMBER	DRAWING NUMBER B1323051	REV. C SCALE

BRUNING 40-22 24984

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	10/14/80			CORRECTIONS



NOTES:

1. ALL CAPACITANCES IN μFARADS UNLESS OTHERWISE INDICATED

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

PROJECT: SYNTHESIZER PHASE LOCK L17-D

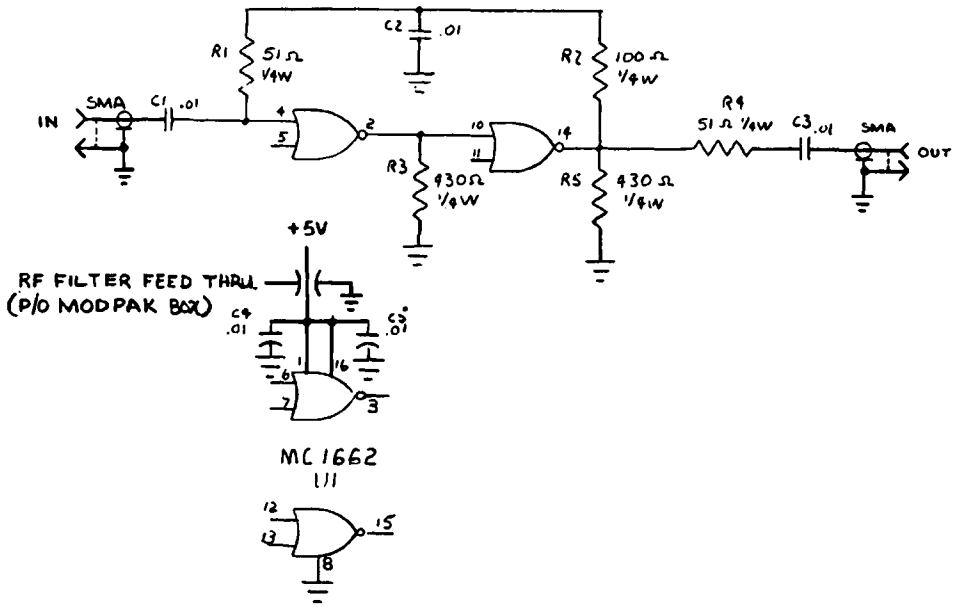
TITLE: 5-400 MHz AMPLIFIER SCHEMATIC A4, A5, A6

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY		DATE 3/23/77
DESIGNED BY		DATE 3/23/77
APPROVED BY		DATE 3/23/77

SHEET NUMBER 1 | DRAWING NUMBER B1322055 | REV. A | SCALE

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	10/14/80			CORRECTIONS



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ±	VLA PROJECT: SYNTHESIZER PHASELOCK L17-D	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801
MATERIAL:	TITLE: 50-350 MHZ MVLT. SCHEMATIC A3	DRAWN BY: 7/01/14
FINISH:		DESIGNED BY: 7/01/14
		APPROVED BY: 3/31/77
NEXT ASSY / USED ON	SHEET NUMBER 1 of 1	DRAWING NUMBER B1322057 REV. A SCALE ~

Thus a 50% duty cycle is obtained despite variations in input duty cycle and input threshold voltage. This 50% duty cycle is used to advantage in this 50-350 MHz multiplier. Suppression of even order harmonics permits less filtering to be required in the selection of the 350 MHz odd order harmonic. A typical output spectrum of the multiplier is shown in Figure 4.1. Even order suppression may vary from unit to unit. However, suppression of unwanted harmonics should remain greater than -65 dBc after filtering.

Phase stability of the multiplier at 350 MHz was measured at 0.1° phase/°C with less than 3×10^{-3} radians peak to peak phase noise in a 100 Hz bandwidth. The excellent phase stability of this device is due to two factors. First the 50% duty cycle results in suppression of even order distortion which can shift the zero crossings of the output waveform.

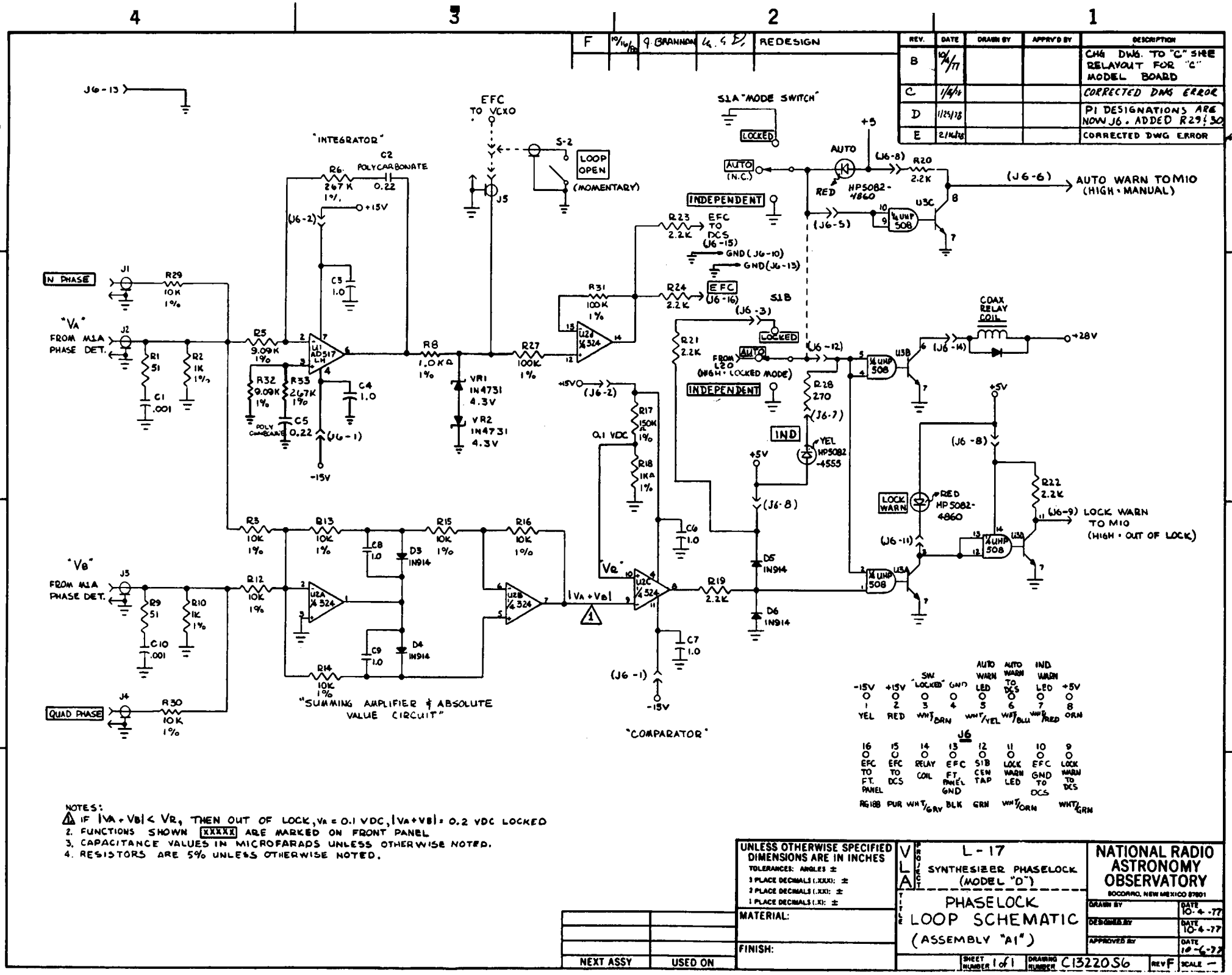
Also ECL gates are essentially differential amplifiers. The difference in voltage between two similiar transistor junctions at the input is used to switch the output. Thus changes in transistor base to emitter junction voltages are to some extent cancelled.

4.4 Phase-Locked Loop (Assembly A1)

Refer to Schematic B13220S6. Each phase detector is terminated in 51 Ω at 350 MHz and a high impedance at DC to provide an output voltage swing of approximately 0.35 volts peak. Thus the phase detector gain is about 0.35 volts/radian at 350 MHz. The voltage controlled crystal oscillator (VCXO) gain varies from unit to unit. A typical unit measured 5 radians/sec·volt at 5 MHz. Since the phase detectors operate at the 70th harmonic of the oscillator frequency, a factor of 70 must be included in the loop equations given below.

$$\omega n = \left(\frac{70KoKd}{\tau 1}\right)^{\frac{1}{2}}$$

$$\delta = \frac{\tau 2}{2}\left(\frac{70KoKd}{\tau 1}\right)^{\frac{1}{2}}$$


4
3
2
1
F 10/14/77 G. BRANNON REDESIGN
REV. DATE DRAWN BY APPR'D BY DESCRIPTION
B 10/4/77 CHG DWG. TO "C" SIZE RELAYOUT FOR "C" MODEL BOARD
C 1/4/78 CORRECTED DWG ERROR
D 1/25/78 PI DESIGNATIONS ARE NOW J6. ADDED R29,30
E 2/14/78 CORRECTED DWG ERROR
J6-13
EFC TO VCXO
J5
S-2
LOOP OPEN
(MOMENTARY)
"INTEGRATOR"
R6 267K 1%
C2 POLYCARBONATE 0.22
+15V
(J6-2)
S1A "MODE SWITCH"
LOCKED
AUTO
AUTO (N.C.)
+5
(J6-8)
R20 2.2K
(J6-6)
AUTO WARN TO MIO (HIGH = MANUAL)
RED HP5082-4860
INDEPENDENT
R23 2.2K
EFC TO DCS (J6-15)
GND (J6-10)
GND (J6-13)
(J6-5)
U3C
IN PHASE
J1
R29 10K 1%
"VA" FROM M1A PHASE DET.
J2
R1 51
C1 .001
R2 1K 1%
R5 9.09K 1%
U1 AD517 LH
C3 1.0
R8 1.0KΩ 1%
R27 100K 1%
R31 100K 1%
U2B ¼ 324
R24 2.2K
EFC (J6-16)
S1B
(J6-3)
LOCKED
AUTO
FROM L20 (HIGH = LOCKED MODE)
INDEPENDENT
R21 2.2K
(J6-12)
COAX RELAY COIL
+28V
U3B
(J6-14)
R32 9.09K 1%
R33 267K 1%
C4 1.0
C5 POLY CAPACITOR 0.22
(J6-1)
-15V
VR1 IN4731 4.3V
VR2 IN4731 4.3V
+15V
(J6-2)
R17 150K 1%
0.1 VDC
R18 1KΩ 1%
R28 270
(J6-7)
IND
YEL HP5082-4555
+5V
(J6-8)
(J6-8)
R22 2.2K
LOCK WARN
RED HP5082-4860
(J6-9) LOCK WARN TO MIO (HIGH = OUT OF LOCK)
(J6-11)
U3D
U3A
R3 10K 1%
R13 10K 1%
C8 1.0
D3 IN914
R15 10K 1%
R16 10K 1%
C6 1.0
"VB" FROM M1A PHASE DET.
J3
R9 51
C10 .001
R10 1K 1%
R12 10K 1%
U2A ¼ 324
C9 1.0
D4 IN914
R14 10K 1%
U2B ¼ 324
|VA+VB|
1
"VC"
U2C ¼ 324
R19 2.2K
D5 IN914
D6 IN914
C7 1.0
(J6-1)
-15V
"SUMMING AMPLIFIER & ABSOLUTE VALUE CIRCUIT"
"COMPARATOR"
QUAD PHASE
J4
R30 10K 1%
-15V +15V SW "LOCKED" GND AUTO WARN LED AUTO WARN TO DCS IND WARN LED +5V
1 2 3 4 5 6 7 8
YEL RED WHT/BRN WHT/YEL WHT/BLU WHT/RED ORN
J6
16 15 14 13 12 11 10 9
EFC TO FT. PANEL
EFC TO DCS
RELAY COIL
EFC FT. PANEL GND
S1B CEN TAP
LOCK WARN LED
EFC GND TO DCS
LOCK WARN TO DCS
RG188 PUR WHT/GRY BLK GRN WHT/ORN WHT/GRN
NOTES:
1. IF |VA+VB| < VR, THEN OUT OF LOCK, VA = 0.1 VDC, |VA+VB| = 0.2 VDC LOCKED
2. FUNCTIONS SHOWN XXXXX ARE MARKED ON FRONT PANEL
3. CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE NOTED.
4. RESISTORS ARE 5% UNLESS OTHERWISE NOTED.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY USED ON
VLA PROJECT L-17 SYNTHESIZER PHASELOCK (MODEL "D")
TITLE PHASELOCK LOOP SCHEMATIC (ASSEMBLY "A1")
NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801
DRAWN BY DATE 10-4-77
DESIGNED BY DATE 10-4-77
APPROVED BY DATE 10-6-77
SHEET NUMBER 1 of 1 DRAWING NUMBER C13220S6 REV F SCALE —

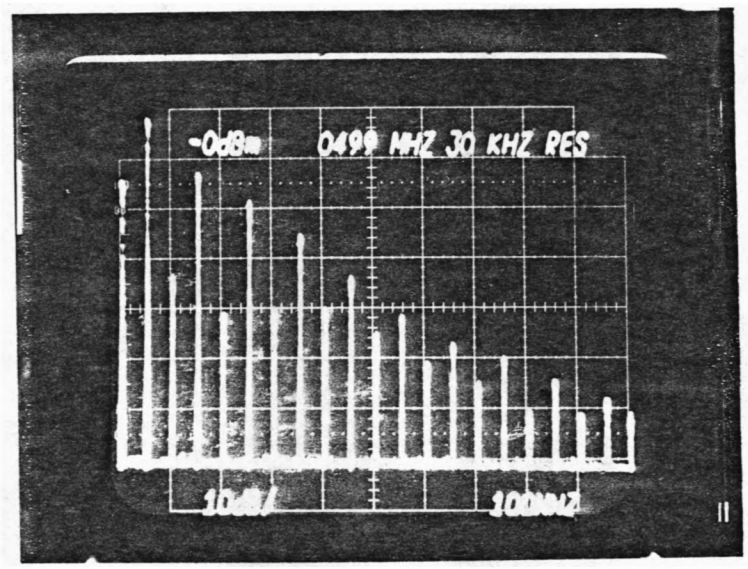


Figure 4.1

MEASURED OUTPUT OF 50 MHz DIGITAL (MC1662L)

COMB GENERATOR INTO RESISTIVE LOAD

where $\tau_1 = R_5 C_1$

$\tau_2 = R_6 C_1$

While these equations can give ball park figures for R_5, R_6, and C_1 after measurement of the individual oscillator gain, final values have to be selected experimentally because of oscillator modulation bandwidth limitations.

Diodes D1 and D2 limit the maximum out of lock frequency excursion of the VCXO. However, to ensure reliable pull-in with a cold oscillator a wide loop bandwidth is still required. The loop bandwidth expermintally chosen for reliable pull-in is 3.5 Hz with a damping factor of 0.8. The high "Q" voltage controlled crystal oscillator, however, introduces an additional pole in this region and makes loop operation unpredictable. Thus the loop component values have to be chosen experimentally. In this way pull-in is reliable under any conditions.

The phase-locked loop is designed to obtain lock as soon as the oscillator warms up within 5×10^{-9} of final value 20 minutes after turn on. See H37-10544A data sheet. Therefore, the maximum frequency offset at 350 MHz that may be encountered after 20 minutes warm up with the frequency control input at OVDC is:

f offset max.

$$\text{@ OVDC} = (5 \times 10^{6}\ \text{Hz})\ (5 \times 10^{-9})\ \left(\frac{350\ \text{MHz}}{5\ \text{MHz}}\right)$$

$$= 1.75\ \text{Hz}$$

However, a high gain loop is utilized to optimize tracking and minimize noise. Therefore it is probable that the integrator will have drifted to one rail long before the oscillator warms up. Zener diodes D_1 and D_2 limit the integrator's swing to ±5 VDC. The HP oscillator data sheet specifies a minimum timing range of 0.5×10^{-7} for a control range of ±5 VDC. Therefore the minimum control range is

$$\Delta f \geq (0.5 \times 10^{-7})\ (5 \times 10^{6}\ \text{Hz})\ \left(\frac{350\ \text{MHz}}{5\ \text{MHz}}\right)$$

$$\geq 17.5\ \text{Hz P.P.}$$

This shall be more than adequate to compensate for oscillator drift at warm up. However, it presents a problem from the standpoint of lock up. HP has stated verbally that the control range should be .5 Hz ± .25 Hz for a 5 MHz oscillator or .05 Hz/volt ± .025Hz/volt. One oscillator, HP1520 A90651 was measured for gain and range.

Ko = (0.05 Hz/volt) @ 5 MHz

Δf_{MAX} = (.075 Hz/volt) (5 volts) $(\frac{350\ MHz}{5\ MHz})$ = 26.25 Hz
at 350 MHz for 5 volts offset.

Therefore the lock-in frequency, the frequency range over which the loop will acquire lock within $\frac{1}{\omega n}$ seconds, should be greater than 26.25 Hz @ 350 MHz

$\Delta f_L \simeq 2\ \delta fn$ Gardner, P. 43

Therefore, $\frac{1}{2}\Delta f_L = 2(.8)\ (3.5\ Hz)$
$= 2.8$ Hz.

But $\Delta f_{max} >> \frac{1}{2}\Delta f_L$

Therefore the loop may not acquire lock immediatly and a calculation for pull-in is in order.

$\Delta\omega_p = 2\sqrt{L\omega_n K_v}$ Gardner P. 46

$K_v = K_o\ K_d\ F(0)$ Gardner P. 29

F(0) = DC Gain of OP Amp = 10^5

K_o = .31 radians/sec/volt

K_d = .22 volts/radian

$\therefore K_v = (.31)(.22)(105) = 6820$

$\therefore \Delta\omega_p = 2\sqrt{(.8)(3.5\ Hz/volt)(2\pi radians/sec/Hz)(6820)}$
$= 692$ radians/sec

$\frac{1}{2}\Delta f_p = 55$ Hz

Since $\frac{1}{2}\ \Delta fp \geq \Delta f$ offset then pull-in should occur. The time required for pull in is

$T_p \simeq \frac{(\Delta\omega)^2}{2\delta(\omega n)^3} = \frac{[(26\ Hz)(2\pi\ rad/sec/Hz)]^2}{2(.8)[(3.5)(2\pi\ rad/sec/Hz)]^3}$

Gardner P. 46

$$T_p = \frac{[107]^2}{2(.8)[22]^3} \text{ seconds}$$

$$T_p = \frac{11449}{1.6(483)} = 15 \text{ seconds}$$

Therefore the loop should take a maximum of 15 seconds to lock-up assuming ideal components with no offset voltages.

The phase-lock loop circuit also contains a lock indicator which operates independent of the wiring of the phase detectors.

Since the tuning range of the oscillator is very small relative to the operating frequency, quadrature phase detector outputs may be realized by inserting an additional 90° electrical length of coax at the input of one of the phase detectors.

When in lock the output of the phase detector at V_a will be zero, while the output of the phase detecor at V_b will be maximum positive or negative depending on the wiring of the phase detectors.

If the loop loses lock, then quadrature sine wave beatnotes will appear at the outputs of the two phase detectors as shown in Figure 4.2. Note that the sum of these two voltages is a periodic wave form which crosses through zero. Also if either the 350 MHz multiplier or the 350 MHz mixer output fails, then both phase detectors will indicate zero average DC voltage.

Therefore a lock indicator is utilized using a window comparator which obeys the following relation:
If $|V_a + V_b| < V_{ref}$, then indicate out of lock where $V_{ref} = \frac{1}{2}|V_{amax}| = \frac{1}{2}|V_{bmax}|$. By using the absolute value of the sum, polarity problems are avoided.

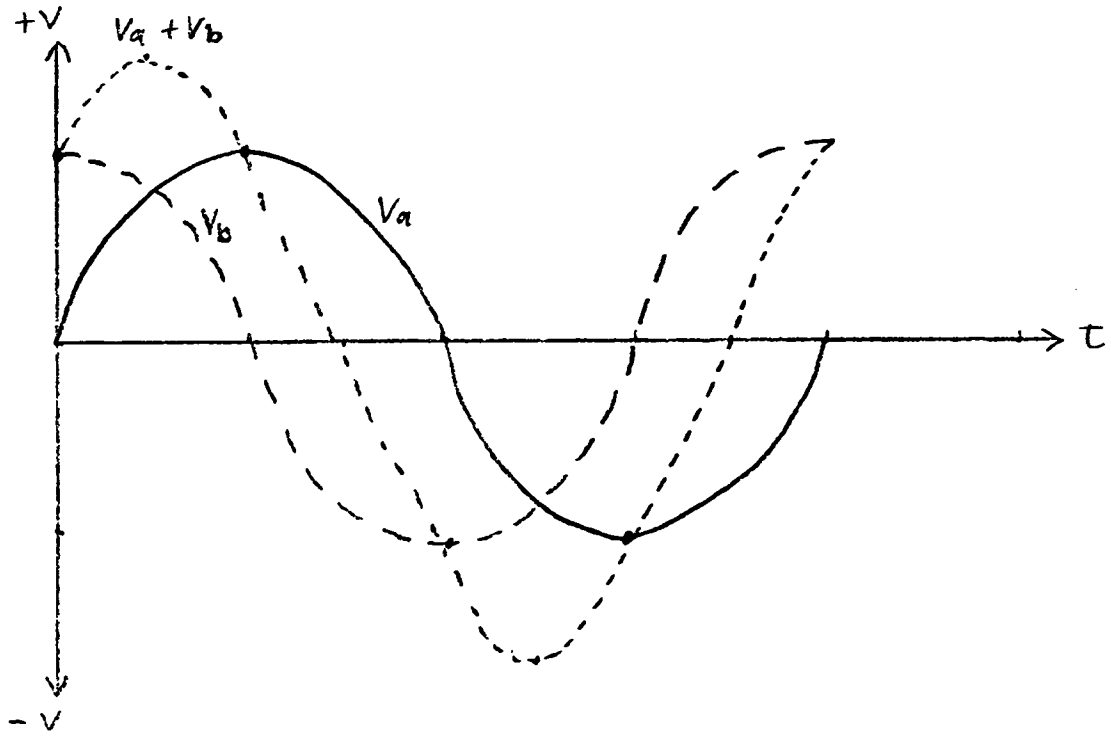
The summing function is accomplished by resistors R_3 and R_{12} with op amp U_{2a}. The absolute value function is performed by op amps U_{2a} and U_{2b}. And the comparison function is done by op amp U_{2c}. The threshold voltage is normally

set for about one half the peak phase detector output voltage, or about .15 VDC. Components R_{19}, D5 and D6 convert the op amp output to a +5 VDC voltage swing to interface to the digital circuitry. Open collector buffer U3 provides enough drive current to drive the LED and provide a high lock warn indication to the DCS system.

One disadvantage of this system is that the out of lock indication will only occur for a small portion of the beat-note cycle which may be very slow to begin with. Therefore, it is recommended that a set-reset latch be utilized in the DCS interface to hold the out of lock condition until manually reset.

4.5 Wire Harness

The wire harness for the L17D module is shown in Drawing D13220S11A.



PHASE DETECTOR OUTPUT VOLTAGES IN THE OUT OF LOCK CONDITION

Assuming $V_a = \sin \omega t$ and $V_b = \cos \omega t$,

$V_a + V_b = \sin \omega t + \cos \omega t = \sqrt{2} \sin (\omega t + 45°)$

Figure 4.2

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	10/24/80			MADE CORRECTIONS

S1 REAR VIEW
ALCO NO. MTA406PA

LOCKED AUTO INDEPENDENT

WHT/PUR
WHT/BRN → A1-P6-12
WHT/BLK → A1-P6-3

BATT
IND
AUTO
LOCK WARN
WHT/RED → A1-P6-7
ORN
WHT/ORN → A1-P6-11
+5V

LOOP OPEN
ALCO MSPS-103C

350 MULT
IN PHASE
EFC
QUAD PHASE
350 MIXER
C÷2/B÷2
A/D

RG-188
OSM 209
OSM 501-3
OSM 201-1A
10dB PAD MECA
OSM 531-3
OSM 221-1

A1 PHASELOCK LOOP P.C. BOARD
A1-J6
J1 IN PHASE, J3 V8, J4 QUAD PHASE, J2 V4, J5

A1-P6 pinout:
1 −15V
2 +15V
3 SW "LOCKED"
4 GND
5 AUTO WARN LED
6 AUTO WARN DCS
7 IND. WARN LED
8 +5V
9 LOCK WARN DCS
10 ANALOG GND
11 LOCK WARN LED
12 S1B CEN TAP
13 EFC GND
14 REF+Y COIL
15 EFC TO DCS
16 EFC FT. PANEL

W/EDGE CONNECTOR # 50-30A-30

1/A	5MHZ OUTPUT SIGNAL
2/B	5MHZ RETURN
3/C	+11 TO +13.5 VDC OSCILLATOR/AMPLIFIER INPUT
4/D	CASE
5/E	EFC RETURN
6/F	EFC INPUT
7/H	N.C.
8/J +	11 TO 13.5 VDC OVEN CONTROLLER INPUT
9/K −	
10/L	N.C.
11/M	OVEN MONITOR
12/N	N.C.
13/P	N.C.
14/R +	20 TO 30 VDC OVEN HEATER INPUT
15/S −	

5MHZ OSCILLATOR H-37-C
HEWLETT-PACKARD

IN4742A 12V
200Ω 1W

A2 VOLTAGE REGULATOR P.C. BOARD
E1 +28V IN, E2, E3, E4, E5

"INDEPENDENT" RG-188 OMQ
"LOCKED" RG-188
OSM501-3
RY1 TRANSCO 919C70100 SPDT COAXIAL RELAY
IN4005
GRY → +28V
WHT/GRY → A1-P6-14

+28V GRY FL 33μf,35V → 29 +28VDC
+15V RED FL 33μf,35V → 16 +15VDC
+5V ORN FL 33μf,35V → 10 +5VDC
−15V YEL FL 33μf,35V → 17 −15VDC
BLK → 34 POWER GND
250 μH(4)

20 BATTERY +
35 BATTERY −

OSM 221-1 → 6B120-350/25-0 K+L → OSM 218 → NRAO A3 MC 1662 50-350 MHZ MULTIPLIER → OSM 218 → 4B51-50/20-0 50 MHZ FILTER K+L → UT 141 → OMQ → J7 50 MHZ FROM MASTER LO +10dBm

+15V → 91Ω RED 2 WATTS 5.1 VDC → IN4733

OSM 201-1A → 4B120-125/60-0 K+L → UT 141 → OMQ → J16 A/D +10dBm OUTPUT

UT 141 → OSM 221-1 → DCG 10-4 10dB COUPLER ANZAC → OSM 201-1A → UT 141 → OMQ → J8 A/D 100-150 MHZ +10dBm, FROM SYNTHESIZER

MERRIMAC PDM-20-165 PWR DIVIDER → OSM 218 → DCG 10-4 10dB COUPLER ANZAC → OSM 201-1A → UT 141 → OMQ → J9 C÷2/B÷2, 100-125 MHZ +10dBm; FROM SYNTHESIZER

WATKINS JOHNSON MIXER M1A "QUAD PHASE" DETECTOR
PDM-30-250 MERRIMAC
GPD A6 402/402/403 AVANTEK
+15V

90° @ 350 MHZ ADDITIONAL COAX

WATKINS JOHNSON MIXER M1A "IN PHASE" DETECTOR
PDM-30-250 MERRIMAC
GPD A5 403/402/402 AVANTEK
+15V

6B120-350/25-0 K+L → W/J M1E MIXER → 10dB PAD MECA → A4 GPD 402/402/405 AMP. AVANTEK → X2 MULT D1-4 ANZAC → DCG 10-4 10dB COUPLER → OSM 218

MERRIMAC PDM-20-165 PWR DIVIDER → 4B120-225/60-0 K+L → UT 141 → OMQ → J15 C/B +10dBm OUTPUT

-10dB PAD MECA

FRONT PANEL
REAR PANEL

NOTES:
1. XXXX INDICATES FRONT PANEL LABELING.
2. S1 AND RY1 SHOWN IN INDEPENDENT MODE.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY | USED ON

VLA PROJECT: L17 SYNTHESIZER PHASELOCK (MODEL "D")

TITLE: SYNTHESIZER PHASELOCK MODULE SCHEMATIC

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 2/11/78
DESIGNED BY	DATE 12/19/77
APPROVED BY	DATE 12/19/77

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D13220 S11 | REV. A | SCALE ~

5.0 FRONT PANEL INDICATORS AND CONTROLS

Lock Warn LED

Lights when an out of lock condition is detected in the locked mode. This indicator is disconnected in the independent mode.

Locked/Auto/Independent Switch

Permits the frequency synthesizers to either be phase locked to the system or to be operated independently in frequency.

In the phase locked mode the sum of the L17 output frequencies must be set to equal 350 MHz. The C ÷2 or B ÷2 synthesizer obtains its 5 MHz reference from the system while the A or D synthesizer obtains its reference from the L17 internal phase locked VCXO. In the independent mode a relay switches the A or D synthesizer input to the same system 5 MHz signal that the C or B synthesizer is using.

In the Auto position, the DCS system controls this mode selection.

EFC OSM Connector

Provides a monitor point for the frequency control output of the phase locked loop. This output should read 0 VDC and should be checked periodically for crystal oscillator aging. The maximum possible range of this voltage is $\simeq \pm 4.7$ VDC.

Loop Open Switch

This switch shorts the electronic frequency control (EFC) input of the HP voltage controlled crystal oscillator. This switch can be used to check for drift of the L17 crystal oscillator by watching the lock warn LED beatnote or by watching the phase detector output on a scope. The beatnote should be near 0 Hz if the oscillator mechanical tuning is correct and the synthesizers are set to the correct frequencies.

Freq Adj Screwdriver Adjustment

Controls the frequency adjustment of the internal 5 MHz VCXO. This should be adjusted to provide 0 VDC on the VCXO voltage control input in the locked mode after the oscillator has stabilized in temperature. This should be checked periodically for oscillator aging.

In Phase OSM Connector

Provides a monitor point for the phase detector output in the phase-lock loop circuit. This point should indicate 0 VDC in lock, and a quadrature beatnote with the Quad Phase OSM connector when out of lock. If either the 350 MHz multiplier output or the 350 MHz mixer output fail then both phase detector outputs will read 0 VDC.

Quad Phase OSM Connector

Provides a monitor point for the phase detector in quadrature with the phase-lock loop's phase detector. In lock this output should read ± 0.35 VDC.

A/D OSM Connector

Monitors the A or the D synthesizer RF input to the L17 module. This signal should read about -10 dBm.

C ÷2/B ÷2 OSM Connector

Monitors the C ÷2 or B ÷2 synthesizer RF input to the L17 module. This signal should be at one half the frequency of the C or B L17 output and should read about -10 dBm.

350 Mult OSM Connector

Monitors the output of the 350 MHz multiplier circuit. This signal should read about -7 dBm.

350 Mixer OSM Connector

Monitors the output of the 350 MHz mixer circuit. This signal should read about +1 dBm.

6.0 PRELIMINARY MODULE ADJUSTMENTS

1. Check power supply distribution wiring with ohmmeter. (Refer to Drawing No. D13220S11).
2. Apply supply voltages to module.
3. Check load current to oscillator which should be about 200 ma when warm. (Use clip on HP 428B)
4. Set regulator pot R4 to give 20.7 VDC measured at E3 on regulator board with a warm oscillator load (200 ma).
5. With the front panel switch in the "Locked" position, apply the proper synthesizer inputs to the L17. Be certain that the sum of the two L17 outputs is 350 MHz. While monitoring the "In Phase" OSM connector with a scope, press the "Loop Open" switch and adjust the front panel "Freq Adj" for zero beatnote, after adequate warmup.
6. With the front panel switch S1 "Locked" release the "Loop Open" switch and observe the "Lock Warn" light extenguish.
7. Place a scope on the "EFC" Front Panel Connector and adjust "Freq Adj" for zero voltage. Place a scope on the "In Phase" monitor connector, and a 50 mVpp output function generator on the L1 voltage control input in the Master LO system. Using a low level sine wave output, vary the function generator through it's range while looking for a peak in sine wave amplitude at the "In Phase" monitor point. Note the frequency at which this occurs and change R5 on the phase-lock loop board until the frequency is observed to be about 3.5 Hz.
8. Now apply a low level square wave with the function generator and observe the damping at the "In Phase" monitor point. Change R6 on the phase-lock loop board until a transient phase error corresponding to a damping factor of 0.8 occurs. The proper response may be found in Figure 4.3, page 34, of Phaselock Techniques by Gardner.

7.0 MEASUREMENTS

Non-harmonically related spurious signals at L17B2 and L17B3 A or C outputs scanning from DC to 200 MHz measured less than -63 dBc. Phase variations measured at the L17 internal phase detector across the tuning ranges of the A and C outputs were less than 1.3° peak to peak at 350 MHz for both modules. This will be worse for the actual A and C outputs because of the extra filters not seen by the phase detector. However, resettability will be much better.

8.0 SYNTHESIZER PHASE-LOCK (L17) DRAWING LIST

Project No. 13220 10/14/80

	Number	Revision
Block Diagrams		
L17D Synthesizer Phase-Lock	D13220B2	C
Schematic and Logic Diagrams		
Synthesizer Phase-Lock Schematic	D13220S11	A
5-400 MHz Amplifier	B13220S5	A
Phase-lock Loop	C13220S6	F
50-350 MHz Multiplier	B13220S7	A
Voltage Regulator Battery Charger	B13230S1	A
Bill of Materials		
Synthesizer Phase-Lock	A13220Z13	-
Positive Voltage Regulator	A13230Z20	-
Assembly Drawings		
+20.7 V Voltage Regulator	B13230P31	-
50-350 MHz Multiplier	B13220P3	-
Phase-Lock Loop	B13220P4	B
Synthesizer Phase-Lock Module	D13220P12	-
Printed Circuit Board Art Work		
50-350 MHz Multiplier	B13220AB3	-
Phase-Lock Loop	B13220AB4	A
Printed Circuit Board Drill Drawings		
50-350 MHz Multiplier	B13220M4	-
Phase-Lock Loop	B13220M5	A
Mechanical Drawings		
Partition Plate	D13220M7	-
Right Side Cover Plate	C13220M8	-
Spacers & Brackets	C13220M9	-
Oscillator Mounting Plate	B13220M10	-
Front Panel	C13220M6	-
Wirelists		
L17D Synthesizer Phase-Lock	A13220W9	-

9.0 DATA SHEETS

HEWLETT hp PACKARD

10 MHz CRYSTAL OSCILLATOR

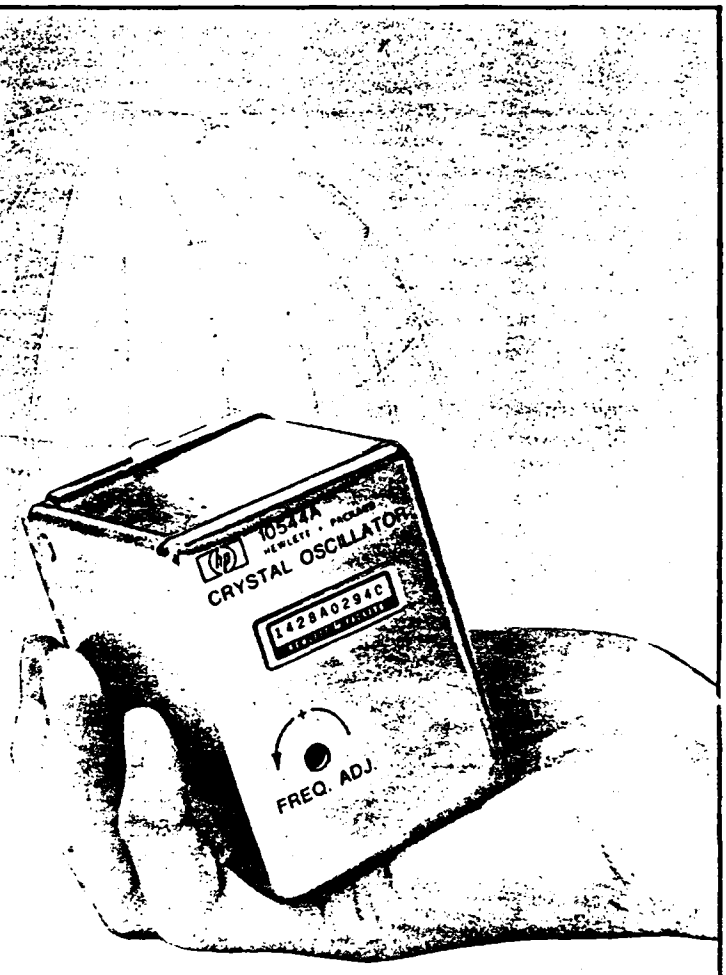
10544A

TECHNICAL DATA JUL 76

aging rate less than 5 x 10^{-10}/day

excellent phase noise

fast warm-up



The HP Model 10544A Quartz Crystal Oscillator is an extremely stable, compact, low-power source of 10 MHz. Fast warm-up and a low aging-rate are important for both instrument and systems applications. This is achieved using a new crystal design ruggedly mounted in a cold-welded enclosure. The crystal, along with the oscillator, buffer amplifier, and oven control circuits are all mounted inside a thermally insulated oven.

A significant improvement in signal-to-single-sideband phase-noise ratio has been accomplished by oscillator circuit modifications. This performance along with the excellent short-term stability of the 10544A make it an ideal oscillator for use in systems where the crystal output is multiplied to a higher frequency.

Model 10544A is designed to mate with standard 15-pin printed circuit board connectors which permit direct connections and eliminates the need for separate sockets and interwiring. The unit is designed to operate into a 1000 ohm load. This satisfies most solid-state input requirements.

Its unique design features, plus production efficiencies enable HP to offer, inexpensively in the 10544A, the better than 5 x 10^{-10}/day aging formerly available only in expensive laboratory-type oscillators. With this low aging rate of less than 1 x 10^{-7}/year the manufacturer of communication and test equipment can offer his customers a real cost saving by reducing the frequency of calibration necessary to stay within FCC accuracy requirements.

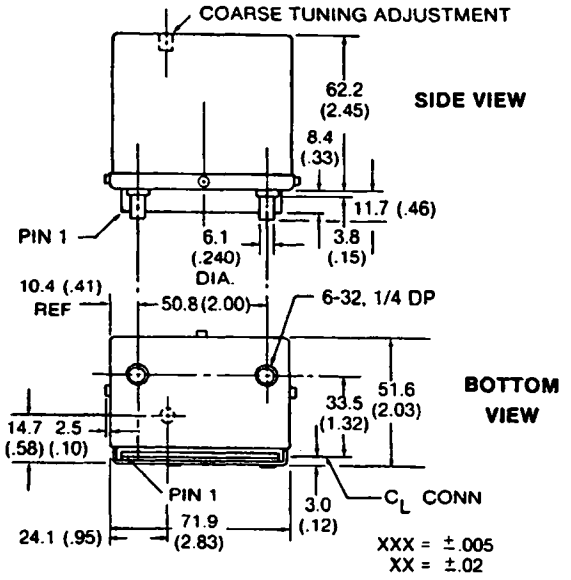
The 10544A is ideally suited for use in communication and navigation systems, synthesizers, time-code generators, counters, and spectrum analyzers. The 10 MHz output frequency is a convenient starting point since it is easily divided or multiplied.

A screwdriver adjustment through the top of the oven permits frequency adjustment over a range of more than 2×10^{-6} (20 Hz), yet the control is sensitive enough to allow adjustment to better than 1×10^{-9} (0.01 Hz). Frequency can also be controlled electronically over a 1 Hz range with an externally applied voltage.

To maximize oven-efficiency in the 10544A, the heater current is controlled by a switching regulator circuit. This produces switching transients at about 4 kHz on the input line and a low level spurious signal on the output. A version of the oscillator with a dc oven controller is available. It should be used when adequate input filtering is difficult or better than -80 dB nonharmonic components on the output are required.

To permit optimum performance and use of available voltages, the power inputs for the oscillator/amplifier, oven controller and oven circuits are available separately. However, with a simple external IC regulator, a single voltage regulated to 10 percent may be used. (See Figure 3.)

Power and signal connections are made through a 15-pin printed-circuit connector, such as CINCH 250-15-30-210 (HP Part No. 1251-0160). Connections are shown in Figure 2.

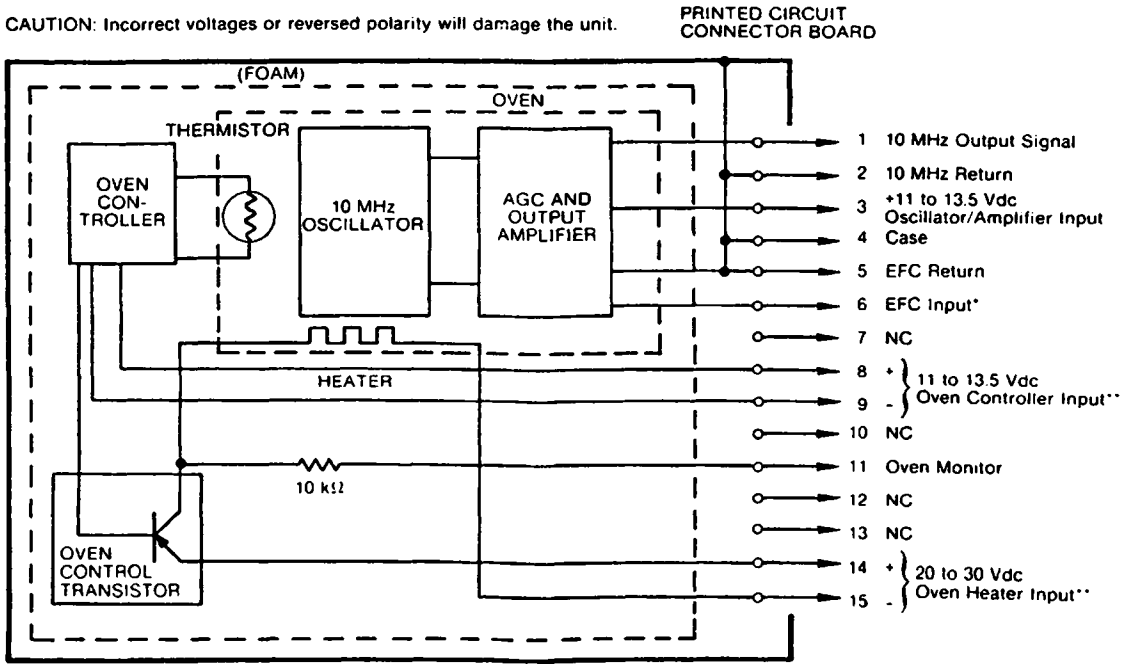


NOTE: DIMENSIONS IN MILLIMETRES AND (INCHES).

FIGURE 1
Outline Drawing

The Oscillator Amplifier and Oven Controller should both operate from a +11 to 13.5 Vdc source. If connected to the same source, an LC circuit, marked B in Figure 3 is then required to isolate controller switching transients from the oscillator. The oven voltage may be obtained from a single source of +20 to 30 Vdc or from a combination of negative and positive sources which combined supply 20 to 30 Vdc. If this is done, the positive oven voltage must be equal to or greater than the oven controller voltage. There must be a current path between the oven controller voltage source and the oven voltage source to return the base drive current for the oven control transistor. This may be accomplished by tying either pins 8 & 14 or 9 & 15 together.

CAUTION: Incorrect voltages or reversed polarity will damage the unit.



*Connect Pin 5 to Pin 6 if external EFC (Electronic Frequency Control) is not used.
**A return path must be provided between the oven controller and heater supplies to return the base drive current from the oven control transistor. This may be accomplished by tying either Pins 8 & 14, or Pins 9 & 15 together.

FIGURE 2
Block Diagram

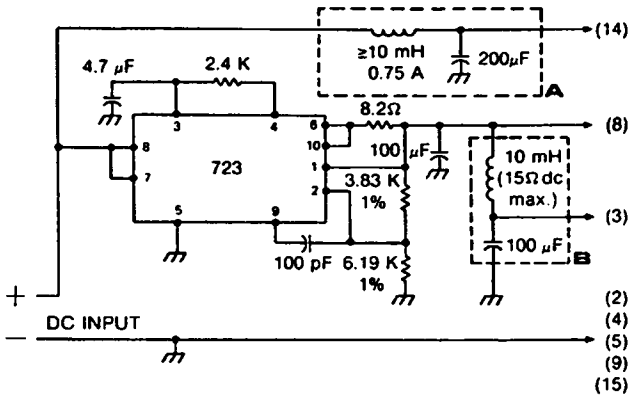


FIGURE 3

I.C. Voltage Regulator 723, (HP Part No. 1826-0010) TO5 configuration to supply 11½V to oscillator/amplifier and oven controller. Circuits A and B are decoupling filters.

Temperature of the oscillator oven is maintained by varying the duty-cycle of the oven input current through a control transistor. A non-inductive voltage source is required to prevent excessive voltage transients that could damage the control transistor. In addition, it may be desirable to provide decoupling between the oven switching transients and other circuits operating from the same power source. The filter marked A in Figure 3 can be used to provide both the non-inductive voltage source and the decoupling filter.

Power for the 10544A may be obtained from a single source of +20 to +30 Vdc (15 to 30 Vdc for 10° to 71°C operation) with 10 percent regulation using a simple IC regulator. A suggested circuit is shown in Figure 3. The resistor and capacitor connected to terminals 3 and 4 of the IC minimize ripple and noise in the regulated output. If the decoupling filter marked A is used, the capacitor should be placed close to the pin 14 connection to minimize radiation of the switching transient noise.

The output signal at pin 11 (with respect to pin 15) indicates the temperature condition of the oscillator oven. The signal voltage level depends on the value of oven supply voltage at pins 14 and 15.

Duty-cycle of the signal at pin 11 depends on the oven temperature; long duty-cycle at turn-on and short duty-cycle at operating temperature. The corresponding dc voltage monitored with a high-impedance voltmeter is maximum when the oven is cold (at turn-on) and minimum when the oven is at operating temperature.

Connect the oscillator through a 15-pin printed-circuit connector. Allow a 24-hour warm-up time for stabilization before adjusting frequency. At initial turn-on, the oscillator may require several days to achieve its specified aging rate.

The crystal in the 10544A oscillator has the typical quartz crystal characteristic of aging (changing resonant frequency) slowly when the unit is off as well as when it is operating. The 10544A crystal is made from high quality natural quartz and extreme care is exercised to eliminate contamination in the crystal enclosure to minimize aging. Each oscillator is aged at the factory to insure that its aging rate is better than 5×10^{-10}/day. This rate can be expected to gradually decrease and typically will reach 1.0×10^{-10} within one year. The coarse tuning adjustment permits periodic change back to exactly 10 MHz. The adjustment range is adequate to cover in excess of 10 years at the typical aging rate.

Oscillator frequency may be adjusted by using the 18-turn screwdriver adjustment located on the top of the oscillator case. Fine frequency adjustments may be made with a range of $\geq 1 \times 10^{-7}$ using -5 to +5 volts dc applied to the electronic frequency control input, pin 6.

A simple method of frequency adjustment is the "oscilloscope drift" method. The oscillator frequency may be adjusted against a reference or "house" standard and drift can be monitored.

Methods for measuring frequency are described in HP Application Note 52-2. For minimum distortion the oscillator output must be terminated with a 1000-ohm load.

Apply the proper input voltages and allow the output frequency to stabilize for 24-hours. Adjust the output frequency to 10 MHz as described under FREQUENCY ADJUSTMENT and check the output voltage with an RF Voltmeter or calibrated oscilloscope. Be sure to terminate the output with a 1000-ohm load. If the output voltage or frequency is not within specification, check the input voltages and determine that the regulation and noise are within specification. If the input power or current are substantially different from those shown in the specifications, return the oscillator to HP for repair. The oven input power should decrease within a few minutes after turn-on as the oven temperature stabilizes. Continued full input power indicates a malfunction of the oven controller and will damage the oscillator by overheating.

The 10544A is designed for factory repair only. Field repair should not be attempted. Repairs are handled promptly on an exchange basis through the nearest HP Sales and Service Office. Order HP Part No. 10544-60511 for exchange oscillator.

SPECIFICATIONS

FREQUENCY: 10 MHz. See note (1).

▶ **AGING RATE:** $<5 \times 10^{-10}$/day after 24-hour warmup. See note (2). $<1 \times 10^{-7}$ per year for continuous operation.

TEMPERATURE COEFFICIENT:
$<1.5 \times 10^{-8}$ frequency change over a -55°C to 71°C temperature range. $<7 \times 10^{-9}$ over 0 to 71°C range.

LOAD:
$<5 \times 10^{-10}$ frequency change for ±25 percent change in 1000 ohm load.

WARMUP:
Within 5×10^{-9} of final value 20 minutes after turn-on, at 25°C and 20 Vdc. See note (3).

ADJUSTMENT:

Coarse Frequency Range:
$>2 \times 10^{-6}$ (20 Hz) centered on 10 MHz with 18 turn control.

Electronic Frequency Control (EFC):
$\geq 1 \times 10^{-7}$, control range -5 Vdc to +5 Vdc. (1 4e)

OUTPUT 10 MHz:

Voltage:
1 Vrms ±20% into 1000 ohms from oscillator's ac coupled (.01 μF) emitter-follower.
(output must be terminated with 1000 ohms)

Harmonic Distortion:
Down more than 25 dB from rated output.

Spurious Phase Modulation, Discrete Sidebands, 10 Hz to 50 kHz:
Down more than 80 dB from rated output.

Signal-to-Single-Sideband Phase-Noise Ratio:
(1 Hz Measurement Bandwidth):

Offset from 10 MHz (Hz)	Ratio (dB)
1	83
10	120
100	140
1,000	145
10,000	145

ENVIRONMENTAL:
Temperature, operating -55°C to +71°C.
Temperature, storage -55°C to +75°C.
Altitude: 15.2 km (50,000 feet)
Humidity: 95% RH at 40°C.
No permanent degradation from the following:
Vibration: 0.01" peak-to-peak, 10 to 55 Hz.
Shock: 30 G, 11 ms, 1/2 sinewave.

SHORT-TERM STABILITY:

Averaging Time (s)	Stability $\left[\sigma_{\Delta f/f}(2,\tau)\right]$
10^{-4}	5×10^{-8}
10^{-3}	5×10^{-9}
10^{-2}	5×10^{-10}
10^{-1}	5×10^{-11}
10^{0}	1×10^{-11}
10^{1}	1×10^{-11}
10^{2}	2×10^{-11}

WARRANTY:
Hewlett-Packard warrants the 10544A 10 MHz Oscillator against defects in materials and workmanship for a period of 1 year from the date of delivery. The oscillator will be repaired or replaced at no charge during the warranty period.

CONNECTORS:
Printed circuit—mates with CINCH 250-15-30-210 (HP 1251-0160) or equivalent (see Figure 2).

SIZE:
72 mm x 52 mm x 62 mm, (see Figure 1).
(2-13/16" x 2-1/32" x 2-7/16",~14 cu. in.)

WEIGHT:
0.31 kg (11 oz).

NOTES:
(1) Frequencies from 4.5 to 12 MHz available on special order.
(2) For oscillator off-time less than 24 hours.
(3) Final value is defined as frequency 24 hours after turn-on. With 15 Vdc oven input, warm-up time is 60 minutes.
(4) A 10% voltage change will cause a frequency change of $<1 \times 10^{-8}$ for <2 min.
▶ (5) 15 Vdc, 10° to 71°C operating temperature, still air.
16 Vdc, 0° to 71°C operating temperature, still air.
(6) Steady state oven power decreases approximately linearly from 6W at -55°C to 0.5 W at +71°C.

▶ **INPUT VOLTAGES/VOLTAGE COEFFICIENTS:**

Input Circuit	Required Voltage	Required Current/Power	Voltage Coefficients	
			Voltage Change	Frequency Change
Oscillator/Amplifier	11.0-13.5 Vdc Noise<100 μV	18 mA typ., 25 mA max.	1%	$<5 \times 10^{-10}$
Oven Controller	11.0-13.5 Vdc	10 mA typ., 15 mA max.		
Oven	20-30 Vdc See note (5).	Turn on load is 43 ohms, minimum. Power drops to steady state value (3W) after 15 min. at 25°C with 20 Vdc applied. See note (6).	10%	$<1 \times 10^{-10}$ See note (4).

NOTE: See Input Voltages section for details concerning use of common power supplies.

▶ INDICATES CHANGES FROM PRIOR SPECIFICATIONS

For more information, call your local HP Sales Office or East (301) 948-6370 • Midwest (312) 677-0400 • South (404) 434-4000 • West (213) 877-1282. Or, write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, California 94304. In Europe, Post Office Box 349, CH-1217 Meyrin 1, Geneva, Switzerland. In Japan, Yokogawa-Hewlett-Packard, 1-59-1, Yoyogi, Shibuya-Ku, Tokyo, 151.

02-5952-7437

PRINTED IN U.S.A.

SUPPLEMENTARY MANUAL

SPECIAL OPTION

H37-10544A

MODIFICATIONS
OPERATION AND
SPECIFICATION
CHANGES

HEWLETT hp PACKARD

SPECIFICATION CHANGES

FOR SPECIAL OPTION

H37-10544A
5 MHz CRYSTAL OSCILLATOR

GENERAL

This special component oscillator is a standard HP Model 10544A Crystal Oscillator with special Option H37.

Special Option H37 provides a 5 MHz component oscillator and changes the oven controller from a switching type thermostat to a DC proportional type oven controller. The series current regulating transistor is mounted on the outer surface of the bottom cover. The transistor is covered with a plastic insulator (HP Part No. 0340-0757) to prevent accident short-circuit damage to the oven power supply.

SPECIFICATIONS

Frequency: 5 MHz

Load: $< 1.5 \times 10^{-9}$ frequency change with ±10% change in 50Ω load.

Adjustment:

Coarse Frequency Range: $> 1 \times 10^{-6}$ with 18-turn control.

Electronic Frequency Control (EFC): $> 0.5 \times 10^{-7}$ control range -5 Vdc to +5 Vdc.

Output 5 MHz: > 0.5 Vrms into 50 ohms.

Non-Harmonic Component: 100 dB down from rated output.

Required Current/Power: Power drops to 4.5 watts at 25°C after 15 minutes.

maa76100

Avantek

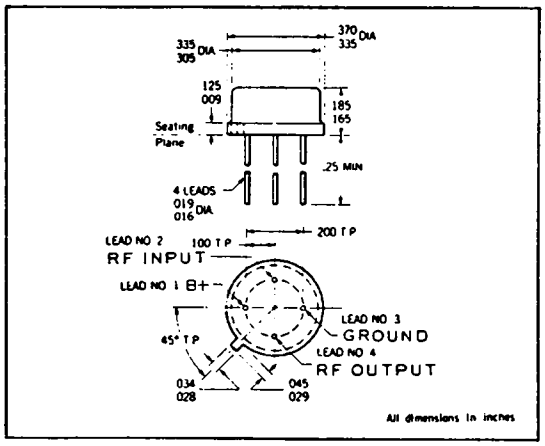
DATA SHEET

GPD-400 Series
Patented*
Thin Film Amplifier
5 to 400 MHz

Miniature Transistor Amplifier

FEATURES

- Low Cost
- Cascadable
- Low Profile TO-12 (4-leaded TO-5) Package
- Thin Film Sapphire Construction
- Over 6 Octaves of Amplifier Bandwidth
- Avantek® Silicon Transistor Chips



DESCRIPTION

The GPD is a complete transistor amplifier, ready to operate in a microstrip circuit upon application of DC voltage. Packaged in a miniature TO-12 transistor package, the Avantek® GPD serves as a completely cascadable amplifier, without bandwidth shrinkage, from 5 to 400 MHz. The low frequency response of the GPD-460 series may be set arbitrarily low by selection of external series input and output capacitors, and the DC bypass capacitor.

The Avantek GPD is an entirely new kind of basic device, designed to provide the circuit engineer major savings in both time and money. Various gain and power output choices are available to permit the user to cascade modules to meet the performance characteristics required in his equipment design. Small size, excellent performance, ready availability and substantial cost savings in equipment manufacture and parts handling are significant advantages that can be gained over standard discrete component methods of manufacture by the use of GPD amplifiers. The costly and time-consuming problems accompanying in-house amplifier design, construction and testing can be totally avoided by inserting GPD's, either singly or cascaded, into a system circuit.

The Avantek GPD is a wideband, single-stage unit of gain, featuring flat response across its greater-than-six-octave bandwidth. The tiny GPD modular amplifier is made with highly reliable ceramic substrates, Avantek microwave transistor chips, thin film circuits, thin film resistors and chip capacitors. All the complex circuitry is encapsulated inside the tiny TO-12 package. The using engineer is spared the normal frustrating RF design problems – impedance matching networks, feedback loops, biasing and stabilization elements.

APPLICATIONS:

The GPD-400 Series amplifier is designed for applications requiring very broadband amplifiers, preamplifiers, isolation amplifiers, and IF amplifiers. The patented circuit design of the GPD permits cascading of units to achieve gain up to any desired level without interstage matching when cascaded in 50-ohm systems. The specified band edges (5 to 400 MHz) are not 3 dB points, but are the points between which the specified gain performance is guaranteed. The low frequency response of the GPD-460 units may be set as close to DC as required.

* U.S. Patent 3493882

INSTALLATION AND OPERATING INSTRUCTIONS:

Installation of the GPD amplifier is similar to the installation of any standard semi-conductor product in a TO-8 or TO-5 package. A clamp is provided to secure the GPD firmly to the ground plane. This step insures positive contact between the GPD package and the ground plane so that no problems with VSWR or oscillation in a multi-stage system will be encountered.

The GPD amplifier is designed for use in a 50-ohm microstrip system. It can be used in other impedance systems, but performance may be degraded.

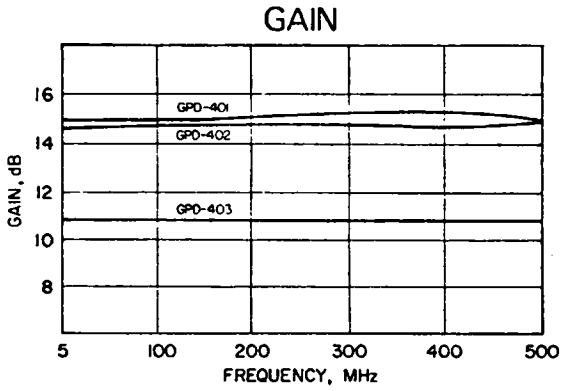
The microwave transistor used in the GPD must be protected from current surges which may be generated by energy storage in system capacitances. Always remove bias voltages from the GPD before inserting or removing the unit under test.

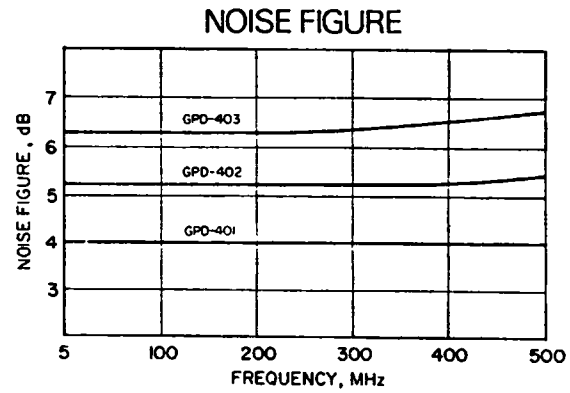
The use of a high-pass filter and/or pad is recommended at the output of gas-discharge-tube noise sources. This protects the transistor in the amplifier from possible high-level ignition-pulse transients which may appear at the RF output ports of these generators (see appropriate manufacturer's literature for further details).

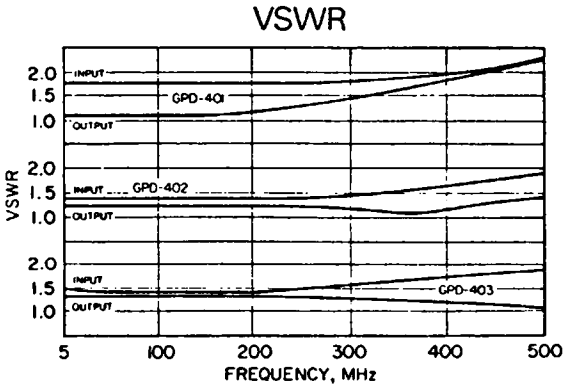
The amplifiers may be stored at temperatures from -65°C to +200°C. The transistors are silicon and all metallization is gold. The operating case temperature is specified at +71°C (+160°F). The amplifiers will operate reliably at temperatures through +125°C (+257°F) although an external heat sink should be used, particularly on the GPD-403.

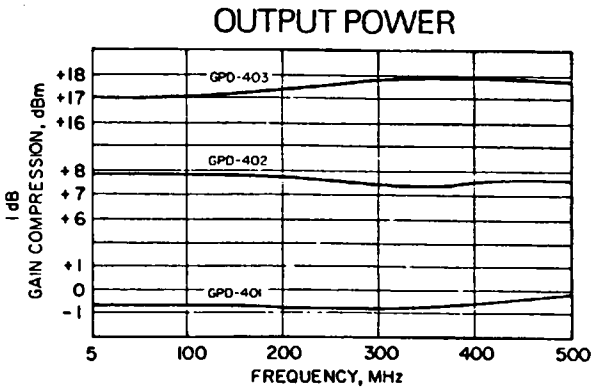
More information concerning applications and use of the GPD amplifier is available from Avantek. Write for the Applications Bulletin *Designing With GPD Amplifiers.*

TYPICAL PERFORMANCE









GUARANTEED SPECIFICATIONS

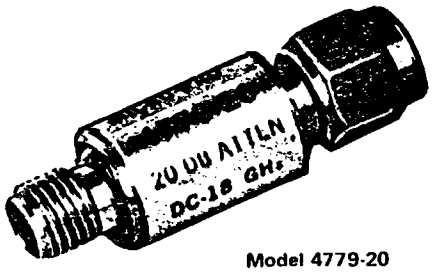
Model	Frequency Response (MHz) Minimum	Gain (dB) Minimum	Flatness (dB) Typical	Noise Figure (dB) Typical	Reverse Isolation (dB) Typical	Power Output for 1 dB Gain Compression (dBm) Typical	Avantek Intercept Point for IM Products (dBm) Typical	VSWR (50 ohms) Typical In	VSWR (50 ohms) Typical Out	Input Power Volts DC	Input Power Current (mA) Typical	Storage Temperature (°C)	Weight (grams)
GPD 401	5-400	13	1.0	4.5	20	7	+8	2.0	2.0	15	10	-65 to +200	1.0
GPD 461	Same as GPD 401, except three external capacitors are required to establish low frequency roll off												
GPD 402	5-400	13	1.0	6.0	20	+6	+18	2.0	2.0	15	24	-65 to +200	1.0
GPD 462	Same as GPD 402, except three external capacitors are required to establish low frequency roll off												
GPD 403	5-400	9	1.0	7.5	20	+15	+26	2.0	2.0	24	65	-65 to +200	1.0
GPD 463	Same as GPD 403, except three external capacitors are required to establish low frequency roll off												

DC to 18 GHz

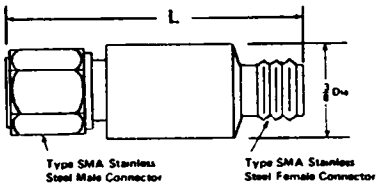
MINIATURE FIXED ATTENUATORS

DC to 18 GHz

Models
4772
4778
4779



Model 4779-20
Miniature Fixed Attenuator



Model No.	L 1-20 dB	L 30, 40 dB
4772	1 1/4	1 9/16
4778	1 15/64	1 31/64
4779	1 15/64	1 31/64

FEATURES:

- SMA Connectors
- DC to 18 GHz
- Flat Frequency Response
- Low VSWR
- 2 Watt Rating
- Miniature Size
- MIL-A-3933B Environmental Performance

Narda 4779 Series miniature attenuators feature flatness with frequency, low VSWR and high power handling capability combined with small size and light weight. The internal construction of 4779 Series attenuators features a thin film distributed constant attenuator element mounted in a capsule which includes a unique matching structure. This attenuator capsule is, in turn, mounted in a sealed barrel with connectors built into each end. This sealed ruggedized construction assures operation in systems under extreme environmental conditions.

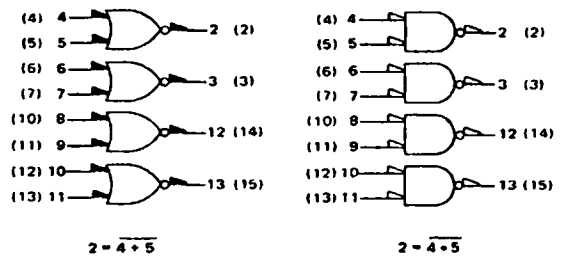
Applications of 4779 Series Attenuators are found in airborne and shipboard EW systems, industrial microwave systems, test equipment, receivers and laboratories.

Model	4779		4778	4772
Frequency Range (GHz)	DC–18		DC–12.4	DC–6
Attenuation (dB)	1-10, 20, 30, 40		1-10, 20, 30, 40	1-10, 20, 30, 40
Max. Frequency Deviation (dB)	DC–12.4 GHz	12.4–18 GHz	DC–12.4 GHz	DC–6 GHz
1 dB	±0.3	±0.5	±0.3	±0.3
2 "	±0.3	±0.5	±0.3	±0.3
3 "	±0.3	±0.3	±0.3	±0.3
4 "	±0.3	±0.3	±0.3	±0.3
5 "	±0.3	±0.3	±0.3	±0.3
6 "	±0.3	±0.3	±0.3	±0.3
7 "	±0.4	±0.5	±0.4	±0.4
8 "	±0.4	±0.5	±0.4	±0.4
9 "	±0.4	±0.5	±0.4	±0.4
10"	±0.3	±0.5	±0.3	±0.3
20"	±0.5	±0.7	±0.5	±0.3
30"	±0.8	±1.0	±0.8	±0.5
40"	±0.8	±1.0	±0.8	±0.5
VSWR (max.)	DC–4 GHz: 1.15 4–12.4 GHz: 1.30 (1–20 dB) 1.35 (30, 40 dB) 12.4–18 GHz: 1.35 (1–20 dB) 1.40 (30, 40 dB)		DC–4 GHz: 1.15 (1–20 dB) 1.35 (30, 40 dB) 4–12.4 GHz: 1.30 (1–20 dB) 1.35 (30, 40 dB)	DC–4 GHz: 1.25 4–6 GHz: 1.40
Input Power Average (Watts) Peak (kW)	2 0.2		2 0.2	2 0.2
Connectors	SMA Stainless Steel; one male, one female			
U.S. Price	3, 6, 10, 20 dB: $82. 1, 2, 4, 5, 7, 8, 9 dB: $92. 30 dB: $90 40 dB: $95.		3, 6, 10, 20 dB: $57. 1, 2, 4, 5, 7, 8, 9 dB: $67. 30 dB: $70. 40 dB: $75.	3, 6, 10, 20 dB: $42. 1, 2, 4, 5, 7, 8, 9 dB: $52. 30 dB: $60. 40 dB: $65.

QUAD 2-INPUT NOR GATE

MC1662
(HIGH Z)

MC1663
(LOW Z)



Number at end of terminals denotes pin number of S package (Case 617).
Number in parenthesis denotes pin number for L package (Case 620).

Four 2-input NOR or NAND gating functions in a single package. An internal bias reference voltage insures that the threshold point remains in the center of the transition region over the temperature range (0 to +75°C).

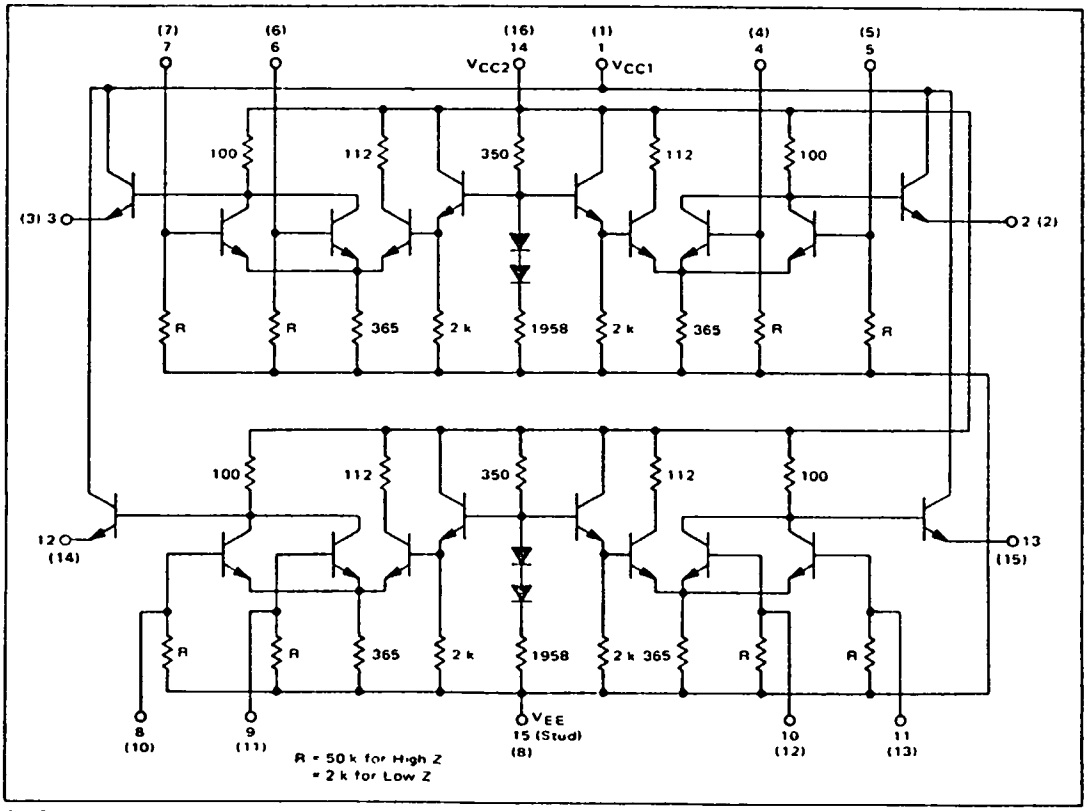
Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

DC Input Loading Factor = 1
DC Output Loading Factor = 70 (High Z)
= 7 (Low Z)

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

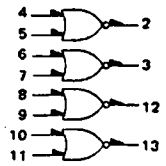
CIRCUIT SCHEMATIC



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS – MC1662S, MC1663S

Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs are tested with a 50-ohm resistor to -2.0 V.



S SUFFIX
CERAMIC PACKAGE
CASE 617

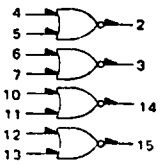
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
0°C	-0.820	-1.870	-1.140	-1.500	-5.2
+25°C	-0.790	-1.850	-1.125	-1.475	-5.2
+75°C	-0.700	-1.830	-1.040	-1.470	-5.2

Characteristic	Symbol	Pin Under Test	MC1662S/MC1663S Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E	15†	–	–	–	56	–	–	mAdc	–	–	–	–	15	1,14
Input Current (Hi-Z)	$I_{in\,H}$	*	–	–	–	350	–	–	μAdc	*	–	–	–	15	1,14
	$I_{in\,L}$	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	15	1,14
Input Current (Lo-Z)	$I_{in\,H}$	*	–	–	–	3.1	–	–	mAdc	*	–	–	–	15	1,14
	$I_{in\,L}$	*	–	–	1.3	–	–	–	mAdc	–	*	–	–	15	1,14
Logic "1" Output Voltage	V_{OH}	2	-0.995	-0.850	-0.950	-0.820	-0.895	-0.730	Vdc	–	4	–	–	15	1,14
		2	-0.995	-0.850	-0.950	-0.820	-0.895	-0.730	Vdc	–	5	–	–	15	1,14
Logic "0" Output Voltage	V_{OL}	2	-1.870	-1.650	-1.850	-1.650	-1.830	-1.630	Vdc	4	–	–	–	15	1,14
		2	-1.870	-1.850	-1.850	-1.650	-1.830	-1.630	Vdc	5	–	–	–	15	1,14
Logic "1" Threshold Voltage	V_{OHA}	2	-1.015	–	-1.000	–	-0.915	–	Vdc	–	–	–	4	15	1,14
		2	-1.015	–	-1.000	–	-0.915	–	Vdc	–	–	–	5	15	1,14
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.625	–	-1.600	–	-1.595	Vdc	–	–	4	–	15	1,14
		2	–	-1.625	–	-1.600	–	-1.595	Vdc	–	–	5	–	15	1,14
Switching Times (50 Ω Load)			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4-2+}	2	1.0	1.5	1.0	1.5	1.1	1.7	ns	4	2	–	–	15	1,14
	t_{4+2-}	2	1.1	1.7	1.1	1.7	1.2	1.9	ns	4	2	–	–	15	1,14
Rise Time	t_{2+}	2	1.4	2.1	1.4	2.1	1.5	2.3	ns	4	2	–	–	15	1,14
Fall Time	t_{2-}	2	1.2	2.1	1.2	2.1	1.3	2.3	ns	4	2	–	–	15	1,14

†Pin 15 is the stud mounting of Case 617 (connected to V_{EE}).
*Individually test each input applying V_{IH} or V_{IL} to input under test.

ELECTRICAL CHARACTERISTICS – MC1662L, MC1663L

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board. Test procedures are shown for only one gate. The other gates are tested in the same manner. See general information section of the MECL III data brochure for complete thermal data.



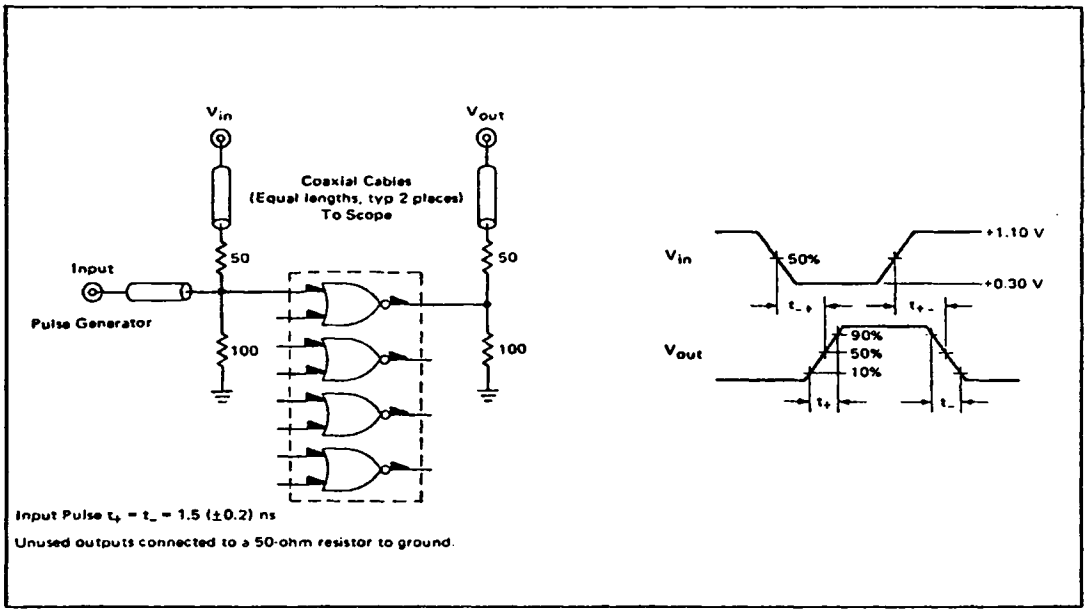
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	-0.840	-1.870	-1.135	-1.500	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+75°C	-0.720	-1.830	-1.035	-1.460	-5.2

Characteristic	Symbol	Pin Under Test	MC1662L/MC1663L Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	--	-	-	56	-	-	mAdc	-	-	-	-	8	1,16
Input Current (Hi-Z)	$I_{in\ H}$	*	-	-	-	350	-	-	µAdc	*	-	--	-	8	1,16
	$I_{in\ L}$	*	-	- -	0.5	-	-	-	µAdc	-	*	-	-	8	1,16
Input Current (Lo Z)	$I_{in\ H}$	*	--	-	-	3.1	-	-	mAdc	*	--	-	-	8	1,16
	$I_{in\ L}$	*	--	-	1.3	-	-	-	mAdc	-	*	-	-	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	-	4	-	-	8	1,16
		2	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	-	5	-	-	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	4	-	-	-	8	1,16
		2	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	5	--	-	-	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.020	-	-0.980	--	-0.920	-	Vdc	--	-	-	4	8	1,16
		2	-1.020	-	-0.980	-	-0.920	-	Vdc	-	-	-	5	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	--	-1.615	-	-1.600	-	-1.575	Vdc	-	-	4	-	8	1,16
		2	-	-1.615	-	-1.600	-	-1.575	Vdc	-	-	5	-	8	1,16
Switching Times (50 Ω Load)			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4-2+}	2	1.0	1.5	1.0	1.5	1.1	1.7	ns	4	2	-	-	8	1,16
	t_{4+2-}	2	1.1	1.7	1.1	1.7	1.2	1.9	ns	4	2	-	-	8	1,16
Rise Time	t_{2+}	2	1.4	2.1	1.4	2.1	1.5	2.3	ns	4	2	-	-	8	1,16
Fall Time	t_{2-}	2	1.2	2.1	1.2	2.1	1.3	2.3	ns	4	2	-	-	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Input Pulse $t_+ = t_- = 1.5\ (\pm 0.2)$ ns

Unused outputs connected to a 50-ohm resistor to ground.

4

custom MODPAK order form

CUSTOMER _____ P.O. # _____

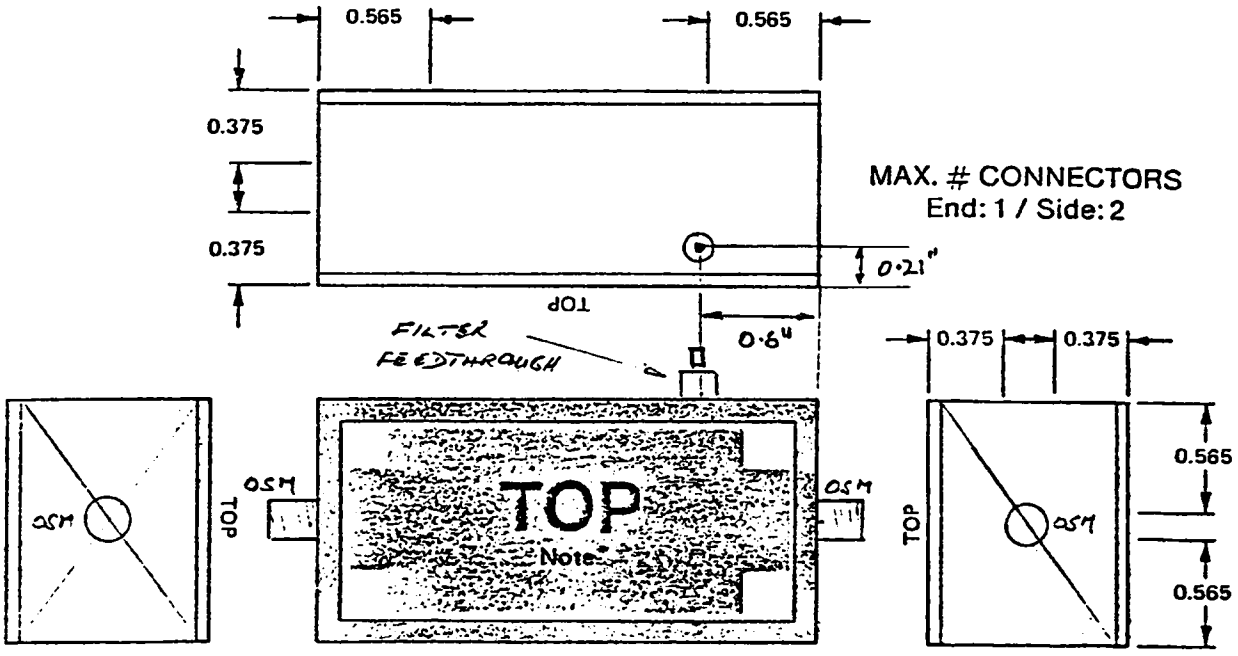
ADDRESS _____

CITY _____ STATE _____ ZIP _____

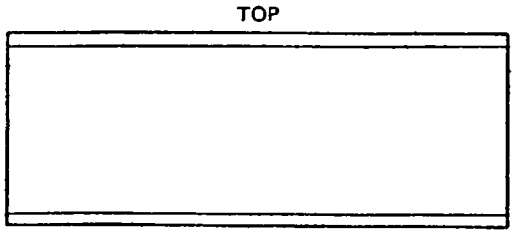
For convenience, you may make an office copy of this form and use it to order Custom MODPAK packages.

Case Size 702 — 1¼" x 2½"

NOTE:
Any case height from ¾" min. to 3" max. (including covers) in 0.250 increments may be ordered. Be sure to indicate ACTUAL HEIGHT DIMENSION and LOCATION of RF connectors and Feedthroughs in clear area specifying distance UP from bottom and DOWN from top.



OSM CONNECTORS TO BE CENTERED ON CENTER POINTS OF BOX ENDS OVERALL BOX HEIGHT 3/4"

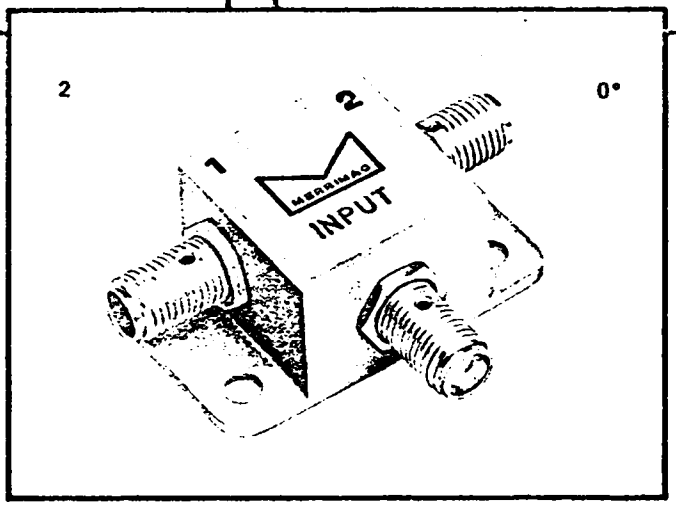


* Max. P.C. Board Dimensions:
2.220 x 0.970 with 0.240(typ) Notched Corners (no connectors);
0.140(typ) on Sides with Connector(s).

MODPAK MODEL # (From page 6)	QUANTITY	PRICE-EACH (From page 6)	TOTAL
702-075-2412	5		

PDM-20 SERIES

MINIATURE POWER DIVIDERS
TWO-WAY
10 KHz-1500 MHz



Merrimac offers this series of miniature broadband reactive power dividers featuring high isolation and excellent phase and amplitude equality characteristics between outputs. These networks find application as array feeds, as signal splitters and as signal combiners in modern communication, radar and telemetry systems.

MINIMUM PERFORMANCE SPECIFICATIONS

Coupling:	−3 db
Isolation:	30 db
Amplitude Balance:	0.2 db
Phase Balance:	1.0°
Insertion Loss:	0.5 db
Impedance:	50 ohms
VSWR:	1.3:1
Power (Matched Loads):	2 watts
Connectors (3):	SMA Female
Weight:	1 oz. (28 grams)

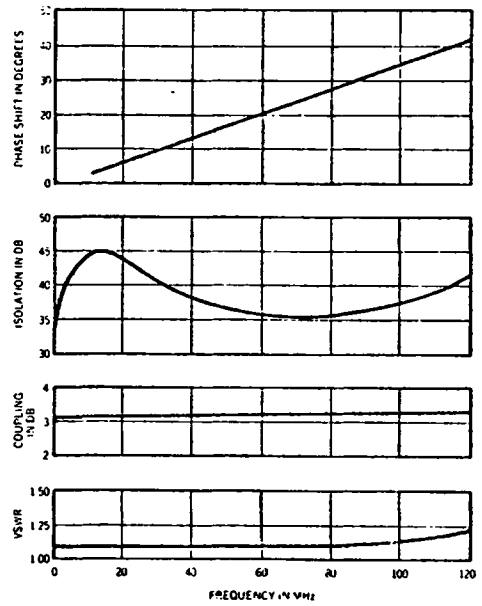
MODEL	FREQUENCY RANGE	PRICE
PDM-20-10	.05-20 MHz	$50.00
PDM-20-50	1-100 MHz	$50.00
PDM-20-110	20-200 MHz	$60.00
PDM-20-165	30-300 MHz	$60.00
PDM-20-200	100-300 MHz	$60.00
PDM-20-300	200-400 MHz	$65.00

Custom models from 10 KHz to 1500 MHz in various bandwidths available on special order.

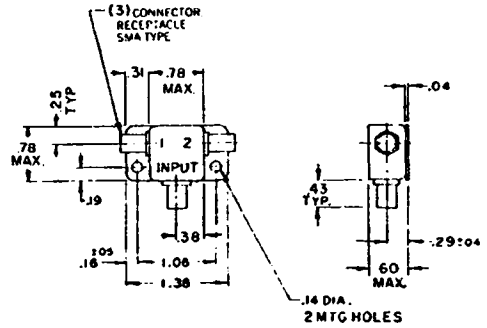
Also available:
- With other connectors
- With any number of outputs
- In other configurations

Prices and specifications subject to change without notice.

TYPICAL CHARACTERISTICS
MODEL PDM-20-50



OUTLINE OF PDM-20 SERIES



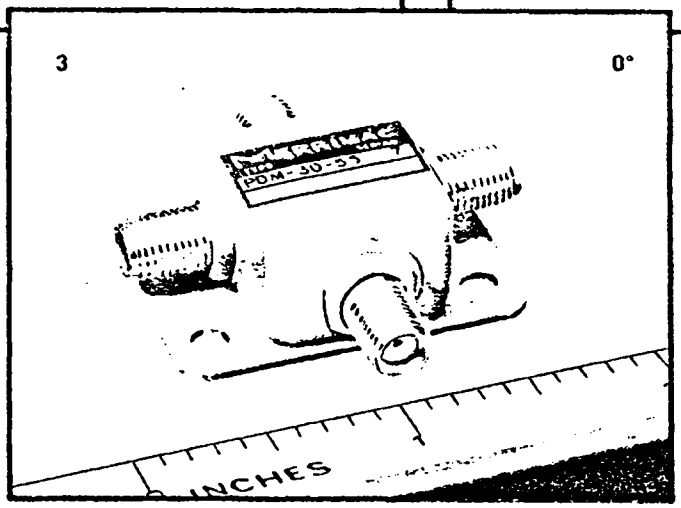
For latest outline details, be sure to contact Merrimac.

MERRIMAC INDUSTRIES, INCORPORATED
41 FAIRFIELD PLACE, WEST CALDWELL, N. J. 07006 • (201) 228-3890 • TWX 710-734-4314

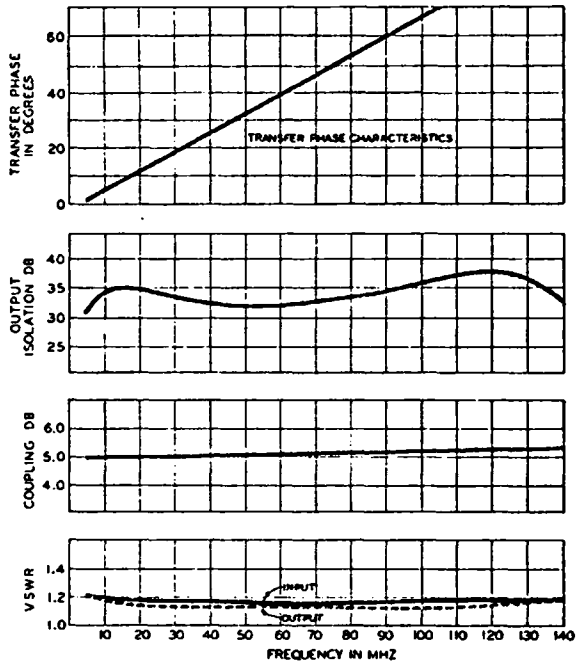
MINIATURE POWER DIVIDERS
THREE-WAY
10KHz-500MHz

PDM-30 SERIES

Merrimac offers a series of conservative, miniature, three-way power dividers with high isolation and uniform output characteristics. These networks are particularly useful in applications involving signal splitting and combining. Their small size and light weight make them particularly suited for airborne and space installations.



TYPICAL CHARACTERISTICS
MODEL PDM-30-55



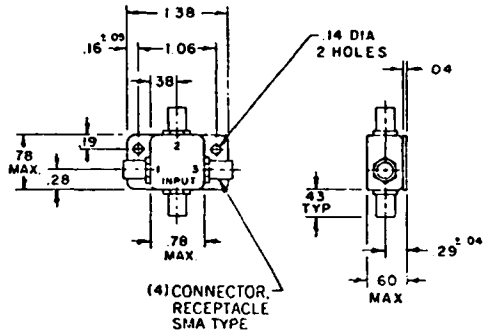
MINIMUM PERFORMANCE SPECIFICATIONS

MODEL:	PDM-30-17	PDM-30-55	PDM-30-250
Frequency Range:	2-32 MHz	10-100 MHz	100-400 MHz
Coupling:	—4.8 db	—4.8 db	—4.8 db
Isolation:	30 db	30 db	25 db
Amplitude Balance:	0.2 db	0.2 db	±0.2 db
Phase Balance:	1°	1°	2°
Insertion Loss:	0.5 db	0.5 db	0.75 db
Impedance:	50 ohms	50 ohms	50 ohms
VSWR:	1.3:1	1.3:1	1.3:1
Power (matched loads):	5 watts	5 watts	5 watts
Connectors (4):	SMA	SMA	SMA
Weight:	55 grams	55 grams	55 grams
PRICE:	**$110.00**	**$110.00**	**$110.00**

Available with other connectors and in other configurations on special order.

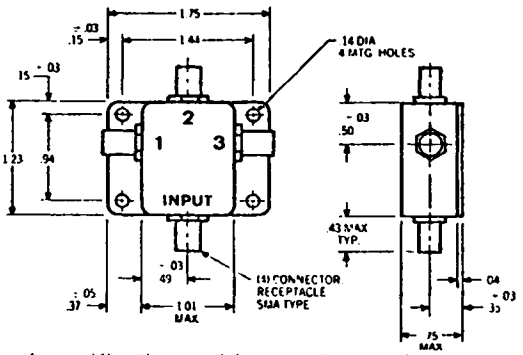
OUTLINES

PDM-30-17 & PDM-30-55



Custom models available from 10 KHz through 500 MHz.

PDM-30-250



For latest outline details, be sure to contact Merrimac.

Prices and specifications subject to change without notice.

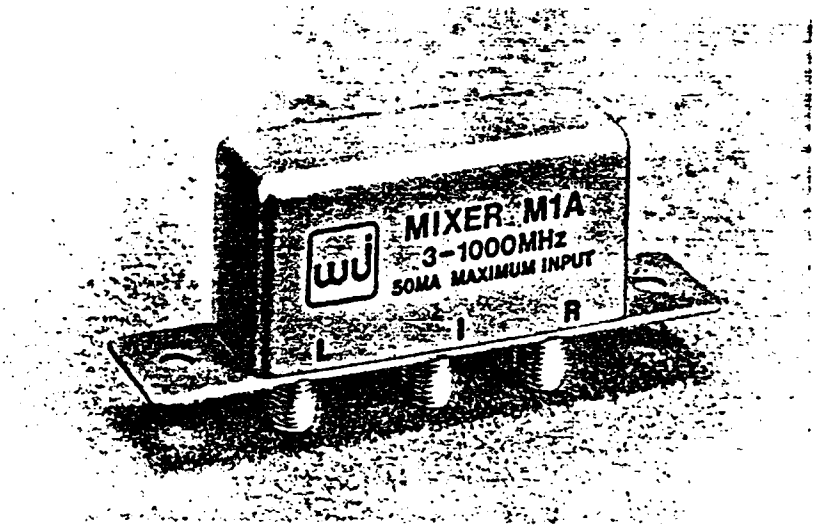
MERRIMAC INDUSTRIES, INCORPORATED
41 FAIRFIELD PLACE, WEST CALDWELL, N. J. 07006 • (201) 228-3890 • TWX 710-734-4314

WJ-M1A

DOUBLE-BALANCED MIXER

LO, RF } 3 TO 1000 MHz
IF DC TO 1000 MHz

- HIGH ISOLATION: >45 dB (TYP.)



Guaranteed Specifications*

Characteristics	Min.	Max.	Test Conditions
Conversion Loss (SSB)		7.5 dB	f_L & f_R 10 MHz to 100 MHz f_I dc to 100 MHz
		10 dB	f_L & f_R 3 MHz to 1000 MHz f_I 1000 MHz
Noise Figure (SSB)		7.5 dB	f_L & f_R 10 MHz to 100 MHz f_I .4 MHz to 100 MHz
		10 dB	f_L & f_R 3 MHz to 1000 MHz f_I .4 MHz to 1000 MHz
Mixer Isolation			
f_L at R	40 dB		3 - 100 MHz
f_L at I	40 dB		
f_L at R	30 dB		100 - 1000 MHz
f_L at I	20 dB		

*These specifications apply to a mixer used in a 50-ohm system with an f_L source of +7 dBm available. A short circuit at the I-port for the unwanted sideband will usually improve CL and NF by 0.5 dB. The 1000 MHz upper frequency range may be extended to 1200 MHz by ordering option 11 (M1A-11).

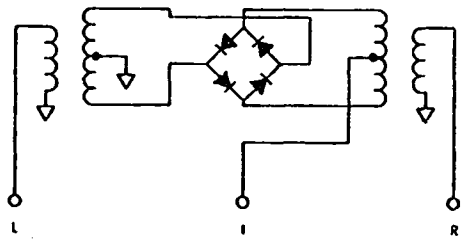
Weight 45 grams (1.6 oz.) maximum

Connectors BNC, TNC, SMA

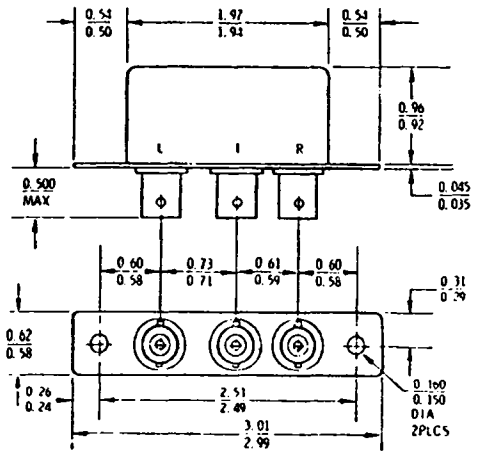
Absolute Maximum Ratings

Storage
Temperature ....−65°C to +100°C
Operating
Temperature ....−54°C to +100°C
Peak Input Power .....50 mW
Peak Input Current .....50 mA

Schematic Diagram



Outline Drawing



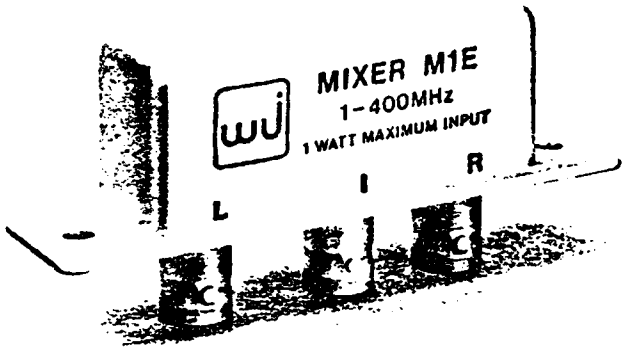
NOTE: DIMENSIONS ARE IN INCHES.

WJ-M1E

DOUBLE-BALANCED MIXER

LO, RF } 1 TO 400 MHz
IF DC TO 400 MHz

- HIGH-INTERCEPT POINT: 32.5 dBm (TYP.)
- LOW NOISE FIGURE: 6 dB (TYP.)
- HIGH-LEVEL INPUT: +20 dBm
- RFI SHIELDED



Guaranteed Specifications[1]

Characteristics	Min.	Max.	Test Conditions
SSB Conversion Loss		6.0 dB	f_L & f_R 2 to 50 MHz f_I 2 to 100 MHz
SSB Conversion Loss		7.5 dB	f_L & f_R 1 to 100 MHz f_I dc to 200 MHz
SSB Conversion Loss[2]		9.0 dB	f_L & f_R 1 to 400 MHz f_I dc to 400 MHz
SSB Noise Figure		6.0 dB	f_L & f_R 2 to 50 MHz f_I 2 to 100 MHz
SSB Noise Figure		8.0 dB	f_L & f_R 1 to 100 MHz f_I 0.4 to 200 MHz
SSB Noise Figure[2]		9.5 dB	f_L & f_R 1 to 400 MHz f_I 2 to 400 MHz
Isolation			
f_L at R	45 dB		f_L 1 to 30 MHz
f_L at I	50 dB		
f_L at R	35 dB		f_L 30 to 100 MHz
f_L at I	40 dB		
f_L at R	25 dB		f_L 100 to 400 MHz
f_L at I	25 dB		
f_R at I	25 dB		f_R 1 to 400 MHz
Conversion Compression		1.0 dB	f_R = +20 dBm
Desensitization Level		1.0 dB	f_{R2} = +18 dBm
Third Order Two-Tone Intermodulation Distortion		60.0 dB	f_L = 350 MHz at +27 dBm f_{R1} = 320 MHz at 0 dBm f_{R2} = 321 MHz at 0 dBm

NOTES:
1. These specifications apply to a mixer used in a 50 ohm system with an f_L source of +27 dBm available. An f_L level of +30 dBm will improve the conversion compression and desensitization level with typically less than 0.5 dB increase in noise figure. A short circuit at the I-port for the unwanted sideband will usually improve the CL and NF by 0.5 dB.
2. For f_R 1-200 MHz, f_I can extend from DC to 500 MHz for the same specifications.

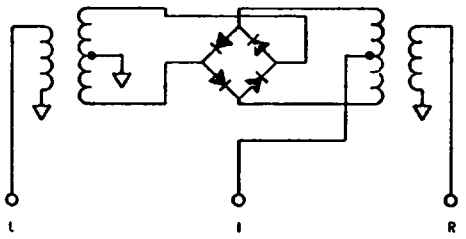
Weight 62.4 gms (2.2 oz.) maximum

Connectors BNC, TNC, SMA

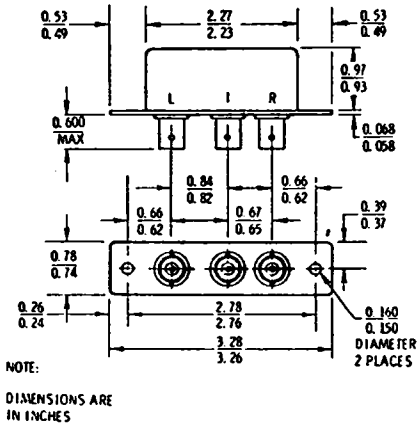
Absolute Maximum Ratings

Storage
Temperature .....−65°C to +100°C
Operating Temperature
+27 dBm
LO power .....−54°C to +71°C
+24 dBm
LO power .....−54°C to +100°C
Maximum Input Power for any single port .....1 watt RMS
2 watts peak
Maximum Total Input Power for all ports .....1.5 watts RMS
3 watts peak

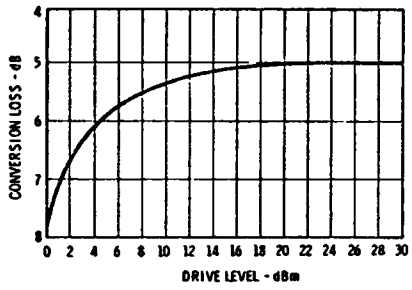
Schematic Diagram



Outline Drawing

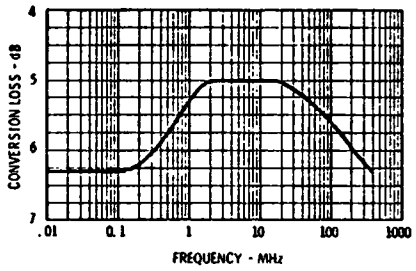


Typical Performance at 25°C

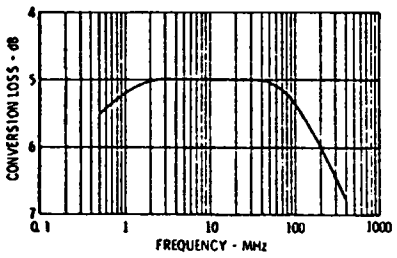


Drive Level: The minimum recommended drive level is +20 dBm.

The maximum recommended drive level is +30 dBm.



Conversion Loss vs. IF Frequency: The frequency ordinate refers to the output f_I with f_R at 50 MHz. Data plotted with an f_L level of +27 dBm.



Conversion Loss vs. Input Frequency: Conversion loss of the mixer when used in an SSB system. The frequency ordinate refers to the inputs f_L and f_R with f_I at 20 MHz for conversion loss measurements. Data plotted with an f_L level of +27 dBm.

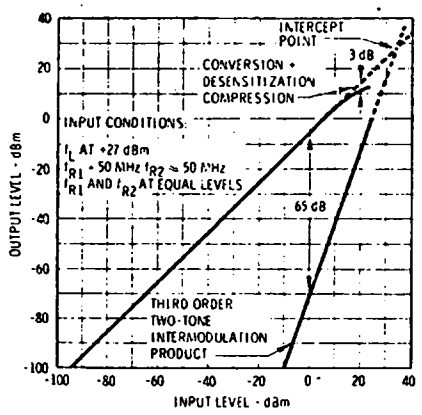
A 1 dB improvement in conversion loss can be made at 400 MHz by reversing the I and R ports ie. by feeding the input signal into the I port and taking the output from the R port. At lower frequencies this performance improvement is not as significant. At 100 MHz, there is a 0.2 dB improvement while at 50 MHz and below there is no improvement.

WJ-M1E

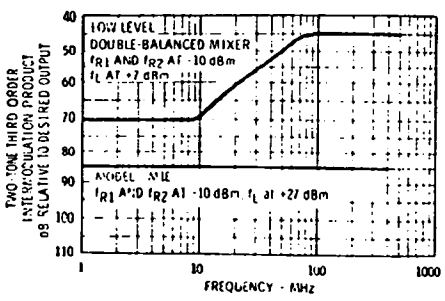
continued

Typical Two-Tone Performance at 25°C

Two-Tone Suppression vs. Input Level: With each dB decrease in input level, the 3rd order product is decreased an additional 2 dB. As shown, the WJ-M1E will reduce third-order products 65 dB with both input signals at 0 dBm and 85 dB with both input signals at −10 dBm. The input intercept point for the WJ-M1E is at +32.5 dBm. This is 19 dB higher than the intercept point for a low-level double-balanced mixer like the WJ-M1. The 3 dB compression shown on the graph is a combination of both conversion compression and desensitization.



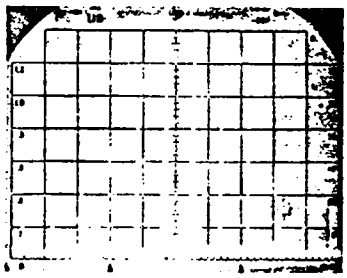
Two-Tone Suppression vs. Input Frequency: The two-tone performance of the WJ-M1E is constant across its frequency range. Other mixers, even other high level mixers, have a degradation in performance about 10 MHz.



Typical Two-Tone Performance Compared to a Well-Balanced, Low-Level Double-Balanced Mixer: In the spectrum analyzer photos below the WJ-M1E is compared to the WJ-M1 Double-Balanced Mixer under similar input conditions. The input conditions were as follows:

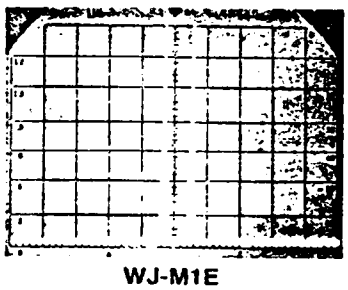
f_L = 352 MHz, f_{R1} = 322 MHz at 0 dBm, f_{R2} = 320 MHz at 0 dBm. Horizontal Scale: 2.5 MHz/cm, centered at ≈ 31 MHz. Vertical Scale: 10 dB/cm.

WJ-M1: With a +7 dBm f_L pump signal, the well-balanced WJ-M1 suppresses many of the two-tone spurs. However, there are still a number of relatively unsuppressed products.



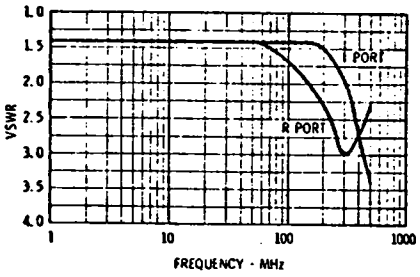
WJ-M1

WJ-M1E: With a +27 dBm f_L pump signal, the WJ-M1E virtually eliminates all two-tone products from the 60 dB spectrum.

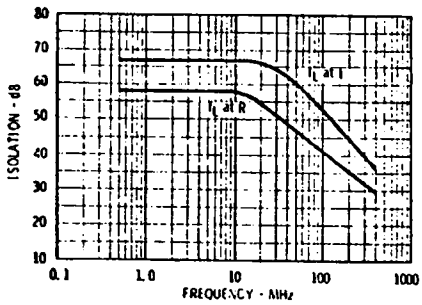


WJ-M1E

VSWR vs. Frequency: VSWR of the R and I ports in a 50-ohm system with f_L = 400 MHz at +27 dBm. Some variation in the I and R port VSWR will occur as a function of the L port frequency. The L port VSWR is typically less than 2.0 to 1 across its 1 to 400 MHz frequency band.



Isolation vs. Frequency: Level of the f_L signal fed through to the R- and I-ports with respect to the level of the f_L signal at the L-port. Maximum isolation can be obtained between the input signals by feeding the input signal (f_R) into the I port with some sacrifice in two-tone performance.



Typical Intermodulation Performance at 25°C

Intermodulation Signal Levels: Intermodulation signals resulting from the mixing of harmonics of the input signal are shown in the table below for the WJ-M1E. Mixing products are indicated by the number of dB below the $f_L \pm f_R$ output. The typical performance in the shaded portion of the table was obtained with f_L and f_R at approximately 50 MHz, f_L at +27 dBm, f_R at 0 dBm, and all resistive terminations. The typical performance in the other portion of the table was obtained under the same conditions as the shaded portion, but with f_R at −10 dBm. Note the improvement in suppression, especially with the higher order products of f_R, when the f_R level is reduced. Improved performance can also be achieved at lower frequencies.

For best suppression of f_R harmonics ≥2, an f_L level of +30 dBm is recommended. For best suppression of f_R harmonics <2, an f_L level less than +27 dBm but not less than +20 dB is recommended.

Harmonics of f_R	0	1	2	3	4	5	6	7	8
7	>99	>99	>99	>99	>99	>99	>99	>99	>99
	>90	>90	>90	>90	>90	>90	>90	>90	>90
6	>99	>99	>99	97	>99	>99	>99	>99	98
	>90	>90	>90	>90	>90	>90	>90	>90	>90
5	>99	96	>99	95	>99	>99	>99	90	>99
	>90	>90	>90	>90	>90	>90	>90	>90	>90
4	88	91	>99	92	90	95	87	94	87
	>90	>90	>90	>90	>90	>90	>90	>90	>90
3	81	73	85	69	85	68	85	64	87
	>90	>90	>90	>90	>90	>90	>90	89	>90
2	64	71	62	70	63	70	61	62	64
	73	83	75	79	80	80	77	82	79
1	24	0	35	11	42	19	50	39	49
	24	0	34	11	42	18	49	37	49
0		29	20	32	24	29	27	30	29
		18	10	23	14	19	17	21	19

Harmonics of f_L

Identification of "in-band" products: When single tones are fed into a mixer, the identification of intermodulation products in the output passband is rather simple. However, when the L-port is being swept or the R-port is wideband, the complexity of the analysis is magnified.

To assist design engineers with this analysis WATKINS-JOHNSON has developed a computer program that calculates which products occur in a specified output band. An example of this calculation is shown below where an f_L signal of 45 ± 3 MHz is mixed with an f_R signal of 55 ± 3 Mz. The output passband is 100 ± 6 MHz and intermods were computed up to the 11th order. The analysis shows the following products are in-band.

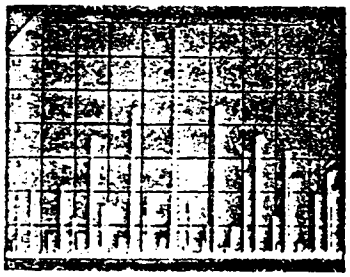
Check with your WATKINS-JOHNSON applications engineer for further information on this customer service.

f_L Multiple	f_R Multiple	Lower Limit (MHz)	Lower Limit (MHz)
2	0	84.0	96.0
2	0	84.0	96.0
1	1	94.0	106.0
0	2	104.0	116.0
5	−2	94.0	136.0
−3	4	64.0	106.0
6	−3	78.0	132.0
−4	5	68.0	122.0
7	−4	62.0	128.0
−5	6	72.0	138.0

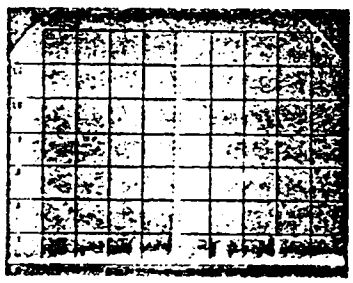
Typical Intermodulation Performance Compared to a Well-Balanced, Low Level Double-Balanced Mixer: In the spectrum analyzer pictures below the WJ-M1E is compared to the WJ-M1 Double-Balanced Mixer under the following similar input conditions:

f_{R1} = 45.6 MHz at −10 dBm, f_{R2} = 27.8 MHz at −2 dBm, f_{R3} = 26.6 MHz at −2 dBm, f_L = 50 MHz. Horizontal Scale: ≈ 2 MHz/cm, centered at 95.6 MHz. Vertical Scale: 10 dB/cm.

With a +7 dBm pump signal, many of the WJ-M1 Mixer generated products are still present. However, the WJ-M1E suppresses the products by an additional 40 dB with a +27 dBm pump signal.



WJ-M1



WJ-M1E

MODULE L21A SYNTHESIZER PHASE-LOCK EMERGENCY POWER

1.0 DESCRIPTION

The L21 Module contains two sets of "Gel Cell" batteries to provide backup power to the L17 modules. The batteries are trickle charged at 20.7 VDC from the L17 A1 voltage regulator assembly. In the event of rack power failure, the batteries supply power to the HP crystal oscillator ovens to remain warm and thus enabling the L17 modules to regain lock immediately upon return of rack power.

2.0 CIRCUIT DETAILS

Circuit details are given in Schematic C13220S10A.

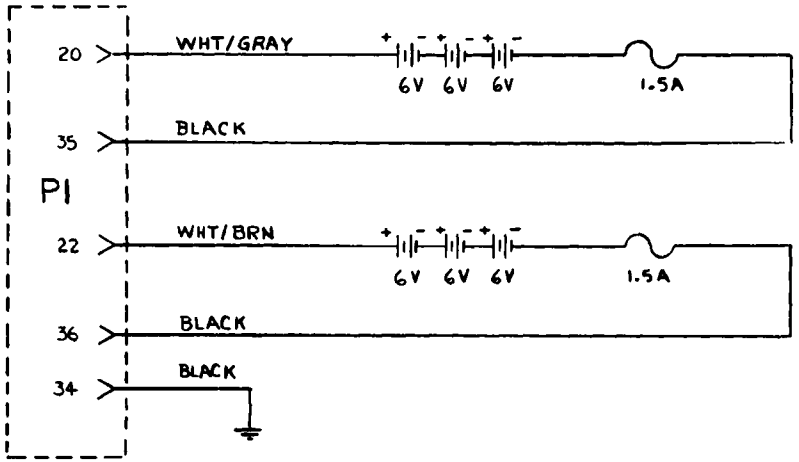
3.0 DRAWING LIST

The L21 Drawing List is given in Figure 3.1.

4.0 BILL OF MATERIALS

The L21 bill of materials is given in A13220Z7.

REV	DATE	DRAWN BY	APPR'D BY	DESCRIPTION
A	11/4/80			BATTERIES WERE DRAWN AS 2 VOLTS, DWG ERROR



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NE[redacted] ON

VLA PROJECT: L21

TITLE: SYNTHESIZER PHASELOCK EMERGENCY POWER SCHEMATIC

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE 11/3/80
DESIGNED BY | DATE 11/4/80
APPROVED BY | DATE

[redacted] SHEET NUMBER [redacted] DRAWING NUMBER 2051[redacted] REV A

SYNTHESIZER PHASE LOCK EMERGENCY POWER (L21) DRAWING LIST

Project No. 13220 11/13/80

	Number	Revision
Schematics		
Synthesizer Phase-Lock Emergency Power	C13220S10	A
Mechanical Drawings		
Battery Clamp	B13220M12	
Panel, Front	C13220M24	
Side Plate (Modified)	D13220M27	
Bill Of Material		
Synthesizer Phase-Lock Emergency Power	A13220Z7	

Figure 3.1

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

[X] ELECTRICAL [ ] MECHANICAL BOM # A13220Z7 REV _____ DATE 1-17-78 PAGE 1 OF 3

Synthesizer Phaselock

MODULE # L21 NAME Emergency Power DWG # D13220P10 SUB ASMB _____ DWG # _____

SCHEMATIC DWG # C13220S10 LOCATION _____ QUA/SYSTEM _____ PREPARED BY Cote APPROVED _____

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		NRAO	A13220Z7			
2		NRAO	B13050M4	Guides	4	
3		NRAO	B13050M18	Side Plate	1	
4		NRAO	D13220M27	Side Plate (MOD)	1	
5		NRAO	C13050M23	Bar Supports	4	
6		NRAO	C13210M4	Rear Panel	1	
7		NRAO	C13220M24	Front Panel	1	
8		NRAO	C13050M22-1	Perforated Cover	1	
9		NRAO	B13220M12	Battery Clamp	2	
10						
11						
12						
13		Globe	GC620	Gel/Cell rechargeable battery 6-volt, 2 AMP HR	6	
14		Littlefuse Int'l.	281006	Fuse Holder	2	
15		Amatom	8233SS0632	Spacer, Hexagon	4	

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

[X] ELECTRICAL [ ] MECHANICAL BOM # A1322027 REV _____ DATE 1/17/78 PAGE 2 OF 3

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
16	P1	AMP Special Indust.	601488-4	42 Pin Mod Conn (Pre Asm)	1	
17		" " "	200833-4	Guide Pin	1	
18		" " "	203964-6	Guide Socket	2	
19		" " "	202514-1	Ground Guide Pin	1	
20		AMP Special Indust.	202394-2	Conn Shield	2	
21			#4-40	Solder Lug	1	
22		Wilshire Electronics	S1187	Terminal Solderless Female	12	
23						
24						
25		Southco	47-11-204-10	Captive Screw	4	
26						
27			6-32 x 5/8	Screw, Pan Hd Slotted SS	4	
28			6-32 x 7/8	Screw, Pan Hd Slotted SS	4	
29			6-32 x 1/2	" " " " "	8	
30			6-32 x 1/4	Screw, Flat Hd, Slotted SS	14	
31			6-32 x 1/2	" " " " "	8	
32			6-32 x 3/8	Screw, Flat Hd Crossed Recessed SS	4	

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

[X] ELECTRICAL [ ] MECHANICAL BOM # A1322027 REV _____ DATE 1/17/78 PAGE 3 OF 3

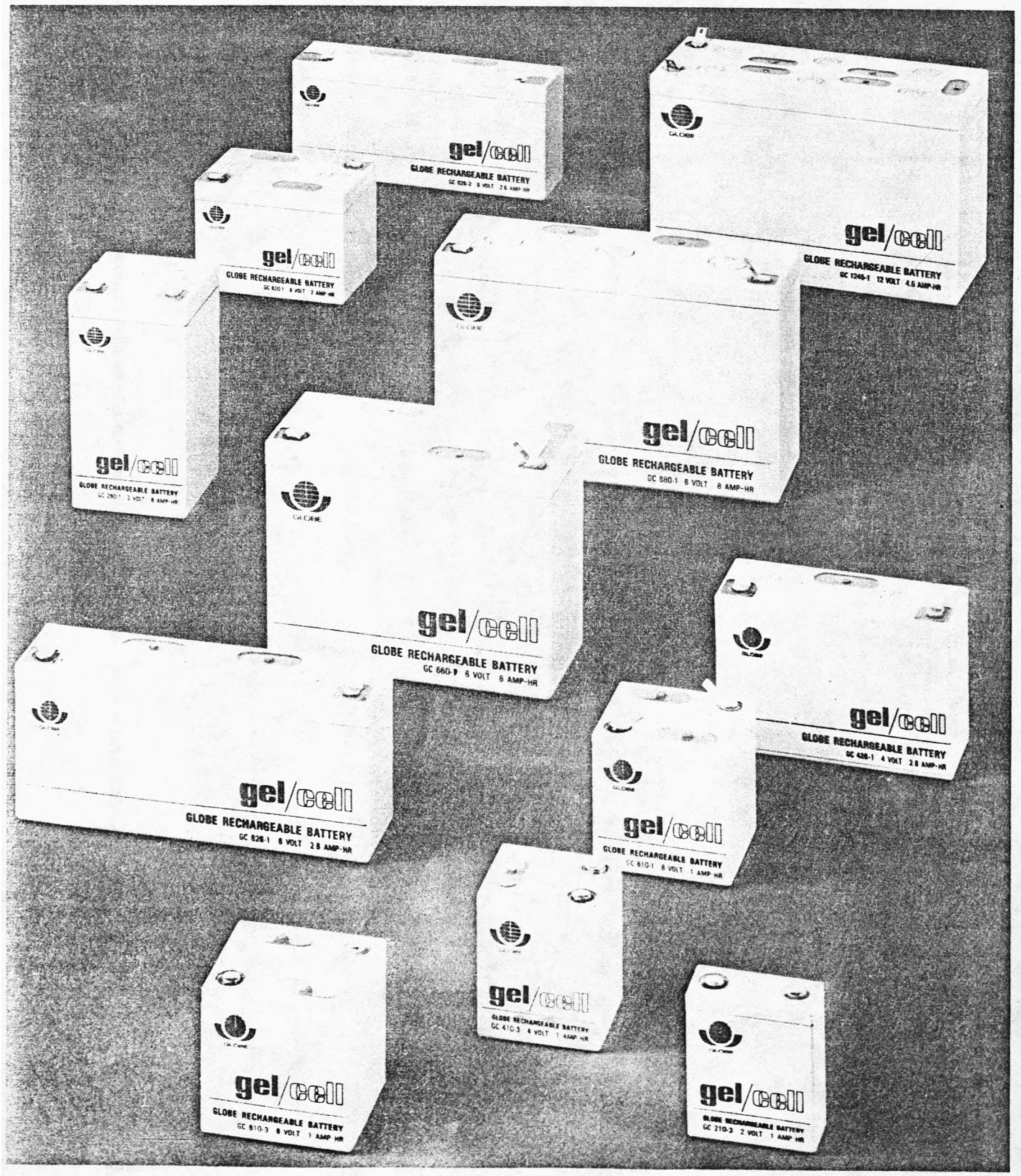
ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
33						
34			6-32 x 1/4	Screw, Hex Hd Socket Cap SS	2	
35			6-32	Lockwasher, Flat, Int Tooth	2	
36						
37			#18 AWG	Hookup Wire, Black, Stranded	As req'd	
38			#18 AWG	Hookup Wire, Wht/Gray, Stranded	As req'd	
39			#18 AWG	Hookup Wire, Wht/Brn, Stranded	As req'd	

5.0 DATA SHEETS

The Data Sheets for the "Gel Cell" type GC 620 Battery are presented.

GLOBE

gel/cell RECHARGEABLE BATTERIES



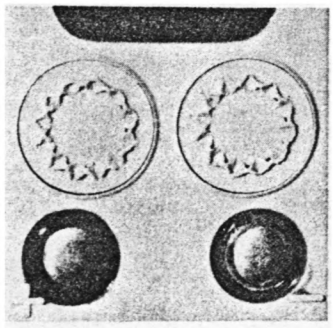
GEL/CELL SPECIFICATIONS

BATTERY PART NO.	NOMINAL VOLTAGE	NOMINAL CAPACITY @ 20 HR. RATE	DISCHARGE CURRENT @ 20 HR. RATE	WEIGHT (LBS.)	DIMENSIONS (INCHES) LENGTH	WIDTH	HEIGHT (over terminal)	POWER TO WEIGHT RATIO (watt-hours/ pound)	POWER TO VOLUME RATIO (watt-hours/ cubic inch)	INTERNAL RESISTANCE OF CHARGED BATTERY (approx. milliohms)
GC 210	2 V.	.9 AH	45 MA	.19	1.65"	.72"	2.0"	9.5	.76	30
GC 410	4 V.	.9	45	.37	1.65	1.36	2.0	9.7	.81	60
GC 610	6 V.	.9	45	.55	2.0	1.65	2.24	9.8	.83	90
GC 620	6 V.	1.8	90	.97	2.95	2.00	2.36	11.1	.88	50
GC 426	4 V.	2.6	130	.86	3.54	1.34	2.63	12.1	.94	45
GC 626	6 V.	2.6	130	1.34	5.28	1.34	2.63*	12.0	.94	70
GC 1245	12 V.	4.5	225	4.5	5.95	2.52	4.01	12.0	.96	40
GC 660	6 V.	6.0	300	2.6	4.55	1.97	3.81	13.9	1.1	25
GC 280	2 V.	7.5	375	1.1	2.06	1.97	3.97	13.7	1.0	6
GC 680	6 V.	7.5	375	3.3	5.96	1.97	3.97	13.6	1.1	20

* DEDUCT .27" for "–2" terminal

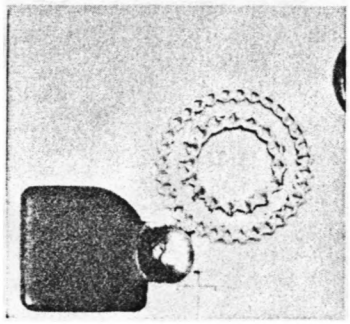
TERMINALS:

Three styles of terminals are used. They are illustrated below. For ordering and identification purposes the terminal style is added as a suffix to the battery part number.



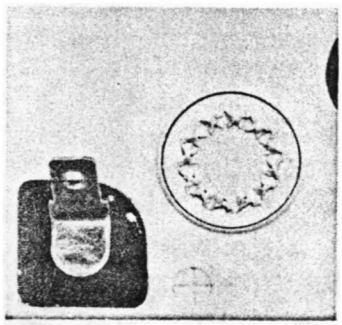
"-3" BUTTON CONTACT

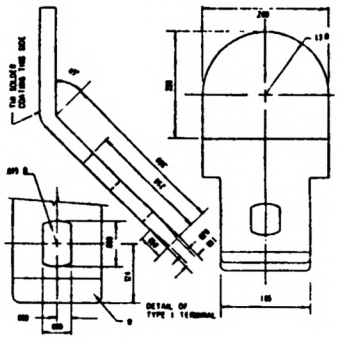
Used only on GC 210-3 and GC 410-3 batteries. Mates with spring loaded type contacts.



"-2" FLAT CONTACT

Used only on GC 626-2 battery. Mates with spring loaded type contacts.





"-1" QUICK-DISCONNECT OR SOLDER LUG

This is the standard terminal. It is used on all batteries except GC 210-3, GC 410-3 and GC 626-2. It mates with AMP, INC. FASTON "187" Series (for .032" tab) receptacle or equivalent.

GLOBE

gel/cell RECHARGEABLE BATTERIES

SIGNIFICANT FEATURES OF THE GLOBE "GEL/CELL" RECHARGEABLE BATTERY

1. **GELLED ELECTROLYTE:** An exclusive, patented gelled electrolyte is used. There is no liquid of any kind to splash around or ooze out. Internally, the battery is drier than a dry cell. Externally, the battery is completely sealed.

2. **RECHARGEABLE:** The "GEL/CELL" battery can be recharged again and again, 100 to 400 or more complete charge/discharge cycles, depending on type of charger used. If the battery is not completely discharged during each cycle, 1000 or more cycles of operation are possible.

3. **LONG-LASTING:** An ideal battery for stand-by service. When "floated" at a constant voltage of 2.25 volts per cell, the GEL/CELL can be maintained for years and will automatically recharge itself—always ready for any power outage.

4. **MAINTENANCE FREE:** Water or electrolyte is never added. Battery is sealed. No need to check liquid levels or perform other routine maintenance.

5. **SMALL SIZE AND WEIGHT:** Compact construction and high power-to-weight ratio make the GEL/CELL battery ideal as a self-contained portable power pack. Perfect for building into transportable equipment such as tape recorders, TV sets, medical apparatus and test instruments.

6. **USE AND RECHARGE IN ANY POSITION:** The GEL/CELL battery can be permanently installed upside down or on its side with no loss of capacity or danger of leakage. Even when tilted or inverted, full capacity is obtained because the gelled electrolyte does not flow away from the plates, exposing the active material, as happens with wet or bound electrolyte type batteries.

7. **LONG SHELF LIFE:** Because of special calcium grids, GEL/CELL batteries lose very little capacity when in storage. The stand loss ranges from 2 to 3% per month at room temperature to 10 to 12% at 95° F and less than 0.5% at 0° F. Other common battery systems lose as much as 20-40% each month at room temperature. This extremely low self-discharge rate means GEL/CELL batteries stay fresh longer and can be used directly out of stock without first being charged.

8. **NO PERMANENT CELL REVERSAL:** Even if the battery is totally discharged due to an extended power outage or because equipment is accidentally left "on", there is no danger of permanent cell reversal or loss of ability to recharge.

9. **WIDE OPERATING TEMPERATURE RANGE:** Can be used in the Tropics or outdoors in the coldest climates. A fully charged battery will operate over a temperature range of -76° F to +158° F (-60° C to +70° C). Batteries are rated at 68° F (20° C). Capacity increases above this temperature and decreases below this temperature. For example, when discharged at 140° F and at a rate of 400 ma, a GC 680, 8 ampere-hour battery will deliver 114% of capacity; at -60° F it will deliver 25% of capacity.

10. **HIGH DISCHARGE RATE CAPABILITY:** The GC 680 battery will deliver up to 80 amperes continuously—higher currents intermittently. Even the little GC 210 battery will put out approximately 15 amperes continuously for one minute.

11. **SERIES OR PARALLEL CONNECTION:** GEL/CELL batteries may be connected in series to obtain any multiple of 2 volts or in parallel to obtain other than standard capacities.

12. **HIGH IMPACT POLYSTYRENE CASE:** Metal cased batteries cause electrical short circuits; they rust and promote the corrosion of nearby components—not the GEL/CELL! The plastic case is non-conductive and chemically neutral. It will not rust or deteriorate nor will it support fungus or other organic growth.

13. **ABSOLUTELY SAFE:** If an excessive pressure build-up should ever occur within the GEL/CELL because of abnormally high recharge currents, patented "one-way" relief valves immediately release the pressure—then automatically reseal. Only clean, dry gas is released. No corrosive fumes and no possibility of explosion, rupture, bulges or corrosion.

14. **EASE OF SHIPMENT:** Sealed construction permits parcel post or air shipment. There is no need for special precautions, expensive containers, warning labels or slow means of transportation.

15. **HIGHLY DEPENDABLE:** The 2 volts-per-cell open circuit voltage of the GEL/CELL is the highest for any commerically available battery. Fewer cells need be connected in series to get 6 volts, 12 volts, etc., and fewer cells means fewer chances for failure. The GEL/CELL is more reliable both statistically and in fact!

16. **NO MEMORY:** Some battery applications require a battery to undergo short, repetitive periods of use which consume only a small portion of the total battery capacity. Under these cyclical conditions, nickel-cadmium batteries, for instance, forget their actual capacity and become conditioned to deliver only the small amount of power normally required. When called upon to deliver full power, they fail. Not the GEL/CELL battery! It delivers full rated power when you need it, irrespective of the previous use history.

17. **COMPETITIVELY PRICED:** The basic material used in GEL/CELL battery construction is lead. Unlike silver, nickel or cadmium, lead is low cost, readily available, and not subject to Government set asides.

Economical "GEL/CELL" rechargeable batteries combine the power and rechargeability of wet batteries, with the handling ease of dry batteries.

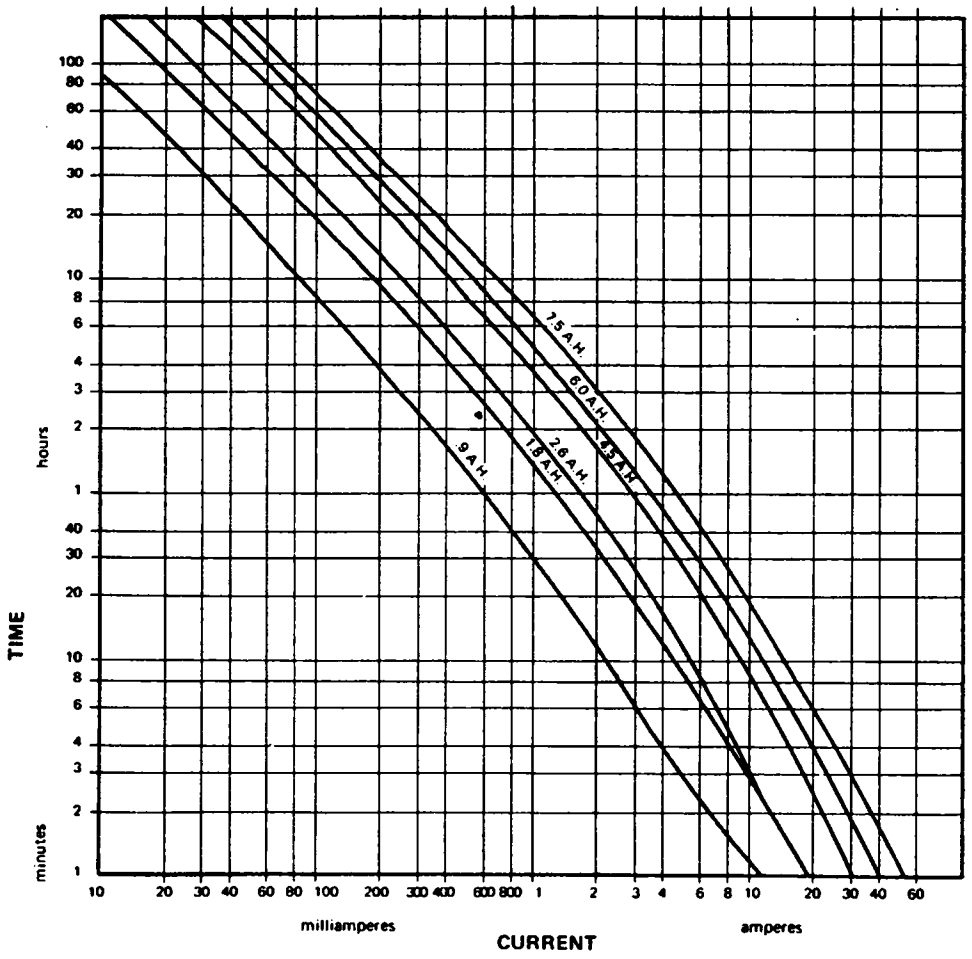
GLOBE

gel/cell

BATTERY SIZE SELECTOR

DISCHARGE TIME AS A FUNCTION OF DISCHARGE CURRENT

The use of this chart will help determine which GEL/CELL battery most closely meets your application needs.



How to choose the correct GEL/CELL battery:

1. Locate required current on the horizontal scale.

2. Locate desired operating time on the vertical scale.

The point where these two lines intersect indicates the needed ampere-hour capacity. The first diagonal line above this intersection represents the smallest GEL/CELL battery that will meet the ampere-hour requirements.

If desired, an operating safety margin can be provided by using a larger battery size than indicated.

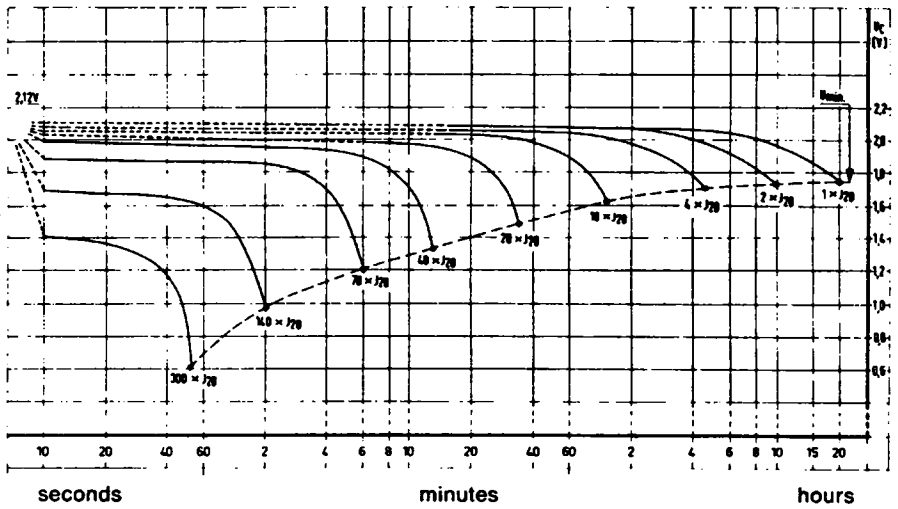
GLOBE Battery Division • GLOBE-UNION INC. • 5757 NORTH GREEN BAY AVENUE • MILWAUKEE, WISCONSIN 53201 • 414 228-2394

GEL/CELL CAPACITY RATINGS

GEL/CELL batteries are rated at the 20 hour rate. The 20 hour rate is abbreviated as "J_{20}" and is defined as that rate of continuous discharge at which the battery will operate for 20 hours before the voltage drops to 1.75 volts per cell, at a temperature of +20° C (68° F).

OPERATING TIME AT DISCHARGE CURRENTS CORRESPONDING TO VARIOUS MULTIPLES OF THE 20 HOUR RATE (J_{20})

.9 A.H. AND 1.8 A.H. BATTERIES

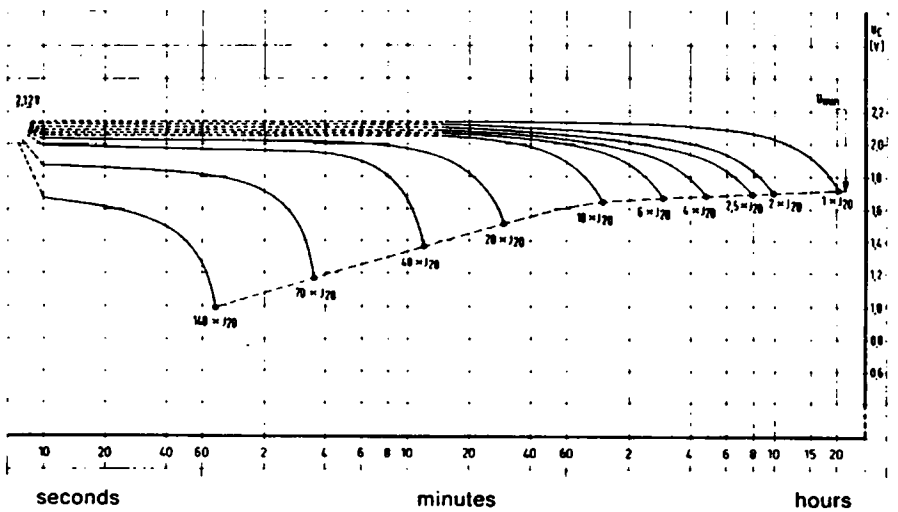


CUT-OFF VOLTAGE (EXPRESSED AS VOLTS PER CELL)

BATTERY PART NO.	RATING	20 HOUR RATE (J_{20})	Selected Discharge Currents (in Amps) Expressed as Multiples of the 20 Hour Rate (J_{20})							
			2 x J_{20}	4 x J_{20}	10 x J_{20}	20 x J_{20}	40 x J_{20}	70 x J_{20}	140 x J_{20}	300 x J_{20}
GC 610, GC 410 GC 210	.9 A.H.	.045 AMP	.090	.180	.450	.900	1.80	3.15	6.30	13.50
GC 620	1.8 A.H.	.090 AMP	.180	.360	.900	1.80	3.60	6.30	12.60	27.00

OPERATING TIME AT DISCHARGE CURRENTS CORRESPONDING TO VARIOUS MULTIPLES OF THE 20 HOUR RATE (J_{20})

2.6 A.H., 4.5 A.H., 6.0 A.H. AND 7.5 A.H. BATTERIES



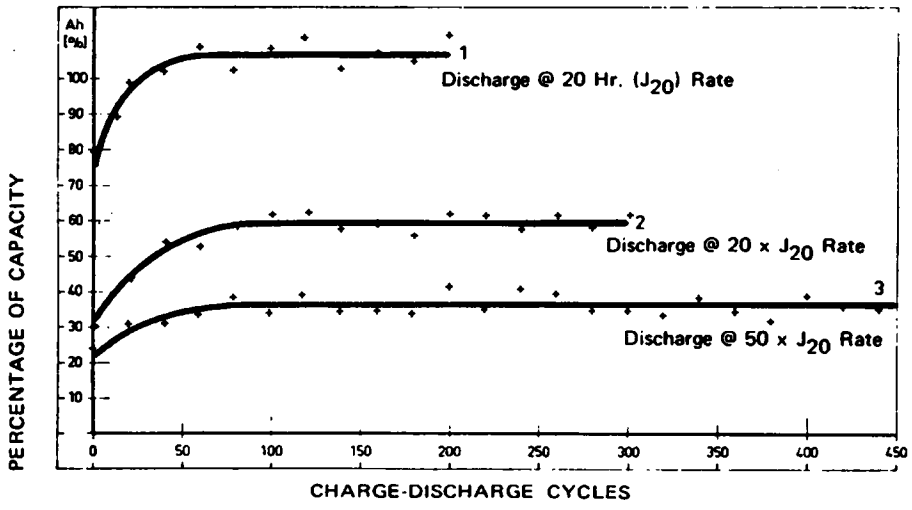
CUT-OFF VOLTAGE (EXPRESSED AS VOLTS PER CELL)

BATTERY PART NO	RATING	20 HOUR RATE (J_{20})	Selected Discharge Currents (in Amps) Expressed as Multiples of the 20 Hour Rate (J_{20})								
			2 x J_{20}	2.5 x J_{20}	4 x J_{20}	6 x J_{20}	10 x J_{20}	20 x J_{20}	40 x J_{20}	70 x J_{20}	140 x J_{20}
GC 626, GC 426	2.6 A.H.	.130 AMP	.260	.325	.520	.780	1.30	2.60	5.20	9.10	18.20
GC 1245	4.5 A.H.	.225 AMP	.450	.562	.900	1.35	2.25	4.50	9.00	15.75	31.50
GC 660	6.0 A.H.	.300 AMP	.600	.750	1.20	1.80	3.00	6.00	12.00	21.00	42.00
GC 680	7.5 A.H.	.375 AMP	.750	.930	1.50	2.25	3.75	7.50	15.00	26.25	52.50

DEVELOPMENT OF CAPACITY

An interesting feature of the Gel/Cell battery is that under cyclical operating conditions (alternate charge and discharge) capacity actually increases with time. In fact, the nominal capacity may not be reached until after 20 or more complete charge/discharge cycles. Once fully developed the capacity is retained over a long period of time.

The figure below illustrates how capacity increases with cyclic operation. It also shows that the increase in capacity occurs sooner if the battery is discharged at a low rate rather than at a high rate. This is because more capacity is taken from the battery at low rates than at high rates and a definite relationship exists between total capacity removed and the rate of capacity increase.

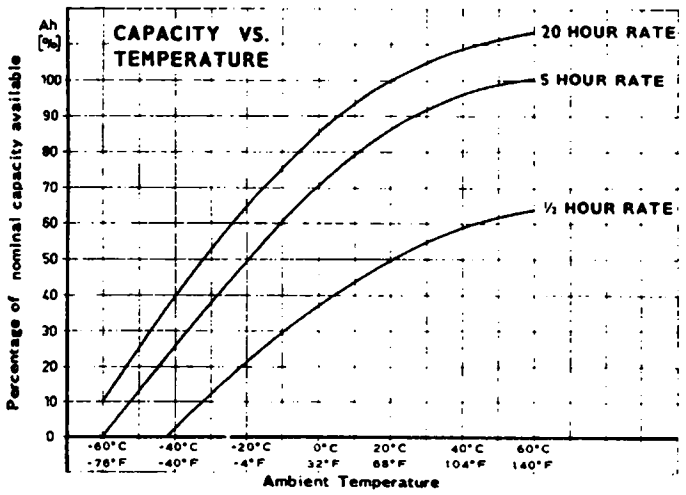


Three (3) examples of increase of capacity during cyclic operation.

EFFECT OF TEMPERATURE ON CAPACITY

Gel/Cell batteries operate over a wide temperature range. The actual capacity available is a function of temperature and rate of discharge. This relationship is shown by the figure below.

Note that batteries are rated at 20°C (68°F). Below this temperature battery capacity decreases. Above this temperature battery capacity increases. At all temperatures, the higher the rate of discharge, the lower the available capacity.



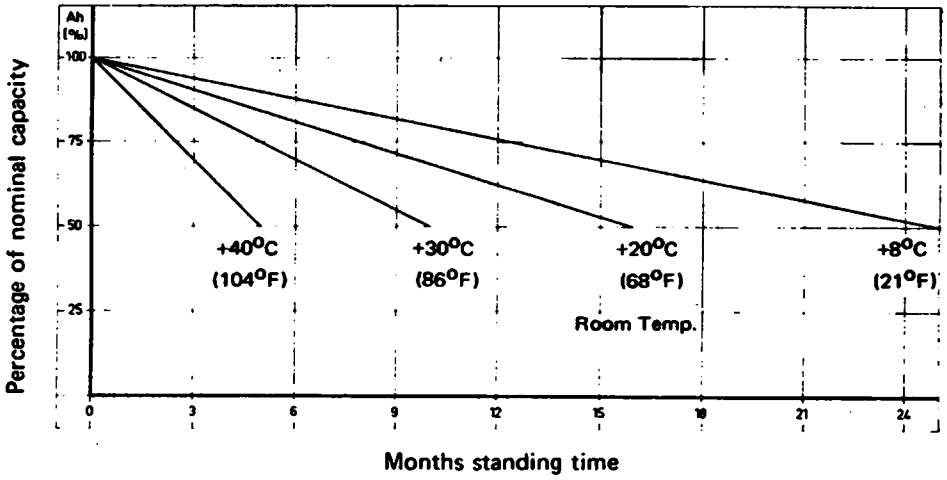
Remember that heat is the enemy of all batteries. Always store batteries at the coolest possible temperature. When designing them into equipment, try to locate them away from heat producing components. As a rule of thumb, it is estimated that battery life is halved for each 20°F increase in ambient over room temperature.

SHELF LIFE

When stored at a mean ambient temperature of +20°C (68°F), Gel/Cell batteries lose only 2 to 3% of their capacity per month. This very low self-discharge is obtained through the use of a special calcium alloy. Because of this favorable property of the Gel/Cell, it is ready for service just as taken from the shelf.

At temperatures below room temperature the self-discharge is even lower than at room temperature. For all practical purposes it can be ignored. Above room temperature the self-discharge increases somewhat; first slowly and then more rapidly. The figure below shows self-discharge as a function of temperature.

SELF-DISCHARGE OF THE GEL/CELL BATTERY AT VARIOUS TEMPERATURES



STORAGE

Batteries should be fully charged before storage. Preferred storage temperature is 70°F or below. Storage at temperatures above 100°F should be avoided.

Batteries stored at room temperature or below should be recharged at least once per year. Higher temperatures require more frequent charging. This boost charge is necessary to insure maximum battery life and performance.

RECHARGING METHODS

1. Limit initial current to 3 times the 20 hour rate (J_{20}). Charge until battery voltage (under charge) reaches 2.4 volts per cell. Hold at 2.4 volts per cell until current drops to approximately:

GC 610, GC 410, GC 210	10-20 ma
GC 620	20-40 ma
GC 626, GC 426	30-60 ma
GC 1245	50-100 ma
GC 660	60-120 ma
GC 680, GC 280	80-160 ma

   Battery is now fully charged. Disconnect charger or switch to float voltage (see 2. below).

2. For "float" or "stand-by" service hold battery across constant voltage source of 2.25 volts per cell continuously. This is considered the "float" voltage. At this voltage, the battery will accept only the current necessary to maintain itself. It will also recharge itself after a power outage.

Method 1 is recommended for applications requiring maximum number of recharge cycles and short recharge time. Method 2 is ideal for alarm systems, emergency lighting and other stand-by power applications where fewer number of charge/recharge cycles are required and recharge time is not critical.

Your request for application assistance will be welcomed by:

Globe Battery Division
GLOBE-UNION INC.
5757 North Green Bay Avenue
Milwaukee, Wisconsin 53201

Telephone (414) 228-2394