VLA TECHNICAL REPORT NO. 47

MODULE T6C BASEBAND CONTROL

W. E. Dumke

December 1980

CONTENTS

FIGURES

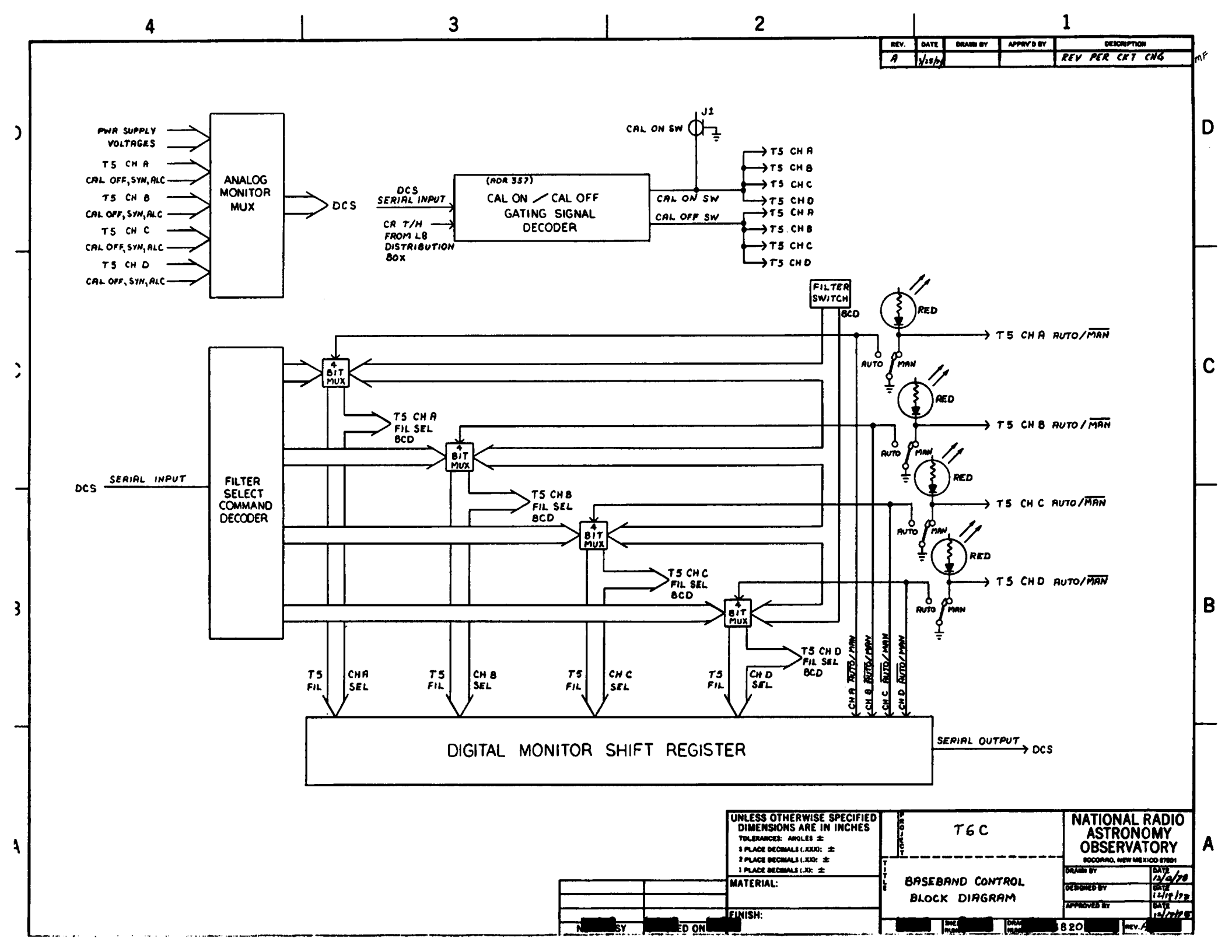
1.0 GENERAL DESCRIPTION

The T6C Baseband Control module serves as an interface for command and monitor data between the T4C Baseband Filter and the T5C Baseband Driver modules and the M1 Data Set module. One T6C module is used for each antenna "D" rack and provides an interface for all four (A, B, C, and D) baseband channels. It also provides for the selection of either manual or automatic gain control independently for each channel. Manual filter selection however, is common to all four baseband channels. The T6C module also provides synchronization and generation of gating signals for the T5C synchronous detectors.

2.0 THEORY OF OPERATION

Operation of the T6C command and monitor system is similar to that of the T6A and B series modules. Refer to Block Diagram C13820B1A.

Input and output of data from the module are controlled by four parallel address lines from the M1 Data set. The address decoder controls the input and output functions of two shift registers through a series of gates. When the appropriate address appears, a 24 bit command word is serially entered into the 24 bit latch. To check the data link the received word can be read back from the command register into the data set if requested by the computer. The 16 least significant bits of the command word contain four sets of four bits which are used to select the required filters in the four T4C baseband filter modules. These four sets of bits enter four two-line to one-line multiplexers, the other inputs to which come from a single front panel BCD thumbwheel switch. The four multiplexers are individually controlled by the four manual/auto front panel switches, so the filter selection of any of the baseband filter modules can either be controlled by the computer or manually, as desired. Under automatic (computer) control the filter selection can be different for each baseband filter module, but in the manual mode the same four bit thumbwheel switch controls all four modules.


4
3
2
1
D
C
B
A
REV. | DATE | DRAWN BY | APPR'D BY | DESCRIPTION
A | 1/28/76 | | | REV PER CKT CHG
PWR SUPPLY VOLTAGES
T5 CH A CAL OFF, SYN, ALC
T5 CH B CAL OFF, SYN, ALC
T5 CH C CAL OFF, SYN, ALC
T5 CH D CAL OFF, SYN, ALC
ANALOG MONITOR MUX
DCS
J1
CAL ON SW
DCS SERIAL INPUT
CR T/H FROM L8 DISTRIBUTION BOX
(ADR 357)
CAL ON / CAL OFF GATING SIGNAL DECODER
CAL ON SW
CAL OFF SW
T5 CH A
T5 CH B
T5 CH C
T5 CH D
T5 CH A
T5 CH B
T5 CH C
T5 CH D
FILTER SWITCH
BCD
RED
T5 CH A AUTO/MAN
AUTO
MAN
RED
T5 CH B AUTO/MAN
AUTO
MAN
RED
T5 CH C AUTO/MAN
AUTO
MAN
RED
T5 CH D AUTO/MAN
AUTO
MAN
DCS
SERIAL INPUT
FILTER SELECT COMMAND DECODER
4 BIT MUX
T5 CH A FIL SEL BCD
4 BIT MUX
T5 CH B FIL SEL BCD
4 BIT MUX
T5 CH C FIL SEL BCD
4 BIT MUX
T5 CH D FIL SEL BCD
T5 FIL CH A SEL
T5 FIL CH B SEL
T5 FIL CH C SEL
T5 FIL CH D SEL
CH A AUTO/MAN
CH B AUTO/MAN
CH C AUTO/MAN
CH D AUTO/MAN
DIGITAL MONITOR SHIFT REGISTER
SERIAL OUTPUT
DCS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
T6C
BASEBAND CONTROL BLOCK DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DESIGNED BY
APPROVED BY
DATE 12/9/75
DATE 12/17/75
DATE 12/22/75
REV. A

From the monitor shift register, a word can be read back into the DCS system. The 16 least significant bits of the monitor register input are connected to the multiplexer output lines to show the filter select signals actually being used and the four most significant bits indicate the state of the four front panel Manual/Auto switches. These four switches also select the ALC voltages applied to the ALC amplifier in the T5C Baseband Driver modules. The ALC voltages are either the output of the ALC loop amplifier or the front panel manual gain adjust potentiometer of the T5C Baseband Driver modules.

In the automatic position, the corresponding T5C Baseband Driver has its gain controlled from the output of the ALC loop amplifiers, and the corresponding T4C Baseband Filter has its filter selected from the DCS system.

The baseband control module also has analog multiplexers which permit any one of 24 differential input voltages to be monitored by the data set. These multiplexers are controlled by the same four address lines, with two seperate data strobes, that control the input and output of the digital data. The inputs to the multiplexers include ALC (Automatic Level Control), Cal Off (noise power at output of T5C module when the front end calibration noise source is turned off), synchronous detector output voltage, and T6C module power supply voltages. The last being reduced by resistive dividers when greater than ten volts positive or less than ten volts negative.

3.0 CIRCUIT DETAILS

3.1 A1 Card

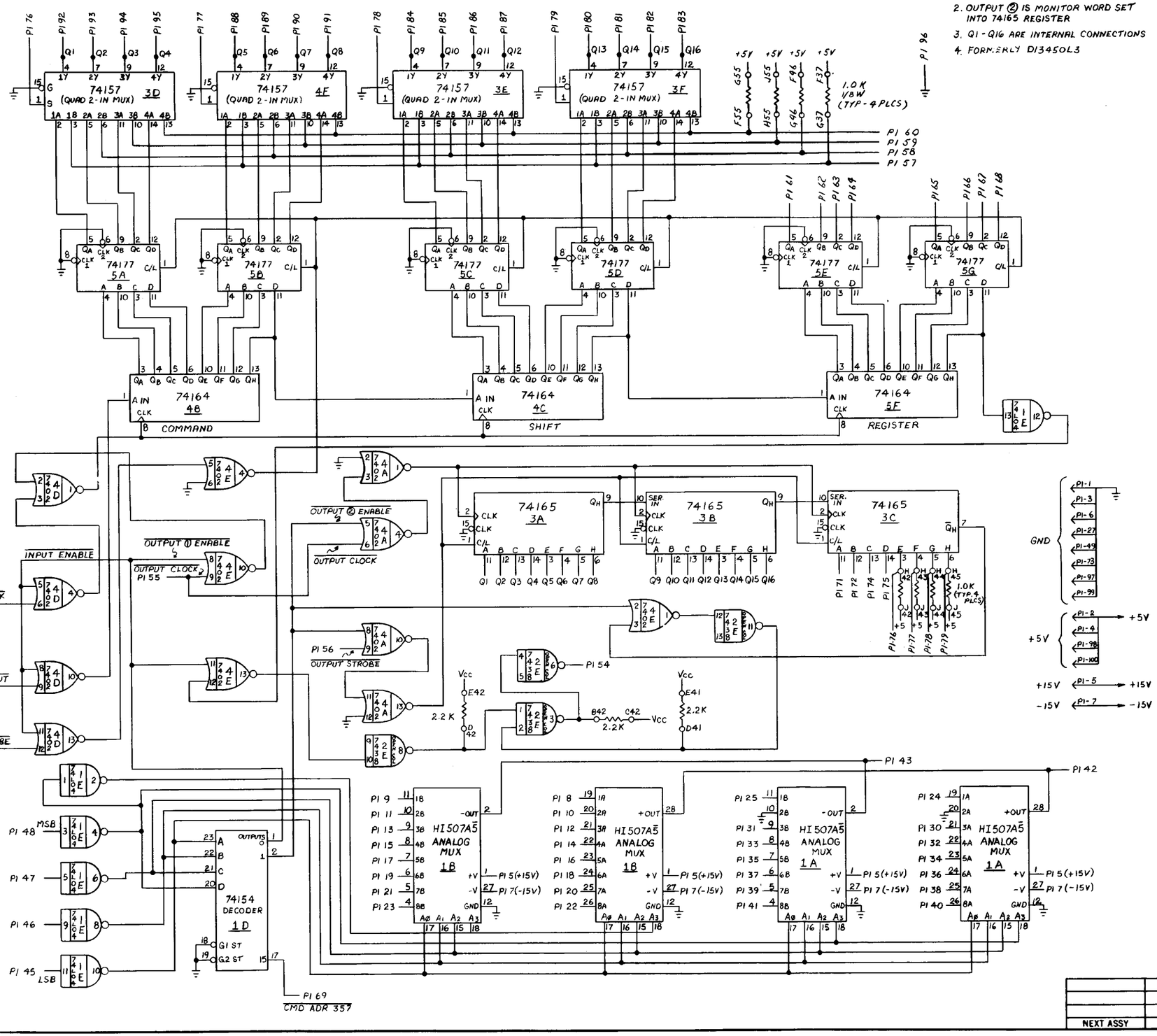
A complete logic diagram is shown in Figure 3.1. All active components are mounted on a 4" x 6½" wirewrap card. Switches and LED's are mounted on the front panel of the module and resistive dividers used in voltage monitoring are mounted on a seperate terminal board.

All inputs from the data set are low-true logic. The input buffers for the four address lines are of the low power type (74L04 inverting gates) to reduce the load on those particular outputs of the data set. The address decoder is a 74154 in a 24 pin package.

8	7	6	5	4	3	2	1

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
D	6/4/79			REV PER CRT CHG

NOTES:
1. OUTPUT ① RETURNS INPUT WORD
2. OUTPUT ② IS MONITOR WORD SET INTO 74165 REGISTER
3. Q1 - Q16 ARE INTERNAL CONNECTIONS
4. FORMERLY D13450L3



CARD	CONN	FUNCTION	DESIGNATION	COLOR	SOURCE
1	B1	GND		BLK	A1 - GND
2	A1	+5V		ORG	P1-C, A2-J1-A1, A1-J1-A2
3	B2	GND		BLK	A1 - GND
4	A2	+5V		ORG	A1-J1-A1, A3 - E11
5	B3	+15V		RED	P1-A, A2-J1-B3, A3-E20
6	A3	GND			
7	B4	-15V		YEL	P1-E, A2-J1-B4, A3-E18
8	A4	1+ ANALOG MUX IN	ALC + CHA 100'+	(ORG) T.P.	P2-A
9	B5	1-	ALC - CHA 100'-	BLK	P2-B
10	A5	2+	ALC + CHB 101'+	ORG	P2-C
11	B6	2-	ALC - CHB 101'-	BLK	P2-D
12	A6	3+	ALC + CHC 102'+	ORG	P2-E
13	B7	3-	ALC - CHC 102'-	BLK	P2-F
14	A7	4+	ALC + CHD 103'+	ORG	P2-H
15	B8	4-	ALC - CHD 103'-	BLK	P2-J
16	A8	5+	CAL OFF + CHA 104'+	PUR	P2-K
17	B9	5-	CAL OFF - CHA 104'-	BLK	P2-L
18	A9	6+	CAL OFF + CHB 105'+	PUR	P2-M
19	B10	6-	CAL OFF - CHB 105'-	BLK	P2-N
20	A10	7+	CAL OFF + CHC 106'+	PUR	P2-P
21	B11	7-	CAL OFF - CHC 106'-	BLK	P2-R
22	A11	8+	CAL OFF + CHD 107'+	PUR	P2-S
23	B12	8-	CAL OFF - CHD 107'-	(WHT) T.P.	P2-T
24	A12	9+	+5V ITERM. BD. 110'+	WH./ORG	A3-E10
25	B13	9- ANALOG MUX IN	GND 110'-	BLK	A1 - GND
26	A13				
27	B14	GND			
28	A14	10+ ANALOG MUX IN	SPARE 111'+		A1-J1-B15
29	B15	10-	SPARE 111'-		A1-J1-A14
30	A15	11+	+15V 2 TERM. BD. 112'+	WH./RED	A3-E1
31	B16	11-	GND TERM. BD. 112'-	BLK	A3-E19
32	A16	12+	-15V 2 TERM. BD. 113'+	WH./YEL	A3-E3
33	B17	12-	GND TERM. BD. 113'-	BLK	A3-E17
34	A17	13+	+28V 4 TERM. BD 114'+	WH./GRAY	A3-E6
35	B18	13-	GND TERM. BD. 114'-	BLK	A3-E14
36	A18	14+	-28V 4 TERM. BD 115'+	WH./GRE.	A3-E8
37	B19	14-	GND TERM. BD. 115'-	BLK	A3-E12
38	A19	15+	SPARE + 116'+		A1-J1-B20
39	B20	15-	SPARE - 116'-		A1-J1-A19
40	A20	16+	SPARE + 117'+		A1-J1-B21
41	B21	16- ANALOG MUX IN	SPARE - 117'-		A1-J1-A20
42	A21	ANALOG MUX OUT (HIGH)	100'-117'+	(WH) → T.P.	P2-MM
43	B22	ANALOG MUX OUT (GND)	100'-117'-	(BLK) → T.P.	P2-NN
44	A22				
45	B23	SMA 0 (LSB)		WH./BRN	P1-M, A2-J1-B23
46	A23	SMA 1		WH./BLU	P1-N, A2-J1-A23
47	B24	SMA 2		WH./PUR	P1-P, A2-J1-B24
48	A24	SMA 3 (MSB)		WH./BLK	P1-R, A2-J1-A24
49	B25	GND			
50	A25				
51	B26	(SERIAL IN) DIG 01		BRN	P1-S
52	A26	(SERIAL IN) CLK 01		PUR	P1-U
53	B27	(SERIAL IN) STR 01		BLU	P1-W, A2-J1-B27
54	A27	(SERIAL OUT) DIG 12		WH./BRN	P1-Y
55	B28	(SERIAL OUT) CLK 12		WH./PUR	P1-a
56	A28	(SERIAL OUT) STR 12		WH./BLU	P1-c
57	B29	MAN. FILTER SEL LSB		WH./BRN	S5-1
58	A29			WH./RED	S5-2
59	B30			WH./YEL	S5-4
60	A30	MAN. FILTER SEL MSB		WH./GRAY	S5-8
61	B31	INPUT WORD BIT 17	SPARE		NC
62	A31	18			
63	B32	19			
64	A32	20			
65	B33	21			
66	A33	22			
67	B34	23			
68	A34	INPUT WORD BIT 24	SPARE		NC
69	B35	CMD ADR 357		PURPLE	A2-J1-B35
70	A35				
71	B36	OUTPUT WORD BIT 17	SPARE		NC
72	A36	OUTPUT WORD BIT 18	SPARE		NC
73	B37	GND			
74	A37	OUTPUT WORD BIT 19	SPARE		NC
75	B38	20	SPARE		NC
76	A38	21	AUTO/MAN SW CH A	WHITE	S1-B
77	B39	22	CH B	PURPLE	S2-B
78	A39	23	CH C	BLUE	S3-B
79	B40	OUTPUT WORD BIT 24	AUTO/MAN SW CH D	WH./BLK	S4-B
80	A40	INPUT WORD BIT 13	FILTER SEL CH D BIT 1 LSB	WH./BRN	P1-V
81	B41	14	2	WH./RED	P1-W
82	A41	15	3	WH./YEL	P1-X
83	B42	16	CH D BIT 4 MSB	WH./GRY	P1-Y
84	A42	9	CH C BIT 1 LSB	WH./BRN	P1-f
85	B43	10	2	WH./RED	P1-h
86	A43	11	3	WH./YEL	P1-k
87	B44	12	CH C BIT 4 MSB	WH./GRY	P1-m
88	A44	5	CH B BIT 1 LSB	WH./BRN	P1-p
89	B45	6	2	WH./RED	P1-r
90	A45	7	3	WH./YEL	P1-t
91	B46	8	CH B BIT 4 MSB	WH./GRY	P1-v
92	A46	1	CH A BIT 1 LSB	WH./BRN	P1-e
93	B47	2	2	WH./RED	P1-g
94	A47	3	3	WH./YEL	P1-j
95	B48	INPUT WORD BIT 4	FILTER SEL CH A BIT 4 MSB	WH./GRY	P1-L
96	A48	PULL UP RESISTOR, FIL. SEL		WH./ORG	S5-C
97	B49	GND			
98	A49	+5V			
99	B50	GND			
100	A50	+5V			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON

PROJECT: T6

TITLE: A1 CONTROL BOARD

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 12/8/78
DESIGNED BY	DATE 12/9/78
APPROVED BY	DATE 12/11/78

SHEET NUMBER 1 of | DRAWING NUMBER D13820L1 | REV. D | SCALE

The control shift register consists of three 74164 serial-in, parallel-out circuits. The input data into this register is controlled by the input enable signal and the output clock. The output when reading back the word is controlled by the output 1 enable signal and the output clock.

The latch consists of six 74177 integrated circuits and the data is loaded into them by the input strobe signal. The four two-line to one-line multiplexers are 74157 integrated circuits. Pull-up resistors are provided on the filter select thumbwheel inputs to insure reliable operation.

The monitor shift register consists of three 74165 parallel-in, serial-out circuits and the data is loaded into them by the output strobe. The shifting out of the data into the data set is controlled by the output 2 signal and the output clock. Digital output circuits to the data set consist of 7438 gates with open connectors which drive a load resistor in the data set.

The analog multiplexer for DCS address 100' through 117' consist of two 507A (Harris Semiconductor) units with balanced inputs and outputs. Input grounds are obtained at the source of the given signal to avoid errors due to ground loops. Note that the two halves of each 507A are shown as seperate blocks in the logic diagram. The voltages connected to the multiplexer inputs along with other DCS address information is given in Section 5.0.

Note that the A1 card is a modification of the logic card in the now obsolete T6A and T6B IF Control modules. The original circuitry has been maintained with minor additions.

Additions include pull-up resistors and the Auto/Man switch monitor inputs and the filter select thumbwheel switch inputs to the command multiplexer. Command address $\overline{357}$' is now extracted from the decoder to be used on the A2 card for the Cal On and Cal Off gating signal synchronization. The A2 card also contains an additional analog voltage multiplexer chip to handle the increase in analog voltage monitoring from the baseband system.

3.2 A2 Card

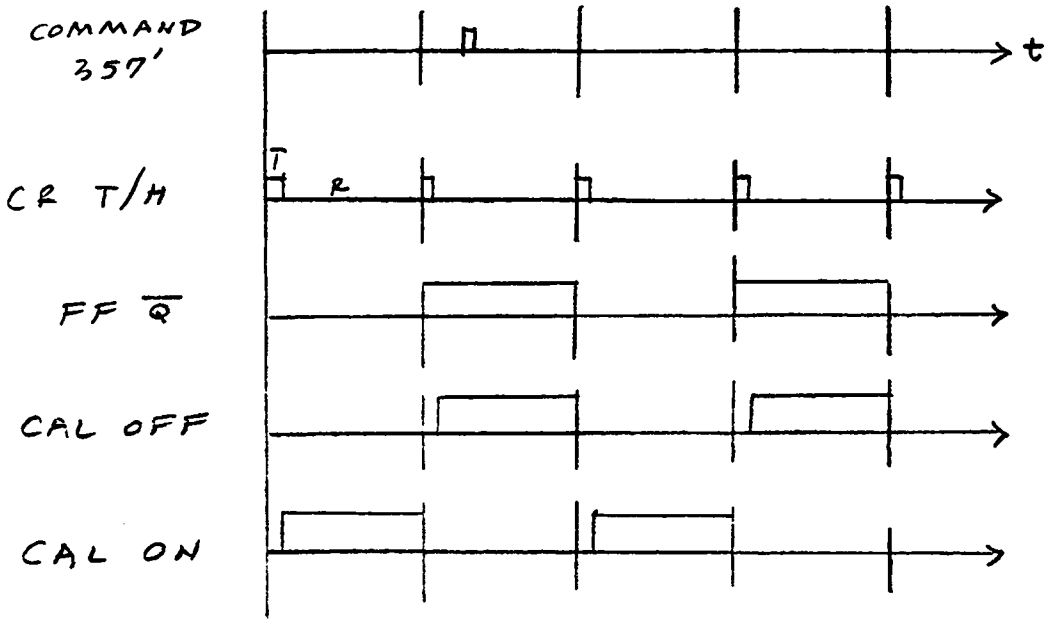
A complete logic diagram is shown in Figure 3.2. The A2 card contains an additional analog multiplexer chip for T5C synchronous detector voltage monitoring in the same configurations as those on the A1 card. A decoder and synchronization circuit provide the Cal On and Cal Off gating signals to the T5C synchronous detector and gated ALC circuit. A diagram of these signals and their relation to system operation is shown in Figure 3.3.

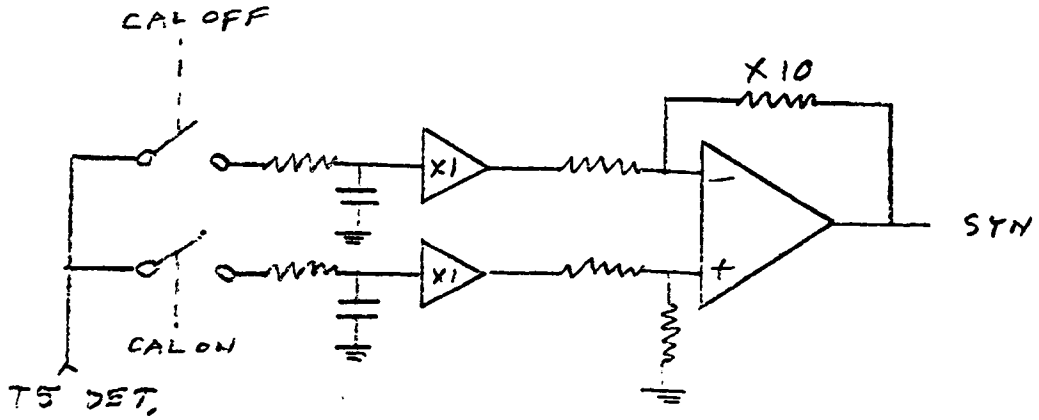
Two problems exist with operation of a synchronous detector at the Central Electronics Room. One problem is the result of the CER modem transmit period (including various switching transients). During the transmit period no antenna IF signals are being received. This transient, while it only occurs for approximately 1 ms out of approximately 50 ms, can have a derogatory effect in a detector system when a maximum error of 0.1% is desired. The ALC circuit would be similarly affected. This problem is solved by utilizing the Central Electronics Room Track and Hold signal to gate both circuits. This signal is only valid when valid IF information is being received.

The other problem involves synchronization of the Central Electronics Room synchronous detector and ALC with the front end noise source that is injected into the front end on every other waveguide cycle, to measure front end effective noise temperature.

In the earlier system only the F4 modules in the front end rack contained a synchronous detector. Therefore, it was trivial to derive a common gating signal for the noise source and the synchronous detector.

In the spectral line retrofit however, the synchronous detector and ALC in the T5C Baseband Driver (after the final analog filtering in the T4C Baseband Filter modules) were required in order to measure the total system effective noise temperature after the communications system and the final analog filtering. This required a system of knowing



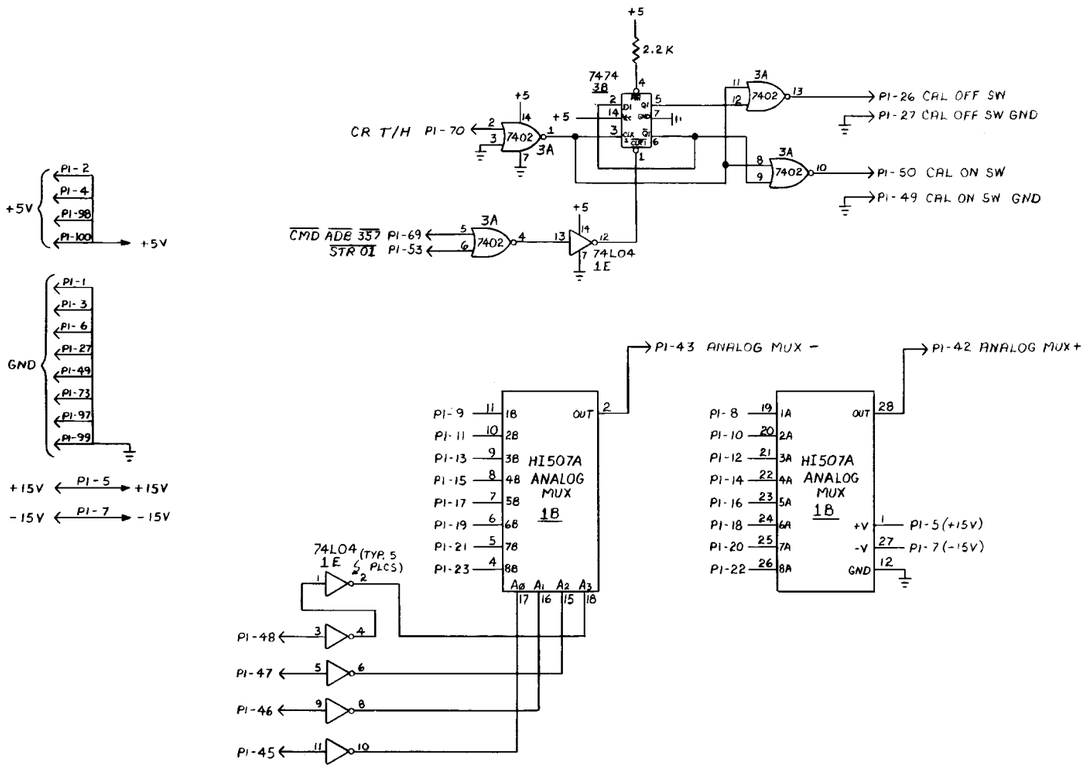


SYNCHRONOUS DETECTOR TIMING

Figure 3.3

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	4/13/78	R Runyan	T. J. P.	CORRECTED DWG ERROR

CARD	CONN	FUNCTION	DESIGNATION	COLOR	SOURCE
1	B1	GND		BLK	A2 - GND
2	A1	+5V		ORG	A1 - J1 - A1
3	B2	GND		BLK	A2 - GND
4	A2	+5V			
5	B3	+15V		RED	A1 - J1 - B3
6	A3	GND			
7	B4	-15V		YEL	A1 - J1 - B4
8	A4	1+ ANALOG MUX IN	SYN + CH A 120'+	(GRN) T. P.	P2 - AA
9	B5	1-	- A 120'-	BLK	P2 - BB
10	A5	2+	+ B 121'+	GRN	P2 - CC
11	B6	2-	- B 121'-	BLK	P2 - DD
12	A6	3+	+ C 122'+	GRN	P2 - EE
13	B7	3-	- C 122'-	BLK	P2 - FF
14	A7	4+	+ D 123'+	GRN	P2 - HH
15	B8	4-	SYN - CH D 123'-	BLK	P2 - JJ
16	A8	5+	SPARE + 124'+	BLK	A2 - J1 - B9
17	B9	5-	- 124'-	BLK	A2 - J1 - A8
18	A9	6+	+ 125'+	BLK	A2 - J1 - B10
19	B10	6-	- 125'-	BLK	A2 - J1 - A9
20	A10	7+	+ 126'+	BLK	A2 - J1 - B11
21	B11	7-	- 126'-	BLK	A2 - J1 - A10
22	A11	8+	+ 127'+	BLK	A2 - J1 - B12
23	B12	8- ANALOG MUX IN	SPARE - 127'-	(BLK) T. P.	A2 - J1 - A11
24	A12				
25	B13				
26	A13	CAL OFF SW	(YEL) →	T. P.	P1 - Z
27	B14	GND	CAL OFF SW GND (BLK) →	T. P.	P1 - AA
28	A14				
29	B15				
30	A15				
31	B16				
32	A16				
33	B17				
34	A17				
35	B18				
36	A18				
37	B19				
38	A19				
39	B20				
40	A20				
41	B21				
42	A21	ANALOG MUX (HIGH)	120' - 137' + (WH) →	T. P.	P2 - KK
43	B22	ANALOG MUX (GND)	120' - 137' - (BLK) →	T. P.	P2 - LL
44	A22				
45	B23	$\overline{SMA}$ 0 (LSB)			A1 - J1 - B23
46	A23	$\overline{SMA}$ 1			A1 - J1 - A23
47	B24	$\overline{SMA}$ 2			A1 - J1 - B24
48	A24	$\overline{SMA}$ 3 (MSB)			A1 - J1 - A24
49	B25	GND	CAL ON SW GND (BLK) →	T.P./COAX	P1 - CC / J1
50	A25	CAL ON SW	(YEL) →	T.P./COAX	P1 - BB / J1
51	B26				
52	A26				
53	B27	(SERIAL IN) $\overline{STR\ 01}$		BLUE	A1 - J1 - B27
54	A27				
55	B28				
56	A28				
57	B29				
58	A29				
59	B30				
60	A30				
61	B31				
62	A31				
63	B32				
64	A32				
65	B33				
66	A33				
67	B34				
68	A34				
69	B35	$\overline{CMD\ ADR\ 357}$		PURPLE	A1 - J1 - B35
70	A35	CR T/H		WHITE	P1 - H
71	B36				
72	A36				
73	B37	GND			
74	A37				
75	B38				
76	A38				
77	B39				
78	A39				
79	B40				
80	A40				
81	B41				
82	A41				
83	B42				
84	A42				
85	B43				
86	A43				
87	B44				
88	A44				
89	B45				
90	A45				
91	B46				
92	A46				
93	B47				
94	A47				
95	B48				
96	A48				
97	B49	GND			
98	A49	+5V			
99	B50	GND			
100	A50	+5V			



NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

PROJECT: T6

TITLE: A2 CONTROL BOARD

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 12/7/78
DESIGNED BY	DATE 12/11/78
APPROVED BY	DATE 12/12/78

SHEET NUMBER | DRAWING NUMBER D13820L2 | REV. A | SCALE

at the Central Electronics Room when the front end noise source had been turned on at the front end. The solution is based on the fact that the DCS commands at both the antenna and the Central Electronics Room are based on odd or even computer (or waveguide) cycles. The appearance of the command address can be used to synchronize a toggle flip-flop in both situations.

Two modifications to the system were required (one at the antenna L8 Timing Generator module and one at the Central Electronics Room T6 module) to implement this system. The L8 Timing Generator module had a 74S73 flip-flop added, wired as a toggle flip-flop. The flip-flop was clocked from the 1200 MHz carrier on signal to obtain the 9.6 Hz 50% duty cycle signal necessary to drive the noise source at the antenna through the F5 Front End Control module. This is shown in Figure 3.4. To synchronize this signal with the Central Electronics Room the strobe for the Walsh function command, address 376' is used to clear the flip-flop. This normally occurs every 24 cycles, so initialization will have a slight delay associated with it.

The T6 Baseband Control module in a similar manner uses the command 357' strobe to clear a 7474 flip-flop wired again as a toggle flip-flop. The clock is obtained from the Central Electronics Room Track and Hold signal. However, in this case the synchronous detector gating signals must only be valid during the time that the front end received signals are present. This is accomplished by "anding" the appropriate flip-flop output with the original Central Electronics Room Track and Hold signal. Thus two seperate gating signals are generated.

"Cal Off" is valid when the received noise power is present with the front end noise calibration source turned off.

"Cal On" is valid when the received noise power is present with the front end noise calibration source turned on.

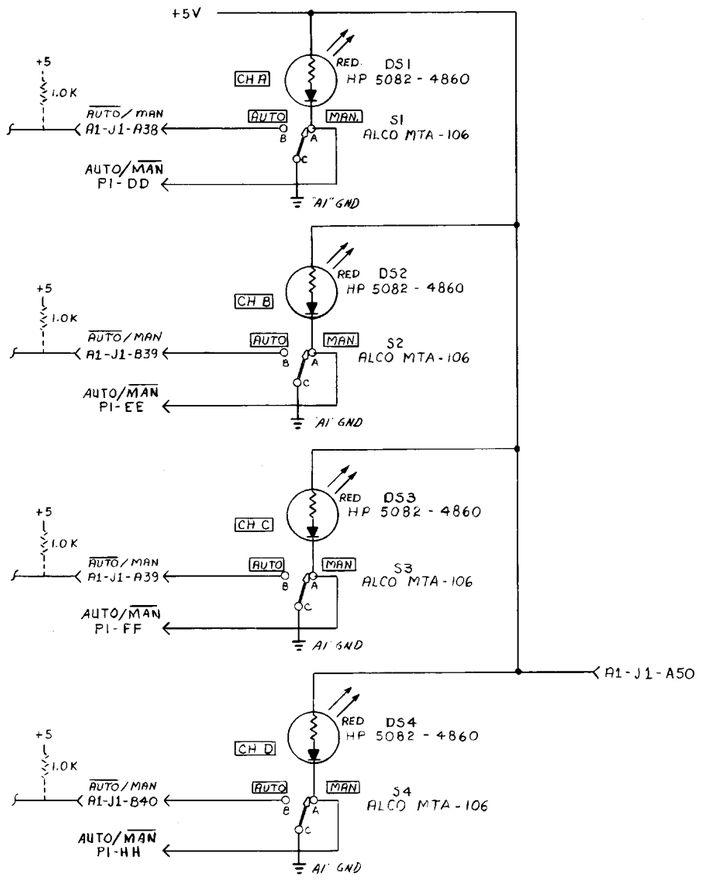
It is important to note that command 357' must be present on a periodic basis to insure proper synchronous detector operation. Only the command 357' strobe must be present. 357' data is not utilized. Proper operation of the system can be diagnosed by looking at the polarity of the analog synchronous detector voltage. If it is negative, a problem is indicated.

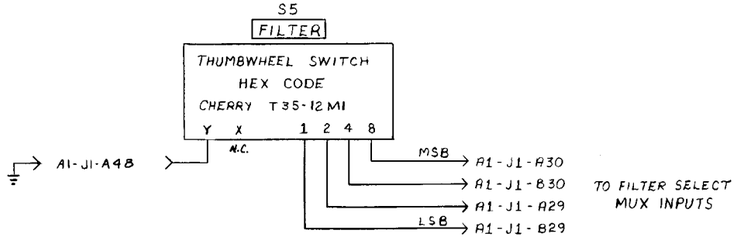
3.3 Module Wiring Harness and A3 Card

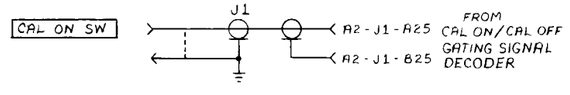
These are shown in D13820L3C. The A3 printed circuit card contains resistive dividers for the power supply voltages monitored by the A1 card analog multiplexer. These dividers limit the monitored voltages to ±10 VDC, and is the same card used in T6A and T6B. The resistors were not put on the A2 wirewrap card in order to make the A1 and A2 cards functionally independent for easier diagnostics.

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	4/.../79			REV. PER CKT CHG
B	4/.../79			ADD "A1" GND - 4 PLC'S
C	7/5/79			CORRECTED S5 TERM

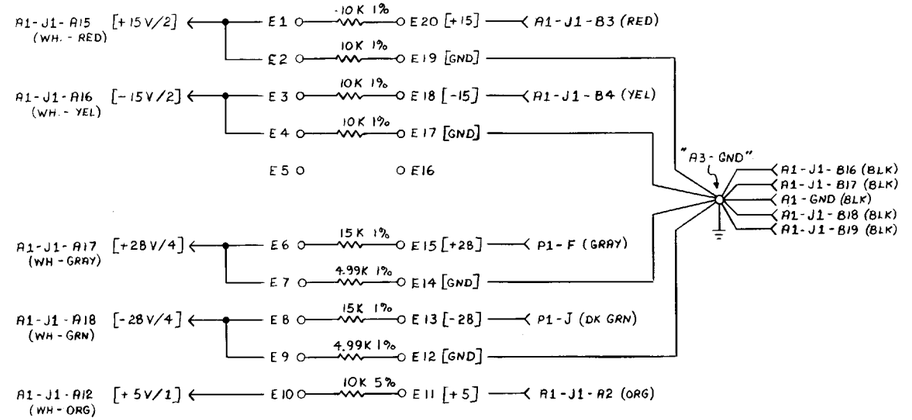
T6C BASEBAND CONTROL FRONT PANEL WIRING







T6C TERMINAL BOARD "A3" WIRING DIAGRAM



NOTE: GROUND DEFINITION & CONNECTIONS

DEF: "A3 GND" = GND TERMINAL LUG ON TERMINAL BOARD

CONN: P1-B —BLK→ P1-GND P1-L —BLK→ P1-GND

P1-GND —BLK→ A2-GND

A2-GND —BLK→ A3-GND

A3-GND —BLK→ A1-GND

(F.P. GROUNDS CONNECT TO "A1-GND" LUG)

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

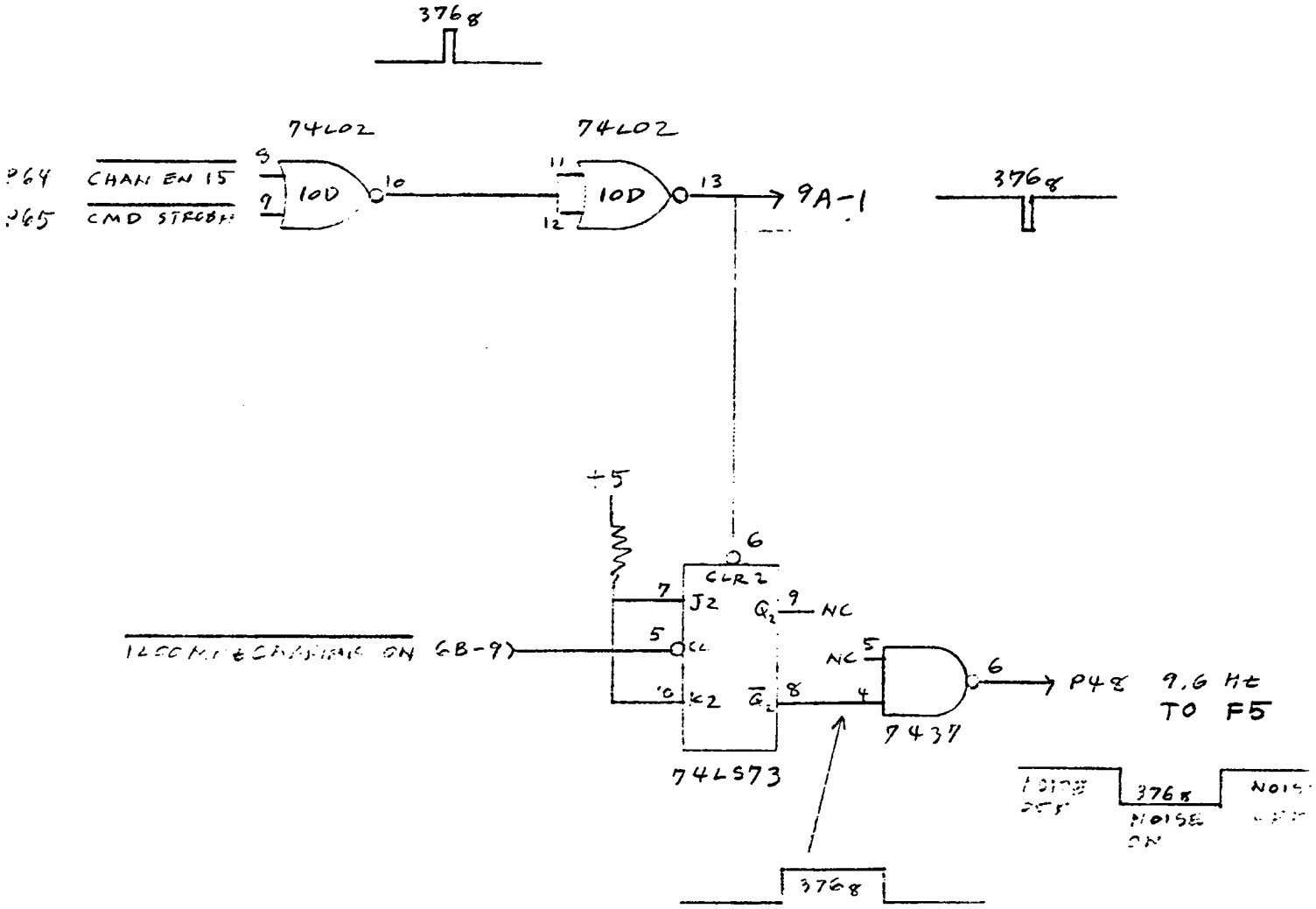
PROJECT: T6C

TITLE: BASEBAND CONTROL & A3

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 4/4/78
DESIGNED BY	DATE 11/.../..
APPROVED BY	DATE 12/.../..

SHEET NUMBER | DRAWING NUMBER D13820L3 | REV. C | SCALE



L8 DIVIDER MODIFICATION

Figure 3.4

4.0 FRONT PANEL INDICATORS AND CONTROLS

4.1 Auto/Man Switches (Channels A, B, C, D)

In the auto position, the appropriate T4C Baseband Filter receives its filter selection command from the T6C DCS interface. Also, the ALC amplifier in the appropriate T5C Baseband Driver receives its gain control voltage from the internal ALC loop amplifier.

In the Man position, the appropriate T4C Baseband Filter receives its filter selection command from the T6C Front Panel filter select thumbwheel switch common to all T4C's in the manual mode. Also, the ALC amplifier in the appropriate T5C Baseband Driver receives its gain control voltage from the T5C Front Panel manual gain control. Also the manual warning LED adjacent to the Auto/Man switch will light, and a warning signal is sent to the DCS digital monitor system.

4.2 Man LEDs (Channels A, B, C, D)

This red LED indicates that the adjacent Auto/Man switch is in the Manual mode. In normal operation this LED should be extinguished.

4.3 Filter Thumbwheel Switch

This BCD switch selects the filter for the appropriate T4C when in the Manual mode.

SWITCH	FILTER SELECTION
0	46 MHz Low Pass Filter
1	23 MHz Low Pass Filter
2	11.5 MHz Low Pass Filter
3	5.75 MHz Low Pass Filter
4	2.88 MHz Low Pass Filter
5	1.438 MHz Low Pass Filter
6	0.719 MHz Low Pass Filter
7	0.210-0.390 MHz Bandpass Filter
8	External Filter
9	Termination

4.4 Cal On Switch BNC Connector

This is a copy of the Cal On TTL gating signal distributed to all T5C Baseband Driver modules, synchronous with the Central Electronics Room Track and Hold signal. See Timing Diagram for further information.

5.0 ADDRESSES AND BIT ASSIGNMENTS

Refer to Figure 5.1.

DCS 5 MONITOR WORDS

Baseband Drivers and Control (T5 and T6)

OCTAL ADDRESS	SOURCE	NAME	NORMAL VOLTAGE	VOLTAGE LIMITS
100'	T5	ALC CH.A	-3.5v	-6/-1 v
101'	T5	ALC CH.B	-3.5v	-6/-1 v
102'	T5	ALC CH.C	-3.5v	-6/-1 v
103'	T5	ALC CH.D	-3.5v	-6/-1 v
104'	T5	CAL OFF CH.A	+6 v	+5/+6.5 v
105'	T5	CAL OFF CH.B	+6 v	+5/+6.5 v
106'	T5	CAL OFF CH.C	+6 v	+5/+6.5 v
107'	T5	CAL OFF CH.D	+6 v	+5/+6.5 v
		Power Supplies (T6)		
110'	P4	+5 v pwr supply	+5 v	+4.95/+5.25 v
111'	T6	Spare		
112'	P5	+15 v pwr supply	+7.5 v	+7.4/+7.6 v
113'	P5	-15 v pwr supply	-7.5 v	-7.6/-7.4 v
114'	P5	+28 v pwr supply	+7 v	+6.9/+7.1 v
115'	P4	-28 v pwr supply	-7 v	-7.1/-6.9 v
116'	T6	Spare		
117'	T6	Spare		
		Baseband Drivers and Control (T5 and T6)		
120'	T5	Sync Det CH.A	+5 v	
121'	T5	Sync Det CH.B	+5 v	
122'	T5	Sync Det CH.C	+5 v	
123'	T5	Sync Det CH.D	+5 v	
124'	T6	Spare		
125'	T6	Spare		
126'	T6	Spare		
127'	T6	Spare		

BASEBAND T4, T5, AND T6 MONITOR AND COMMAND WORD ADDRESS ASSIGNMENTS

Figure 5.1A

Baseband Filters And Control (T4 and T6)

240' T4 Baseband Filter monitor coding identical to command word coding. See word 340.

Baseband Drivers And Control (T5 and T6)

241' T5 Monitor word from baseband

Control	AUTO/MAN Switch CH.A	BIT 21
	AUTO/MAN Switch CH.B	BIT 22
	AUTO/MAN Switch CH.C	BIT 23
	AUTO/MAN Switch CH.D	BIT 24

DCS 5 Command Word

340' T4 Baseband Filter Commands

Baseband Filter A Bandwidth		Hex Command
46 MHz	LPF	0
23 MHz	LPF	1
11.5 MHz	LPF	2
5.75 MHz	LPF	3
2.88 MHz	LPF	4
1.438 MHz	LPF	5
0.719 MHz	LPF	6
0.201-0.390 MHz	BPF	7
External Filter		8
Termination		9

Baseband Filter B Bandwidth		
46 MHz	LPF	00
23 MHz	LPF	10
11.5 MHz	LPF	20
5.75 MHz	LPF	30
2.88 MHz	LPF	40
1.438 MHz	LPF	50
0.719 MHz	LPF	60
0.201-0.390 MHz	BPF	70
External Filter		80
Termination		90

Figure 5.1B

Baseband Filter C Bandwidth		Hex Command
46 MHz	LPF	000
23 MHz	LPF	100
11.5 MHz	LPF	200
5.75 MHz	LPF	300
2.88 MHz	LPF	400
1.438 MHz	LPF	500
0.719 MHz	LPF	600
0.201-0.390 MHz	BPF	700
External Filter		800
Termination		900

Baseband Filter D Bandwidth		
46 MHz	LPF	0000
23 MHz	LPF	1000
11.5 MHz	LPF	2000
5.75 MHz	LPF	3000
2.88 MHz	LPF	4000
1.438 MHz	LPF	5000
0.719 MHz	LPF	6000
0.201-0.390 MHz	BPF	7000
External Filter		8000
Termination		9000

357' T5 Synchronization command (only address is used) (must be periodically sent for proper T5 synchronous detector operation)	ANY

Figure 5.1C

6.0 LIST OF DRAWINGS

The T6C Baseband Control Drawing List is given in A13820C3.

7.0 RELATED PUBLICATIONS AND MEMORANDA

VLA Technical Report #5, Module T6 IF Control, A. R. Thompson (Obsolete).

VLA Technical Report #44, An Overview of the Monitor and Control System, D. W. Weber, March 1980.

VLA Technical Report #48, T4C Baseband Filter, W. E. Dumke, December 1980.

VLA Technical Report #49, T5C Baseband Driver, W. E. Dumke, December 1980.

Memorandum, Subject "Baseband System DCS Manual Revisions", W. E. Dumke, July 24, 1980.

Rack D Central Electronics Room Block Diagram, Drawing No. D16000B5D

REVISIONS

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	11-8-79			RE-DRAWN BY DRAFTING

DRAWN BY	DATE 10-31-79			
DESIGNED BY	DATE			
APPROVED BY	DATE		NEXT ASSY	USED ON

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT (T6C)

TITLE BASEBAND CONTROL

DWG NO. A1382003 SHEET 1 OF

ASSEMBLY NAME (T6C) BASEBAND CONTROL | SERIES/MODEL | USED ON

DWG. NO. A139203

SHEET 2 of 3

REV. /

DRAWING NO.	REV.	TITLE	NOTES
A139203	D	BASEBAND CONTROL MODULE - BOM	
B1305	B	- ASSY	
C1382	A	- BLOCK DIAGRAM	
D1382	C	- LOGIC DIAGRAM	
A1382	A	- WIRE LIST	
A1382	A	W.W. CARD ASSY (A2) - BOM	
C1382	—	- ASSY	
D1382	A	- LOGIC DIAGRAM	
A1382	—	ASSEMBLERS LIST BY BOARD COORDINATES (A2)	
A1382	—	ASSEMBLERS LIST BY IC COORDINATES (A2)	
A1382	—	I C LIST (A2)	
A1382	—	WIRE LIST (A2)	
A1382	—	MACHINE CARD LIST (A2)	
A1382	—	W.W. CARD ASSY (A1) - BOM	
C1382	—	- ASSY	
D1382	D	- LOGIC DIAGRAM	
A1382	A	WIRE LIST (A1)	
C1305	E	PERFORATED COVER	1
B1305	C	FASTENER FOR PERFORATED COVER	1
B1305	F	SUPPORT BARS TOP & BOTTOM	1

NOTES:

1. GENERAL USE ITEM

ASSEMBLY NAME (T6C) BASEBAND CONTROL | SERIES/MODEL | USED ON

DRAWING NO.	REV.	TITLE	NOTES
513050M04	D	GUIDE	1
B13925M32	B	PANEL, REAR	1
C13920M03	A	PANEL, FRONT	
D13920M14	B	SIDE PLATE	
B13820M13	A	CONNECTOR SUPPORT	

DWG. NO. A13820C3

SHEET 3 of 3

NOTES:

1. GENERAL USE ITEM